CS22230 Data Sheet
Wireless Mini PCI / USB Controller

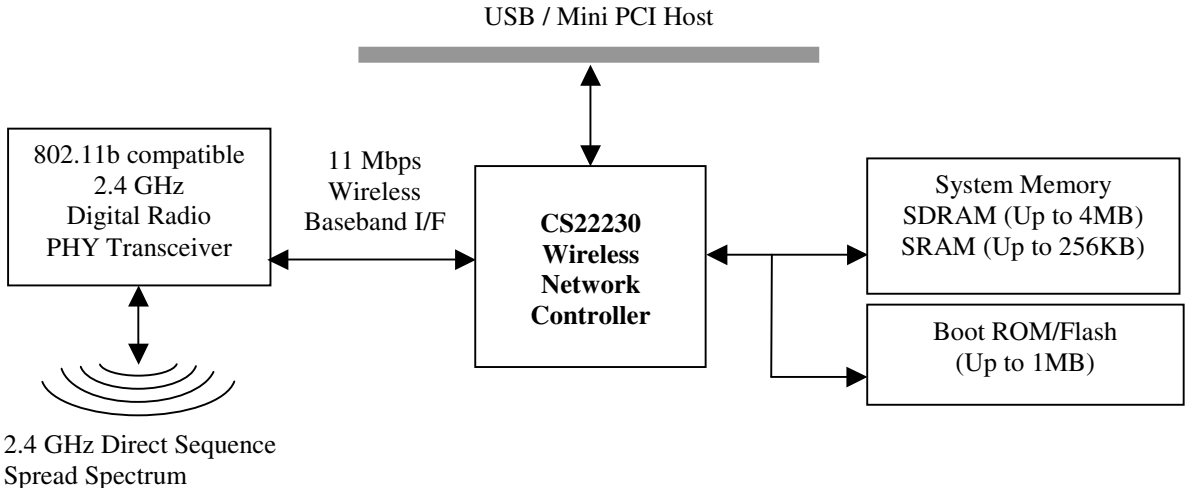
1 Description

The Cirrus Logic CS22230 Wireless Network Controller enables high speed, 11 Mbps digital wireless connectivity for a variety of platforms including embedded systems, mobile applications, and other cost sensitive applications capable of supporting a standard Mini PCI or USB interface.

The CS22230 is a highly integrated single-chip Mini PCI / USB solution for wireless networks supporting video, audio, voice, and data traffic. The programmable controller executes Cirrus Logic's Whitecap™2 networking protocol that provides Wi-Fi™ (802.11b) compliance as well as multimedia and quality of service (QoS) support. The device includes several high performance components including an ARM7TDMI RISC processor core, a Forward Error Correction (FEC) codec and a wireless Radio MAC supporting up to 11 Mbps throughput. The CS22230 is designed to support both a standard Mini PCI 2.2 compliant interface or USB 1.1 compliant device interface, making it an ideal choice for cost effective standalone and multifunction embedded high-speed wireless networking products.

The CS22230 utilizes state-of-the-art 0.18um CMOS process and is housed in a 208 MQFP package designed to provide integrated low cost IEEE 802.11 standard compliant system solutions. The core is powered at 1.8 V to reduce overall power consumption. In addition, the CS22230 supports various power management modes for host, MAC, baseband, and radio interfaces.

Figure 1. Example System Block Diagram



2 Features

Embedded ARM Core and System Support Logic

- High Performance ARM7TDMI RISC processor core at 77MHz
- 4KB integrated, one-way set associative, unified, write through cache
- Individual interrupt for each functional block
- Two 23-bit programmable (periodic or one-shot) general purpose timers
- 8 Dword (32-bits) memory write and read buffers for high system performance
- Abort cycle detection and reporting for debugging
- ARM performance monitoring function for system fine-tuning
- Programmable performance improvement logic based on system configuration
- Flexible independent DMA engines for Mini PCI and Digital Radio functional units

Enhanced Memory Controller Unit

- Programmable memory controller unit supporting SDRAM /async SRAM/boot ROM interface
- 16-bit data bus with 12-bit address supporting up to 4MB at up to 103MHz SDRAM
- 8-bit data bus with addressing support up to 1MB of boot ROM/Flash
- Programmable SDRAM timing and size parameters such as CAS latencies and number of banks columns and rows

FEC codec

- High performance Reed-Solomon coding for error correction (255:239 block coding)
- Reduces symbol error probability of a typical 10e-3 error rate environment to 10e-9
- Programmable rate FEC engine to optimize channel efficiency
- Low latency, fully pipelined hardware encoding and decoding. Support byte wise single cycle throughput up to 77MHz, with a sustain rate of 77MBps.
- Double buffering (64 Dword read/write buffer) to enhance system performance
- On the fly configuration of encoder and decoder

Digital Wireless Radio MAC

- Glue-less interface to 802.11b radio baseband transceiver
- 11Mbps data rate
- 32 Dword transmit/receive FIFO
- Supports clear channel assessment (CCA)

Power Management

- Host (Mini PCI) ACPI compliant
- Remote USB host wakeup
- Supports variable rate radio transmit, receive and standby radio power modes through two DACs

Clock and PLL Interface

- Single 44MHz crystal oscillator reference clock for Mini PCI version. 48MHz reference clock required in USB option.
- Internal PLL to generate internal and on board clocks

USB Controller Interface

- 12 Mbps USB 1.1 compliant device
- Supports 1 to 16 endpoints, endpoints can be bulk, isochronous or interrupt
- Variable endpoint buffer depths providing maximum flexibility for endpoint configurations
- Flexible configuration programming via EEPROM or firmware download
- Remote host wakeup

Mini PCI Controller Interface

- 33MHz 5V/3.3V Mini PCI 2.2 compliant master/target 32-bit data interface
- ARM communication with Mini PCI controller through simple mailbox scheme
- Generic Mini PCI controller programming interface
- Flexible configuration programming via EEPROM

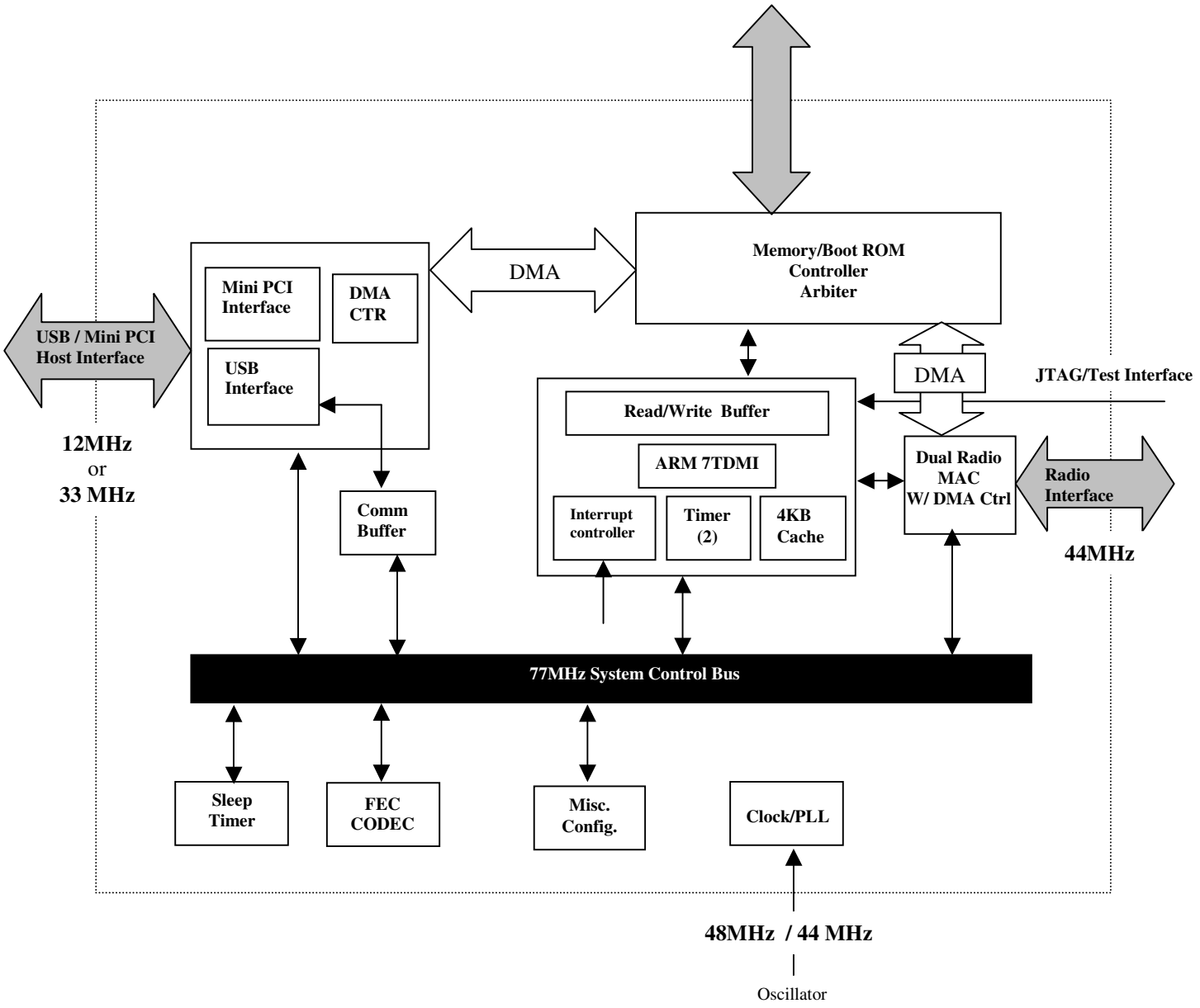
Chip Processing and Packaging

- 208 MQFP package and 0.18 um state-of-the-art CMOS process
- 1.8 V core for low power consumption. 3.3V I/O and 5V tolerant

IMPORTANT NOTICE

3 Functional Description

Figure 2. Block Diagram of Major Functional Units



3.1 Embedded ARM core and System Support Logic

The processing elements of the CS22230 include the ARM7TDMI core and its associated system control logic. The ARM Processor and System Controller consists of a Memory Management Unit, 4-KB write through Cache Controller, 20 IRQ and 4 FIRQ interrupt controller, and 2 general purpose timers. The ARM processor and integrated system support logic provide the necessary execution engine to support a real time multi-tasking operating system, the network protocol stack, and firmware services. In addition, system performance monitor logic is included to aid in system performance fine-tuning (e.g. cache hit, CPI numbers).

Memory Management Unit
ARM instructions and data are fetched from system memory a cache-line (4/8 – Dwords /Programmable) at a time when caching is turned on. During a cache line fill, critical word data, i.e., the access that caused the miss, is forwarded to the ARM and also written into the data RAM cache. The non-critical words in the line fetched following the critical word are then written to the cache on a Dword basis, as they become available.

Memory writes are posted to dual 4-Dwords (32-bit) memory write posting buffers. Write posts use the sequential addressing feature on the memory bus. With dual buffering an out of sequence write will post to one write buffer while the other buffer is flushed to memory.

There is one 8Dword Read Buffers in the MEM block. The buffer is used for both cacheable and non-cacheable memory space.

Interrupt Controller
The Interrupt Controller provides two interrupt channels to the ARM processor. One interrupt channel is presented to the ARM on its *nFIQ*, and the other channel is presented on its *nIRQ* pin. These are referred to as the FIQ channel and the IRQ channel. Both channels operate in identical but independent fashion. The FIQ channel has a higher priority on the ARM processor than the IRQ channel.

The Interrupt Controller includes a CONTROL register for each logical interrupt in the ARM Complex. The CONTROL register serves the following main purposes:

- Provides the mapping between the EXT_INT inputs (physical interrupts) and the logical interrupt
- Selects the particular type of signaling expected on the EXT_INT inputs: level, edge, active level high/low etc.
- Enables or disables a logical interrupt

3.2 Digital Wireless Radio Interface

The CS22230 digital radio MAC I/F supports multiple radio baseband and RF interfaces. The baseband registers can be programmed during the configuration time using the control port interface. The MAC also provides the capability of programming the signal, service and length on per packet basis without ARM intervention. This significantly improves the performance of the system.

There are three primary digital interface ports for the CS22230 that are used for configuration and during normal operation.

These ports are:

- The Control Port, which is used to configure, set power consumption modes, write and/or read the status of the radio base band registers.
- The TX Port, which is used to output the data that needs to be transmitted from the network processor.
- The RX Port, which is used to input the received demodulated data to the network processor.

3.3 FEC Codec

The FEC codec performs Reed-Solomon code encoding to protect the data before it is transmitted to a noisy channel. It is a similar code as employed by digital broadcast industry, such as ITU-T J.83 for DVB. The RS(255, 239) code implemented by the SWG2710 can reduce error probability to 1/10e-9 in a typical 1/10e-3 error rate environment. The encoder/decoder can be programmed to vary the coding block length (*N*) and correctable error (*t*) to optimize the tradeoff between channel utilization and data protection. The range of *N* is currently set to be from 50 to 255, and the *t* is 8. The symbol size is fixed at 8 bits.

Coding parameters can be set real time, allowing maximum flexibility for the system to adjust the FEC setting, such as block size, in order to optimize channel efficiency. The encoder also has a very low latency of two cycles. Both the encoder and decoder are fully pipelined in structure to achieve single cycle throughput. The FEC can be disabled in firmware.

3.4 Programmable Memory Controller

The CS22230 incorporates a general-purpose memory controller that supports a SDRAM/async SRAM memory and FLASH memory interface.

In the RAM configuration, the system memory interface supports up to 16-Mbyte of 16-bit SDRAM running at a frequency up to 103 MHz single-state access cycles or 256KB of 16 bit async SRAM. The Memory Controller provides programming of SDRAM parameters such as CAS latency, refresh rate, etc; these registers are located in miscellaneous configuration registers. When there are no pending memory requests from any internal requester, the SWG2110 will keep Clock Enable (CKE) signal low to cause the SDRAM to stay in power down mode. Once a memory request is active, the SWG2110 will assert CKE high to cause the SDRAM to come out of power down mode. Typically, this can reduce memory power consumption by up to 50%.

In ROM configuration, firmware for CS22230 is stored in non-volatile memory and is accessed through the Boot ROM interface. The maximum addressable ROM space supported is 1MB. ROM read/write and output enable are shared with RAM control pins. The ROM can be re-flashed allowing for software upgrades.

3.5 Mini PCI Controller Interface

Embedded in the CS22230 is a Mini PCI 2.2 fully compliant master/target 32 bit data interface including power management support (PME signal). The communication buffer logic was designed to be flexible and generic to both the PC Software and ARM firmware.

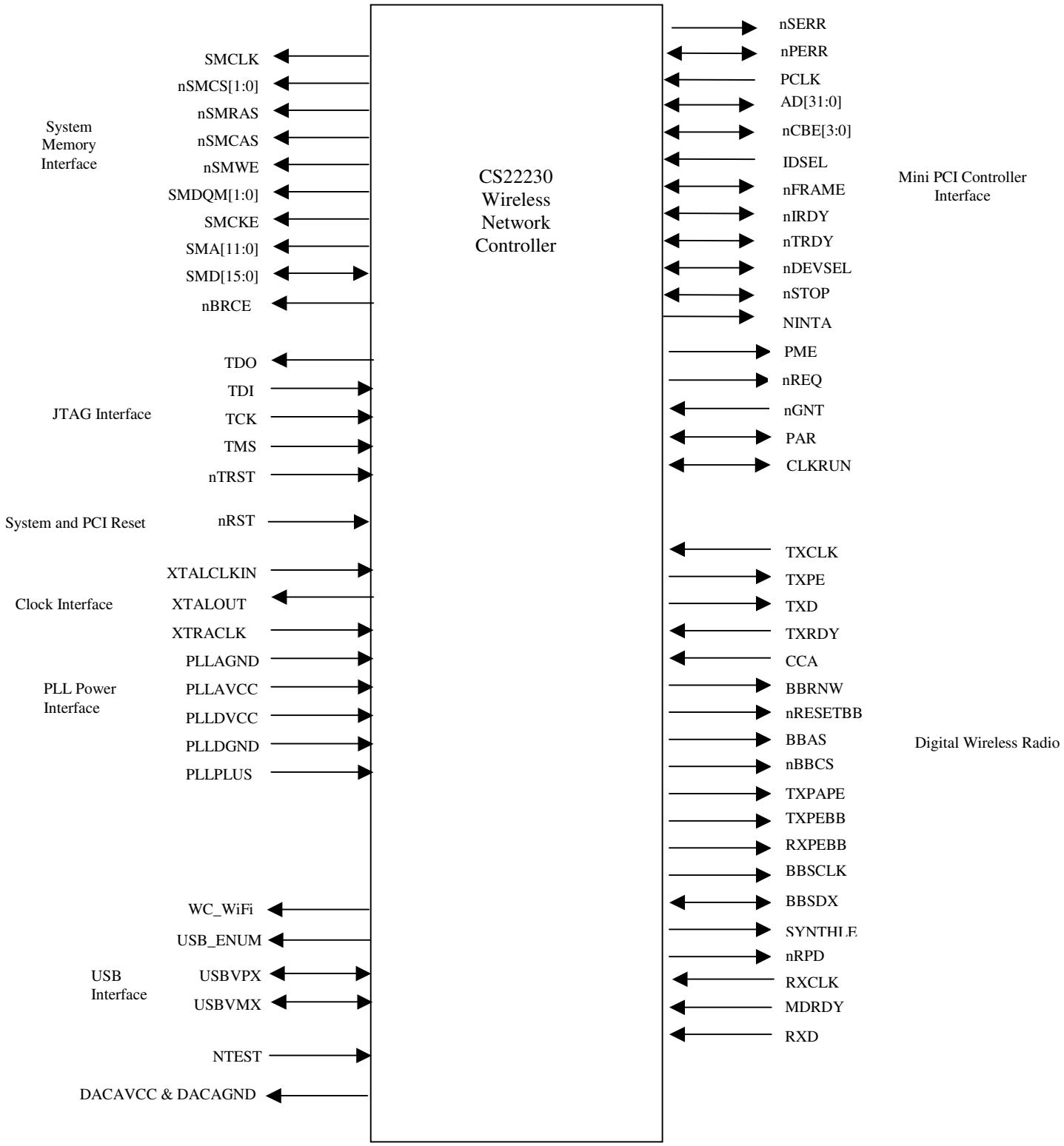
Mini PCI data transfer is supported by a DMA Control Block (DCB). The DCB is configured by the ARM, allowing the ARM to control how often it is interrupted. Mini PCI data transfers are done by the Mini PCI master, and the DCB, offloading CPU overhead.

3.6 USB Interface

Embedded within the CS22230 is a full speed USB 1.1 compliant device interface. The device supports from 1 to 16 endpoints and is completely programmable via firmware download or external EEPROM.

All “setup” commands are passed to the system processor for interpretation. The device also contains a DMA engine to transfer arbitrary amounts of data to and from main memory before interrupting the system processor.

Figure 3. CS22230 Logical Pin Groupings (note: not all signals are shown)



This section provides detailed information on the CS22230 signals. The signal descriptions are useful for hardware designers who are interfacing the CS22230 with other devices.

System Memory Interface

The system memory interface supports standard SDRAM interface, async SRAM and FLASH. There are total of 37 signals in this interface.

SMCLK **Output**

System Mem Clock for SDRAM. Currently the interface supports 103 MHz for a maximum bandwidth of 200Mbytes/sec.

nSMCS0 **Output**

Chip select bit 0. This signal is used to select or deselect the SDRAM for command entry. When SMNCS is low it qualifies the sampling of nSMRAS, nSMCAS and nSMWE. Also used as testmode(2) when NTEST pin is '0'.

nSMCS **Output**

Chip select bit 1.

nBRCE **Output**

Chip select for ROM access. This signal is used to select or deselect the boot ROM memory.

nSMRAS **Output**

Row address select. Used in combination with nSMCAS, nSMWE and nSMCS to specify which SDRAM page to open for access. Also used during reset to latch in the strap value for clk_bypass; if set to a '1' implies bypassing clock module; whatever clk is applied on the input clock is used for memclk and ctlclk. Also shared as the ROMOE signal.

nSMCAS **Output**

Column address select. Used in combination with nSMRAS, nSMWE and nSMCS to specify which piece of data to access in selected page. Also used during reset to latch in the strap value for same_freq; if set to a '1' implies internal mem_clk and arm_clk are running at the same frequency and 180 degrees out of phase.

nSMWE **Output**

Write Enable. Used in combination with nSMRAS, nSMCAS, and nSMWE to specify whether the current cycle is a read or a write cycle. Also used during reset to latch in the strap value for tst_bypass; if set to a '1' implies PLL bypass. Also shared as the ROMWE to do flash programming.

SMDQM[1:0] **Output**

Data mask bit 1:0. These signals function as byte enable lines masking unwanted bytes on memory writes. Also used as testmode(1:0) when NTEST pin is '0'.

SMCKE **Output**

Clock enable. SMCKE is used to enable and disable clocking of internal RAM logic.

SMA0 **Output**

Address bit0. The address bus specifies either the row address or column address. Also shared as boot-rom address bit0. This pin should be pull-down.

SMA1 **Output**

Address bit1. Also shared as boot-rom address bit1. Also used during reset to latch in the strap value for Mini PCI sel; if set to a '1' implies Mini PCI mode.

SMA2 **Output**

Address bit2. Also shared as boot-rom address bit2. Also used during reset to latch in the strap value for usbsel; if set to a '1' implies usb mode.

SMA3 **Output**

Address bit3. Also shared as boot-rom address bit3. This pin should be pull-down.

SMA4 **Output**

Address bit4. Also shared as boot-rom address bit4. Also used during reset to latch in the strap value for romcfg; if set to a '1' implies Mini PCI configuration data should be downloaded from ROM.

SMA5 **Output**

Address bit5. Also shared as boot-rom address bit5. Also used during reset to latch in the strap value for test_rst_enb; if set to a '0' implies normal operation mode.

SMA6 **Output**

Address bit6. Also shared as boot-rom address bit6. Also used during reset to latch in the strap value for freq_sel(0). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x, and 111=8x).

SMA7 **Output**

Address bit7. Also shared as boot-rom address bit7. Also used during reset to latch in the strap value for freq_sel(1). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x, and 111=8x).

SMA8 **Output**

Address bit8. Also shared as boot-rom address bit8. Also used during reset to latch in the strap value for freq_sel(2). Freq_sel(2:0) is used to select the multiplication factor for the internal PLL (000=1x, and 111=8x).

SMA9 **Output**

Address bit9. Also shared as boot-rom address bit9. Also used during reset to latch in the strap value for sdram_delay(0). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns, and 111=1.75ns with each .25ns increments).

SMA10 **Output**

Address bit10. Also shared as boot-rom address bit10. Also used during reset to latch in the strap value for sdram_delay(1). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns, and 111=1.75ns with each .25ns increments).

SMA11 **Output**

Address bit11. Also shared as boot-rom address bit11. Also used during reset to latch in the strap value for sdram_delay(2). Sdram_delay(2:0) is used to select the delay factor for the internal memory clock (000=0ns, and 111=1.75ns with each .25ns increments).

SMD[7:0] **Bi-directional**

Data bus. The data bus contains the data to be written to memory on a write cycle and the read return data on a read cycle.

SMD[15:8] **Bi-directional**

Shared data bus. The data bus contains the data to be written to RAM memory on a write cycle and the read return data on a read cycle. Data bit [15:8] is also shared as boot ROM address bit [19:12].

Digital Wireless Radio Interface

All Radio input buffers are Schmitt triggered input buffers. There are total of 21 signals in this interface.

TXCLK **Input**

Transmit clock is a clock input from the radio baseband processor. This signal is used to clock out the transmit data on the rising edge of TXCLK.

TXPEBB **Output**

Baseband transmit power enable, an output from the MAC to the radio baseband processor. When active, the baseband processor transmitter is configured to be operational, otherwise the transmitter is in standby mode.

TXD **Output**

It is the serial data output from the MAC to the radio baseband processor. The data is transmitted serially with the LSB first. The data is driven by the MAC on the rising edge of TXCLK and is sampled by the radio baseband processor on the falling edge of TXCLK (in 3824 mode) and rising edge of TXCLK (in 3860B mode).

TXRDY **Input**

Transmit data ready is an input to the MAC from the radio baseband processor to indicate that the radio baseband processor is ready to receive the data packet over the TXD signal. The signal is sampled by the MAC on the rising edge of TXCLK.

CCA **Input**

Clear channel assessment is an input from the radio baseband processor to signal that the channel is clear to transmit. When this signal is a 0, the channel is clear to transmit. When this signal is a 1, the channel is not clear to transmit. This helps the MAC to determine when to switch from receive to transmit mode.

BBRNW **Output**

Baseband read/write is an output from the MAC to indicate the direction of the SD bus when used for reading or writing data. This signal has to be setup to the rising edge of BBSCLK for the baseband processor and is driven on the falling edge of BBSCLK.

nRESETBB **Output**

Baseband reset is an output of the MAC to reset the baseband processor.

BBAS **Output**

Baseband address strobe is used to envelop the address or the data on the BBSDX bus. Logic 1 envelops the address and a logic 0 envelops the data. This signal has to be setup to the rising edge of BBSCLK for the baseband processor and is driven on the falling edge of BBSCLK.

nBBCS **Output**

Baseband chip select is an active low output to activate the serial control port. When inactive the SD, BBSCLK, BBAS and BBRNW signals are 'don't cares'.

TXPAPE **Output**

Radio power amplifier power enable is a software-controlled output. This signal is used to gate power to the power amplifier.

TXPE **Output**

Radio transmit power enable indicates if transmit mode is enabled. When low, this signal indicates receive mode.

RXPEBB **Output**

Baseband receive power enable is an output that indicates if the MAC is in receive mode. Output to baseband processor enables receive mode in baseband processor.

BBSCLK **Output**

Baseband serial clock is a programmable output generated by dividing ARM_CLK by 14 (default). This clock is used for the serial control port to sample the control and data signals.

BBSDX **Bi-directional**

Baseband serial data is a bi-directional serial data bus, which is used to transfer address and data to/from the internal registers of the baseband processor.

SYNTHLE **Output**

Synthesizer latch enable is an active high signal used to send data to the synthesizer.

nRPD **Output**

Radio PowerDown Enable. This active low signal is used for power management purposes for the radio circuitry.

RXCLK **Input**

This is an input from Base Band Processor. It is used to clock in received data from Base Band Processor.

MDRDY **Input**

Receive data ready is an input signal from the baseband processor, indicating a data packet is ready to be transferred to the MAC. The signal returns to inactive state when there is no more receiver data or when the link has been interrupted. This signal is sampled on the falling edge of RXCLK (in 3824 mode), and sampled at rising edge of RXCLK (in 3860B mode).

RXD **Input**

Receive data is an input from the baseband processor transferring demodulated header information and data in a serial format. The data is frame aligned with MD_RDY. This signal is sampled on the falling edge of RXCLK (in 3824 mode), and sampled at rising edge of RXCLK (in 3860B mode).

DACAVCC **Input**

Analog power for DAC. 3.3V input.

DACAGND **Input**

Analog ground for DAC.

PLL and Clock Interface

There are three clock pins and five PLL power pins. There are a t of 8 signals in this interface.

XTAL_CLKIN **Input**

44 MHz Reference clock input/crystal clock input for Mini PCI and 48 MHz for USB.

XTALOUT **Output**

Reference crystal clock output.

XTRACLK **Input**

Second clock input to clock module. This input allows independent control for mem_clk and ctl_clk. The usage of this clock input is determined by the clk module configuration, which is determined by the three strapping input pin values.

PLLAGND **Input**

Analog PLL ground.

PLLAVCC **Input**

Analog PLL power. 3.3V input.

PLLDGND **Input**

Digital PLL ground.

PLLDVCC **Input**

Digital PLL power. 1.8V input.

PLLPLUS **Input**

Analog PLL ground.

Mini PCI Interface

The Mini PCI interface is a standard 2.2 compliant interface. There are a total of 52 signals.

AD[31:0] **Bi-directional**

Mini PCI Address/Data. This bus contains a physical address during the first clock of a Mini PCI transfer and data during subsequent clocks. The signals are inputs during the address and write data phases of a transaction, or outputs during the read data phase of a transaction.

nCBE[3:0] **Bi-directional**

Control/Byte Enable. This bus defines the bus command during the first clock of a Mini PCI transaction and the data byte enables during subsequent clocks.

IDSEL **I/O OD**

Mini PCI Initialization device select. Used as a chip select during configuration read and write cycles.

nFRAME **Bi-directional**

Mini PCI cycle frame. This signal marks the beginning and duration of a current bus cycle.

nIRDY **Bi-directional**

Mini PCI Initiator ready. IRDY holds off the beginning of a write cycle and the completion of a read cycle until sampled active.

nTRDY **Bi-directional**

Mini PCI Target ready. This signal is driven active to indicate that write data has been sampled or that read data has been delivered.

nDEVSEL **Bi-directional**

Mini PCI Device select. As a medium speed device, this signal is driven active two Mini PCI clocks after NFRAME is sampled active indicating a positive decode. It remains active until the end of the transaction.

nSTOP **Bi-directional**

Mini PCI Stop. This signal indicates a target initiated termination of the current cycle.

nINTA **Output/Open Drain**

Mini PCI Interrupt request A. Generates an interrupt on the Mini PCI bus.

nCLKRUN **I/O OD**

Mini PCI clock run. This signal is an optional signal used by devices to indicate the clock status.

PCLK **I/O OD**

Mini PCI clock. Typically a 33 MHz. All CS22230 Mini PCI activity is synchronous to PCLK.

nPERR **Bi-directional**

Mini PCI Parity error. This signal is asserted two clocks after a data parity error is detected on the Mini PCI bus.

nSERR **Output/Open Drain**

Mini PCI system error. This open drain signal is used to indicate a fatal parity error on Mini PCI address.

nREQ **Input**

Mini PCI Master Request. Used by the Mini PCI master to indicate it needs drive the Mini PCI bus.

nGNT **Bi-directional**

Mini PCI Master Grant. Used by the Mini PCI master to indicate OK to drive the Mini PCI bus.

PAR **Bi-directional**

Mini PCI parity. This signal is asserted one clock after data transfer has occurred on the Mini PCI bus.

PME **Output/Open Drain**

Power management event. Use to let the system knows a change in power management event has occurred.

System Reset

nRST **Input**

System reset and Mini PCI Reset. Reset is an asynchronous signal that forces the chip to go to a known state. This is an active low signal.

USB Interface

USBVP **Bi-directional**

Differential USB data plus. For high-speed mode, this signal is pull up to 5 volt during IDLE state (see USB_ENUM).

USBVM **Bi-directional**

Differential USB data minus.

USB_ENUM **Output**

USB Enumeration – Indicates disconnect/connect event. USB_ENUM is used to pull the D+ line high, indicating to the host or hub a USB bus "full rate" connection is active.

Debug Interface

TDO **Output**

Test data output.

TDI **Input**

Test data input. The input has an integral pull up.

TCK **Input**

Test clock signal.

TMS **Input**

Test mode select. The input has an integral pull up.

nTRST **Input**

Test interface reset. The input has an integral pull up.

Miscellaneous Interface

SPIO_8,12,13,16 **Bi-directional**

Special Purpose I/O reserved for supporting custom interfaces.
Note: SPIO 13 is used for USB_ENUM during USB modes.

nTEST **Input**

Chip test mode pin. Used in conjunction with SMNCS0, SMDQM[0:1]. Pull up for normal operation.

Power and Ground

VCC (5V and 3.3V)[1] **Input**

5V inputs. There are a total of 3 pins.

VDD (3.3V) **Input**

3.3V inputs. There are a total of 26 pins.

VEE (1.8V) **Input**

1.8 inputs to the core. There are a total of 9 pins.

VSS **Input**

Ground. There are a total of 33 pins.

[1] 5V or 3.3V depending on desired PCI configuration

Figure 4. CS22230 208 pin FPBGA Pinout Diagram

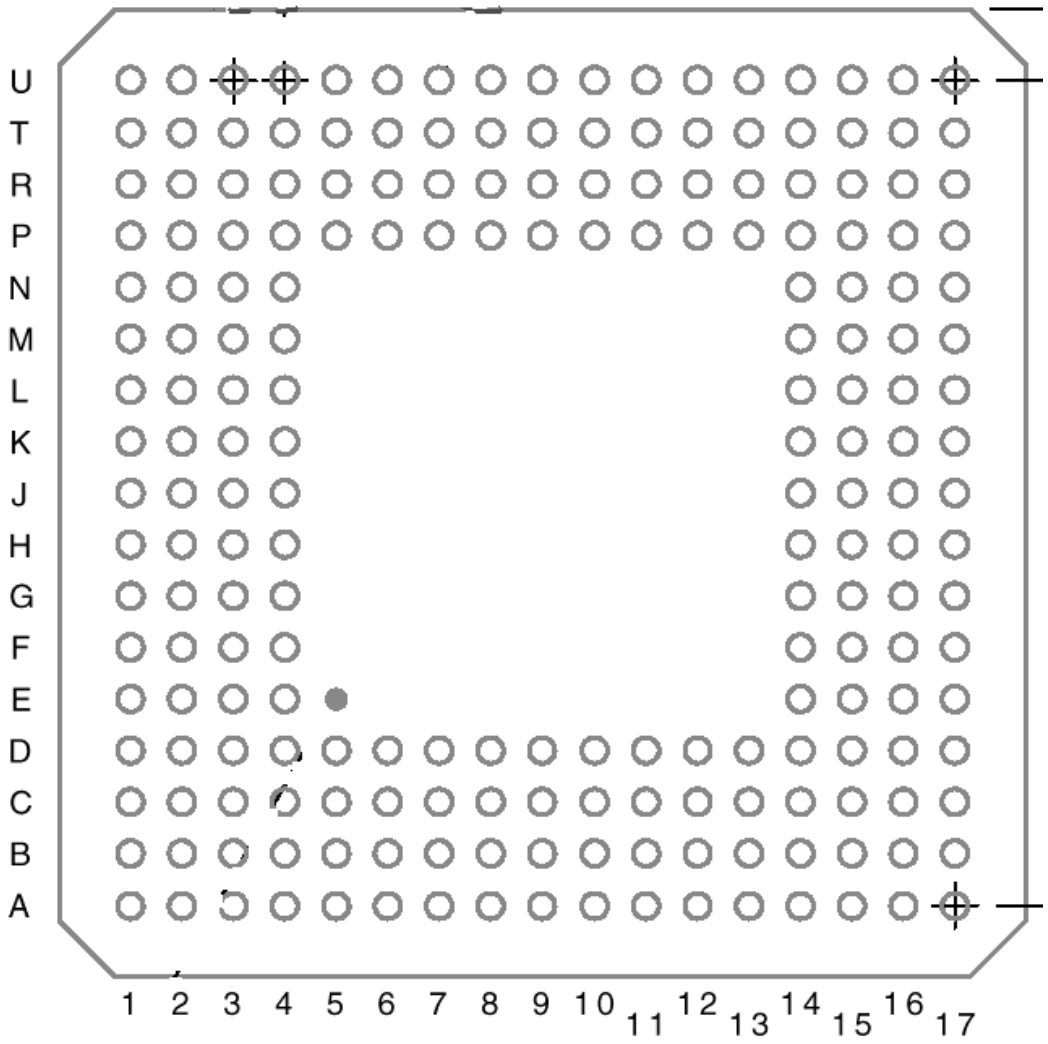


Table 1. Pin Listing by Ball

ball	name	ball	name	ball	name	ball	name
A01	VCC	C12	N/C	G16	VDD	N04	PAR
A02	EXT_NRESET	C13	DACAVSS	G17	RXCLK	N14	SMA06
A03	AD31	C14	XTALCLKIN	H01	NCBE02	N15	SMA08
A04	NGNT	C15	VDD	H02	VSS	N16	VSS
A05	VSS	C16	CCA	H03	AD16	N17	VDD
A06	VDD	C17	VSS	H04	AD18	P01	VDD
A07	CLKRUN	D01	AD24	H14	BBSD	P02	AD13
A08	USBVP	D02	VDD	H15	BBRNW	P03	AD12
A09	VEE	D03	AD25	H16	VSS	P04	NCBE00
A10	TCK	D04	AD28	H17	BBAS	P05	VDD
A11	VSS	D05	PME	J01	VCC	P06	AD02
A12	VDD	D06	N/C	J02	VSS	P07	SMNCS01
A13	N/C	D07	VSS	J03	VEE	P08	VSS
A14	VSS	D08	VSS	J04	VEE	P09	VDD
A15	PLLPLUS	D09	VDD	J14	VEE	P10	VSS
A16	PLLAGND	D10	TMS	J15	VDD	P11	VSS
A17	PLLDVCC	D11	DACAVDD	J16	BBSCLK	P12	SMCLK
B01	AD27	D12	RSVD	J17	SYNTHLE	P13	SMD07
B02	PCD10	D13	XTALOUT	K01	NTRDY	P14	SMA02
B03	AD30	D14	PLLAVCC	K02	NFRAME	P15	SMA05
B04	NREQ	D15	TXD	K03	VDD	P16	VDD
B05	NINTA	D16	TXRDY	K04	VSS	P17	SMA07
B06	VDD	D17	TXCLK	K14	NTEST	R01	VSS
B07	N/C	E01	AD23	K15	VSS	R02	AD10
B08	VEE	E02	NCBE03	K16	VEE	R03	AD09
B09	VSS	E03	IDSEL	K17	BBNCS	R04	AD05
B10	TDI	E04	VSS	L01	NPERR	R05	VSS
B11	VDD	E14	SPIO13	L02	VSS	R06	SMNCS00
B12	RSVD	E15	TXPEBB	L03	NDEVSEL	R07	SMDQM01
B13	XTRACLK	E16	TXPAPE	L04	NIRDY	R08	SMD00
B14	VDD	E17	VDD	L14	SMNWE	R09	VEE
B15	PLLDGND	F01	AD20	L15	NBRCE	R10	SMD02
B16	RNPD	F02	AD22	L16	SMNRAS	R11	SMD05
B17	TXPE	F03	VSS	L17	VSS	R12	SMD06
C01	AD26	F04	VDD	M01	VSS	R13	SMD09
C02	AD29	F14	RXD	M02	VDD	R14	SMD12
C03	VSS	F15	SPIO12	M03	NSERR	R15	SMD15
C04	VDD	F16	VSS	M04	NSTOP	R16	VSS
C05	PCLK	F17	RXPEBB	M14	SMA09	R17	SMA04
C06	SPIO8	G01	AD17	M15	SMA11	T01	AD11
C07	USBVM	G02	AD19	M16	SMA10	T02	VCC
C08	VSS	G03	VDD	M17	VSS	T03	AD08
C09	VEE	G04	AD21	N01	AD14	T04	AD06
C10	TDO	G14	NRESETBB	N02	NCBE01	T05	AD03
C11	NTRST	G15	MDRDY	N03	AD15	T06	AD00

ball	name	ball	name	ball	name	ball	name
T07	SMDQM00	T14	VDD	U04	AD04	U11	VSS
T08	SMCKE	T15	VSS	U05	AD01	U12	SMD08
T09	VEE	T16	SMA00	U06	VDD	U13	SMD10
T10	SMD01	T17	SMA03	U07	SMNCAS	U14	SMD11
T11	SMD04	U01	VDD	U08	VSS	U15	SMD13
T12	VDD	U02	VSS	U09	VDD	U16	SMD14
T13	VSS	U03	AD07	U10	SMD03	U17	SMA01

Table 2. Pin Listing by Name

ball	name	ball	name	ball	name	ball	name
T06	AD00	A13	N/C	M15	SMA11	B06	VDD
U05	AD01	B07	N/C	T08	SMCKE	B11	VDD
P06	AD02	C12	N/C	P12	SMCLK	B14	VDD
T05	AD03	D06	N/C	R08	SMD00	C04	VDD
U04	AD04	L15	NBRCE	T10	SMD01	C15	VDD
R04	AD05	P04	NCBE00	R10	SMD02	D02	VDD
T04	AD06	N02	NCBE01	U10	SMD03	D09	VDD
U03	AD07	H01	NCBE02	T11	SMD04	E17	VDD
T03	AD08	E02	NCBE03	R11	SMD05	F04	VDD
R03	AD09	L03	NDEVSEL	R12	SMD06	G03	VDD
R02	AD10	K02	NFRAME	P13	SMD07	G16	VDD
T01	AD11	A04	NGNT	U12	SMD08	J03	VDD
P03	AD12	B05	NINTA	R13	SMD09	J04	VDD
P02	AD13	L04	NIRDY	U13	SMD10	J14	VDD
N01	AD14	L01	NPERR	U14	SMD11	J15	VDD
N03	AD15	B04	NREQ	R14	SMD12	K03	VDD
H03	AD16	G14	NRESETBB	U15	SMD13	M02	VDD
G01	AD17	M03	NSERR	U16	SMD14	N17	VDD
H04	AD18	M04	NSTOP	R15	SMD15	P01	VDD
G02	AD19	K14	NTEST	T07	SMDQM00	P05	VDD
F01	AD20	K01	NTRDY	R07	SMDQM01	P09	VDD
G04	AD21	C11	NTRST	U07	SMNCAS	P16	VDD
F02	AD22	N04	PAR	R06	SMNCS00	T12	VDD
E01	AD23	B02	PCD10	P07	SMNCS01	T14	VDD
D01	AD24	C05	PCLK	L16	SMNRAS	U01	VDD
D03	AD25	A16	PLLAGND	L14	SMNWE	U06	VDD
C01	AD26	D14	PLLAVCC	E14	SPIO13	U09	VDD
B01	AD27	B15	PLLDGND	C06	SPIO8	A09	VEE
D04	AD28	A17	PLLDVCC	J17	SYNTHLE	B08	VEE
C02	AD29	A15	PLLPLUS	A10	TCK	C09	VEE
B03	AD30	D05	PME	B10	TDI	K16	VEE
A03	AD31	B16	RNPD	C10	TDO	R09	VEE
H17	BBAS	G17	RXCLK	D10	TMS	T09	VEE
K17	BBNCS	F14	RXD	D17	TXCLK	A05	VSS
H15	BBRNW	F17	RXPEBB	D15	TXD	A11	VSS
J16	BBSCLK	T16	SMA00	E16	TXPAPE	A14	VSS
H14	BBSD	U17	SMA01	B17	TXPE	B09	VSS
C16	CCA	P14	SMA02	E15	TXPEBB	C03	VSS
A07	CLKRUN	T17	SMA03	D16	TXRDY	C08	VSS
D11	DACAVDD	R17	SMA04	C07	USBVM	C17	VSS
C13	DACAVSS	P15	SMA05	A08	USBVP	D07	VSS
D12	RSVD	N14	SMA06	A01	VCC	D08	VSS
B12	RSVD	P17	SMA07	J01	VCC	E04	VSS
A02	EXT_NRESET	N15	SMA08	T02	VCC	F03	VSS
E03	IDSEL	M14	SMA09	A06	VDD	F16	VSS
G15	MDRDY	M16	SMA10	A12	VDD	H02	VSS

ball	name	ball	name	ball	name	ball	name
H16	VSS	M17	VSS	R16	VSS	C14	XTALCLKIN
J02	VSS	N16	VSS	T13	VSS	D13	XTALOUT
K04	VSS	P08	VSS	T15	VSS	B13	XTRACLK
K15	VSS	P10	VSS	U02	VSS		
L02	VSS	P11	VSS	U08	VSS		
L17	VSS	R01	VSS	U11	VSS		
M01	VSS	R05	VSS	F15	WC_WiFi		

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V_{EE}	Voltage at Core	1.62 to 2.0	V
V_{DD}	DC Supply (I/O)	-0.3 to 3.9	V
V_{in} (Mini PCI)	Mini PCI Voltage	-0.5 to 5.25	V
V_{IN}	Input Voltage	-0.1 to Vdd + 0.33	V
I_{IN}	DC Input Current	+/- 10	µA
XTALIN	Input frequency [1]	0 to 60	MHz
T_{STGP}	Storage Temperature Range	-40 to 125	°C

Notes:
1. The XTALIN & XTALOUT pins have minimal ESD protection.
2. This device may have ESD sensitivity above 500V HBM per JESD22-A114. Normal ESD precautions need to be followed.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Limits	Units
V_{DD} Vcc Vee	DC Supply	3.0 to 3.60 (3V I/O) 4.5 to 5.5 (5V I/O) 1.6 to 2.0 (core)	V
XTALCLKIN	Input frequency	44 or 48	MHz
armclk	Internal ARM clock frequency	44(4x11) to 77	MHz
memclk	Internal Memory clock frequency	72 to 103	MHz
F_{TCK}	JTAG clock frequency	0 to 10	MHz
T_A	Ambient Temperature	0 to +70	°C
T_J	Junction Temperature	0 to +105	°C

Table 5. Capacitance

Symbol	Parameter	Value	Units
C_{IN}	Input Capacitance	3.4	pF
C_{OUT}	Output Capacitance	4.0	pF

Table 6. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Voltage Input Low		-0.5		0.8	V
V_{IH}	Voltage Input High		2.0		Vcc + 0.5	V
V_{OL}	Voltage Output Low	I_{OL} = 1500 µA			0.55	V
V_{OH}	Voltage Output High	I_{OH} = -500 µA	0.24			V
I_{IL}	Input Leakage Current	$V_{IN} = V_{SS}$ or V_{DD}	-10		10	µA
I_{OZ}	3-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10		10	µA
I_{CC} & I_{DD} I_{EE}	Dynamic Supply Current Note 1	$V_{CC\ \&\ DD}$ = 5V & 3.3V V_{DD} = 1.8V		35 135		ma

5.1 AC Characteristics and Timing

Table 7. System Memory Interface Timing

Parameter	Parameter Description	Min	Max	Units
t_dSMD	SMCLK to SMD[31:0] output delay		7	ns
t_dSMA	SMCLK to SMA[11:0] output delay		4.7	ns
t_dSMDQM	SMCLK to SMDQM[3:0] output delay		5.1	ns
t_dSMNCS	SMCLK to SMNCS[1:0] output delay		4.1	ns
t_dSMNWE	SMCLK to SMNWE output delay		4.5	ns
t_dSMCKE	SMCLK to SMCKE output delay		4.3	ns
t_dSMNCAS	SMCLK to SMNCAS output delay		4.0	ns
t_dSMNRAS	SMCLK to SMNRAS output delay		5.0	ns
T_{per}SMCLK	SMCLK period	72	103	ns
T_{su}SMD	SMD[31:0] setup to SMCLK	1.0		ns
T_hSMD	SMD[31:0] hold from SMCLK	2.4		ns

Notes:

1. Outputs are loaded with 35pf on SMD, 25pf on SMA, SMDQM, SMNRAS, and SMNCAS and 20pf on SMCLK, SMNCS, and SMCKE.
2. An attempt has been made to balance the setup time needed by the SDRAM and the setup needed by CS22230 to read data. If there is a problem meeting setup on the SDRAM, there is a programmable delay line on SMCLK which can help meet the setup time. Care must be taken, however, not to violate the setup on the return read data. The delay can be increased by a multiple of 0.25ns by using the SMA[11:09] pins to selectively set the clock delay .

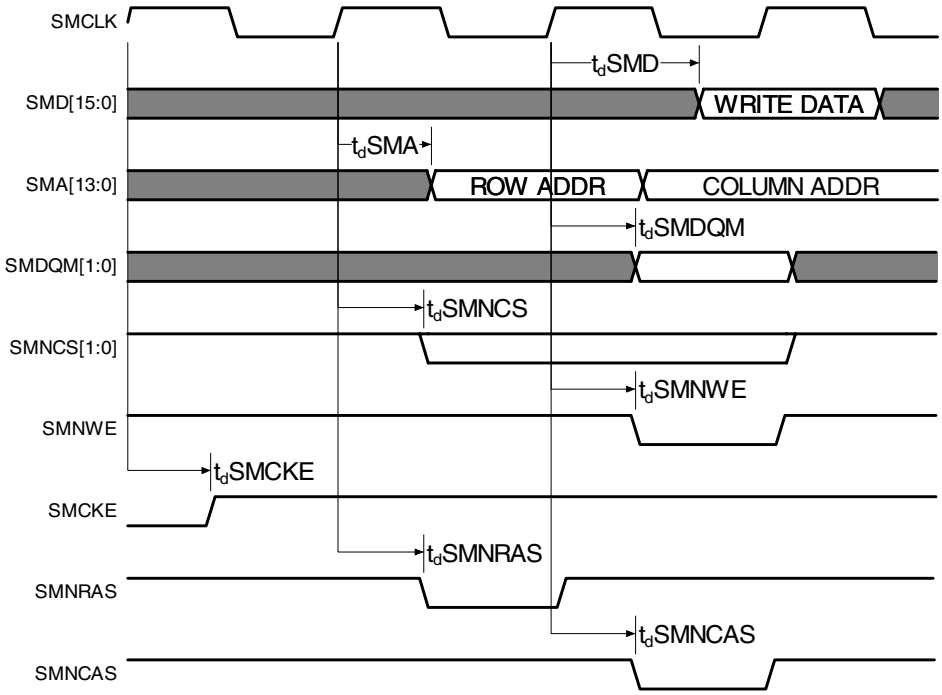


Figure 5. System Memory Interface 'Write' Timing Diagram

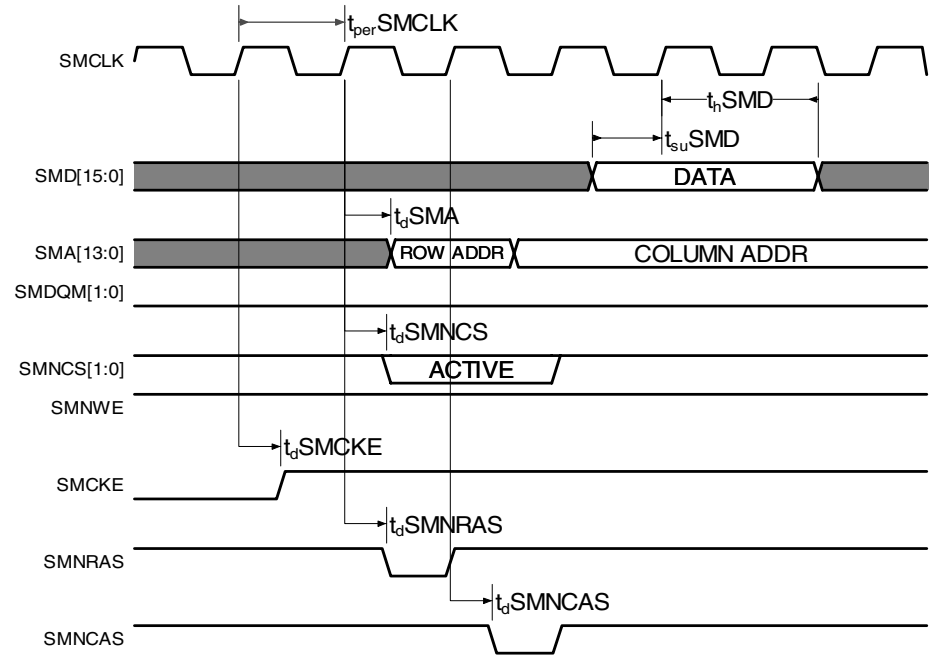


Figure 6. System Memory Interface 'Read' Timing Diagram

Table 8. ROM/Flash Memory Read Timing

Item	Symbol		
		Min	Max
Clock Period (1)	t_{per}SMCLK	72 MHz	103 MHz
$\overline{CE}$ to SMD Latched Data (2)	t_{id} SMD		221 ns
$\overline{OE}$ de-asserted to OE asserted (3)	t_f SMRAS	$6(t_{per}SMCLK)$	
ROM address to output delay (4)	t_{ACC}		220 ns
SMCLK to SMA output delay	t_d SMA		4.0 ns
SMCLK to BRCE output delay ($\overline{CE}$)	t_d BRCE		4.5 ns
SMCLK to SMRAS output delay ($\overline{OE}$)	t_d SMRAS		5.0 ns
SMD setup to SMCLK	t_{su} SMD	1.0 ns	
SMD hold from SMCLK	t_h SMD	2.4 ns	

1. The memclock timing is derived by bootstrap PLL settings. Synchronous modes at 77 MHz & 72 MHz are currently supported.
2. t_{id} SMD is based on the fm_romrdlat register settings – default is 09h max. (77Mhz ~ 17 times SMCLK = 221ns).
3. t_f SMRAS is the Minimum time required before the next OE is active on the bus (6 times SMCLK). The ROM device must release the bus within this time frame (77MHz ~ 78 ns).
4. Based on default fm_romrdlat register settings (note: 09h translates to 11h) *see fm_romrdlat register settings for more information)*

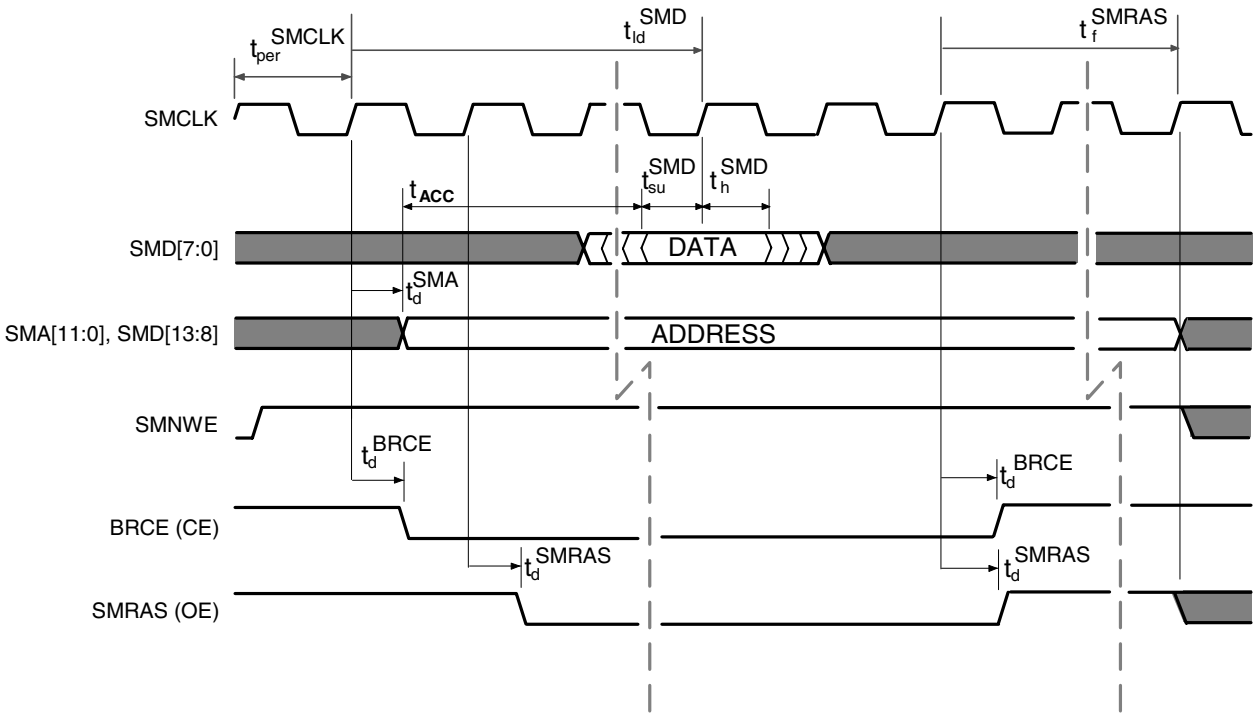


Figure 7. ROM Memory Interface 'Read' Timing Diagram

Table 9. Mini PCI Interface Timings

Parameter	Parameter Description	Min	Max	Units
t_dAD	PCLK to ADX[31:0] output delay		10.93	ns
t_dNCBE	PCLK to NCBEX[3:0] output delay		10.93	ns
t_dNFRAMEX	PCLK to NFRAMEX output delay		10.93	ns
t_dNDEVSELX	PCLK to NDEVSELX output delay		10.92	ns
t_dNIRDYX	PCLK to NIRDYX output delay		10.92	ns
t_dNTRDYX	PCLK to NTRDYX output delay		10.92	ns
t_dNSTOPX	PCLK to NSTOPX output delay		10.92	ns
t_dPARX	PCLK to NPARX output delay		10.92	ns
t_dNPERRX	PCLK to NPERRX output delay		10.93	ns
t_dNSERR	PCLK to NSERR output delay		10.93	ns
T_{su}ALL	All inputs setup to PCLK	5		ns
T_hALL	All inputs hold from PCLK	1.1		ns

Notes:
1. All outputs are loaded with 50pf.

Table 10. USB Interface Timings

Parameter	Description	Min	Max	Units
USBVPX	Differential data positive	4	20	ns
USBVPM	Differential data negative	4	20	ns

Table 11. Radio MAC AC Timings – Intersil Modes

Parameter	Parameter Description	Min	Max	Units
t_dBBAS	BBAS output delay from falling BBSCLK		8.2	ns
t_dBBRNW	BBRNW output delay from falling BBSCLK		8.0	ns
t_dnBBCS	nBBCS output delay from falling BBSCLK		59.0	ns
t_dBBSDX	BBSDX output delay from falling BBSCLK		7.0	ns
T_{su}BBSDX	BBSDX setup to rising edge of BBSCLK	14.8		ns
T_hBBSDX	BBSDX hold from rising edge of BBSCLK	0.0		ns
t_dTXD	TXD output delay from rising TXCLK (SMAC Mode)		33.5	ns
t_dTXD	TXD output delay from rising TXCLK (RMAC Mode)		15.4	ns
T_{su}RXD	RXD setup to rising edge of RXCLK	1.0		ns
T_hRXD	RXD hold from rising edge of RXCLK	1.8		ns
T_{su}MDRDY	MDRDY setup to falling edge of RXCLK	2		ns
T_hMDRDY	MDRDY hold from falling edge of RXCLK	1		ns
t_dTXPEBB	TXPEBB output delay from rising TXCLK		15.0	ns
t_dRXPEBB	RXPEBB output delay from rising RXCLK		16.0	ns
T_{su}TXRDY	TXRDY setup to falling edge of TXCLK	6.5		ns
T_hTXRDY	TXRDY hold from falling edge of TXCLK	0		ns
T_{duty}RXCLK [2]	RXCLK period	See Note		ns
T_{duty}TXCLK [2]	TXCLK period	See Note		ns

Notes:
1. CCA signal is double synchronized to ARMCLKIN.
2. ARMCLK must be at least 4 times the TXCLK and RXCLK frequency.
3. Harris baseband (3824/3824A) generates RXCLK and TXCLK of 4 Mhz. the duty cycle varies between 33-40% with a high time of 90.9ns and low time that alternates between 136 and 182ns. The clock period varies between 227 and 272 ns, giving an effective period of 250ns.
4. TXD delay in 802.11b mode is the result of sampling the TXCLK with the ctlclk, therefore the maximum delay is equal to two ctlclk periods plus the flop-to-output delay. In this table, ctlclk is assumed to have a 13 ns period.
5. BBNCS output delay = [(1/ARMCLK freq)*ceiling(SER_CLK_DIV/2)] + 7ns, the specified value is based on ARMCLK of 77 Mhz and SER_CLK_DIV=8.

Table 12. Radio MAC AC Timings – RFMD Modes

Parameter	Parameter Description	Min	Max	Units
t_dBBRNW	BBRNW output delay from falling BBSCLK		6.7	ns
t_dnBBCS	nBBCS output delay from falling BBSCLK		110.79	ns
t_dBBSDX	BBSDX output delay from falling BBSCLK		7.0	ns
T_{su}BBSDX	BBSDX setup to rising edge of BBSCLK	14.5		ns
T_hBBSDX	BBSDX hold from rising edge of BBSCLK	0.0		ns
t_dTXD	TXD output delay from rising TXCLK (SMAC Mode)		33.5	ns
t_dTXD	TXD output delay from rising TXCLK (RMAC Mode)		15.4	ns
T_{su}RXD	RXD setup to rising edge of RXCLK	1.0		ns
T_hRXD	RXD hold from rising edge of RXCLK	1.8		ns
T_{su}MDRDY	MDRDY setup to falling edge of RXCLK	2		ns
T_hMDRDY	MDRDY hold from falling edge of RXCLK	1		ns
t_dTXPEBB	TXPEBB output delay from rising TXCLK		15.0	ns
t_dRXPEBB	RXPEBB output delay from rising RXCLK		16.0	ns
T_{su}TXRDY	TXRDY setup to falling edge of TXCLK	6.5		ns
T_hTXRDY	TXRDY hold from falling edge of TXCLK	0		ns

Notes:
1. CCA signal is double synchronized to ARMCLKIN.
2. ARMCLK must be at least 4 times the TXCLK and RXCLK frequency.
3. TXD delay in 802.11b mode is the result of sampling the TXCLK with the ctlclk, therefore the maximum delay is equal to two ctlclk periods plus the flop-to-output delay. In this table, ctlclk is assumed to have a 13 ns period.
4. BBNCS output delay = [(1/ARMCLK freq)*ceiling(SER_CLK_DIV/2)] + 7ns, the specified value is based on ARMCLK of 77 Mhz and SER_CLK_DIV=8.

5.2 Table 13. Package Specifications

Symbol	Parameter	Value	Units
θ_{JC}	Junction-to-Case Thermal Resistance	2.5	°C/W
θ_{JA}	Junction-to-Open Air Thermal Resistance	26.9	°C/W
T_{J_MAX}	Max Junction Temperature	105	°C

Notes:
1. ARMCLK / MEMCLK = 77MHz

6 Packaging

The CS22230 controller is available in a 208 Fine Pitch Ball Grid Array (FPBGA) package. Figure 8 contains the package mechanical drawing.

Figure 8. CS22230 FPBGA-pin Mechanical Drawing