HDMI Source/Sink Port Protection and Interface Device

Features

- Long HDMI cable support with integrated I^2C accelerator
- Low Capacitance DDC for HDMI Compliance
- Improved CEC Signal Quality and Compatibility
- Translates I^2C level to CMOS level on DDC line
- Overcurrent output protection for Source
- 5V Diode Bridge for EEPROM for Sink
- Level shifting isolation circuitry, including ±8kV ESD protection on all external I/O lines
- Backdrive protection and Isolation <5µA on all pins

Applications

- PC and Consumer Electronics
- Set Top Box, DVDRW Players
- Consumer Electronics
- Displays and Digital Television

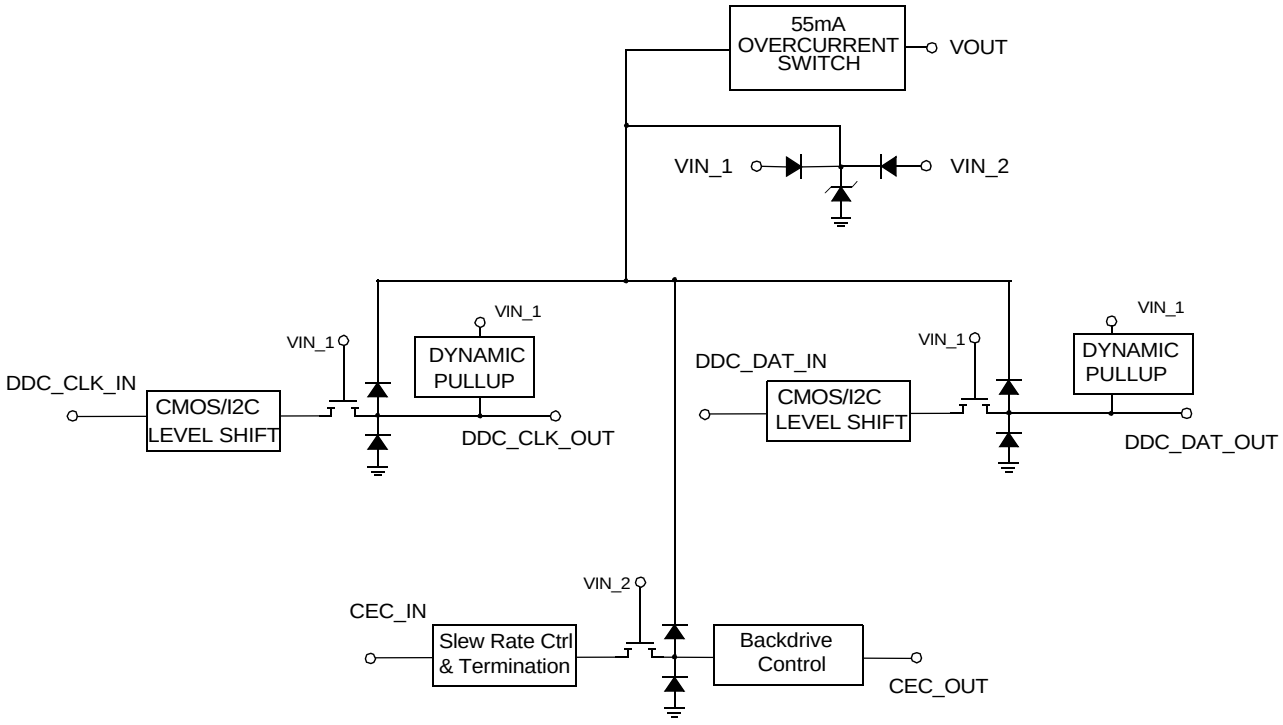
Product Description

The CM20LT-C HDMI Port Protection and Interface Device is designed for next generation HDMI Source and Sink interface protection.

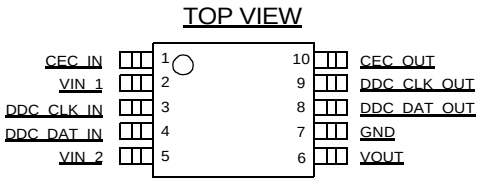
An integrated package provides complete low capacitance ESD, level shifting/isolation, slew rate limiting and terminations, overcurrent output protection, EEPROM and backdrive protection to ensure HDMI Compliance in a single 10-Pin MSOP package.

The CM20LT-C part is specifically designed to provide the designer with the most reliable path to HDMI 1.3 CTS compliance.

Electrical Schematic



PACKAGE / PINOUT DIAGRAM



Note: This drawing is not to scale. 10-PIN MSOP PACKAGE

PIN DESCRIPTIONS

PINS	NAME	ESD Level	DESCRIPTION
2	VIN_1	2kV[4]	System Side Voltage Supply. This pin provides power to VOUT when VIN_2 is "off". VIN_1 also enables/disables backdrive isolation protection on the DDC lines when VIN_1 is "off."
5	VIN_2	8kV[3]	Cable Side Voltage Supply. This pin provides power to VOUT when VIN_1 is "off". VIN_2 also provides supply current for the CEC slew-rate limiting and termination logic.
1	CEC_IN	2kV[4]	Bi-directional System Side CEC Input from uP.
10	CEC_OUT	8kV[3]	Bi-directional Cable Side CEC Output (VIN_2=3.3V referenced logic level) plus 3.5pF ESD. Includes Long Cable accelerator/driver. Connect to HDMI Pin 13.
3	DDC_CLK_IN	2kV[4]	Bi-directional System Side (VIN_1 referenced logic level). Includes CMOS low-level shifter for guaranteed local V_{OL}.
9	DDC_CLK_OUT	8kV[3]	Bi-directional Cable Side (VIN_2 referenced logic level) plus 3.5pF ESD. Includes Long Cable accelerator/driver. Connect to HDMI Pin 15.
4	DDC_DAT_IN	2kV[4]	Bi-directional System Side (VIN_1 referenced logic level). Includes CMOS low-level shifter for guaranteed local V_{OL}.
8	DDC_DAT_OUT	8kV[3]	Bi-directional Cable Side (VIN_2 referenced logic level) plus 3.5pF ESD. Includes Long Cable accelerator/driver. Connect to HDMI Pin 16.
6	VOUT	8kV[3]	55mA minimum overcurrent protected 5V output.This output must be bypassed with a 0.1µF ceramic capacitor. For Source, connect this to HDMI Pin. For Sink, use this to replace a diode bridge for local and external power to the E-EDID EEPROM.
7	GND	N/A	GND reference.

Note 1: These 2 pins need to be connected together in-line on the PCB. See recommended layout diagram.

Note 2: This output can be connected to an external 0.1µF ceramic capacitor/pads to mainatain backward compatibility with the CM2020.

Note 3: Standard IEC 61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω, VIN_2 and VIN_1 within recommended operating conditions, GND=0V, 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1µF ceramic capacitor connected to GND.

Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{DISCHARGE}$=100pF, $R_{DISCHARGE}$=1.5kΩ, VIN_2and VIN_1 within recommended operating conditions, GND=0V, 5V_OUT (pin 38), and HOTPLUG_DET_OUT (pin 20) each bypassed with a 0.1µF ceramic capacitor connected to GND.

Note 5: These pins should be routed directly to the associated GND pins on the HDMI connector with single point ground vias at the connector

Backdrive Protection and Isolation

Backdrive current is defined as the undesirable current flow through an I/O pin when that I/O pin's voltage exceeds the related local supply voltage for that circuitry. This is a potentially common occurrence in multimedia entertainment systems with multiple components and several power plane domains in each system.

For example, if a DVD player is switched off and an HDMI connected TV is powered on, there is a possibility of reverse current flow back into the main power supply rail of the DVD player from pull-ups in the TV. As little as a few milliamps of backdrive current flowing back into the power rail can charge the DVD player's bulk bypass capacitance on the power rail to some intermediate level. If this level rises above the power-on-reset (POR) voltage level of some of the integrated circuits in the DVD player, then these devices may not reset properly when the DVD player is turned back on.

If any SOC devices are incorporated in the design which have built-in level shifter and/or ESD protection structures, there can be a risk of permanent damage due to backdrive. In this case, backdrive current can forward bias the on-chip ESD protection structure. If the current flow is high enough, even as little as a few milliamps, it could destroy one of the SOC chip's internal DRC diodes, as they are not designed for passing DC.

To avoid either of these situations, the CM20LT-C was designed to block backdrive current, guaranteeing less than 5µA into any I/O pin when the I/O pin voltage exceeds its related operating CM20LT-C supply voltage.

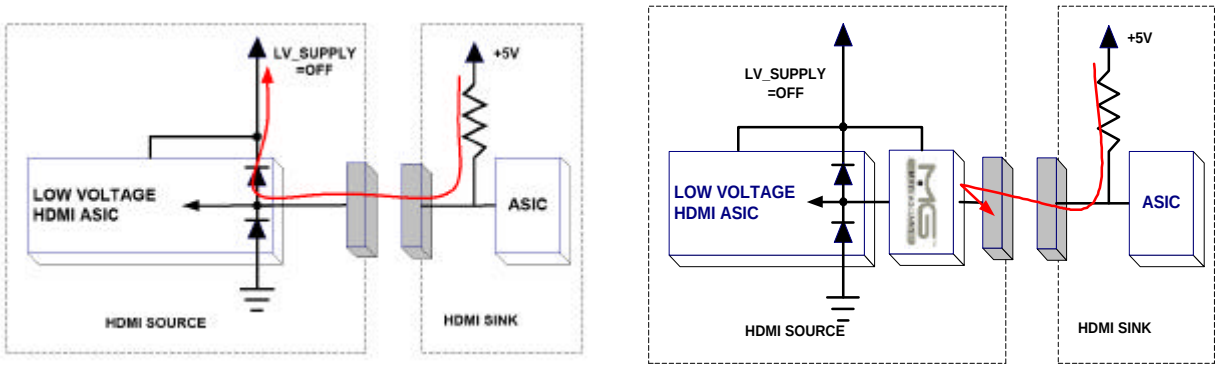


Figure 1. Backdrive Protection Diagram.

Display Data Channel (DDC) lines

The DDC interface is based on the I^2C serial bus protocol for EDID configuration.

DYNAMIC PULLUPS

Based on the HDMI specification, the maximum capacitance of the DDC line can approach 800pF (50pF from source, 50pF from sink, and 700pF from cable). At the upper range of capacitance values (i.e. long cables), it becomes impossible for the DDC lines to meet the I^2C timing specifications with the minimum pull-up resistor of 1.5k Ω.

For this reason, the CM20LT-C was designed with an internal I^2C accelerator to meet the AC timing specification even with very long and non-compliant cables.

The internal accelerator increases the positive slew rate of the DDC_CLK_OUT and DDC_DAT_OUT lines whenever the sensed voltage level exceeds 0.3*VIN_2 (approximately 1.5V). This provides faster overall rise-time in heavily loaded situations without overloading the mutli-drop open drain I^2C outputs elsewhere.

DYNAMIC PULLUPS (CONT'D)

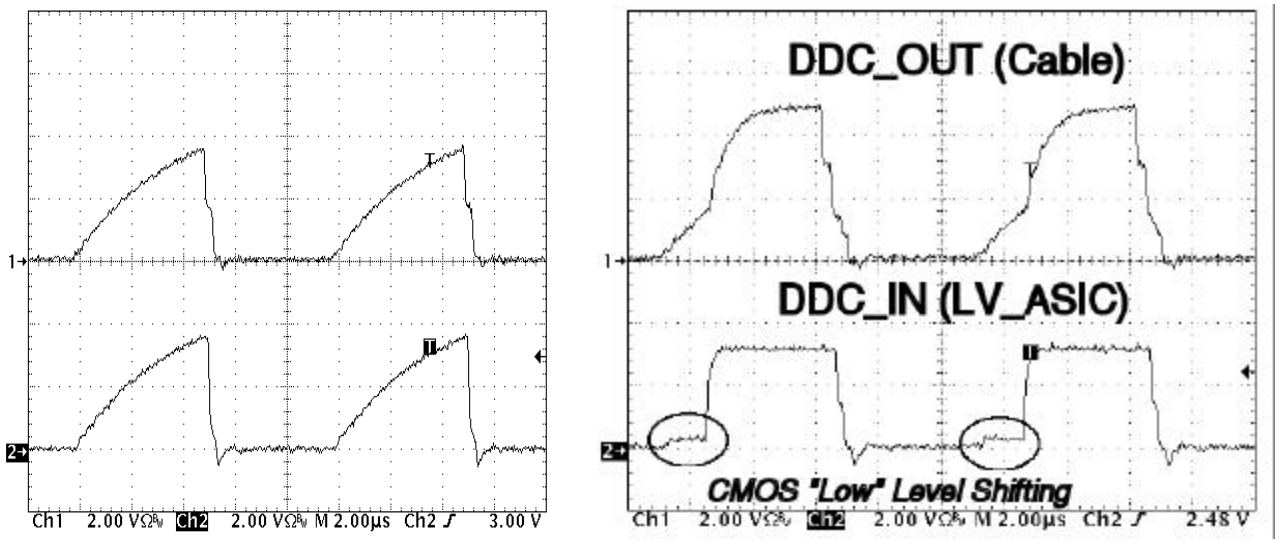


Figure 2. Dynamic DDC Pullups *(Discrete - Left. CM20LT-C - Right.)*

Figure 2 demonstrates the "worst case" operation of the dynamic CM20LT-C DDC level shifting circuitry (right) against a discrete NFET common-gate level shifter circuit with a typical 1.5k pullup (left.) Both are shown driving an off-spec, but unfortunately readily available 31m HDMI cable which exceeds the 700pF HDMI specification.

When the standard I/OD cell releases the NFET discrete shifter, the risetime is limited by the pullup and the parasitics of the cable, source and sink. For long cables, this can extend the risetime and reduce the margin for reading a valid "high" level on the data line. In this case, an HDMI source may not be able to read uncorrupted data and will not be able to initiate a link.

With the CM20LT-C's dynamic pullups, when the ASIC driver releases its DDC line and the "OUT" line reaches at least 0.3*VDD (of VIN_2), then the "OUT" active pullups are enabled and the CM20LT-C takes over driving the cable until the "OUT" voltage approaches the VIN_2 rail.

The internal pass element and the dynamic pullups also work together to damp reflections on the longer cables and keep them from glitching the local ASIC.

I^2C/CMOS LEVEL SHIFTING

Using a standard CMOS input buffer for the DDC interface on the local HDMI ASIC can create a failure to communicate at the specified I^2C levels. With an I^2C VIL of approximately 1.5V (0.3*VDD), and typical CMOS/TTL VIL input levels of 0.8V or less, an incompatibility can arise where valid HDMI specified logic lows on the cable are not recognized within the ASIC.

The CM20LT-C incorporates automatic CMOS/I^2C logic low translation on the DDC_CLK_IN and DDC_DAT_IN lines.

As highlighted in Figure 2 above, when the cable-side level ("OUT" side) of each DDC line is below 0.3*VDD, the ASIC-side ("IN" side) of the DDC line is forced to a CMOS low-level while the "OUT" side is allowed to slew normally.

The CM20LT-C dynamic pullups, low level shifters, and pass element shifters are all matched to allow transparent operation. This bi-directional circuit can be used as easily as any discrete common-gate NFET level shifter, but with the added functionality.

Multiport DDC Multiplexing

Additionally, by switching VIN_1, the DDC/HPD blocks can be independently disabled by engaging their inherent "backdrive" protection. This allows N:1 multiplexing of the low-speed HDMI signals without any additional FET switches.

Consumer Electronics Control (CEC)

The Consumer Electronics Control (CEC) line is a high level command and control protocol, based on a single wire multidrop open drain communication bus running at approximately 1kHz (See Figure 3). While the HDMI link provides only a single point-to-point connection, up to ten (10) CEC devices may reside on the bus, and they may be daisy chained out through other physical connectors including other HDMI ports or other dedicated CEC links. The high level protocol of CEC can be implemented in a simple microcontroller or other interface with any I/OD (input/open-drain) GPIO.

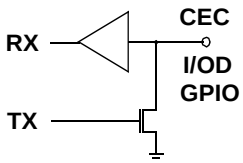


Figure 3. Typical μC I/OD Driver

To limit possible EMI and ringing in this potentially complex connection topology, the rise- and fall-time of this line are limited by the specification. However, meeting the slew-rate limiting requirements with additional discrete circuitry in this bi-directional block is not trivial without an additional RX/TX control line to limit the output slew-rate without affecting the input sensing (See Figure 4).

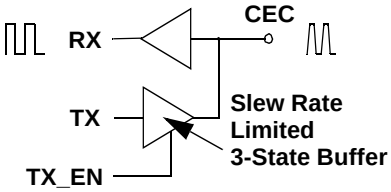


Figure 4. Three-Pin External Buffer Control

Simple CMOS buffers cannot be used in this application since the load can vary so much (total pullup of 27kΩ to less than 2kΩ, and up to 7.3nF total capacitance.) The CM20LT-C targets an output drive slew-rate of less than 100mV/μs regardless of static load for the CEC line. Additionally, the same internal circuitry will perform active termination, thus reducing ringing and overshoot in entertainment systems connected to legacy or poorly designed CEC nodes.

The CM20LT-C's bi-directional slew rate limiting is integrated into the CEC level-shifter functionality thus allowing the designer to directly interface a simple low voltage CMOS GPIO directly to the CEC bus and simultaneously guarantee meeting all CEC output logic levels and HDMI slew-rate and isolation specifications (See Figure 5).

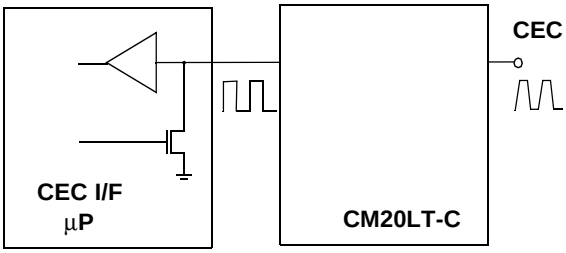


Figure 5. Integrated CM20LT-C Solution

The CM20LT-C also includes an internal backdrive protected static pullup 120μA current source from the CE_SUPPLY rail in addition to the dynamic slew rate control circuitry.

Figure 6 shows a typical shaped CM20LT-C CEC output.

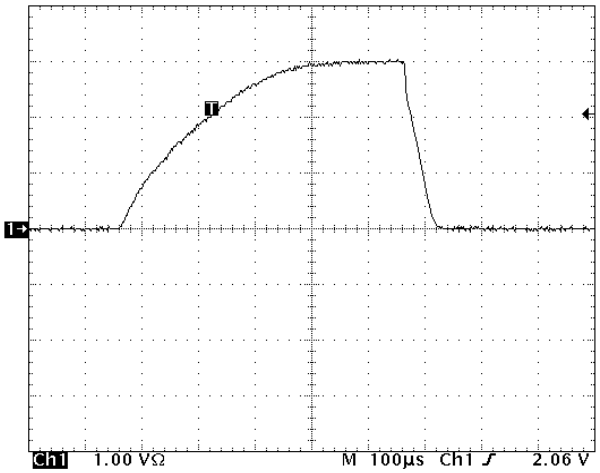


Figure 6. CM20LT-C CEC Output

Ordering Information

PART NUMBERING INFORMATION					
		Standard Finish		Lead-free Finish	
Pins	Package	Ordering Part Number[1]	Part Marking	Ordering Part Number[1]	Part Marking
10	MSOP-10	CM20LT-C-00TS	CM20LT-C-00TS	CM20LT-C-00TR	CM20LT-C-00TR

Note 1: Parts are shipped in Tape & Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
V_{CC2}, V_{CC1}	6.0	V
DC Voltage at any Channel Input	[GND - 0.5] to [VCC + 0.5]	V
Storage Temperature Range	-65 to +150	°C

STANDARD (RECOMMENDED) OPERATING CONDITIONS					
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VIN_2	Operating Supply Voltage		5	5.5	V
VIN_1	Bias Supply Voltage	1	3.3	5.5	V
	Operating Temperature Range	-40		85	°C

Specifications (cont'd)

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)						
SYMBOL	**PARAMETER**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
I_{CC2}	Operating Supply Current	VIN_2= 5.0V, VIN_1= 3.3V, DDC=5V		250		µA
I_{CC1}	Bias Supply Current	VIN_1 = 3.3V		10		µA
V_{DROP}	5V_OUT Overcurrent Output Drop	VIN_@= 5.0V, I_{OUT}=55mA		65	100	mV
I_{SC}	5V_OUT Short Circuit Current Limit	VIN_2= 5.0V, VOUT = GND	90	135	175	mA
I_{OFF}	OFF state leakage current, level shifting NFET	VIN_1 = 0V		0.1	5	µA
$I_{BACKDRIVE}$	Current conducted from output pins to V_SUPPLY rails when powered down	VIN_2 < V_{CH_OUT}; Signal pins: TMDS_[2:0]+/-, TMDS_CK+/-, CE_REMOTE_OUT, DDC_DAT_OUT, DDC_CLK_OUT, HOTPLUG_DET_OUT, 5V_OUT Only		0.1		µA
V_{ACC}	Turn On of I^2C Accelerator	Voltage is 0.3*VIN2		1.5		V
V_F	Diode Forward Voltage Top Diode Bottom Diode	I_F = 8mA, T_A = 25°C, Note 2	 0.6 0.6	 0.85 0.85	 0.95 0.95	 V V
V_{ESD}	ESD Withstand Voltage (IEC)	Pins 4, 7, 10, 13, 20, 21, 22, 23, 24, 27, 30, 33; Notes 2 and 3	±8			kV
V_{ESD}	ESD Withstand Voltage (HBM)	Pins 1, 2, 16, 17, 18, 19, 37, 38; Notes 2 and 4	±2			kV
V_{CL}	Channel Clamp Voltage @ 8kV HBM ESD Positive Transients Negative Transients	T_A=25°C, I_{PP} = 1A, t_P = 8/20uS; Notes 2, & 6		 9.0 -9.0		 V V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	T_A=25°C, I_{PP} = 1A, t_P = 8/20uS Any I/O pin to Ground; Note 6		 1.4 0.9		 Ω Ω
I_{LEAK}	Channel Leakage Current	T_A = 25°C, Note 2		0.01	1	µA
$C_{IN,}$ DDC	Level Shifting Input Capacitance, Capacitance to GND	VIN_2= 0V, Measured at 100KHz, V_{BIAS}=2.5V, Note 2		3.5		pF

Note 1: Operating Characteristics are over Standard Operating Conditions unless otherwise specified.
Note 2: This parameter is guaranteed by design and verified by device characterization.
Note 3: Standard IEC61000-4-2, $C_{DISCHARGE}$=150pF, $R_{DISCHARGE}$=330Ω, VIN_2=5V, 3.3V_SUPPLY=3.3V, VIN_1=3.3V, GND=0V.
Note 4: Human Body Model per MIL-STD-883, Method 3015, $C_{DISCHARGE}$=100pF, $R_{DISCHARGE}$=1.5kΩ, VIN_2=5V, 3.3V_SUPPLY=3.3V, VIN_1=3.3V, GND=0V.
Note 5: Intra-pair matching, each TMDS pair (i.e. D+, D-)
Note 6: These measurements performed with no external capacitor on V_P (V_P floating)

Application Information (SOURCE)

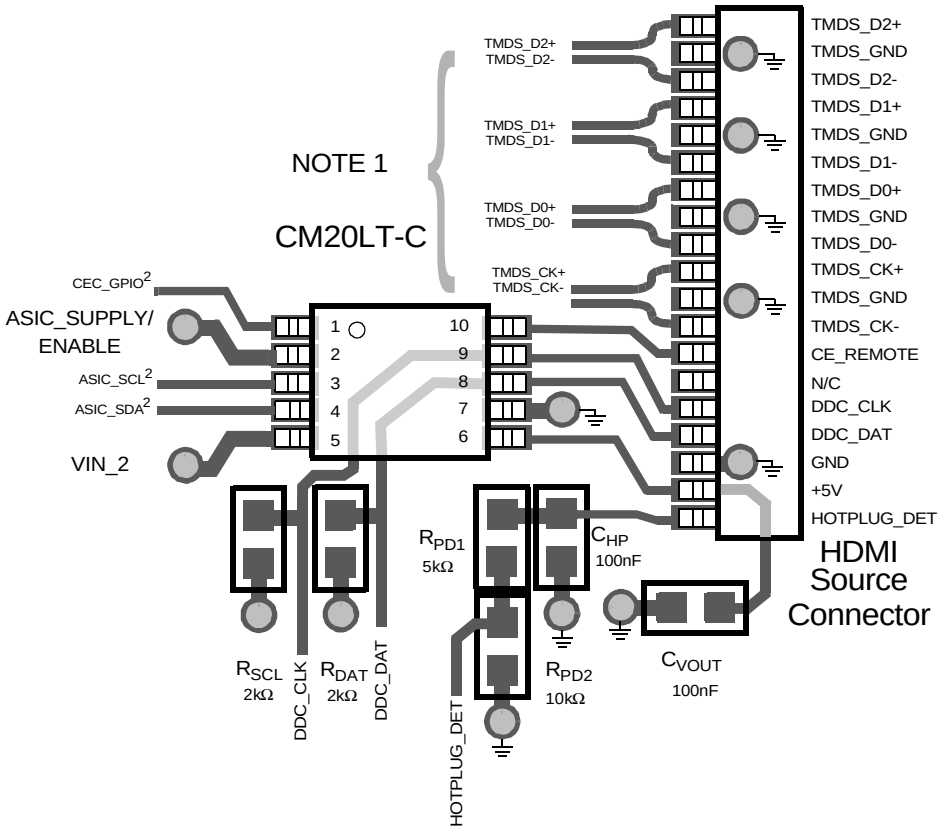


Figure 7. Typical Source Application for CM20LT-C

LAYOUT NOTES

[1] **Differential TMDS Pairs should be designed as normal** 100W **HDMI Microstrip, with CMD PicoGuard CM1213-04MS/MRESD Protection or equivalent.**

[2] Level Shifter signals should be biased with a weak pullup to the desired local VIN_1. If the local ASIC includes sufficient pullups to register a logic high, then external pullups may not be needed.

Application Information (SINK)

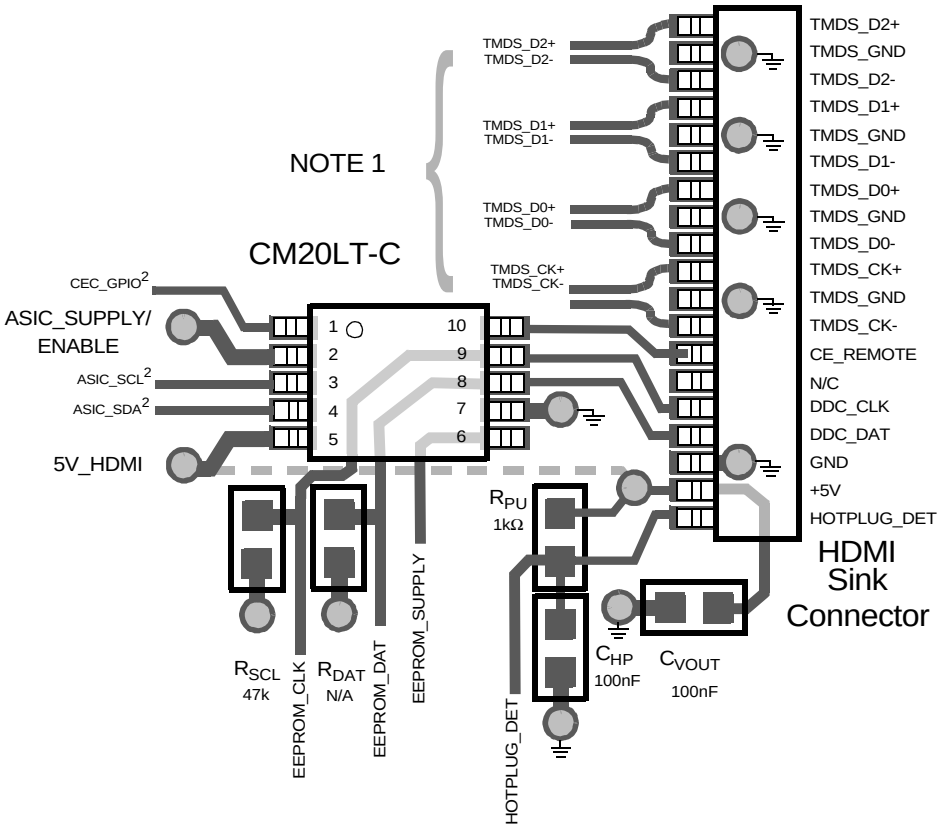


Figure 8. Typical Sink Application for CM20LT-C

LAYOUT NOTES

[1] **Differential TMDS Pairs should be designed as normal** 100W **HDMI Microstrip, with CMD PicoGuard CM1213-04MS/MRESD Protection or equivalent.**

[2] Level Shifter signals should be biased with a weak pullup to the desired local VIN_1. If the local ASIC includes sufficient pullups to register a logic high, then external pullups may not be needed.