

ACT-SF512K32 High Speed 512Kx32 SRAM / 512Kx32 Flash Multichip Module



FEATURES

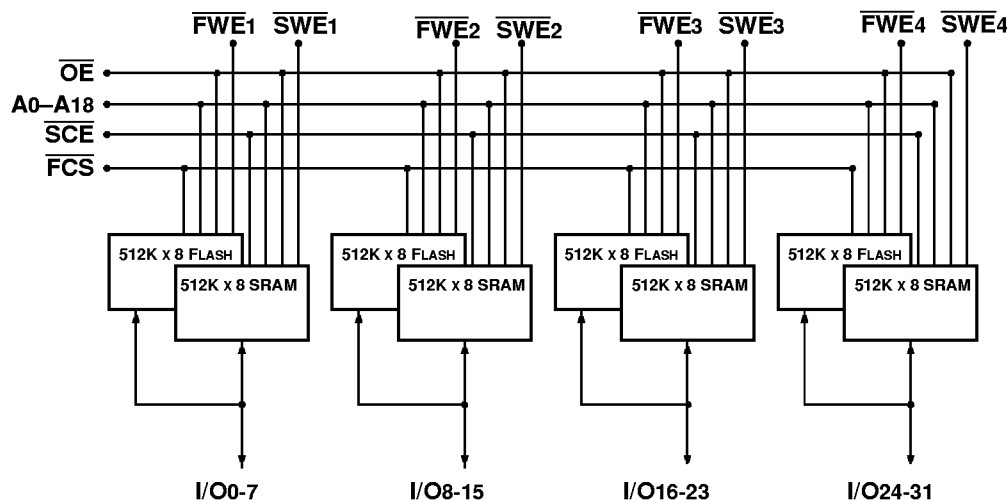
- 4 – 512K x 8 SRAMs & 4 – 512K x 8 Flash Die in One MCM
- Access Times of 25ns, 35ns (SRAM) and 60ns, 70ns, 90ns (Flash)
- Organized as 512K x 32 of SRAM and 512K x 32 of Flash Memory with Common Data Bus
- Low Power CMOS
- Input and Output TTL Compatible Design
- MIL-PRF-38534 Compliant MCMs Available
- Decoupling Capacitors and Multiple Grounds for Low Noise
- Commercial, Industrial and Military Temperature Ranges
- Industry Standard Pinouts
- TTL Compatible Inputs and Outputs
- Packaging – Hermetic Ceramic
 - 66-Lead, PGA-Type, 1.385"SQ x 0.245"max, Aeroflex code# "P1,P5 with/without shoulders"
 - 68-Lead, Dual-Cavity CQFP(F2), 0.88"SQ x .20"max (.18 max thickness available, contact factory for details) (*Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint*)

FLASH MEMORY FEATURES

- Sector Architecture (Each Die)
 - 8 Equal Sectors of 64K bytes each
 - Any combination of sectors can be erased with one command sequence
- +5V Programming, +5V Supply
- Embedded Erase and Program Algorithms
- Hardware and Software Write Protection
- Page Program Operation and Internal Program Control Time.
- 10,000 Erase/Program Cycles



Block Diagram – PGA Type Package(P1 & P5) & CQFP(F2)



PIN DESCRIPTION

I/O0-31	Data I/O
A0-18	Address Inputs
FWE1-4	Flash Write Enables
SWE1-4	SRAM Write Enables
FCE	Flash Chip Enable
SCE	SRAM Chip Enable
OE	Output Enable
NC	Not Connected
Vcc	Power Supply
GND	Ground

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T_C	Operating Temperature	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C
V_G	Maximum Signal Voltage to Ground	-0.5 to +7	V
T_L	Maximum Lead Temperature (10 seconds)	300	°C

Parameter	
Flash Data Retention	10 Years
Flash Endurance (Write/Erase Cycles)	10,000

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V_{CC}	Power Supply Voltage	+4.5	+5.5	V
V_{IH}	Input High Voltage	+2.2	$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage	-0.5	+0.8	V

Capacitance

($V_{IN} = 0V$, $f = 1MHz$, $T_C = 25^\circ C$)

Symbol	Parameter	Maximum	Units
C_{AD}	$A_0 - A_{18}$ Capacitance	80	pF
C_{OE}	$\overline{OE}$ Capacitance	80	pF
C_{WE1-4}	F/S Write Enable Capacitance	30	pF
C_{CE}	F/S Chip Enable Capacitance	50	pF
$C_{I/O}$	I/O ₀ – I/O ₃₁ Capacitance	30	pF

This parameter is guaranteed by design but not tested

DC Characteristics

($V_{CC} = 5.0V$, $V_{SS} = 0V$, $T_C = -55^\circ C$ to $+125^\circ C$)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	$V_{CC} = \text{Max}$, $V_{IN} = 0$ to V_{CC}		10	μA
Output Leakage Current	I_{LO}	$\overline{FCE} = \overline{SCE} = V_{IH}$, $\overline{OE} = V_{IH}$, $V_{OUT} = 0$ to V_{CC}		10	μA
SRAM Operating Supply Current x 32 Mode	I_{CCx32}	$\overline{SCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = \text{Max}$, $\overline{FCE} = V_{IH}$		550	mA
Standby Current	I_{SB}	$\overline{FCE} = \overline{SCE} = V_{IH}$, $\overline{OE} = V_{IH}$, $f = 5MHz$, $V_{CC} = \text{Max}$		80	mA
SRAM Output Low Voltage	V_{OL}	$I_{OL} = 8 \text{ mA}$, $V_{CC} = \text{Min}$, $\overline{FCE} = V_{IH}$		0.4	V
SRAM Output High Voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$, $V_{CC} = \text{Min}$, $\overline{FCE} = V_{IH}$	2.4		V
Flash Vcc Active Current for Read (1)	I_{CC1}	$\overline{FCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCE} = V_{IH}$		260	mA
Flash Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{FCE} = V_{IL}$, $\overline{OE} = V_{IH}$, $\overline{SCE} = V_{IH}$		300	mA
Flash Output Low Voltage	V_{OL}	$I_{OL} = 12 \text{ mA}$, $V_{CC} = \text{Min}$, $\overline{SCE} = V_{IH}$		0.45	V
Flash Output High Voltage	V_{OH1}	$I_{OH} = -2.5 \text{ mA}$, $V_{CC} = \text{Min}$, $\overline{SCE} = V_{IH}$	$0.85 \times V_{CC}$		V
Flash Low Vcc Lock Out Voltage	V_{LKO}		3.2	4.2	V

Notes: 1) The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5MHz). The frequency component typically is less than 2mA/MHz, with $\overline{OE}$ at V_{IH} 2) I_{CC} active while Embedded Algorithm (program or erase) is in progress 3) DC test conditions: $V_{IL} = 0.3V$, $V_{IH} = V_{CC} - 0.3V$

SRAM AC Characteristics

(V_{CC} = 5.0V, V_{SS} = 0V, T_C = -55°C to +125°C)

Read Cycle

Parameter	Symbol	-025		-035		Units
		Min	Max	Min	Max	
Read Cycle Time	t _{RC}	25		35		ns
Address Access Time	t _{AA}		25		35	ns
Chip Select Access Time	t _{ACE}		25		35	ns
Output Hold from Address Change	t _{OH}	0		0		ns
Output Enable to Output Valid	t _{OE}		12		25	ns
Chip Select to Output in Low Z *	t _{CLZ}	2		4		ns
Output Enable to Output in Low Z *	t _{OLZ}	0		0		ns
Chip Deselect to Output in High Z *	t _{CHZ}		12		15	ns
Output Disable to Output in High Z *	t _{OHZ}		12		15	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Symbol	-025		-035		Units
		Min	Max	Min	Max	
Write Cycle Time	t _{WC}	25		35		ns
Chip Select to End of Write	t _{CW}	17		25		ns
Address Valid to End of Write	t _{AW}	17		25		ns
Data Valid to End of Write	t _{DW}	13		20		ns
Write Pulse Width	t _{WP}	17		25		ns
Address Setup Time	t _{AS}	2		2		ns
Output Active from End of Write *	t _{OW}	4		4		ns
Write to Output in High Z *	t _{WHZ}		13		15	ns
Data Hold from Write Time	t _{DH}	0		0		ns
Address Hold Time	t _{AH}	0		0		ns

* Parameters guaranteed by design but not tested

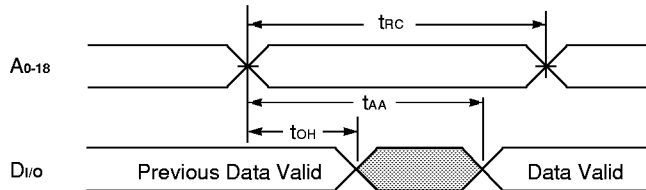
Truth Table

Mode	$\overline{\text{SCE}}$	$\overline{\text{OE}}$	$\overline{\text{SWE}}$	Data I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	Data Out	Active
Output Disable	L	H	H	High Z	Active
Write	L	X	L	Data In	Active

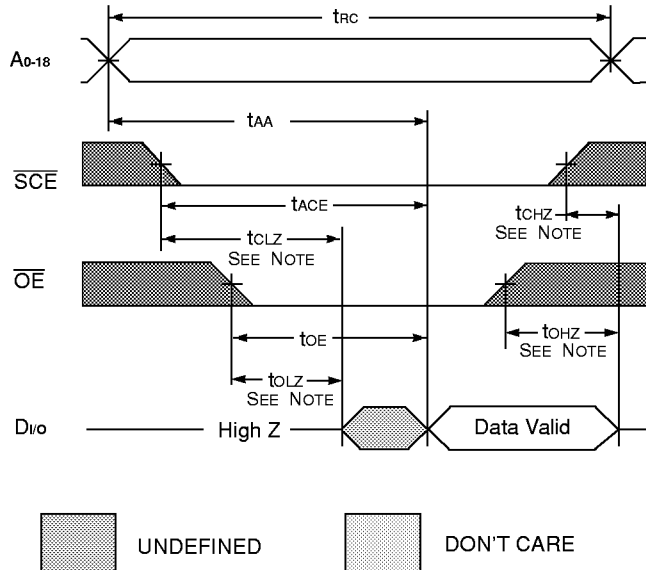
Timing Diagrams — SRAM

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{SCE} = \overline{OE} = V_{IL}$, $\overline{SWE} = V_{IH}$)

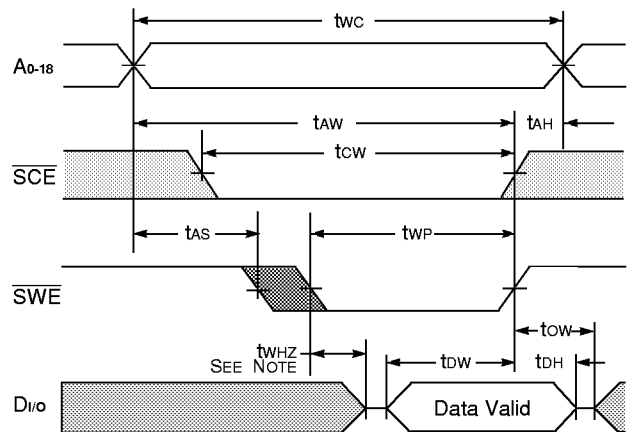


Read Cycle 2 ($\overline{SWE} = V_{IH}$)

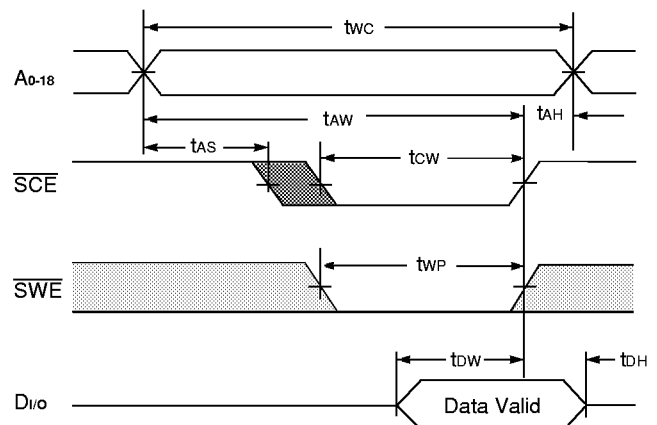


Write Cycle Timing Diagrams

Write Cycle ($\overline{SWE}$ Controlled, $\overline{OE} = V_{IH}$)

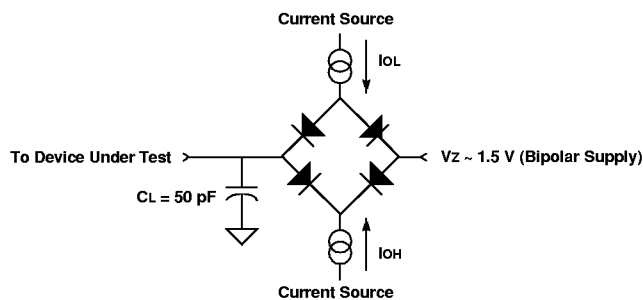


Write Cycle ($\overline{SCE}$ Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



AC Test Conditions

Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:

- 1) V_Z is programmable from -2V to +7V.
- 2) I_{OL} and I_{OH} programmable from 0 to 16 mA.
- 3) Tester Impedance $Z_O = 75\Omega$.
- 4) V_Z is typically the midpoint of V_{OH} and V_{OL} .
- 5) I_{OL} and I_{OH} are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Flash AC Characteristics – Read Only Operations

(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		ns
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90	ns
Chip Enable Access Time	t _{ELQV}	t _{CE}		60		70		90	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		30		35		35	ns
Chip Enable to Output High Z (1)	t _{EHQZ}	t _{DF}		20		20		20	ns
Output Enable High to Output High Z(1)	t _{GHQZ}	t _{DF}		20		20		20	ns
Output Hold from Address, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns

Note 1. Guaranteed by design, but not tested

Flash AC Characteristics – Write / Erase / Program Operations, $\overline{FWE}$ Controlled

(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAC}	t _{WC}	60		70		90		ns
Chip Enable Setup Time	t _{ELWL}	t _{CE}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	40		45		45		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	40		45		45		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		45		45		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Programming Operation	t _{WHWH1}		14	TYP	14	TYP	14	TYP	μs
Sector Erase Time	t _{WHWH2}			30		30		30	Sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{CC} Setup Time		t _{VCE}		50		50		50	μs
Chip Programming Time			50		50		50		Sec
Chip Enable Hold Time		t _{OE¹}	10		10		10		ns
Chip Erase Time	t _{WHWH3}			120		120		120	Sec

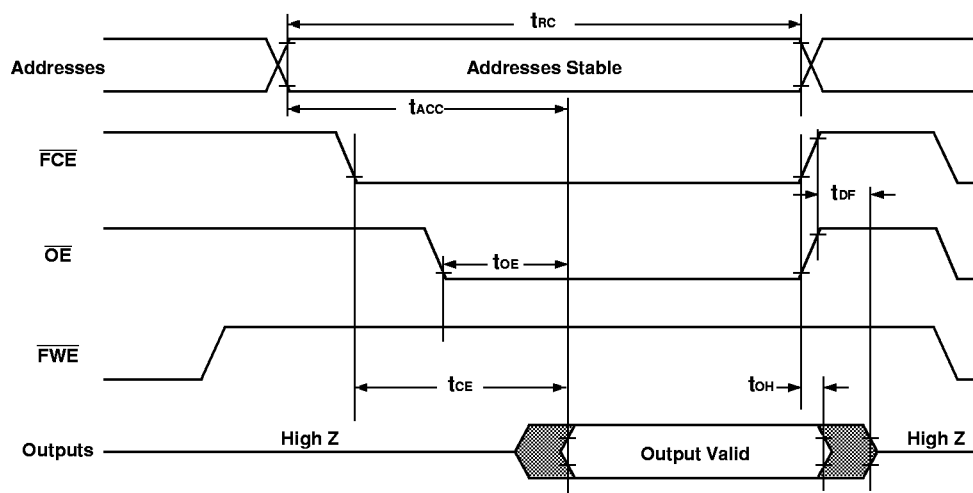
1. Toggle and Data Polling only.

Flash AC Characteristics – Write / Erase / Program Operations, $\overline{FCE}$ Controlled

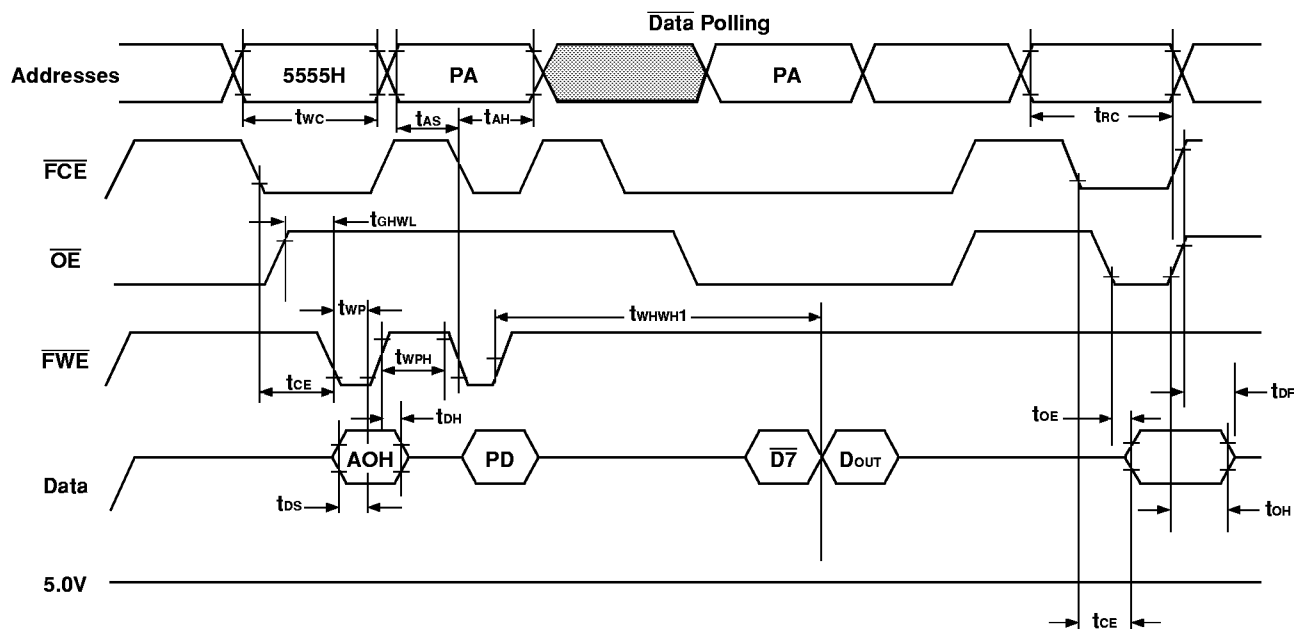
(V_{CC} = 5.0V, V_{SS} = 0V, T_c = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		Units
	JEDEC	Stand'd	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAC}	t _{WC}	60		70		90		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		ns
Chip Enable Pulse Width	t _{LEH}	t _{CP}	40		45		45		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	40		45		45		ns
Data Hold Time	t _{EHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		45		45		ns
Chip Enable Pulse Width High	t _{EH}	t _{CPH}	20		20		20		ns
Duration of Byte Programming	t _{WHWH1}		14	TYP	14	TYP	14	TYP	μs
Sector Erase Time	t _{WHWH2}			30		30		30	Sec
Read Recovery Time	t _{GH}		0		0		0		ns
Chip Programming Time				50		50		50	Sec
Chip Erase Time	t _{WHWH3}			120		120		120	Sec

AC Waveforms for Flash Memory Read Operations



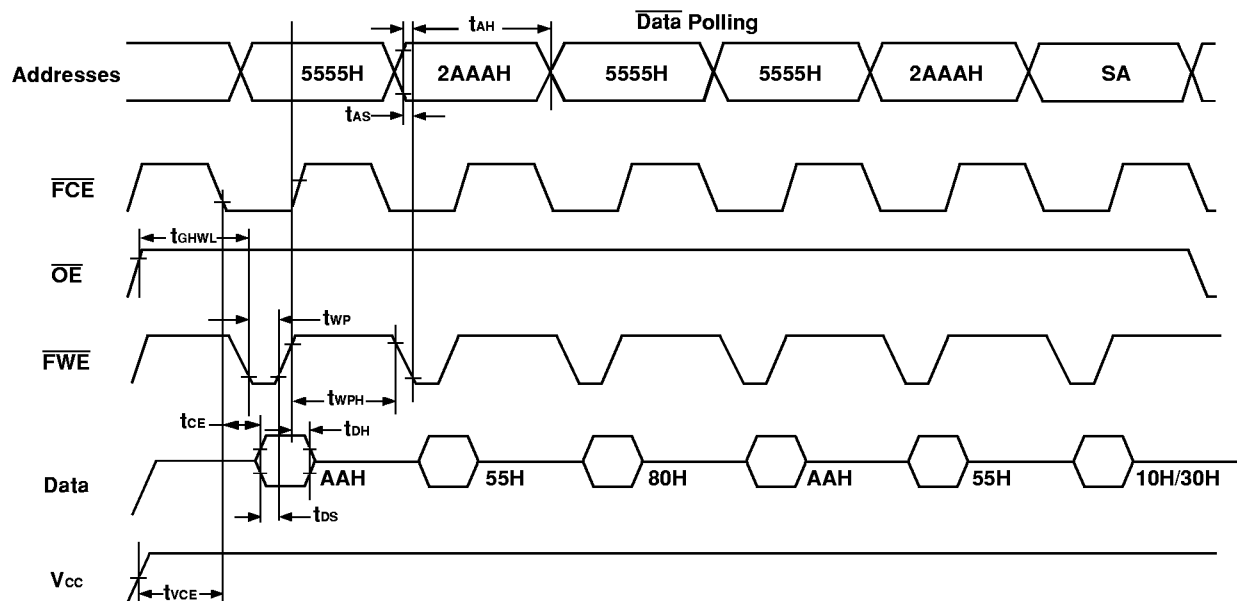
Write/Erase/Program Operation for Flash Memory, $\overline{FWE}$ Controlled



Notes:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the Output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

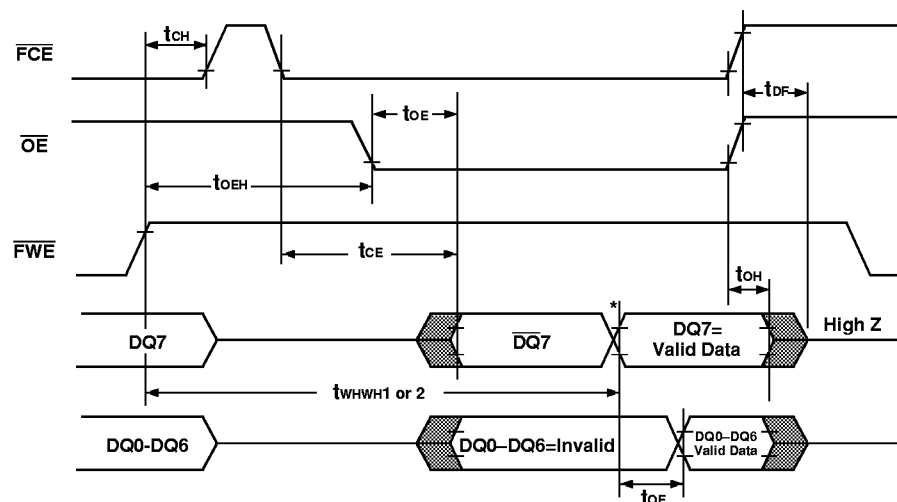
AC Waveforms Chip/Sector Erase Operations for Flash Memory



Notes:

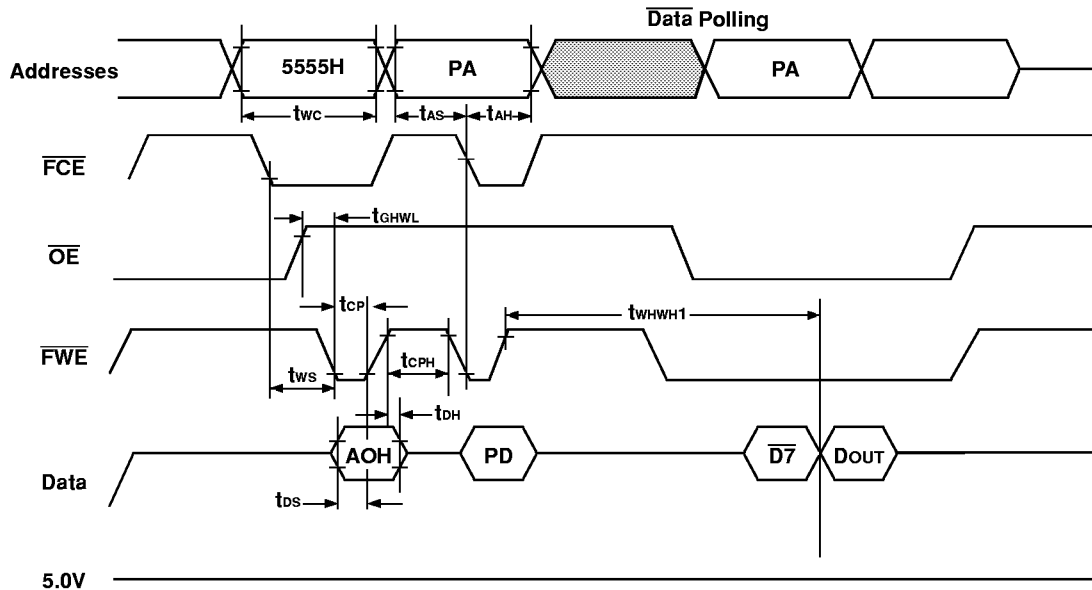
1. SA is the sector address for sector erase.

AC Waveforms for Data Polling During Embedded Algorithm Operations for Flash Memory



* DQ7=Valid Data (The device has completed the Embedded operation).

Write/Erase/Program Operation for Flash Memory, $\overline{\text{FCE}}$ Controlled



Notes:

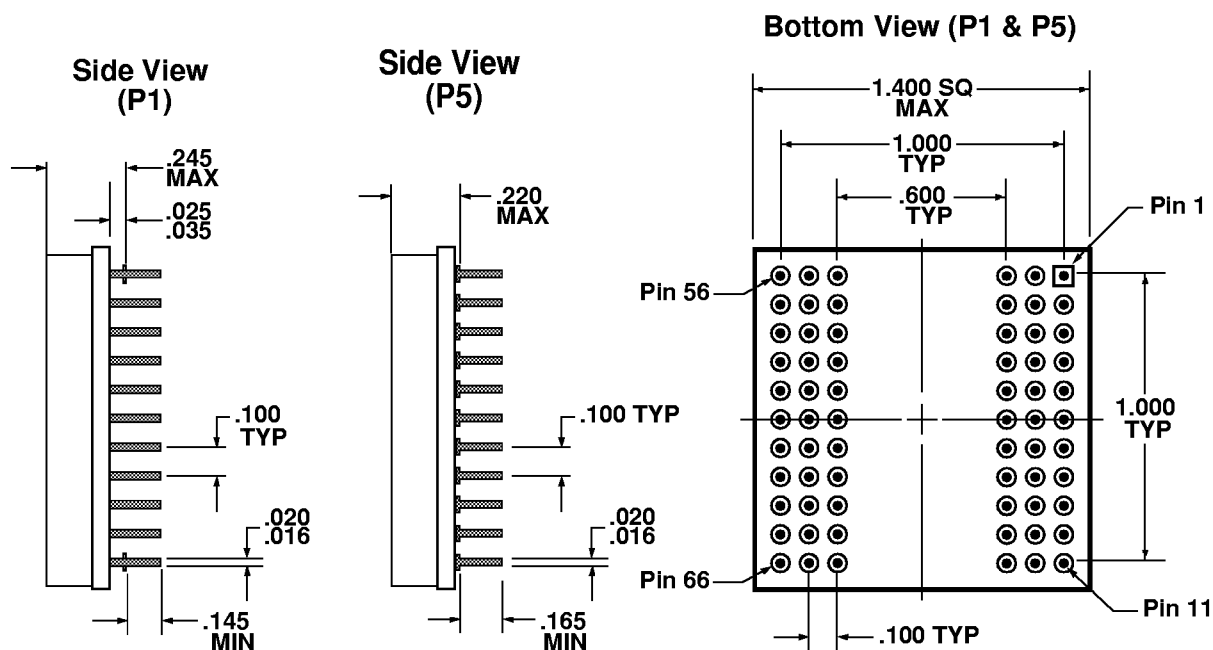
1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. $\overline{\text{D7}}$ is the Output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Pin Numbers & Functions

66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	18	A15	35	I/O25	52	$\overline{\text{FWE}}_3$
2	I/O9	19	V _{cc}	36	I/O26	53	$\overline{\text{SWE}}_3$
3	I/O10	20	$\overline{\text{FCE}}$	37	A7	54	GND
4	A14	21	$\overline{\text{SCE}}$	38	A12	55	I/O19
5	A16	22	I/O3	39	$\overline{\text{SWE}}_1$	56	I/O31
6	A11	23	I/O15	40	A13	57	I/O30
7	A0	24	I/O14	41	A8	58	I/O29
8	A18	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A1
10	I/O1	27	$\overline{\text{OE}}$	44	I/O18	61	A2
11	I/O2	28	A17	45	V _{cc}	62	A3
12	$\overline{\text{FWE}}_2$	29	$\overline{\text{FWE}}_1$	46	$\overline{\text{SWE}}_4$	63	I/O23
13	$\overline{\text{SWE}}_2$	30	I/O7	47	$\overline{\text{FWE}}_4$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A4	66	I/O20
16	A10	33	I/O4	50	A5		
17	A9	34	I/O24	51	A6		

"P1" — 1.385" SQ PGA Type Package Standard (with shoulders on Pins 1, 11, 56 & 66)

"P5" — 1.385" SQ PGA Type Special Order Package (without shoulders)



All dimensions in inches

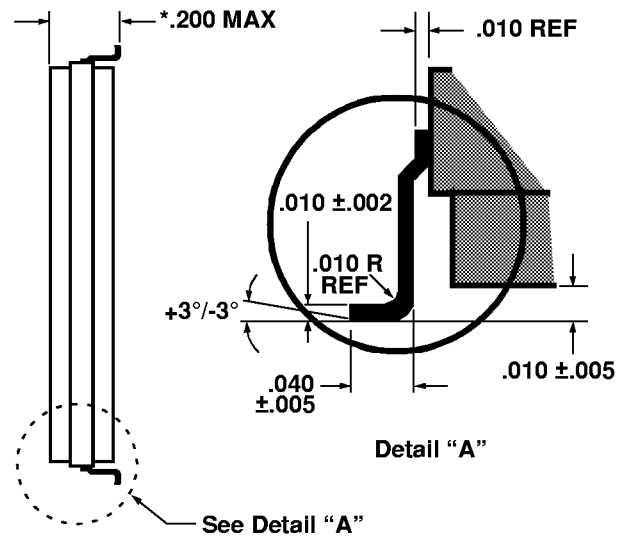
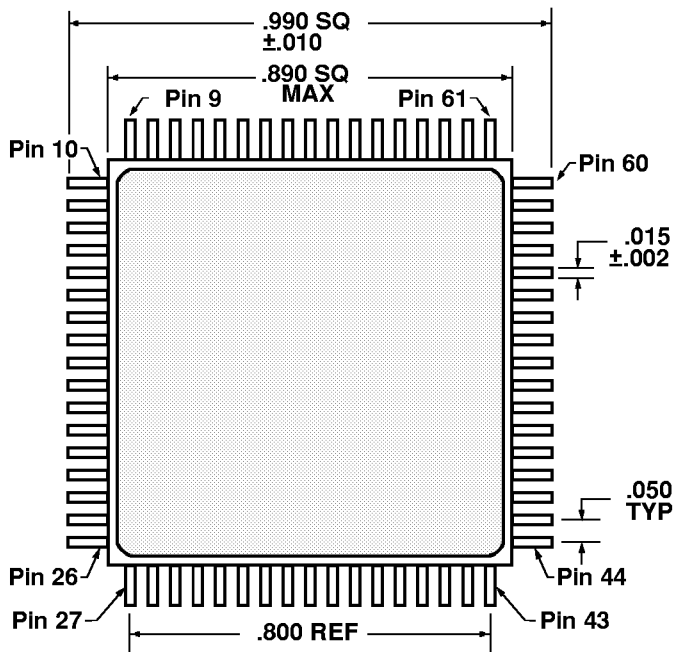
Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	$\overline{OE}$	52	GND
2	$\overline{SWE}_3$	19	I/O ₈	36	$\overline{SWE}_2$	53	FI/O ₂₃
3	A ₅	20	I/O ₉	37	A ₁₇	54	FI/O ₂₂
4	A ₄	21	I/O ₁₀	38	$\overline{FWE}_2$	55	FI/O ₂₁
5	A ₃	22	I/O ₁₁	39	$\overline{FWE}_3$	56	FI/O ₂₀
6	A ₂	23	I/O ₁₂	40	$\overline{FWE}_4$	57	FI/O ₁₉
7	A ₁	24	I/O ₁₃	41	A ₁₈	58	FI/O ₁₈
8	A ₀	25	I/O ₁₄	42	$\overline{SCE}$	59	FI/O ₁₇
9	NC	26	I/O ₁₅	43	$\overline{SWE}_1$	60	FI/O ₁₆
10	I/O ₀	27	V _{CC}	44	FI/O ₃₁	61	V _{CC}
11	I/O ₁	28	A ₁₁	45	FI/O ₃₀	62	A ₁₀
12	I/O ₂	29	A ₁₂	46	FI/O ₂₉	63	A ₉
13	I/O ₃	30	A ₁₃	47	FI/O ₂₈	64	A ₈
14	I/O ₄	31	A ₁₄	48	FI/O ₂₇	65	A ₇
15	I/O ₅	32	A ₁₅	49	FI/O ₂₆	66	A ₆
16	I/O ₆	33	A ₁₆	50	FI/O ₂₅	67	$\overline{FWE}_1$
17	I/O ₇	34	$\overline{FCE}$	51	FI/O ₂₄	68	$\overline{SWE}_4$

Package Outline — Dual-Cavity CQFP "F2"

Top View



*.180 MAX available, call factory for details

All dimensions in inches

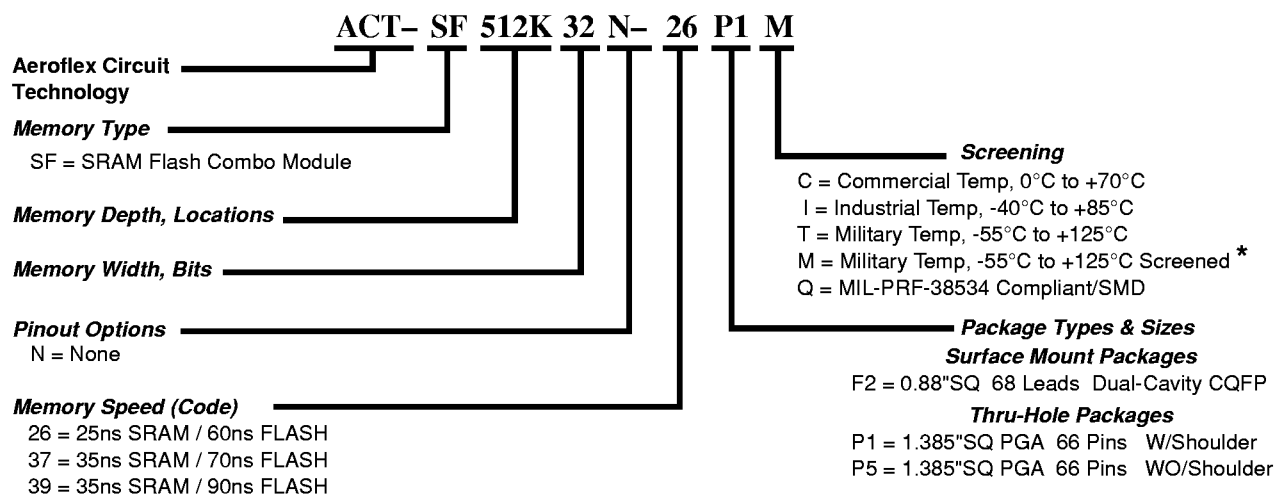


Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-SF512K32N-26P1X	TBD	25(S) / 60(F) ns	1.385"sq PGA-Type
ACT-SF512K32N-37P1X	TBD	35(S) / 70(F) ns	1.385"sq PGA-Type
ACT-SF512K32N-39P1X	TBD	35(S) / 90(F) ns	1.385"sq PGA-Type
ACT-SF512K32N-26F2X	TBD	25(S) / 60(F) ns	.88"sq CQFP
ACT-SF512K32N-37F2X	TBD	35(S) / 70(F) ns	.88"sq CQFP
ACT-SF512K32N-39F2X	TBD	35(S) / 90(F) ns	.88"sq CQFP

Note: (S) = Speed for SRAM, (F) = Speed for FLASH

Part Number Breakdown



* Screened to the individual test methods of MIL-STD-883

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