XC5400 HardWire™ Array Family

Preliminary

Product Specification

Features

- Mask Programmed version of the XC5200 Field Programmable Gate Array (FPGA)
  - Specifically designed for easy XC5200 conversion
  - Significant cost reduction for high volume production applications
  - Meets XC5200 series -4 speed grades
  - Supports all major XC5200 design features including:
    - IEEE 1149.1 Boundary Scan
    - Configuration Emulation logic (patent pending)
  - State of the art submicron process
- Easy conversion with guaranteed results
  - Little customer engineering required
  - No simulation required after conversion
  - Fully pin-for-pin compatible
  - Supports most popular package types
  - Up to 15,000 gate complexity
  - CLB and IOB placement preserved
  - FPGA design file used to generate production ready prototypes
  - Prototypes built on production fab line
  - NO_PROM feature provides additional cost savings

Description

The XC5200 FPGA family is engineered to deliver the lowest cost of any FPGA. Building on experiences gained with three previous successful FPGA families, the XC5200 brings a robust feature set to high-density programmable logic design. The VersaBlock logic module, the VersaRing I/O interface, and a rich hierarchy of interconnect resources combine to enhance design flexibility and reduce time-to-market. These architectural advances, along with silicon efficiency derived from triple layer metal technology and a CMOS SRAM process position the XC5200 as a cost-effective, high volume alternative to gate arrays.

The XC5400 HardWire Arrays are advanced mask-programmed versions of the XC5200 programmable devices. In high volume applications the programmable FPGA devices used for prototyping and initial production can be replaced by an equivalent HardWire device. This conversion offers a significant cost reduction with virtually no risk or engineering resources required.

In a programmable FPGA device, the logic functions and interconnections are determined by the configuration program data, loaded and stored in internal static-memory cells. The HardWire Array has the identical functional architecture as the programmed FPGA device it replaces, but does not require the configuration memory cells. In the HardWire Array, the FPGA logic is optimized for area by removing all unused logic elements as well as the memory cells required to store the FPGA configuration data.

Table 1. Summary of HardWire Product Availability For Each Member of the XC5200 FPGA Family

HardWire Device	Replacement for Pin-compatible Programmable Device	Speed Grade of HardWire Conversion*		Packages										
			Max	PLCC	VQFP	TQFP		PQFP				HQ	BG	
			I/O	84	100	144	176	100	160	208	240	304	225	352
XC5402	XC5202	-4	84	65	81	84	84	81						
XC5404	XC5204	-4	124	65	81	117	148	81	124					
XC5406	XC5206	-4	148	65	81	117	149	81	133	148				
XC5410	XC5210	-4	196	65		117		81	133	164	196		196	
XC5415	XC5215	-4	244						133	164	197	244	196	244

*Consult factory for informationif faster speed grades are required.

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Architectural Overview

The XC5400 has the same functional architecture as the programmed XC5200 it replaces. Proprietary Xilinx software tools are used to migrate the XC5200 design into the XC5400 HardWire Array.

Architectural Details

XC5200 / XC5400 User Logic

The XC5200 and XC5400 supports several different 'User Logic' features. These include the STARTUP User Logic and the BSCAN User Logic.

STARTUP

The STARTUP User Logic block is completely supported in the XC5400. The input pins for GSR and GTS can be tied anywhere in the design. Each of these pins can also be inverted, as in the XC5200 FPGA. Refer to Figure 1 for a detailed block diagram of the STARTUP User Logic block. Xilinx recommends the use of the STARTUP block for FPGA designs. By utilizing the GSR pin, all flip-flops in the design may be cleared. It is further recommended that the GSR input be driven directly from a device pin rather than from internal logic. This permits the design to be fully reset from an external device pin, resulting in greater testability.

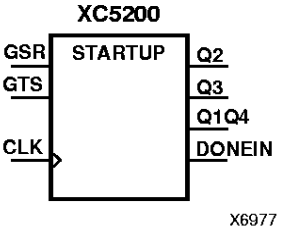

Figure 1. STARTUP User Logic Block

Similary, the GTS pin should also be connected to an external device pin so that the FPGA/HardWire may have all I/O pins at a three-state condition. This condition is often necessary for printed circuit board level manufacturing testing and is therefore a recommended design practice.

Configuration Modes

XC5200 devices have six configuration modes. XC5400 devices have the same six modes, plus an additional configuration mode. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. These are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode, which is used primarily for daisy-chain devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration of the high-capacity XC5400 devices. The coding for modes selection is shown in Table 2.

Table 2. Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output increment	Byte-Wide, from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous*	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	–	–

Note: * Synchronous Peripheral can be considered byte-wide Slave Parallel

A detailed description of each configuration mode, with timing information, is included in the XC5200 data sheet. For more information on Configuration Emulation, refer to the Design Considerations section of this Data Book.

Production Test Methodology

The Xilinx XC5400 utilizes a Production Test Methodology which permits total testability of all testable faults. This is achieved through high fault coverage vectors generated by an Automatic Test Vector Generator (ATPG). The vectors are fed via both a serial and a parallel data path for the highest degree of fault observation.

One major advantage of Xilinx's test methodology is that the customer is not required to generate any production test vectors. Since this can often consume a great deal of time, Xilinx HardWire can save valuable customer engineering resources.

The user flip-flops in the design are converted into scannable elements. All flip-flops in the dedicated logic such as Configuration Emulation or Boundary Scan are also converted into scannable elements. These elements are then combined to form full-scan chains. Up to eight chains are used in order to reduce the total required test time. By using a combination of random and deterministic fault alogrithms, high fault coverage is achieved resulting in total testability of all testable faults.

ESD Considerations

The XC5400 has similar ESD protection as the XC5200 FPGA, and is able to withstand ESD up to 2,000 volts. The HardWire is manufactured in CMOS process technology, and appropriate Electro-Static Discharge (ESD) handling precautions should be followed.

3 V/5 V Considerations

The XC5400 HardWire Array can operate either as 5 volt only, or as a 3.3 volt device (part number XC5400L).

Table 3. 5 Volt and 3.3 Volt Operation

	5 Volt Operation				3.3 Volt Operation			
	Vil (max)	Vih (min)	Vol (max)	Voh (min)	Vil (max)	Vih (min)	Vol (max)	Voh (min)
XC5400	0.80	2.00	0.40	V_{CC} -0.4	0.80	2.20	0.30	V_{CC} -0.3

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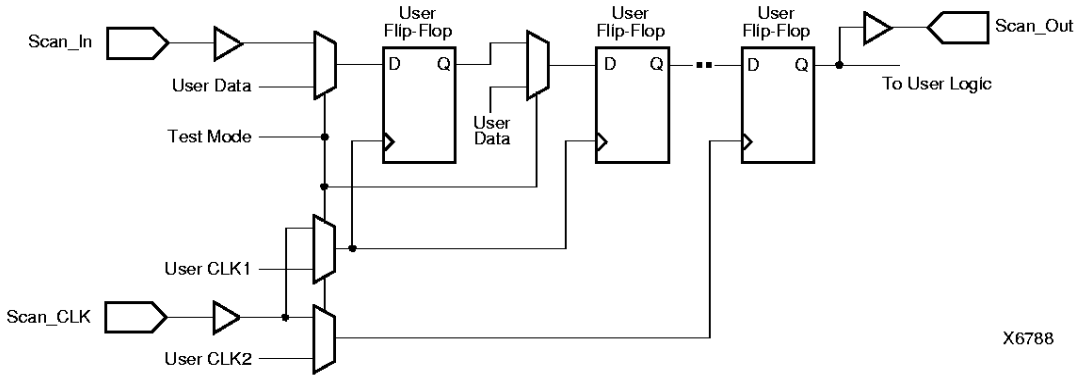

Figure 2. XC5400 Scan Chain Sample

Device-Specific Pinout Tables

XC5402 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	VCC	2	92	89	128	H3	-
1.	I/O (A8)	3	93	90	129	H1	51
2.	I/O (A9)	4	94	91	130	G1	54
3.	I/O	-	95	92	131	G2	57
4.	I/O	-	96	93	132	G3	63
5.	I/O (A10)	5	97	94	133	F1	66
6.	I/O (A11)	6	98	95	134	F2	69
	-	-	-	-	135*	-	-
	-	-	-	-	136*	-	-
	GND	-	-	-	137	F3	-
7.	I/O (A12)	7	99	96	138	E3	78
8.	I/O (A13)	8	100	97	139	C1	81
	-	-	-	-	140*	-	-
	-	-	-	-	141*	-	-
9.	I/O (A14)	9	1	98	142	B1	90
10.	I/O (A15)	10	2	99	143	B2	93
	VCC	11	3	100	144	C3	-
	GND	12	4	1	1	C4	-
11.	GCK1 (A16, I/O)	13	5	2	2	B3	102
12.	I/O (A17)	14	6	3	3	A1	105
	-	-	-	-	4*	-	-
	-	-	-	-	5*	-	-
13.	I/O (TDI)	15	7	4	6	B4	111
14.	I/O (TCK)	16	8	5	7	A3	114
	GND	-	-	-	8	C6	-
	-	-	-	-	9*	-	-
	-	-	-	-	10*	-	-
15.	I/O (TMS)	17	9	6	11	A5	117
16.	I/O	18	10	7	12	C7	123
17.	I/O	-	-	-	13	B7	126
18.	I/O	-	11	8	14	A6	129
19.	I/O	19	12	9	15	A7	135
20.	I/O	20	13	10	16	A8	138
	GND	21	14	11	17	C8	-
	VCC	22	15	12	18	B8	-
21.	I/O	23	16	13	19	C9	141
22.	I/O	24	17	14	20	B9	147
23.	I/O	-	18	15	21	A9	150
24.	I/O	-	-	-	22	B10	153
25.	I/O	25	19	16	23	C10	159
26.	I/O	26	20	17	24	A10	162
	-	-	-	-	25*	-	-
	-	-	-	-	26*	-	-
	GND	-	-	-	27	C11	-
27.	I/O	27	21	18	28	B12	165
28.	I/O	-	22	19	29	A13	171
	-	-	-	-	30*	-	-
	-	-	-	-	31*	-	-
29.	I/O	28	23	20	32	B13	174

XC5402 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
30.	I/O	29	24	21	33	B14	177
31.	M1 (I/O)	30	25	22	34	A15	186
	GND	31	26	23	35	C13	-
32.	M0 (I/O)	32	27	24	36	A16	189
	VCC	33	28	25	37	C14	-
33.	M2 (I/O)	34	29	26	38	B15	192
34.	GCK2 (I/O)	35	30	27	39	B16	195
35.	I/O (HDC)	36	31	28	40	D14	204
	-	-	-	-	41*	-	-
	-	-	-	-	42*	-	-
36.	I/O	-	32	29	43	E14	207
37.	I/O (LDC)	37	33	30	44	C16	210
	GND	-	-	-	45	F14	-
	-	-	-	-	46*	-	-
	-	-	-	-	47*	-	-
38.	I/O	38	34	31	48	F16	216
39.	I/O	39	35	32	49	G14	219
40.	I/O	-	36	33	50	G15	222
41.	I/O	-	37	34	51	G16	228
42.	I/O	40	38	35	52	H16	231
43.	I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	39	36	53	H15	234
	VCC	42	40	37	54	H14	-
	GND	43	41	38	55	J14	-
44.	I/O	44	42	39	56	J15	240
45.	I/O	45	43	40	57	J16	243
46.	I/O	-	44	41	58	K16	246
47.	I/O	-	45	42	59	K15	252
48.	I/O	46	46	43	60	K14	255
49.	I/O	47	47	44	61	L16	258
	-	-	-	-	62*	-	-
	-	-	-	-	63*	-	-
	GND	-	-	-	64	L14	-
50.	I/O	48	48	45	65	P16	264
51.	I/O	49	49	46	66	M14	267
	-	-	-	-	67*	-	-
	-	-	-	-	68*	-	-
52.	I/O	50	50	47	69	N14	276
53.	I/O	51	51	48	70	R16	279
	GND	52	52	49	71	P14	-
	DONE	53	53	50	72	R15	-
	VCC	54	54	51	73	P13	-
	PROG	55	55	52	74	R14	-
54.	I/O (D7)	56	56	53	75	T16	288
55.	GCK3 (I/O)	57	57	54	76	T15	291
	-	-	-	-	77*	-	-
	-	-	-	-	78*	-	-
56.	I/O (D6)	58	58	55	79	T14	300
57.	I/O	-	59	56	80	T13	303
	GND	-	-	-	81	P11	-
	-	-	-	-	82*	-	-

XC5402 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	-	-	-	-	83*	-	-
58.	I/O (D5)	59	60	57	84	T10	306
59.	I/O ($\overline{CS0}$)	60	61	58	85	P10	312
60.	I/O	-	62	59	86	R10	315
61.	I/O	-	63	60	87	T9	318
62.	I/O (D4)	61	64	61	88	R9	324
63.	I/O	62	65	62	89	P9	327
	VCC	63	66	63	90	R8	-
	GND	64	67	64	91	P8	-
64.	I/O (D3)	65	68	65	92	T8	336
65.	I/O ($\overline{RS}$)	66	69	66	93	T7	339
66.	I/O	-	70	67	94	T6	342
67.	I/O	-	-	-	95	R7	348
68.	I/O (D2)	67	71	68	96	P7	351
69.	I/O	68	72	69	97	T5	360
	-	-	-	-	98*	-	-
	-	-	-	-	99*	-	-
	GND	-	-	-	100	P6	-
70.	I/O (D1)	69	73	70	101	T3	363
71.	I/O ($\overline{RCLK-BUSY}$/ RDY)	70	74	71	102	P5	366
	-	-	-	-	103*	-	-
	-	-	-	-	104*	-	-
72.	I/O (D0, DIN)	71	75	72	105	P4	372
73.	I/O (DOUT)	72	76	73	106	T2	375
	CCLK	73	77	74	107	R2	-
	VCC	74	78	75	108	P3	-
74.	I/O (TDO)	75	79	76	109	T1	0
	GND	76	80	77	110	N3	-
75.	I/O (A0, $\overline{WS}$)	77	81	78	111	R1	9
76.	GCK4 (A1, I/O)	78	82	79	112	P2	15
	-	-	-	-	113*	-	-
	-	-	-	-	114*	-	-
77.	I/O (A2, CS1)	79	83	80	115	P1	18
78.	I/O (A3)	80	84	81	116	N1	21
	-	-	-	-	117*	-	-
	GND	-	-	-	118	L3	-
	-	-	-	-	119*	-	-
	-	-	-	-	120*	-	-
79.	I/O (A4)	81	85	82	121	K3	27
80.	I/O (A5)	82	86	83	122	K2	30
81.	I/O	-	87	84	123	K1	33
82.	I/O	-	88	85	124	J1	39
83.	I/O (A6)	83	89	86	125	J2	42
84.	I/O (A7)	84	90	87	126	J3	45
	GND	1	91	88	127	H2	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 18 or Figure 19.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

XC5404 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
	VCC	2	92	89	128	H3	142	-
1.	I/O (A8)	3	93	90	129	H1	143	78
2.	I/O (A9)	4	94	91	130	G1	144	81
3.	I/O	-	95	92	131	G2	145	87
4.	I/O	-	96	93	132	G3	146	90
5.	I/O (A10)	5	97	94	133	F1	147	93
6.	I/O (A11)	6	98	95	134	F2	148	99
7.	I/O	-	-	-	135	E1	149	102
8.	I/O	-	-	-	136	E2	150	105
	GND	-	-	-	137	F3	151	-
9.	I/O	-	-	-	-	D1	152	111
10.	I/O	-	-	-	-	D2	153	114
11.	I/O (A12)	7	99	96	138	E3	154	117
12.	I/O (A13)	8	100	97	139	C1	155	123
13.	I/O	-	-	-	140	C2	156	126
14.	I/O	-	-	-	141	D3	157	129
15.	I/O (A14)	9	1	98	142	B1	158	138
16.	I/O (A15)	10	2	99	143	B2	159	141
	VCC	11	3	100	144	C3	160	-
	GND	12	4	1	1	C4	1	-
17.	GCK1 (A16, I/O)	13	5	2	2	B3	2	150
18.	I/O (A17)	14	6	3	3	A1	3	153
19.	I/O	-	-	-	4	A2	4	159
20.	I/O	-	-	-	5	C5	5	162
21.	I/O (TDI)	15	7	4	6	B4	6	165
22.	I/O (TCK)	16	8	5	7	A3	7	171
	-	-	-	-	-	-	8*	-
	-	-	-	-	-	-	9*	-
	GND	-	-	-	8	C6	10	-
23.	I/O	-	-	-	9	B5	11	174
24.	I/O	-	-	-	10	B6	12	177
25.	I/O (TMS)	17	9	6	11	A5	13	180
26.	I/O	18	10	7	12	C7	14	183
27.	I/O	-	-	-	13	B7	15	186
28.	I/O	-	11	8	14	A6	16	189
29.	I/O	19	12	9	15	A7	17	195
30.	I/O	20	13	10	16	A8	18	198
	GND	21	14	11	17	C8	19	-
	VCC	22	15	12	18	B8	20	-
31.	I/O	23	16	13	19	C9	21	201
32.	I/O	24	17	14	20	B9	22	207
33.	I/O	-	18	15	21	A9	23	210
34.	I/O	-	-	-	22	B10	24	213
35.	I/O	25	19	16	23	C10	25	219
36.	I/O	26	20	17	24	A10	26	222
37.	I/O	-	-	-	25	A11	27	225
38.	I/O	-	-	-	26	B11	28	231
	GND	-	-	-	27	C11	29	-
	-	-	-	-	-	-	30*	-
	-	-	-	-	-	-	31*	-

XC5404 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
39.	I/O	27	21	18	28	B12	32	234
40.	I/O	-	22	19	29	A13	33	237
41.	I/O	-	-	-	30	A14	34	240
42.	I/O	-	-	-	31	C12	35	243
43.	I/O	28	23	20	32	B13	36	246
44.	I/O	29	24	21	33	B14	37	249
45.	M1 (I/O)	30	25	22	34	A15	38	258
	GND	31	26	23	35	C13	39	-
46.	M0 (I/O)	32	27	24	36	A16	40	261
	VCC	33	28	25	37	C14	41	-
47.	M2 (I/O)	34	29	26	38	B15	42	264
48.	GCK2 (I/O)	35	30	27	39	B16	43	267
49.	I/O (HDC)	36	31	28	40	D14	44	276
50.	I/O	-	-	-	41	C15	45	279
51.	I/O	-	-	-	42	D15	46	282
52.	I/O	-	32	29	43	E14	47	288
53.	I/O (LDC)	37	33	30	44	C16	48	291
54.	I/O	-	-	-	-	E15	49	294
55.	I/O	-	-	-	-	D16	50	300
	GND	-	-	-	45	F14	51	-
56.	I/O	-	-	-	46	F15	52	303
57.	I/O	-	-	-	47	E16	53	306
58.	I/O	38	34	31	48	F16	54	312
59.	I/O	39	35	32	49	G14	55	315
60.	I/O	-	36	33	50	G15	56	318
61.	I/O	-	37	34	51	G16	57	324
62.	I/O	40	38	35	52	H16	58	327
63.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	36	53	H15	59	330
	VCC	42	40	37	54	H14	60	-
	GND	43	41	38	55	J14	61	-
64.	I/O	44	42	39	56	J15	62	336
65.	I/O	45	43	40	57	J16	63	339
66.	I/O	-	44	41	58	K16	64	348
67.	I/O	-	45	42	59	K15	65	351
68.	I/O	46	46	43	60	K14	66	354
69.	I/O	47	47	44	61	L16	67	360
70.	I/O	-	-	-	62	M16	68	363
71.	I/O	-	-	-	63	L15	69	366
	GND	-	-	-	64	L14	70	-
72.	I/O	-	-	-	-	N16	71	372
73.	I/O	-	-	-	-	M15	72	375
74.	I/O	48	48	45	65	P16	73	378
75.	I/O	49	49	46	66	M14	74	384
76.	I/O	-	-	-	67	N15	75	387
77.	I/O	-	-	-	68	P15	76	390
78.	I/O	50	50	47	69	N14	77	396
79.	I/O	51	51	48	70	R16	78	399
	GND	52	52	49	71	P14	79	-
	DONE	53	53	50	72	R15	80	-
	VCC	54	54	51	73	P13	81	-
	PROG	55	55	52	74	R14	82	-

XC5404 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
80.	I/O (D7)	56	56	53	75	T16	83	408
81.	GCK3 (I/O)	57	57	54	76	T15	84	411
82.	I/O	-	-	-	77	R13	85	420
83.	I/O	-	-	-	78	P12	86	423
84.	I/O (D6)	58	58	55	79	T14	87	426
85.	I/O	-	59	56	80	T13	88	432
	-	-	-	-	-	-	89*	-
	-	-	-	-	-	-	90*	-
	GND	-	-	-	81	P11	91	-
86.	I/O	-	-	-	82	R11	92	435
87.	I/O	-	-	-	83	T11	93	438
88.	I/O (D5)	59	60	57	84	T10	94	444
89.	I/O ($\overline{CS0}$)	60	61	58	85	P10	95	447
90.	I/O	-	62	59	86	R10	96	450
91.	I/O	-	63	60	87	T9	97	456
92.	I/O (D4)	61	64	61	88	R9	98	459
93.	I/O	62	65	62	89	P9	99	462
	VCC	63	66	63	90	R8	100	-
	GND	64	67	64	91	P8	101	-
94.	I/O (D3)	65	68	65	92	T8	102	468
95.	I/O ($\overline{RS}$)	66	69	66	93	T7	103	471
96.	I/O	-	70	67	94	T6	104	474
97.	I/O	-	-	-	95	R7	105	480
98.	I/O (D2)	67	71	68	96	P7	106	483
99.	I/O	68	72	69	97	T5	107	486
100.	I/O	-	-	-	98	R6	108	492
101.	I/O	-	-	-	99	T4	109	495
	GND	-	-	-	100	P6	110	-
	-	-	-	-	-	-	111*	-
	-	-	-	-	-	-	112*	-
102.	I/O (D1)	69	73	70	101	T3	113	498
103.	I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	74	71	102	P5	114	504
104.	I/O	-	-	-	103	R4	115	507
105.	I/O	-	-	-	104	R3	116	510
106.	I/O (D0, DIN)	71	75	72	105	P4	117	516
107.	I/O (DOUT)	72	76	73	106	T2	118	519
	CCLK	73	77	74	107	R2	119	-
	VCC	74	78	75	108	P3	120	-
108.	I/O (TDO)	75	79	76	109	T1	121	0
	GND	76	80	77	110	N3	122	-
109.	I/O (A0, $\overline{WS}$)	77	81	78	111	R1	123	9
110.	GCK4 (A1, I/O)	78	82	79	112	P2	124	15
111.	I/O	-	-	-	113	N2	125	18
112.	I/O	-	-	-	114	M3	126	21
113.	I/O (A2, CS1)	79	83	80	115	P1	127	27
114.	I/O (A3)	80	84	81	116	N1	128	30
115.	I/O	-	-	-	117	M2	129	33
116.	I/O	-	-	-	-	M1	130	39
	GND	-	-	-	118	L3	131	-
117.	I/O	-	-	-	119	L2	132	42
118.	I/O	-	-	-	120	L1	133	45

XC5404 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
119.	I/O (A4)	81	85	82	121	K3	134	51
120.	I/O (A5)	82	86	83	122	K2	135	54
	-	-	-	-	-	-	136*	-
121.	I/O	-	87	84	123	K1	137	57
122.	I/O	-	88	85	124	J1	138	63
123.	I/O (A6)	83	89	86	125	J2	139	66
124.	I/O (A7)	84	90	87	126	J3	140	69
	GND	1	91	88	127	H2	141	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 20 or Figure 21.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

XC5406 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	VCC	2	92	89	128	142	155	J4	183	-
1.	I/O (A8)	3	93	90	129	143	156	J3	184	87
2.	I/O (A9)	4	94	91	130	144	157	J2	185	90
3.	I/O	-	95	92	131	145	158	J1	186	93
4.	I/O	-	96	93	132	146	159	H1	187	99
5.	I/O	-	-	-	-	-	160	H2	188	102
6.	I/O	-	-	-	-	-	161	H3	189	105
7.	I/O (A10)	5	97	94	133	147	162	G1	190	111
8.	I/O (A11)	6	98	95	134	148	163	G2	191	114
9.	I/O	-	-	-	135	149	164	F1	192	117
10.	I/O	-	-	-	136	150	165	E1	193	123
	GND	-	-	-	137	151	166	G3	194	-
	-	-	-	-	-	-	-	-	195*	-
	-	-	-	-	-	-	167*	-	196*	-
11.	I/O	-	-	-	-	152	168	C1	197	126
12.	I/O	-	-	-	-	153	169	E2	198	129
13.	I/O (A12)	7	99	96	138	154	170	F3	199	138
14.	I/O (A13)	8	100	97	139	155	171	D2	200	141
15.	I/O	-	-	-	140	156	172	B1	201	150
16.	I/O	-	-	-	141	157	173	E3	202	153
17.	I/O (A14)	9	1	98	142	158	174	C2	203	162
18.	I/O (A15)	10	2	99	143	159	175	B2	204	165
	VCC	11	3	100	144	160	176	D3	205	-
	-	-	-	-	-	-	-	-	206*	-
	-	-	-	-	-	-	-	-	207*	-
	-	-	-	-	-	-	-	-	208*	-
	-	-	-	-	-	-	-	-	1*	-
	GND	12	4	1	1	1	1	D4	2	-
	-	-	-	-	-	-	-	-	3*	-
19.	GCK1 (A16, I/O)	13	5	2	2	2	2	C3	4	174
20.	I/O (A17)	14	6	3	3	3	3	C4	5	177
21.	I/O	-	-	-	4	4	4	B3	6	183
22.	I/O	-	-	-	5	5	5	C5	7	186
23.	I/O (TDI)	15	7	4	6	6	6	A2	8	189
24.	I/O (TCK)	16	8	5	7	7	7	B4	9	195
25.	I/O	-	-	-	-	8	8	C6	10	198
26.	I/O	-	-	-	-	9	9	A3	11	201
	-	-	-	-	-	-	-	-	12*	-
	-	-	-	-	-	-	-	-	13*	-
	GND	-	-	-	8	10	10	C7	14	-
27.	I/O	-	-	-	9	11	11	A4	15	207
28.	I/O	-	-	-	10	12	12	A5	16	210
29.	I/O (TMS)	17	9	6	11	13	13	B7	17	213
30.	I/O	18	10	7	12	14	14	A6	18	219
31.	I/O	-	-	-	-	-	15	C8	19	222
32.	I/O	-	-	-	-	-	16	A7	20	225
33.	I/O	-	-	-	13	15	17	B8	21	234
34.	I/O	-	11	8	14	16	18	A8	22	237
35.	I/O	19	12	9	15	17	19	B9	23	246
36.	I/O	20	13	10	16	18	20	C9	24	249

XC5406 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	GND	21	14	11	17	19	21	D9	25	-
	VCC	22	15	12	18	20	22	D10	26	-
37.	I/O	23	16	13	19	21	23	C10	27	255
38.	I/O	24	17	14	20	22	24	B10	28	258
39.	I/O	-	18	15	21	23	25	A9	29	261
40.	I/O	-	-	-	22	24	26	A10	30	267
41.	I/O	-	-	-	-	-	27	A11	31	270
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
	-	-	-	-	-	-	-	-	38*	-
	-	-	-	-	-	-	-	-	39*	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	-	-	-	-	-	-	-	-	51*	-
	-	-	-	-	-	-	-	-	52*	-
	-	-	-	-	-	-	-	-	53*	-
	-	-	-	-	-	-	-	-	54*	-
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	-	-	-	-	-	-	-	-	65*	-
	-	-	-	-	-	-	-	-	66*	-
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408

XC5406 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
	-	-	-	-	-	-	-	-	91*	-
	-	-	-	-	-	-	-	-	92*	-
86.	I/O	-	-	-	-	71	79	T18	93	459
87.	I/O	-	-	-	-	72	80	P17	94	468
88.	I/O	48	48	45	65	73	81	N16	95	471
89.	I/O	49	49	46	66	74	82	T17	96	480
90.	I/O	-	-	-	67	75	83	R17	97	483
91.	I/O	-	-	-	68	76	84	P16	98	486
92.	I/O	50	50	47	69	77	85	U18	99	492
93.	I/O	51	51	48	70	78	86	T16	100	495
	GND	52	52	49	71	79	87	R16	101	-
	-	-	-	-	-	-	-	-	102*	-
	DONE	53	53	50	72	80	88	U17	103	-
	-	-	-	-	-	-	-	-	104*	-
	-	-	-	-	-	-	-	-	105*	-
	VCC	54	54	51	73	81	89	R15	106	-
	-	-	-	-	-	-	-	-	107*	-
	PROG	55	55	52	74	82	90	V18	108	-
94.	I/O (D7)	56	56	53	75	83	91	T15	109	504
95.	GCK3 (I/O)	57	57	54	76	84	92	U16	110	507
96.	I/O	-	-	-	77	85	93	T14	111	516
97.	I/O	-	-	-	78	86	94	U15	112	519
98.	I/O (D6)	58	58	55	79	87	95	V17	113	522
99.	I/O	-	59	56	80	88	96	V16	114	528
100.	I/O	-	-	-	-	89	97	T13	115	531
101.	I/O	-	-	-	-	90	98	U14	116	534
	-	-	-	-	-	-	-	-	117*	-
	-	-	-	-	-	-	-	-	118*	-
	GND	-	-	-	81	91	99	T12	119	-
102.	I/O	-	-	-	82	92	100	U13	120	540
103.	I/O	-	-	-	83	93	101	V13	121	543
104.	I/O (D5)	59	60	57	84	94	102	U12	122	552
105.	I/O ($\overline{CS0}$)	60	61	58	85	95	103	V12	123	555
106.	I/O	-	-	-	-	-	104	T11	124	558
107.	I/O	-	-	-	-	-	105	U11	125	564
108.	I/O	-	62	59	86	96	106	V11	126	567

XC5406 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
109.	I/O	-	63	60	87	97	107	V10	127	570
110.	I/O (D4)	61	64	61	88	98	108	U10	128	576
111.	I/O	62	65	62	89	99	109	T10	129	579
	VCC	63	66	63	90	100	110	R10	130	-
	GND	64	67	64	91	101	111	R9	131	-
112.	I/O (D3)	65	68	65	92	102	112	T9	132	588
113.	I/O ($\overline{RS}$)	66	69	66	93	103	113	U9	133	591
114.	I/O	-	70	67	94	104	114	V9	134	600
115.	I/O	-	-	-	95	105	115	V8	135	603
116.	I/O	-	-	-	-	-	116	U8	136	612
117.	I/O	-	-	-	-	-	117	T8	137	615
118.	I/O (D2)	67	71	68	96	106	118	V7	138	618
119.	I/O	68	72	69	97	107	119	U7	139	624
120.	I/O	-	-	-	98	108	120	V6	140	627
121.	I/O	-	-	-	99	109	121	U6	141	630
	GND	-	-	-	100	110	122	T7	142	-
	-	-	-	-	-	-	-	-	143*	-
	-	-	-	-	-	-	-	-	144*	-
122.	I/O	-	-	-	-	111	123	U5	145	636
123.	I/O	-	-	-	-	112	124	T6	146	639
124.	I/O (D1)	69	73	70	101	113	125	V3	147	642
125.	I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	74	71	102	114	126	V2	148	648
126.	I/O	-	-	-	103	115	127	U4	149	651
127.	I/O	-	-	-	104	116	128	T5	150	654
128.	I/O (D0, DIN)	71	75	72	105	117	129	U3	151	660
129.	I/O (DOUT)	72	76	73	106	118	130	T4	152	663
	CCLK	73	77	74	107	119	131	V1	153	-
	VCC	74	78	75	108	120	132	R4	154	-
	-	-	-	-	-	-	-	-	155*	-
	-	-	-	-	-	-	-	-	156*	-
	-	-	-	-	-	-	-	-	157*	-
	-	-	-	-	-	-	-	-	158*	-
130.	I/O (TDO)	75	79	76	109	121	133	U2	159	-
	GND	76	80	77	110	122	134	R3	160	-
131.	I/O (A0, $\overline{WS}$)	77	81	78	111	123	135	T3	161	9
132.	GCK4 (A1, I/O)	78	82	79	112	124	136	U1	162	15
133.	I/O	-	-	-	113	125	137	P3	163	18
134.	I/O	-	-	-	114	126	138	R2	164	21
135.	I/O (A2, CS1)	79	83	80	115	127	139	T2	165	27
136.	I/O (A3)	80	84	81	116	128	140	N3	166	30
137.	I/O	-	-	-	117	129	141	P2	167	33
138.	I/O	-	-	-	-	130	142	T1	168	42
	-	-	-	-	-	-	-	-	169*	-
	-	-	-	-	-	-	-	-	170*	-
	GND	-	-	-	118	131	143	M3	171	-
139.	I/O	-	-	-	119	132	144	P1	172	45
140.	I/O	-	-	-	120	133	145	N1	173	51
141.	I/O (A4)	81	85	82	121	134	146	M2	174	54
142.	I/O (A5)	82	86	83	122	135	147	M1	175	57
143.	I/O	-	-	-	-	-	148	L3	176	63

XC5406 Pinouts

Pin	Description †	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
144.	I/O	-	-	-	-	136	149	L2	177	66
145.	I/O	-	87	84	123	137	150	L1	178	69
146.	I/O	-	88	85	124	138	151	K1	179	75
147.	I/O (A6)	83	89	86	125	139	152	K2	180	78
148.	I/O (A7)	84	90	87	126	140	153	K3	181	81
	GND	1	91	88	127	141	154	K4	182	-

Notes: * Indicates unconnected package pins.
† leading numbers refer to bonded pad, shown in Figure 22 or Figure 23.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	VCC	2	128	142	155	183	J4	VCC**	212	-
1.	I/O (A8)	3	129	143	156	184	J3	E8	213	111
2.	I/O (A9)	4	130	144	157	185	J2	B7	214	114
3.	I/O	-	131	145	158	186	J1	A7	215	117
4.	I/O	-	132	146	159	187	H1	C7	216	123
5.	I/O	-	-	-	160	188	H2	D7	217	126
6.	I/O	-	-	-	161	189	H3	E7	218	129
	-	-	-	-	-	-	-	-	219*	-
7.	I/O (A10)	5	133	147	162	190	G1	A6	220	135
8.	I/O (A11)	6	134	148	163	191	G2	B6	221	138
	VCC	-	-	-	-	-	-	VCC**	222	-
9.	I/O	-	-	-	-	-	H4	C6	223	141
10.	I/O	-	-	-	-	-	G4	F7	224	150
11.	I/O	-	135	149	164	192	F1	A5	225	153
12.	I/O	-	136	150	165	193	E1	B5	226	162
	GND	-	137	151	166	194	G3	GND**	227	-
13.	I/O	-	-	-	-	195	F2	D6	228	165
14.	I/O	-	-	-	167	196	D1	C5	229	171
15.	I/O	-	-	152	168	197	C1	A4	230	174
16.	I/O	-	-	153	169	198	E2	E6	231	177
17.	I/O (A12)	7	138	154	170	199	F3	B4	232	183
18.	I/O (A13)	8	139	155	171	200	D2	D5	233	186
19.	I/O	-	-	-	-	-	F4	A3	234	189
20.	I/O	-	-	-	-	-	E4	C4	235	195
21.	I/O	-	140	156	172	201	B1	B3	236	198
22.	I/O	-	141	157	173	202	E3	F6	237	201
23.	I/O (A14)	9	142	158	174	203	C2	A2	238	210
24.	I/O (A15)	10	143	159	175	204	B2	C3	239	213
	VCC	11	144	160	176	205	D3	VCC**	240	-
	-	-	-	-	-	206*	-	-	-	-
	-	-	-	-	-	207*	-	-	-	-
	-	-	-	-	-	208*	-	-	-	-
	-	-	-	-	-	1*	-	-	-	-
	GND	12	1	1	1	2	D4	GND**	1	-
	-	-	-	-	-	3*	-	-	-	-
25.	GCK1 (A16, I/O)	13	2	2	2	4	C3	D4	2	222
26.	I/O (A17)	14	3	3	3	5	C4	B1	3	225
27.	I/O	-	4	4	4	6	B3	C2	4	231
28.	I/O	-	5	5	5	7	C5	E5	5	234
29.	I/O (TDI)	15	6	6	6	8	A2	D3	6	237
30.	I/O (TCK)	16	7	7	7	9	B4	C1	7	243
31.	I/O	-	-	8	8	10	C6	D2	8	246
32.	I/O	-	-	9	9	11	A3	G6	9	249
33.	I/O	-	-	-	-	12	B5	E4	10	255
34.	I/O	-	-	-	-	13	B6	D1	11	258
35.	I/O	-	-	-	-	-	D5	E3	12	261
36.	I/O	-	-	-	-	-	D6	E2	13	267
	GND	-	8	10	10	14	C7	GND**	14	-
37.	I/O	-	9	11	11	15	A4	F5	15	270

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
38.	I/O	-	10	12	12	16	A5	E1	16	273
39.	I/O (TMS)	17	11	13	13	17	B7	F4	17	279
40.	I/O	18	12	14	14	18	A6	F3	18	282
	VCC	-	-	-	-	-	-	VCC**	19	-
41.	I/O	-	-	-	-	-	D7	F2	20	285
42.	I/O	-	-	-	-	-	D8	F1	21	291
	-	-	-	-	-	-	-	-	22*	-
43.	I/O	-	-	-	15	19	C8	G4	23	294
44.	I/O	-	-	-	16	20	A7	G3	24	297
45.	I/O	-	13	15	17	21	B8	G2	25	306
46.	I/O	-	14	16	18	22	A8	G1	26	309
47.	I/O	19	15	17	19	23	B9	G5	27	318
48.	I/O	20	16	18	20	24	C9	H3	28	321
	GND	21	17	19	21	25	D9	GND**	29	-
	VCC	22	18	20	22	26	D10	VCC**	30	-
49.	I/O	23	19	21	23	27	C10	H4	31	327
50.	I/O	24	20	22	24	28	B10	H5	32	330
51.	I/O	-	21	23	25	29	A9	J2	33	333
52.	I/O	-	22	24	26	30	A10	J1	34	339
53.	I/O	-	-	-	27	31	A11	J3	35	342
54.	I/O	-	-	-	28	32	C11	J4	36	345
	-	-	-	-	-	-	-	-	37*	-
55.	I/O	-	-	-	-	-	D11	J5	38	351
56.	I/O	-	-	-	-	-	D12	K1	39	354
	VCC	-	-	-	-	-	-	VCC**	40	-
57.	I/O	25	23	25	29	33	B11	K2	41	357
58.	I/O	26	24	26	30	34	A12	K3	42	363
59.	I/O	-	25	27	31	35	B12	J6	43	366
60.	I/O	-	26	28	32	36	A13	L1	44	369
	GND	-	27	29	33	37	C12	GND**	45	-
61.	I/O	-	-	-	-	-	D13	L2	46	375
62.	I/O	-	-	-	-	-	D14	K4	47	378
63.	I/O	-	-	-	-	38	B13	L3	48	381
64.	I/O	-	-	-	-	39	A14	M1	49	387
65.	I/O	-	-	30	34	40	A15	K5	50	390
66.	I/O	-	-	31	35	41	C13	M2	51	393
67.	I/O	27	28	32	36	42	B14	L4	52	399
68.	I/O	-	29	33	37	43	A16	N1	53	402
69.	I/O	-	30	34	38	44	B15	M3	54	405
70.	I/O	-	31	35	39	45	C14	N2	55	411
71.	I/O	28	32	36	40	46	A17	K6	56	414
72.	I/O	29	33	37	41	47	B16	P1	57	417
73.	M1 (I/O)	30	34	38	42	48	C15	N3	58	426
	GND	31	35	39	43	49	D15	GND**	59	-
74.	M0 (I/O)	32	36	40	44	50	A18	P2	60	429
	-	-	-	-	-	51*	-	-	-	-
	-	-	-	-	-	52*	-	-	-	-
	-	-	-	-	-	53*	-	-	-	-
	-	-	-	-	-	54*	-	-	-	-
	VCC	33	37	41	45	55	D16	VCC**	61	-

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
75.	M2 (I/O)	34	38	42	46	56	C16	M4	62	432
76.	GCK2 (I/O)	35	39	43	47	57	B17	R2	63	435
77.	I/O (HDC)	36	40	44	48	58	E16	P3	64	444
78.	I/O	-	41	45	49	59	C17	L5	65	447
79.	I/O	-	42	46	50	60	D17	N4	66	450
80.	I/O	-	43	47	51	61	B18	R3	67	456
81.	I/O (LDC)	37	44	48	52	62	E17	P4	68	459
82.	I/O	-	-	49	53	63	F16	K7	69	462
83.	I/O	-	-	50	54	64	C18	M5	70	468
84.	I/O	-	-	-	-	65	D18	R4	71	471
85.	I/O	-	-	-	-	66	F17	N5	72	474
86.	I/O	-	-	-	-	-	E15	P5	73	480
87.	I/O	-	-	-	-	-	F15	L6	74	483
	GND	-	45	51	55	67	G16	GND**	75	-
88.	I/O	-	46	52	56	68	E18	R5	76	486
89.	I/O	-	47	53	57	69	F18	M6	77	492
90.	I/O	38	48	54	58	70	G17	N6	78	495
91.	I/O	39	49	55	59	71	G18	P6	79	504
	VCC	-	-	-	-	-	-	VCC**	80	-
92.	I/O	-	-	-	60	72	H16	R6	81	507
93.	I/O	-	-	-	61	73	H17	M7	82	510
	-	-	-	-	-	-	-	-	83*	-
94.	I/O	-	-	-	-	-	G15	N7	84	516
95.	I/O	-	-	-	-	-	H15	P7	85	519
96.	I/O	-	50	56	62	74	H18	R7	86	522
97.	I/O	-	51	57	63	75	J18	L7	87	528
98.	I/O	40	52	58	64	76	J17	N8	88	531
99.	I/O ($\overline{ERR}$, $\overline{INIT}$)	41	53	59	65	77	J16	P8	89	534
	VCC	42	54	60	66	78	J15	VCC**	90	-
	GND	43	55	61	67	79	K15	GND**	91	-
100.	I/O	44	56	62	68	80	K16	L8	92	540
101.	I/O	45	57	63	69	81	K17	P9	93	543
102.	I/O	-	58	64	70	82	K18	R9	94	546
103.	I/O	-	59	65	71	83	L18	N9	95	552
104.	I/O	-	-	-	72	84	L17	M9	96	555
105.	I/O	-	-	-	73	85	L16	L9	97	558
	-	-	-	-	-	-	-	-	98*	-
106.	I/O	-	-	-	-	-	L15	R10	99	564
107.	I/O	-	-	-	-	-	M15	P10	100	567
	VCC	-	-	-	-	-	-	VCC**	101	-
108.	I/O	46	60	66	74	86	M18	N10	102	570
109.	I/O	47	61	67	75	87	M17	K9	103	576
110.	I/O	-	62	68	76	88	N18	R11	104	579
111.	I/O	-	63	69	77	89	P18	P11	105	588
	GND	-	64	70	78	90	M16	GND**	106	-
112.	I/O	-	-	-	-	-	N15	M10	107	591
113.	I/O	-	-	-	-	-	P15	N11	108	600
114.	I/O	-	-	-	-	91	N17	R12	109	603
115.	I/O	-	-	-	-	92	R18	L10	110	606
116.	I/O	-	-	71	79	93	T18	P12	111	612

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
117.	I/O	-	-	72	80	94	P17	M11	112	615
118.	I/O	48	65	73	81	95	N16	R13	113	618
119.	I/O	49	66	74	82	96	T17	N12	114	624
120.	I/O	-	67	75	83	97	R17	P13	115	627
121.	I/O	-	68	76	84	98	P16	K10	116	630
122.	I/O	50	69	77	85	99	U18	R14	117	636
123.	I/O	51	70	78	86	100	T16	N13	118	639
	GND	52	71	79	87	101	R16	GND**	119	-
	-	-	-	-	-	102*	-	-	-	-
	DONE	53	72	80	88	103	U17	P14	120	-
	-	-	-	-	-	104*	-	-	-	-
	-	-	-	-	-	105*	-	-	-	-
	VCC	54	73	81	89	106	R15	VCC**	121	-
	-	-	-	-	-	107*	-	-	-	-
	PROG	55	74	82	90	108	V18	M12	122	-
124.	I/O (D7)	56	75	83	91	109	T15	P15	123	648
125.	GCK3 (I/O)	57	76	84	92	110	U16	N14	124	651
126.	I/O	-	77	85	93	111	T14	L11	125	660
127.	I/O	-	78	86	94	112	U15	M13	126	663
128.	I/O	-	-	-	-	-	R14	N15	127	666
129.	I/O	-	-	-	-	-	R13	M14	128	672
130.	I/O (D6)	58	79	87	95	113	V17	J10	129	675
131.	I/O	-	80	88	96	114	V16	L12	130	678
132.	I/O	-	-	89	97	115	T13	M15	131	684
133.	I/O	-	-	90	98	116	U14	L13	132	687
134.	I/O	-	-	-	-	117	V15	L14	133	690
135.	I/O	-	-	-	-	118	V14	K11	134	696
	GND	-	81	91	99	119	T12	GND**	135	-
136.	I/O	-	-	-	-	-	R12	L15	136	699
137.	I/O	-	-	-	-	-	R11	K12	137	708
138.	I/O	-	82	92	100	120	U13	K13	138	711
139.	I/O	-	83	93	101	121	V13	K14	139	714
	VCC	-	-	-	-	-	-	VCC**	140	-
140.	I/O (D5)	59	84	94	102	122	U12	K15	141	720
141.	I/O ($\overline{CS0}$)	60	85	95	103	123	V12	J12	142	723
	-	-	-	-	-	-	-	-	143*	-
142.	I/O	-	-	-	104	124	T11	J13	144	726
143.	I/O	-	-	-	105	125	U11	J14	145	732
144.	I/O	-	86	96	106	126	V11	J15	146	735
145.	I/O	-	87	97	107	127	V10	J11	147	738
146.	I/O (D4)	61	88	98	108	128	U10	H13	148	744
147.	I/O	62	89	99	109	129	T10	H14	149	747
	VCC	63	90	100	110	130	R10	VCC**	150	-
	GND	64	91	101	111	131	R9	GND**	151	-
148.	I/O (D3)	65	92	102	112	132	T9	H12	152	756
149.	I/O ($\overline{RS}$)	66	93	103	113	133	U9	H11	153	759
150.	I/O	-	94	104	114	134	V9	G14	154	768
151.	I/O	-	95	105	115	135	V8	G15	155	771
152.	I/O	-	-	-	116	136	U8	G13	156	780
153.	I/O	-	-	-	117	137	T8	G12	157	783

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	-	-	-	-	-	-	-	-	158*	-
154.	I/O (D2)	67	96	106	118	138	V7	G11	159	786
155.	I/O	68	97	107	119	139	U7	F15	160	792
	VCC	-	-	-	-	-	-	VCC**	161	-
156.	I/O	-	98	108	120	140	V6	F14	162	795
157.	I/O	-	99	109	121	141	U6	F13	163	798
158.	I/O	-	-	-	-	-	R8	G10	164	804
159.	I/O	-	-	-	-	-	R7	E15	165	807
	GND	-	100	110	122	142	T7	GND**	166	-
160.	I/O	-	-	-	-	-	R6	E14	167	810
161.	I/O	-	-	-	-	-	R5	F12	168	816
162.	I/O	-	-	-	-	143	V5	E13	169	819
163.	I/O	-	-	-	-	144	V4	D15	170	822
164.	I/O	-	-	111	123	145	U5	F11	171	828
165.	I/O	-	-	112	124	146	T6	D14	172	831
166.	I/O (D1)	69	101	113	125	147	V3	E12	173	834
167.	I/O ($\overline{\text{RCLK}}$-BUSY/RDY)	70	102	114	126	148	V2	C15	174	840
168.	I/O	-	103	115	127	149	U4	D13	175	843
169.	I/O	-	104	116	128	150	T5	C14	176	846
170.	I/O (D0, DIN)	71	105	117	129	151	U3	F10	177	855
171.	I/O (DOUT)	72	106	118	130	152	T4	B15	178	858
	CCLK	73	107	119	131	153	V1	C13	179	-
	VCC	74	108	120	132	154	R4	VCC**	180	-
	-	-	-	-	-	155*	-	-	-	-
	-	-	-	-	-	156*	-	-	-	-
	-	-	-	-	-	157*	-	-	-	-
	-	-	-	-	-	158*	-	-	-	-
172.	I/O (TDO)	75	109	121	133	159	U2	A15	181	-
	GND	76	110	122	134	160	R3	GND**	182	-
173.	I/O (A0, $\overline{\text{WS}}$)	77	111	123	135	161	T3	A14	183	9
174.	GCK4 (A1, I/O)	78	112	124	136	162	U1	B13	184	15
175.	I/O	-	113	125	137	163	P3	E11	185	18
176.	I/O	-	114	126	138	164	R2	C12	186	21
177.	I/O (CS1, A2)	79	115	127	139	165	T2	A13	187	27
178.	I/O (A3)	80	116	128	140	166	N3	B12	188	30
179.	I/O	-	-	-	-	-	P4	F9	189	33
180.	I/O	-	-	-	-	-	N4	D11	190	39
181.	I/O	-	117	129	141	167	P2	A12	191	42
182.	I/O	-	-	130	142	168	T1	C11	192	45
183.	I/O	-	-	-	-	169	R1	B11	193	51
184.	I/O	-	-	-	-	170	N2	E10	194	54
	-	-	-	-	-	-	-	GND**	195*	-
	GND	-	118	131	143	171	M3	-	196	-
185.	I/O	-	119	132	144	172	P1	A11	197	57
186.	I/O	-	120	133	145	173	N1	D10	198	66
187.	I/O	-	-	-	-	-	M4	C10	199	69
188.	I/O	-	-	-	-	-	L4	B10	200	75
	VCC	-	-	-	-	-	-	VCC**	201	-
189.	I/O (A4)	81	121	134	146	174	M2	A10	202	78
190.	I/O (A5)	82	122	135	147	175	M1	D9	203	81

XC5410 Pinouts

Pin	Description †	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	-	-	-	-	-	-	-	-	204*	-
191.	I/O	-	-	-	148	176	L3	C9	205	87
192.	I/O	-	-	136	149	177	L2	B9	206	90
193.	I/O	-	123	137	150	178	L1	A9	207	93
194.	I/O	-	124	138	151	179	K1	E9	208	99
195.	I/O (A6)	83	125	139	152	180	K2	C8	209	102
196.	I/O (A7)	84	126	140	153	181	K3	B8	210	105
	GND	1	127	141	154	182	K4	GND**	211	-

Notes: * Indicates unconnected package pins.

† leading numbers refer to bonded pad, shown in Figure 24 or Figure 25.

** Pins labeled VCC** are internally bonded to a VCC plane within the BG225 package. The external pins are: B2, D8, H15, R8, B14, R1, H1, and R15.

Pins labeled GND** are internally bonded to a ground plane within the BG225 package. The external pins are: A1, D12, G7, G9, H6, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8.

Boundary Scan Bit 0 = TDO.T

Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
	VCC	142	183	212	K1	38	VCC**	VCC**	-
1.	I/O (A8)	143	184	213	K2	37	E8	D14	138
2.	I/O (A9)	144	185	214	K3	36	B7	C14	141
3.	I/O	145	186	215	K5	35	A7	A15	147
4.	I/O	146	187	216	K4	34	C7	B15	150
5.	I/O	-	188	217	J1	33	D7	C15	153
6.	I/O	-	189	218	J2	32	E7	D15	159
	-	-	-	219*	-	-	-	-	-
7.	I/O (A10)	147	190	220	H1	31	A6	A16	162
8.	I/O (A11)	148	191	221	J3	30	B6	B16	165
	-	-	-	-	-	29*	-	-	-
	-	-	-	-	-	28*	-	-	-
9.	I/O	-	-	-	H2	27	-	C17	171
10.	I/O	-	-	-	G1	26	-	B18	174
	VCC	-	-	222	E1	25	VCC**	VCC**	-
	-	-	-	-	-	24*	-	-	-
11.	I/O	-	-	223	H3	23	C6	C18	177
12.	I/O	-	-	224	G2	22	F7	D17	183
13.	I/O	149	192	225	H4	21	A5	A20	186
14.	I/O	150	193	226	F2	20	B5	B19	189
	GND	151	194	227	F1	19	GND**	GND**	-
15.	I/O	-	-	-	H5	18	-	C19	195
16.	I/O	-	-	-	G3	17	-	D18	198
17.	I/O	-	195	228	D1	16	D6	A21	201
18.	I/O	-	196	229	G4	15	C5	B20	207
19.	I/O	152	197	230	E2	14	A4	C20	210
20.	I/O	153	198	231	F3	13	E6	B21	213
21.	I/O (A12)	154	199	232	G5	12	B4	B22	219
	-	-	-	-	-	11*	-	-	-
22.	I/O (A13)	155	200	233	C1	10	D5	C21	222
23.	I/O	-	-	-	F4	9	-	D20	225
24.	I/O	-	-	-	E3	8	-	A23	234
25.	I/O	-	-	234	D2	7	A3	D21	237
26.	I/O	-	-	235	C2	6	C4	C22	243
27.	I/O	156	201	236	F5	5	B3	B24	246
28.	I/O	157	202	237	E4	4	F6	C23	249
29.	I/O (A14)	158	203	238	D3	3	A2	D22	258
30.	I/O (A15)	159	204	239	C3	2	C3	C24	261
	VCC	160	205	240	A2	1	VCC**	VCC**	-
	-	-	206*	-	-	-	-	-	-
	-	-	207*	-	-	-	-	-	-
	-	-	208*	-	-	-	-	-	-
	-	-	1*	-	-	-	-	-	-
	GND	1	2	1	B1	304	GND**	GND**	-
	-	-	3*	-	-	-	-	-	-
31.	GCK1 (A16, I/O)	2	4	2	D4	303	D4	D23	270
32.	I/O (A17)	3	5	3	B2	302	B1	C25	273
33.	I/O	4	6	4	B3	301	C2	D24	279
34.	I/O	5	7	5	E6	300	E5	E23	282
35.	I/O (TDI)	6	8	6	D5	299	D3	C26	285

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
36.	I/O (TCK)	7	9	7	C4	298	C1	E24	294
37.	I/O	-	-	-	A3	297	-	F24	297
38.	I/O	-	-	-	D6	296	-	E25	303
39.	I/O	8	10	8	E7	295	D2	D26	306
40.	I/O	9	11	9	B4	294	G6	G24	309
41.	I/O	-	12	10	C5	293	E4	F25	315
42.	I/O	-	13	11	A4	292	D1	F26	318
43.	I/O	-	-	12	D7	291	E3	H23	321
44.	I/O	-	-	13	C6	290	E2	H24	327
45.	I/O	-	-	-	E8	289	-	G25	330
46.	I/O	-	-	-	B5	288	-	G26	333
	GND	10	14	14	A5	287	GND**	GND**	-
47.	I/O	11	15	15	B6	286	F5	J23	339
48.	I/O	12	16	16	D8	285	E1	J24	342
49.	I/O (TMS)	13	17	17	C7	284	F4	H25	345
50.	I/O	14	18	18	B7	283	F3	K23	351
	VCC	-	-	19	A6	282	VCC**	VCC**	-
	-	-	-	-	-	281*	-	-	-
51.	I/O	-	-	20	C8	280	F2	L24	354
52.	I/O	-	-	21	E9	279	F1	K25	357
	-	-	-	22*	-	-	-	-	-
	-	-	-	-	-	278*	-	-	-
	-	-	-	-	-	277*	-	-	-
53.	I/O	-	-	-	B8	276	-	L25	363
54.	I/O	-	-	-	A8	275	-	L26	366
55.	I/O	-	19	23	C9	274	G4	M23	369
56.	I/O	-	20	24	B9	273	G3	M24	375
57.	I/O	15	21	25	E10	272	G2	M25	378
58.	I/O	16	22	26	A9	271	G1	M26	381
59.	I/O	17	23	27	D10	270	G5	N24	390
60.	I/O	18	24	28	C10	269	H3	N25	393
	GND	19	25	29	A10	268	GND**	GND**	-
	VCC	20	26	30	A11	267	VCC**	VCC**	-
61.	I/O	21	27	31	B10	266	H4	N26	399
62.	I/O	22	28	32	B11	265	H5	P25	402
63.	I/O	23	29	33	C11	264	J2	P23	405
64.	I/O	24	30	34	E11	263	J1	P24	411
65.	I/O	-	31	35	D11	262	J3	R26	414
66.	I/O	-	32	36	A12	261	J4	R25	417
67.	I/O	-	-	-	B12	260	-	R24	423
68.	I/O	-	-	-	A13	259	-	R23	426
	-	-	-	37*	-	-	-	-	-
	-	-	-	-	-	258*	-	-	-
	-	-	-	-	-	257*	-	-	-
69.	I/O	-	-	38	E12	256	J5	T26	429
70.	I/O	-	-	39	B13	255	K1	T25	435
	-	-	-	-	-	254*	-	-	-
	VCC	-	-	40	A16	253	VCC**	VCC**	-
71.	I/O	25	33	41	A14	252	K2	U24	438
72.	I/O	26	34	42	C13	251	K3	V25	441
73.	I/O	27	35	43	B14	250	J6	V24	447

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
74.	I/O	28	36	44	D13	249	L1	U23	450
	GND	29	37	45	A15	248	GND**	GND**	-
75.	I/O	-	-	-	B15	247	-	Y26	453
76.	I/O	-	-	-	E13	246	-	W25	459
77.	I/O	-	-	46	C14	245	L2	W24	462
78.	I/O	-	-	47	A17	244	K4	V23	465
79.	I/O	-	38	48	D14	243	L3	AA26	471
80.	I/O	-	39	49	B16	242	M1	Y25	474
81.	I/O	30	40	50	C15	241	K5	Y24	477
82.	I/O	31	41	51	E14	240	M2	AA25	483
83.	I/O	-	-	-	A18	239	-	AB25	486
84.	I/O	-	-	-	D15	238	-	AA24	489
85.	I/O	32	42	52	C16	237	L4	Y23	495
86.	I/O	33	43	53	B17	236	N1	AC26	498
87.	I/O	34	44	54	B18	235	M3	AA23	501
88.	I/O	35	45	55	E15	234	N2	AB24	507
89.	I/O	36	46	56	D16	233	K6	AD25	510
90.	I/O	37	47	57	C17	232	P1	AC24	513
91.	M1 (I/O)	38	48	58	A20	231	N3	AB23	522
	GND	39	49	59	A19	230	GND**	GND**	-
92.	M0 (I/O)	40	50	60	C18	229	P2	AD24	525
	-	-	51*	-	-	-	-	-	-
	-	-	52*	-	-	-	-	-	-
	-	-	53*	-	-	-	-	-	-
	-	-	54*	-	-	-	-	-	-
	VCC	41	55	61	B20	228	VCC**	VCC**	-
93.	M2 (I/O)	42	56	62	D17	227	M4	AC23	528
94.	GCK2 (I/O)	43	57	63	B19	226	R2	AE24	531
95.	I/O (HDC)	44	58	64	C19	225	P3	AD23	540
96.	I/O	45	59	65	F16	224	L5	AC22	543
97.	I/O	46	60	66	E17	223	N4	AF24	546
98.	I/O	47	61	67	D18	222	R3	AD22	552
99.	I/O (LDC)	48	62	68	C20	221	P4	AE23	555
100.	I/O	-	-	-	F17	220	-	AE22	558
101.	I/O	-	-	-	G16	219	-	AF23	564
102.	I/O	49	63	69	D19	218	K7	AD20	567
103.	I/O	50	64	70	E18	217	M5	AE21	570
104.	I/O	-	65	71	D20	216	R4	AF21	576
105.	I/O	-	66	72	G17	215	N5	AC19	579
106.	I/O	-	-	73	F18	214	P5	AD19	582
107.	I/O	-	-	74	H16	213	L6	AE20	588
108.	I/O	-	-	-	E19	212	-	AF20	591
109.	I/O	-	-	-	F19	211	-	AC18	594
	GND	51	67	75	E20	210	GND**	GND**	-
110.	I/O	52	68	76	H17	209	R5	AD18	600
111.	I/O	53	69	77	G18	208	M6	AE19	603
112.	I/O	54	70	78	G19	207	N6	AC17	606
113.	I/O	55	71	79	H18	206	P6	AD17	612
	-	-	-	-	-	205*	-	-	-
	VCC	-	-	80	F20	204	VCC**	VCC**	-
114.	I/O	-	72	81	J16	203	R6	AE17	615

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
115.	I/O	-	73	82	G20	202	M7	AE16	618
	-	-	-	83*	-	-	-	-	-
	-	-	-	-	-	201*	-	-	-
	-	-	-	-	-	200*	-	-	-
116.	I/O	-	-	-	H20	199	-	AF16	624
117.	I/O	-	-	-	J18	198	-	AC15	627
118.	I/O	-	-	84	J19	197	N7	AD15	630
119.	I/O	-	-	85	K16	196	P7	AE15	636
120.	I/O	56	74	86	J20	195	R7	AF15	639
121.	I/O	57	75	87	K17	194	L7	AD14	642
122.	I/O	58	76	88	K18	193	N8	AE14	648
123.	I/O ($\overline{ERR}$, $\overline{INIT}$)	59	77	89	K19	192	P8	AF14	651
	VCC	60	78	90	L20	191	VCC**	VCC**	-
	GND	61	79	91	K20	190	GND**	GND**	-
124.	I/O	62	80	92	L19	189	L8	AE13	660
125.	I/O	63	81	93	L18	188	P9	AC13	663
126.	I/O	64	82	94	L16	187	R9	AD13	672
127.	I/O	65	83	95	L17	186	N9	AF12	675
128.	I/O	-	84	96	M20	185	M9	AE12	678
129.	I/O	-	85	97	M19	184	L9	AD12	684
130.	I/O	-	-	-	N20	183	-	AC12	687
131.	I/O	-	-	-	M18	182	-	AF11	690
	-	-	-	98*	-	-	-	-	-
	-	-	-	-	-	181*	-	-	-
	-	-	-	-	-	180*	-	-	-
132.	I/O	-	-	99	N19	179	R10	AE11	696
133.	I/O	-	-	100	P20	178	P10	AD11	699
	VCC	-	-	101	T20	177	VCC**	VCC**	-
	-	-	-	-	-	176*	-	-	-
134.	I/O	66	86	102	N18	175	N10	AE9	702
135.	I/O	67	87	103	P19	174	K9	AD9	708
136.	I/O	68	88	104	N17	173	R11	AC10	711
137.	I/O	69	89	105	R19	172	P11	AF7	714
	GND	70	90	106	R20	171	GND**	GND**	-
138.	I/O	-	-	-	N16	170	-	AE8	720
139.	I/O	-	-	-	P18	169	-	AD8	723
140.	I/O	-	-	107	U20	168	M10	AC9	726
141.	I/O	-	-	108	P17	167	N11	AF6	732
142.	I/O	-	91	109	T19	166	R12	AE7	735
143.	I/O	-	92	110	R18	165	L10	AD7	738
144.	I/O	71	93	111	P16	164	P12	AE6	744
145.	I/O	72	94	112	V20	163	M11	AE5	747
146.	I/O	-	-	-	R17	162	-	AD6	750
147.	I/O	-	-	-	T18	161	-	AC7	756
148.	I/O	73	95	113	U19	160	R13	AF4	759
149.	I/O	74	96	114	V19	159	N12	AF3	768
150.	I/O	75	97	115	R16	158	P13	AD5	771
151.	I/O	76	98	116	T17	157	K10	AE3	774
152.	I/O	77	99	117	U18	156	R14	AD4	780
153.	I/O	78	100	118	X20	155	N13	AC5	783
	GND	79	101	119	W20	154	GND**	GND**	-

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
	-	-	102*	-	-	-	-	-	-
	DONE	80	103	120	V18	153	P14	AD3	-
	-	-	104*	-	-	-	-	-	-
	-	-	105*	-	-	-	-	-	-
	VCC	81	106	121	X19	152	VCC**	VCC**	-
	-	-	107*	-	-	-	-	-	-
	PROG	82	108	122	U17	151	M12	AC4	-
154.	I/O (D7)	83	109	123	W19	150	P15	AD2	792
155.	GCK3 (I/O)	84	110	124	W18	149	N14	AC3	795
156.	I/O	85	111	125	T15	148	L11	AB4	804
157.	I/O	86	112	126	U16	147	M13	AD1	807
158.	I/O	-	-	127	V17	146	N15	AA4	810
159.	I/O	-	-	128	X18	145	M14	AA3	816
160.	I/O	-	-	-	U15	144	-	AB2	819
161.	I/O	-	-	-	T14	143	-	AC1	828
162.	I/O (D6)	87	113	129	W17	142	J10	Y3	831
163.	I/O	88	114	130	V16	141	L12	AA2	834
164.	I/O	89	115	131	X17	140	M15	AA1	840
165.	I/O	90	116	132	U14	139	L13	W4	843
166.	I/O	-	117	133	V15	138	L14	W3	846
167.	I/O	-	118	134	T13	137	K11	Y2	852
168.	I/O	-	-	-	W16	136	-	Y1	855
169.	I/O	-	-	-	W15	135	-	V4	858
	GND	91	119	135	X16	134	GND**	GND**	-
170.	I/O	-	-	136	U13	133	L15	V3	864
171.	I/O	-	-	137	V14	132	K12	W2	867
172.	I/O	92	120	138	W14	131	K13	U4	870
173.	I/O	93	121	139	V13	130	K14	U3	876
	VCC	-	-	140	X15	129	VCC**	VCC**	-
	-	-	-	-	-	128*	-	-	-
174.	I/O (D5)	94	122	141	T12	127	K15	V2	879
175.	I/O ($\overline{CS0}$)	95	123	142	X14	126	J12	V1	882
	-	-	-	143*	-	-	-	-	-
	-	-	-	-	-	125*	-	-	-
	-	-	-	-	-	124*	-	-	-
176.	I/O	-	-	-	X13	123	-	T1	888
177.	I/O	-	-	-	V12	122	-	R4	891
178.	I/O	-	124	144	W12	121	J13	R3	894
179.	I/O	-	125	145	T11	120	J14	R2	900
180.	I/O	96	126	146	X12	119	J15	R1	903
181.	I/O	97	127	147	U11	118	J11	P3	906
182.	I/O (D4)	98	128	148	V11	117	H13	P2	912
183.	I/O	99	129	149	W11	116	H14	P1	915
	VCC	100	130	150	X10	115	VCC**	VCC**	-
	GND	101	131	151	X11	114	GND**	GND**	-
184.	I/O (D3)	102	132	152	W10	113	H12	N2	924
185.	I/O ($\overline{RS}$)	103	133	153	V10	112	H11	N4	927
186.	I/O	104	134	154	T10	111	G14	N3	936
187.	I/O	105	135	155	U10	110	G15	M1	939
188.	I/O	-	136	156	X9	109	G13	M2	942
189.	I/O	-	137	157	W9	108	G12	M3	948

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
190.	I/O	-	-	-	X8	107	-	M4	951
191.	I/O	-	-	-	V9	106	-	L1	954
	-	-	-	158*	-	-	-	-	-
	-	-	-	-	-	105*	-	-	-
	-	-	-	-	-	104*	-	-	-
192.	I/O (D2)	106	138	159	W8	103	G11	J1	960
193.	I/O	107	139	160	X7	102	F15	K3	963
	VCC	-	-	161	X5	101	VCC**	VCC**	
	-	-	-	-	-	100*	-	-	
194.	I/O	108	140	162	V8	99	F14	J2	966
195.	I/O	109	141	163	W7	98	F13	J3	972
196.	I/O	-	-	164	U8	97	G10	K4	975
197.	I/O	-	-	165	W6	96	E15	G1	978
	GND	110	142	166	X6	95	GND**	GND**	
198.	I/O	-	-	-	T8	94	-	H2	984
199.	I/O	-	-	-	V7	93	-	H3	987
200.	I/O	-	-	167	X4	92	E14	J4	990
201.	I/O	-	-	168	U7	91	F12	F1	996
202.	I/O	-	143	169	W5	90	E13	G2	999
203.	I/O	-	144	170	V6	89	D15	G3	1002
204.	I/O	111	145	171	T7	88	F11	F2	1008
205.	I/O	112	146	172	X3	87	D14	E2	1011
206.	I/O (D1)	113	147	173	U6	86	E12	F3	1014
207.	I/O ($\overline{\text{RCLK}}$-BUSY/RDY)	114	148	174	V5	85	C15	G4	1020
208.	I/O	-	-	-	W4	84	-	D2	1023
209.	I/O	-	-	-	W3	83	-	F4	1032
210.	I/O	115	149	175	T6	82	D13	E3	1035
211.	I/O	116	150	176	U5	81	C14	C2	1038
212.	I/O (D0, DIN)	117	151	177	V4	80	F10	D3	1044
213.	I/O (DOUT)	118	152	178	X1	79	B15	E4	1047
	CCLK	119	153	179	V3	78	C13	C3	-
	VCC	120	154	180	W1	77	VCC**	VCC**	-
	-	-	155*	-	-	-	-	-	-
	-	-	156*	-	-	-	-	-	-
	-	-	157*	-	-	-	-	-	-
	-	-	158*	-	-	-	-	-	-
214.	I/O (TDO)	121	159	181	U4	76	A15	D4	0
	GND	122	160	182	X2	75	GND**	GND**	-
215.	I/O (A0, $\overline{\text{WS}}$)	123	161	183	W2	74	A14	B3	9
216.	GCK4 (A1, I/O)	124	162	184	V2	73	B13	C4	15
217.	I/O	125	163	185	R5	72	E11	D5	18
218.	I/O	126	164	186	T4	71	C12	A3	21
219.	I/O (A2, CS1)	127	165	187	U3	70	A13	D6	27
220.	I/O (A3)	128	166	188	V1	69	B12	C6	30
221.	I/O	-	-	-	R4	68	-	B5	33
222.	I/O	-	-	-	P5	67	-	A4	39
223.	I/O	-	-	189	U2	66	F9	C7	42
224.	I/O	-	-	190	T3	65	D11	B6	45
225.	I/O	129	167	191	U1	64	A12	A6	51
226.	I/O	130	168	192	P4	63	C11	D8	54
227.	I/O	-	169	193	R3	62	B11	B7	57

XC5415 Pinouts

Pin	Description †	PQ160	HQ208	HQ240	PG299	HQ304	BG225	BG352	Boundary Scan Order
228.	I/O	-	170	194	N5	61	E10	A7	63
229.	I/O	-	-	195	T2	60	-	D9	66
230.	I/O	-	-	-	R2	59	-	C9	69
	GND	131	171	196	T1	58	GND**	GND**	-
231.	I/O	132	172	197	N4	57	A11	B8	75
232.	I/O	133	173	198	P3	56	D10	D10	78
233.	I/O	-	-	199	P2	55	C10	C10	81
234.	I/O	-	-	200	N3	54	B10	B9	87
	-	-	-	-	-	53*	-	-	-
	VCC	-	-	201	R1	52	VCC**	VCC**	-
235.	I/O	-	-	-	M5	51	-	B11	90
236.	I/O	-	-	-	P1	50	-	A11	93
	-	-	-	-	-	49*	-	-	-
	-	-	-	-	-	48*	-	-	-
237.	I/O (A4)	134	174	202	N1	47	A10	D12	99
238.	I/O (A5)	135	175	203	M3	46	D9	C12	102
	-	-	-	204*	-	-	-	-	-
239.	I/O	-	176	205	M2	45	C9	B12	105
240.	I/O	136	177	206	L5	44	B9	A12	111
241.	I/O	137	178	207	M1	43	A9	C13	114
242.	I/O	138	179	208	L4	42	E9	B13	117
243.	I/O (A6)	139	180	209	L3	41	C8	A13	126
244.	I/O (A7)	140	181	210	L2	40	B8	B14	129
	GND	141	182	211	L1	39	GND**	GND**	-

Notes: * Indicates unconnected package pins.

† leading numbers refer to bonded pad.

** Pins labeled VCC** are internally bonded to a VCC plane within the BG225 and BG352 packages. The external pins for the BG225 are: B2, D8, H15, R8, B14, E1, and R15. The external pins for the BG352 are: A10, A17, B2, B25, D13, D19, D7, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC14, AC20, AC8, AE2, AE25, AF10, and AF17.
Pins labeled GND** are internally bonded to a ground plane within the BG225 and BG352 packages. The external pins for the BG225 are: A1, D12, G7, G9, H9, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8. The external pins for the BG352 are: A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF13, AF19, AF2, AF22, AF25, AF26, AF5, AF8.

Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD