

# 1-Mbit (128K x 8) nvSRAM

## Features

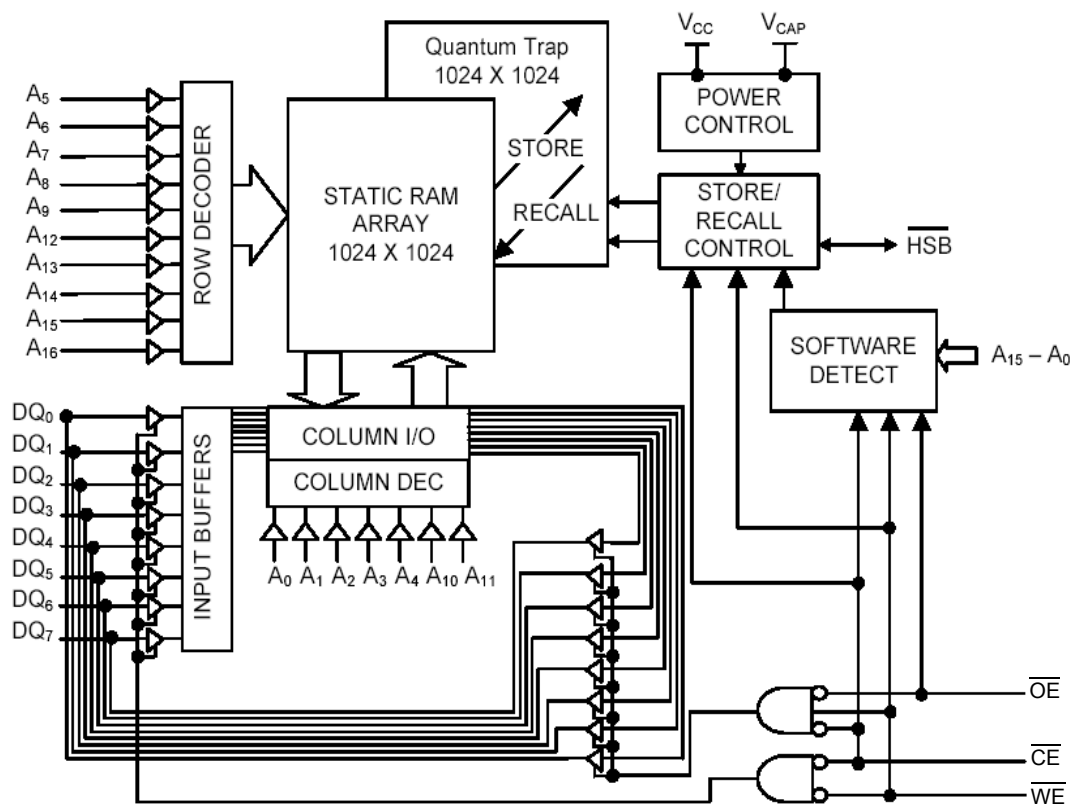
- 25 ns, 35 ns, and 45 ns Access Times
- “Hands-off” Automatic *STORE* on Power-down with only a small capacitor
- *STORE* to QuantumTrap™ Nonvolatile Elements is initiated by Software, device pin or Autostore™ on Power-down
- *RECALL* to SRAM Initiated by Software or Power-up
- Unlimited *READ*, *WRITE* and *RECALL* Cycles
- 5 mA Typical  $I_{CC}$  at 200-ns Cycle Time
- 1,000,000 *STORE* Cycles to QuantumTrap
- 100-Year Data Retention
- Single 3V Operation +20%, -10%

- Commercial and Industrial Temperature
- SOIC and SSOP Packages
- RoHS Compliance

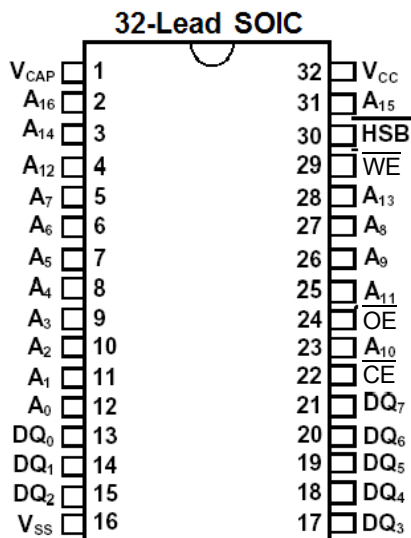
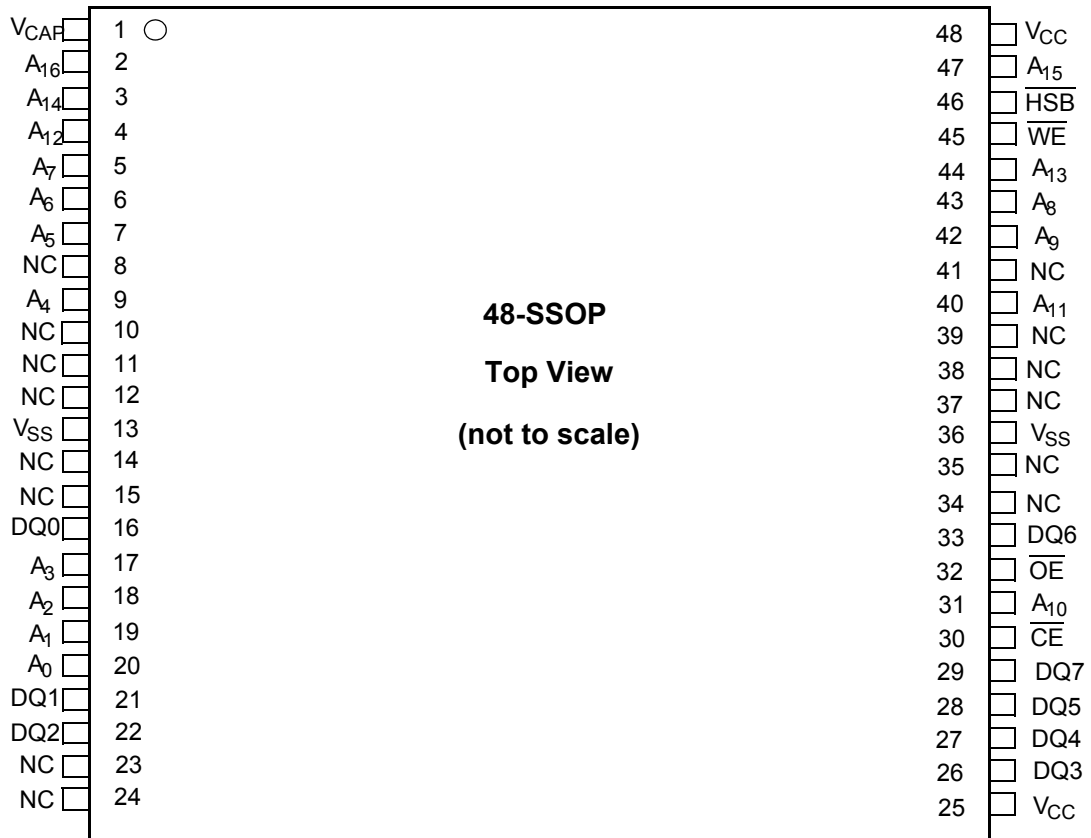
## Functional Description

The Cypress CY14B101L is a fast static RAM with a nonvolatile element in each memory cell. The embedded nonvolatile elements incorporate QuantumTrap technology producing the world's most reliable nonvolatile memory. The SRAM provides unlimited read and write cycles, while independent, nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the *STORE* operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the *RECALL* operation) from the nonvolatile memory. Both the *STORE* and *RECALL* operations are also available under software control.

## Logic Block Diagram



**Pin Configurations**



## Pin Definitions

Pin Name	I/O Type	Description
A <sub>0</sub> -A <sub>16</sub>	Input	<b>Address Inputs used to select one of the 131,072 bytes of the nvSRAM.</b>
DQ0-DQ7	Input/Output	<b>Bidirectional Data I/O lines.</b> Used as input or output lines depending on operation.
$\overline{WE}$	Input	<b>Write Enable Input, active LOW.</b> When selected LOW, enables data on the I/O pins to be written to the address location latched by the falling edge of $\overline{CE}$ .
$\overline{CE}$	Input	<b>Chip Enable Input, active LOW.</b> When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	<b>Output Enable, active LOW.</b> The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. Deasserting OE high causes the I/O pins to tri-state.
V <sub>SS</sub>	Ground	<b>Ground for the device.</b> Should be connected to ground of the system.
V <sub>CC</sub>	Power Supply	<b>Power Supply inputs to the device.</b>
$\overline{HSB}$	Input/Output	<b>Hardware Store Busy.</b> When low this output indicates a Hardware Store is in progress. When pulled low external to the chip it will initiate a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected. (Connection Optional)
V <sub>CAP</sub>	Power Supply	<b>Autostore Capacitor.</b> Supplies power to nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	<b>No Connects.</b> This pin is not connected to the die.

## Device Operation

The CY14B101L nvSRAM is made up of two functional components paired in the same physical cell. These are a SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM can be transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to SRAM (the RECALL operation). This unique architecture allows all cells to be stored and recalled in parallel. During the STORE and RECALL operations SRAM READ and WRITE operations are inhibited. The CY14B101L supports unlimited reads and writes just like a typical SRAM. In addition, it provides unlimited RECALL operations from the nonvolatile cells and up to 1 million STORE operations.

### SRAM Read

The CY14B101L performs a READ cycle whenever  $\overline{CE}$  and  $\overline{OE}$  are low while  $\overline{WE}$  and  $\overline{HSB}$  are high. The address specified on pins A<sub>0-16</sub> determines which of the 131,072 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of t<sub>AA</sub> (READ cycle #1). If the READ is initiated by  $\overline{CE}$  or  $\overline{OE}$ , the outputs will be valid at t<sub>ACE</sub> or at t<sub>DOE</sub>, whichever is later (READ cycle #2). The data outputs will repeatedly respond to address changes within the t<sub>AA</sub> access time without the need for transitions on any control input pins, and will remain valid until another address change or until  $\overline{CE}$  or  $\overline{OE}$  is brought high, or  $\overline{WE}$  or  $\overline{HSB}$  is brought low.

### SRAM Write

A WRITE cycle is performed whenever  $\overline{CE}$  and  $\overline{WE}$  are low and  $\overline{HSB}$  is high. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\overline{CE}$  or  $\overline{WE}$  goes high at the end of the cycle. The data on the common I/O pins I/O<sub>0-7</sub> will be written into the memory if it is valid t<sub>SD</sub> before the end of a  $\overline{WE}$  controlled WRITE or before the end of an  $\overline{CE}$  controlled WRITE. It is recommended that  $\overline{OE}$  be kept high during the entire WRITE cycle to avoid data

bus contention on common I/O lines. If  $\overline{OE}$  is left low, internal circuitry will turn off the output buffers t<sub>HZWE</sub> after  $\overline{WE}$  goes low.

### AutoStore™ Operation

The CY14B101L stores data to nvSRAM using one of three storage operations. These three operations are Hardware Store, activated by  $\overline{HSB}$ , Software Store, activated by an address sequence, and AutoStore, on device power-down. AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101L.

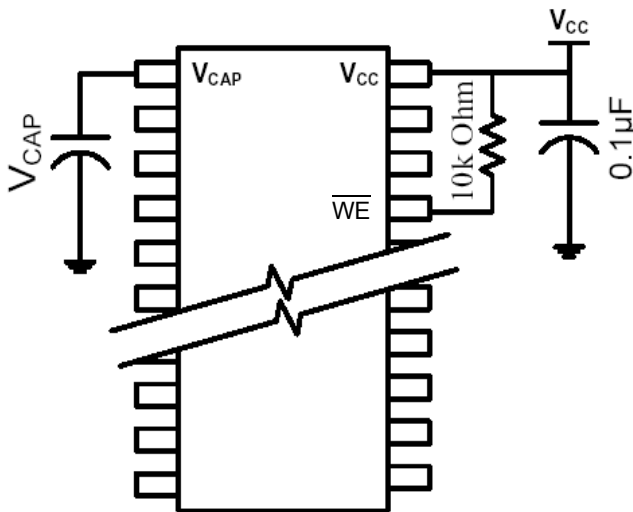
During normal operation, the device will draw current from V<sub>CC</sub> to charge a capacitor connected to the V<sub>CAP</sub> pin. This stored charge will be used by the chip to perform a single STORE operation. If the voltage on the V<sub>CC</sub> pin drops below V<sub>SWITCH</sub>, the part will automatically disconnect the V<sub>CAP</sub> pin from V<sub>CC</sub>. A STORE operation will be initiated with power provided by the V<sub>CAP</sub> capacitor.

Figure 1 shows the proper connection of the storage capacitor (V<sub>CAP</sub>) for automatic store operation. Refer to the DC Characteristics table for the size of V<sub>CAP</sub>. The voltage on the V<sub>CAP</sub> pin is driven to 5V by a charge pump internal to the chip. A pull-up should be placed on  $\overline{WE}$  to hold it inactive during power-up.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware Store operations will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a WRITE operation has taken place. The  $\overline{HSB}$  signal can be monitored by the system to detect an AutoStore cycle is in progress.

### Hardware STORE (HSB) Operation

The CY14B101L provides the  $\overline{HSB}$  pin for controlling and acknowledging the STORE operations. The  $\overline{HSB}$  pin can be used to request a hardware STORE cycle. When the  $\overline{HSB}$  pin is driven low, the CY14B101L will conditionally initiate a STORE operation after t<sub>DELAY</sub>. An actual STORE cycle will only begin if a WRITE to the SRAM took place since the last



**Figure 1. AutoStore™ Mode**

STORE or RECALL cycle. The  $\overline{\text{HSB}}$  pin also acts as an open drain driver that is internally driven low to indicate a busy condition while the STORE (initiated by any means) is in progress.

SRAM READ and WRITE operations that are in progress when  $\overline{\text{HSB}}$  is driven low by any means are given time to complete before the STORE operation is initiated. After  $\overline{\text{HSB}}$  goes low, the CY14B101L will continue SRAM operations for  $t_{\text{DELAY}}$ . During  $t_{\text{DELAY}}$ , multiple SRAM READ operations may take place. If a WRITE is in progress when  $\overline{\text{HSB}}$  is pulled low it will be allowed a time,  $t_{\text{DELAY}}$ , to complete. However, any SRAM WRITE cycles requested after  $\overline{\text{HSB}}$  goes low will be inhibited until  $\overline{\text{HSB}}$  returns high.

During any STORE operation, regardless of how it was initiated, the CY14B101L will continue to drive the  $\overline{\text{HSB}}$  pin low, releasing it only when the STORE is complete. Upon completion of the STORE operation the CY14B101L will remain disabled until the  $\overline{\text{HSB}}$  pin returns high.

If  $\overline{\text{HSB}}$  is not used, it should be left unconnected.

### Hardware RECALL (Power-up)

During power-up, or after any low-power condition ( $V_{\text{CC}} < V_{\text{SWITCH}}$ ), an internal RECALL request will be latched. When  $V_{\text{CC}}$  once again exceeds the sense voltage of  $V_{\text{SWITCH}}$ , a RECALL cycle will automatically be initiated and will take  $t_{\text{HRECALL}}$  to complete.

### Software STORE

Data can be transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B101L software STORE cycle is initiated by executing sequential

$\overline{\text{CE}}$ -controlled READ cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other READ or WRITE accesses intervene in the sequence, or the sequence will be aborted and no STORE or RECALL will take place.

To initiate the software STORE cycle, the following READ sequence must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with  $\overline{\text{CE}}$  controlled READs or  $\overline{\text{OE}}$  controlled READs. Once the sixth address in the sequence has been entered, the STORE cycle will commence and the chip will be disabled. It is important that READ cycles and not WRITE cycles be used in the sequence, although it is not necessary that  $\overline{\text{OE}}$  be low for the sequence to be valid. After the  $t_{\text{STORE}}$  cycle time has been fulfilled, the SRAM will again be activated for READ and WRITE operation.

### Software RECALL

Data can be transferred from the nonvolatile memory to the SRAM by a software address sequence. A software RECALL cycle is initiated with a sequence of READ operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of  $\overline{\text{CE}}$  controlled READ operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two-step procedure. First, the SRAM data is cleared, and second, the nonvolatile information is transferred into the SRAM cells. After the  $t_{\text{RECALL}}$  cycle time the SRAM will once again be ready for READ and WRITE operations. The RECALL operation in no way alters the data in the nonvolatile elements.

**Table 1. Mode Selection**

$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	A15 - A0	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active  [1,2,3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Autostore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active  [1,2,3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active $I_{CC2}$  [1,2,3]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active  [1,2,3]

### Preventing AutoStore

The AutoStore function can be disabled by initiating an AutoStore Disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore Disable sequence, the following sequence of CE-controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore can be re-enabled by initiating an AutoStore Enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore Enable sequence, the following sequence of CE-controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (Hardware or Software) needs to be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

### Data Protection

The CY14B101L protects data from corruption during low-voltage conditions by inhibiting all externally initiated STORE and WRITE operations. The low voltage condition is detected when  $V_{CC} \leq V_{SWITCH}$ . If the CY14B101L is in a WRITE mode (both CE and WE low) at power-up, after a RECALL, or after a STORE, the WRITE will be inhibited until a negative transition on CE or WE is detected. This protects

**Notes:**

1. The six consecutive address locations must be in the order listed.  $\overline{\text{WE}}$  must be HIGH during all six cycles to enable a non-volatile cycle.
2. While there are 17 address lines on the CY14B101L, only the lower 16 lines are used to control software modes.
3. I/O state depends on the state of  $\overline{\text{OE}}$ . The I/O table shown assumes  $\overline{\text{OE}}$  Low.

against inadvertent writes during power-up or brown-out conditions.

6. I/O loading.

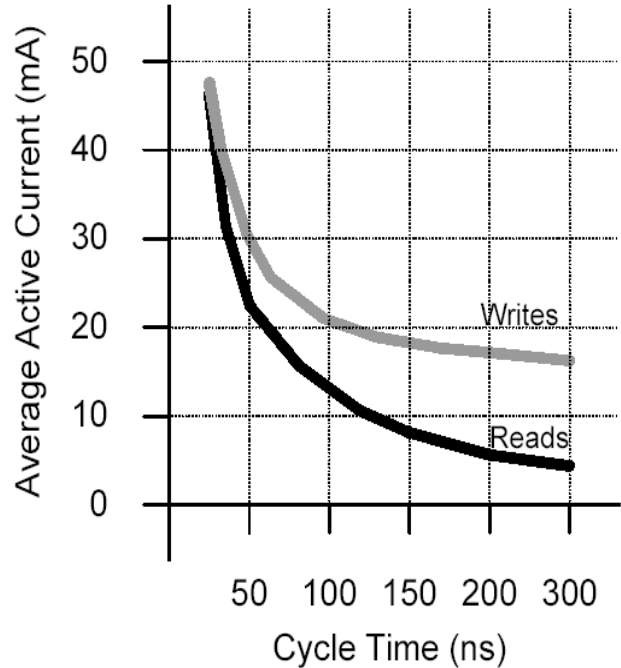
**Noise Considerations**

The CY14B101L is a high-speed memory and so must have a high-frequency bypass capacitor of approximately 0.1  $\mu$ F connected between  $V_{CC}$  and  $V_{SS}$ , using leads and traces that are as short as possible. As with all high-speed CMOS ICs, careful routing of power, ground and signals will reduce circuit noise.

**Low Average Active Power**

CMOS technology provides the CY14B101L the benefit of drawing significantly less current when it is cycled at times longer than 50 ns. *Figure 2* shows the relationship between  $I_{CC}$  and READ/WRITE cycle time. Worst-case current consumption is shown for commercial temperature range,  $V_{CC} = 3.6V$ , and chip enable at maximum frequency. Only standby current is drawn when the chip is disabled. The overall average current drawn by the CY14B101L depends on the following items:

1. The duty cycle of chip enable.
2. The overall cycle rate for accesses.
3. The ratio of READs to WRITEs.
4. The operating temperature.
5. The  $V_{CC}$  level.



**Figure 2. Current vs. Cycle Time**

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage on V <sub>CC</sub> Relative to GND.....	-0.5V to 4.1V
Voltage Applied to Outputs in High-Z State .....	-0.5V to V <sub>CC</sub> + 0.5V
Input Voltage .....	-0.5V to V <sub>CC</sub> + 0.5V
Transient Voltage (<20 ns) on Any Pin to Ground Potential.....	-2.0V to V <sub>CC</sub> + 2.0V

Package Power Dissipation Capability (T <sub>A</sub> = 25°C) .....	1.0W
Surface Mount Lead Soldering Temperature (3 Seconds).....	+240°C
Output Short Circuit Current <sup>[4]</sup> .....	15 mA
Static Discharge Voltage..... (per MIL-STD-883, Method 3015)	> 2001V
Latch-up Current.....	> 200 mA

**Table 2. Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	-40°C to +85°C	2.7V to 3.6V

Shaded area contains Advance Information

### DC Electrical Characteristics Over the Operating Range (V<sub>CC</sub> = 2.7V to 3.6V)<sup>[5]</sup>

Parameter	Description	Test Conditions	Min.	Max.	Unit
I <sub>CC1</sub>	Average V <sub>CC</sub> Current	t <sub>RC</sub> = 25 ns t <sub>RC</sub> = 35 ns t <sub>RC</sub> = 45 ns Dependent on output loading and cycle rate. Values obtained without output loads. I <sub>OUT</sub> = 0mA.	Commercial	65 55 50	mA mA mA
I <sub>CC2</sub>	Average V <sub>CC</sub> Current during STORE	All Inputs Don't Care, V <sub>CC</sub> = Max. Average current for duration t <sub>STORE</sub>		3	mA
I <sub>CC3</sub>	Average V <sub>CC</sub> Current at t <sub>AA</sub> = 200 ns, 3V, 25°C typical	WE > (V <sub>CC</sub> - 0.2). All other inputs cycling. Dependent on output loading and cycle rate. Values obtained without output loads. I <sub>OUT</sub> = 0mA.		5	mA
I <sub>CC4</sub>	Average V <sub>CAP</sub> Current during AutoStore Cycle	All Inputs Don't Care, V <sub>CC</sub> = Max. Average current for duration t <sub>STORE</sub>		3	mA
I <sub>SB</sub>	V <sub>CC</sub> Standby Current	WE > (V <sub>CC</sub> - 0.2). All others V <sub>IN</sub> < 0.2V or > (V <sub>CC</sub> - 0.2V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0MHz.		2	mA
I <sub>IX</sub>	Input Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>	-1	+1	μA
I <sub>OZ</sub>	Off-State Output Leakage Current	V <sub>CC</sub> = Max., V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub> , CE or OE > V <sub>IH</sub>	-1	+1	μA
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		V <sub>SS</sub> - 0.5	0.8	V
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OUT</sub> = -2 mA	2.4		V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OUT</sub> = 4 mA		0.4	V
V <sub>CAP</sub>	Storage Capacitor	Between V <sub>CAP</sub> pin and V <sub>SS</sub> , 5V Rated	17	57	μF

**Table 3. Capacitance<sup>[6]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz,	7	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 0 to 3.0V	7	pF

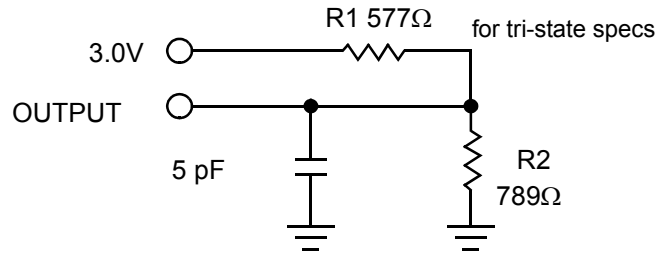
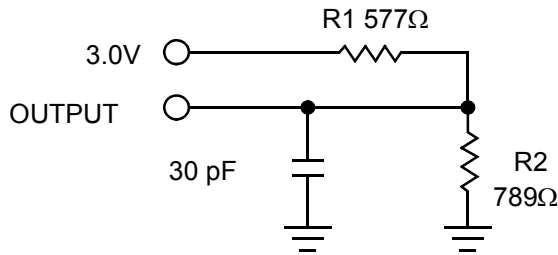
**Notes:**

4. Outputs shorted for no more than one second. No more than one output shorted at a time.
5. Typical conditions for the Active Current shown on the front page of the data sheet are average values at 25°C (room temperature), and V<sub>CC</sub> = 3V. Not 100% tested.
6. These parameters are guaranteed but not tested.

**Table 4. Thermal Resistance<sup>[6]</sup>**

Parameter	Description	Test Conditions	48-SSOP	32-SOIC	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	TBD	TBD	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		TBD	TBD	°C/W

**AC Test Loads**



**AC Test Conditions**

Input Pulse Levels..... 0V to 3V  
 Input Rise and Fall Times (10% - 90%)..... ≤5ns  
 Input and Output Timing Reference Levels..... 1.5V



**Table 5. AC Switching Characteristics**

Parameters		Description	CY14B101L-25		CY14B101L-35		CY14B101L-45		Unit
Cypress Parameter	Alt. Parameter		Min.	Max.	Min.	Max.	Min.	Max.	
<b>SRAM Read Cycle</b>									
$t_{ACE}$	$t_{ACS}$	Chip Enable Access Time		25		35		45	ns
$t_{RC}^{[7]}$	$t_{RC}$	Read Cycle Time	25		35		45		ns
$t_{AA}^{[8]}$	$t_{AA}$	Address Access Time		25		35		45	ns
$t_{DOE}$	$t_{OE}$	Output Enable to Data Valid		12		15		20	ns
$t_{OHA}$	$t_{OH}$	Output Hold After Address Change	3		3		3		ns
$t_{LZCE}^{[9]}$	$t_{LZ}$	Chip Enable to Output Active	3		3		3		ns
$t_{HZCE}^{[9]}$	$t_{HZ}$	Chip Disable to Output Inactive		10		13		15	ns
$t_{LZOE}^{[9]}$	$t_{OLZ}$	Output Enable to Output Active	0		0		0		ns
$t_{HZOE}^{[9]}$	$t_{OHZ}$	Output Disable to Output Inactive		10		13		15	ns
$t_{PU}^{[6]}$	$t_{PA}$	Chip Enable to Power Active	0		0		0		ns
$t_{PD}^{[6]}$	$t_{PS}$	Chip Disable to Power Standby		25		35		45	ns
<b>SRAM Write Cycle</b>									
$t_{WC}$	$t_{WC}$	Write Cycle Time	25		35		45		ns
$t_{PWE}$	$t_{WP}$	Write Pulse Width	20		25		30		ns
$t_{SCE}$	$t_{CW}$	Chip Enable To End of Write	20		25		30		ns
$t_{SD}$	$t_{DW}$	Data Set-Up to End of Write	10		12		15		ns
$t_{HD}$	$t_{DH}$	Data Hold After End of Write	0		0		0		ns
$t_{AW}$	$t_{AW}$	Address Set-Up to End of Write	20		25		30		ns
$t_{SA}$	$t_{AS}$	Address Set-Up to Start of Write	0		0		0		ns
$t_{HA}$	$t_{WR}$	Address Hold After End of Write	0		0		0		ns
$t_{HZWE}^{[9,10]}$	$t_{WZ}$	Write Enable to Output Disable		10		13		15	ns
$t_{LZWE}^{[9]}$	$t_{OW}$	Output Active after End of Write	3		3		3		ns

**Notes:**

7.  $\overline{WE}$  must be HIGH during SRAM Read Cycles.
8. Device is continuously selected with  $\overline{CE}$  and  $\overline{OE}$  both Low.
9. Measured  $\pm 200\text{mV}$  from steady state output voltage.
10. If  $\overline{WE}$  is Low when  $\overline{CE}$  goes Low, the outputs remain in the High Impedance State

**Table 6. AutoStore/Power-Up RECALL**

Parameters	Description	CY14B101L		Units
		Min.	Max.	
$t_{HRECALL}^{[11]}$	Power-Up RECALL Duration		20	ms
$t_{STORE}^{[12]}$	STORE Cycle Duration		12.5	ms
$V_{SWITCH}$	Low Voltage Trigger Level	2.55	2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		$\mu$ s

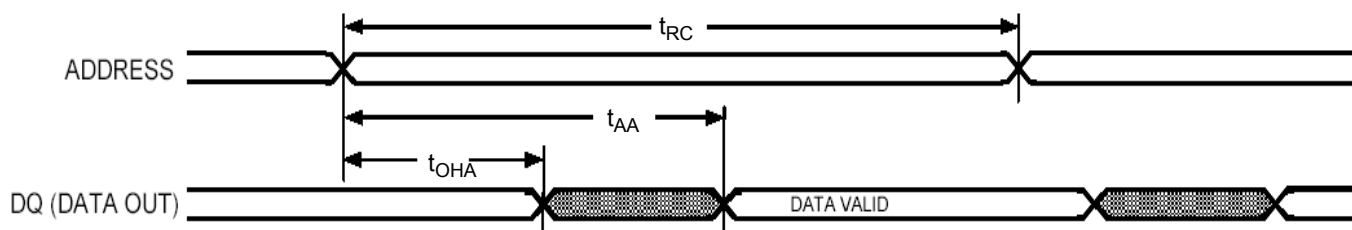
**Table 7. Software Controlled STORE/RECALL Cycle<sup>[13,14]</sup>**

Parameters	Description	CY14B101L-25		CY14B101L-35		CY14B101L-45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	STORE/RECALL Initiation Cycle Time	25		35		45		ns
$t_{AS}$	Address Set-Up Time	0		0		0		ns
$t_{CW}$	Clock Pulse Width	20		25		30		ns
$t_{GLAX}$	Address Hold Time	20		20		20		ns
$t_{RECALL}$	RECALL Duration		40		40		40	$\mu$ s

**Table 8. Hardware STORE Cycle**

Parameters	Description	CY14B101L		Units
		Min	Max	
$t_{DELAY}^{[15]}$	Time allowed to complete SRAM Cycle	1		$\mu$ s
$t_{HLHX}$	Hardware STORE Pulse Width	15		ns
$t_{HLBL}$	Hardware STORE Low to STORE Busy		300	ns

### Switching Waveforms

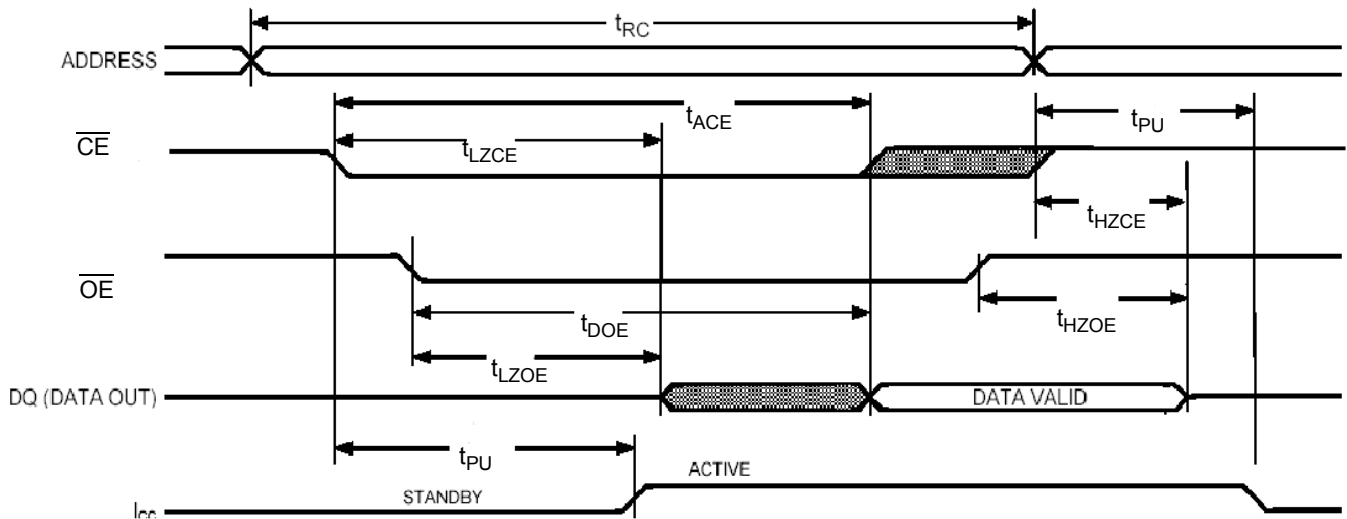


**Figure 3. SRAM Read Cycle #1: Address Controlled<sup>[7,8,16]</sup>**

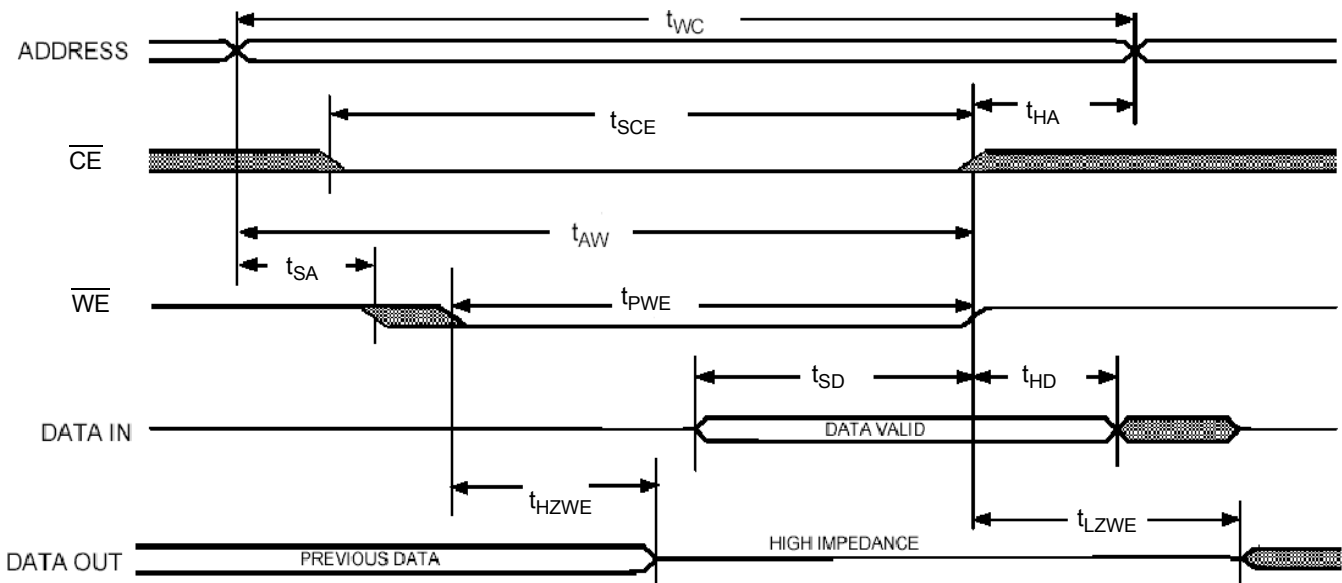
**Notes:**

11.  $t_{HRECALL}$  starts from the time  $V_{CC}$  rises above  $V_{SWITCH}$ .
12. If an SRAM Write has not taken place since the last nonvolatile cycle, no STORE will take place.
13. The software sequence is clocked with CE controlled or OE controlled READS.
14. The six consecutive addresses must be read in the order listed in the Mode Selection table.  $\overline{WE}$  must be HIGH during all six consecutive cycles.
15. Read and Write cycles in progress before  $\overline{HSB}$  are given this amount of time to complete.
16.  $\overline{HSB}$  must remain HIGH during READ and WRITE cycles.

**Switching Waveforms (continued)**



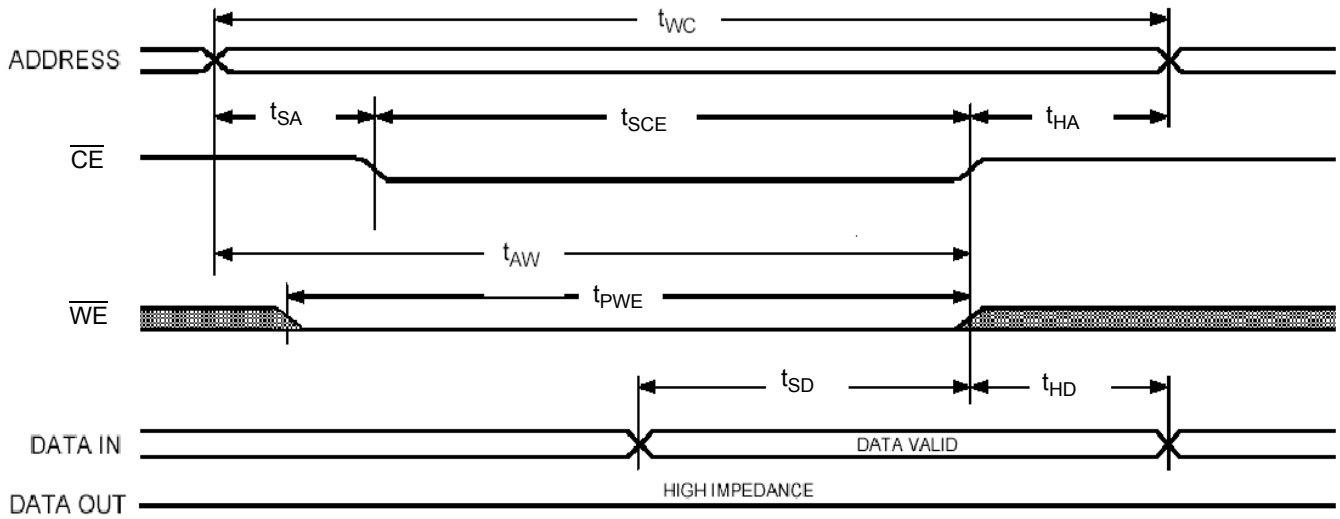
**Figure 4. SRAM Read Cycle #2:  $\overline{CE}$  and  $\overline{OE}$  Controlled<sup>[7,16]</sup>**



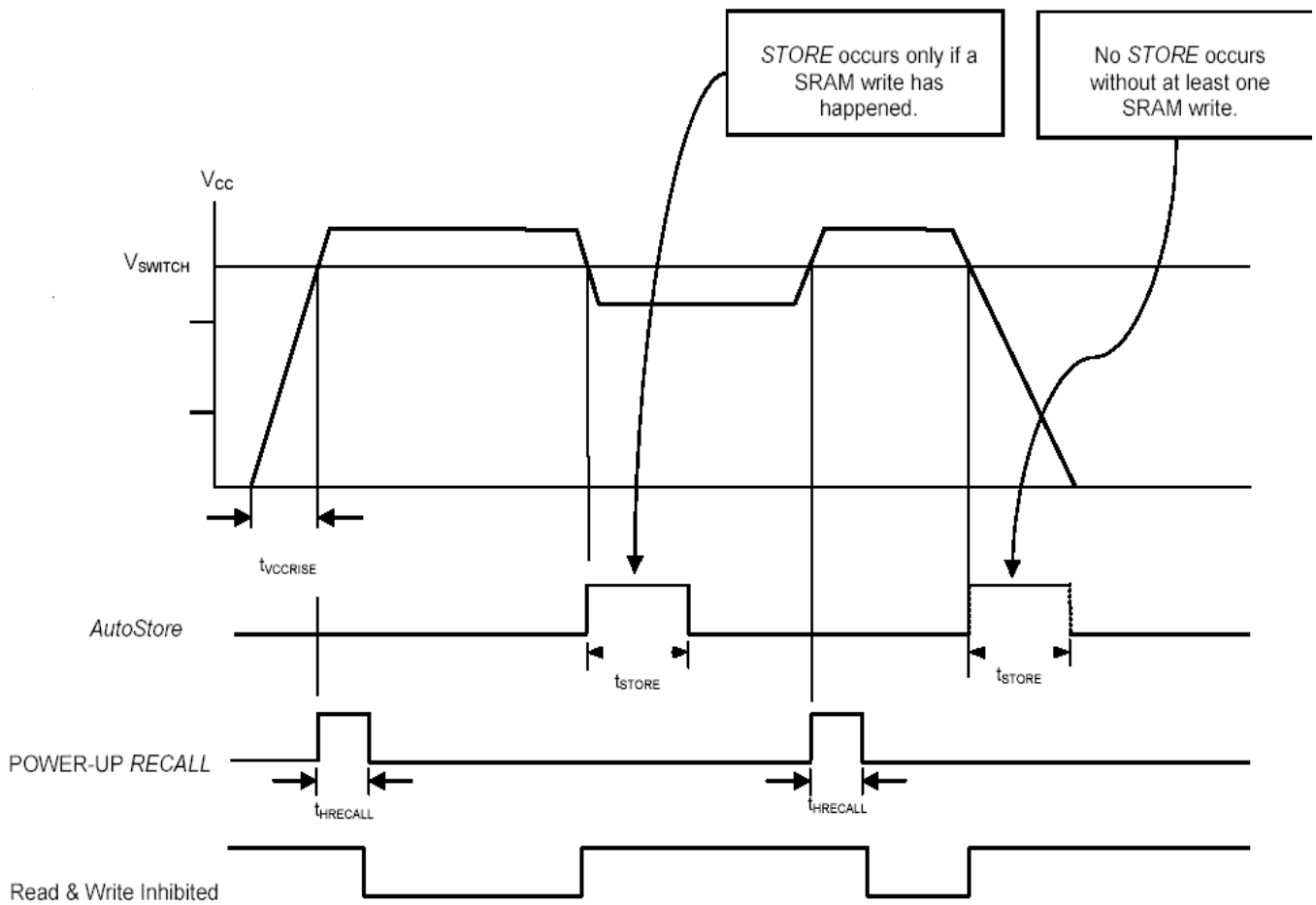
**Figure 5. SRAM Write Cycle #1:  $\overline{WE}$  Controlled<sup>[16,17]</sup>**

**Note:**  
17.  $\overline{CE}$  or  $\overline{WE}$  must be  $\geq V_{IH}$  during address transitions.

**Switching Waveforms** (continued)

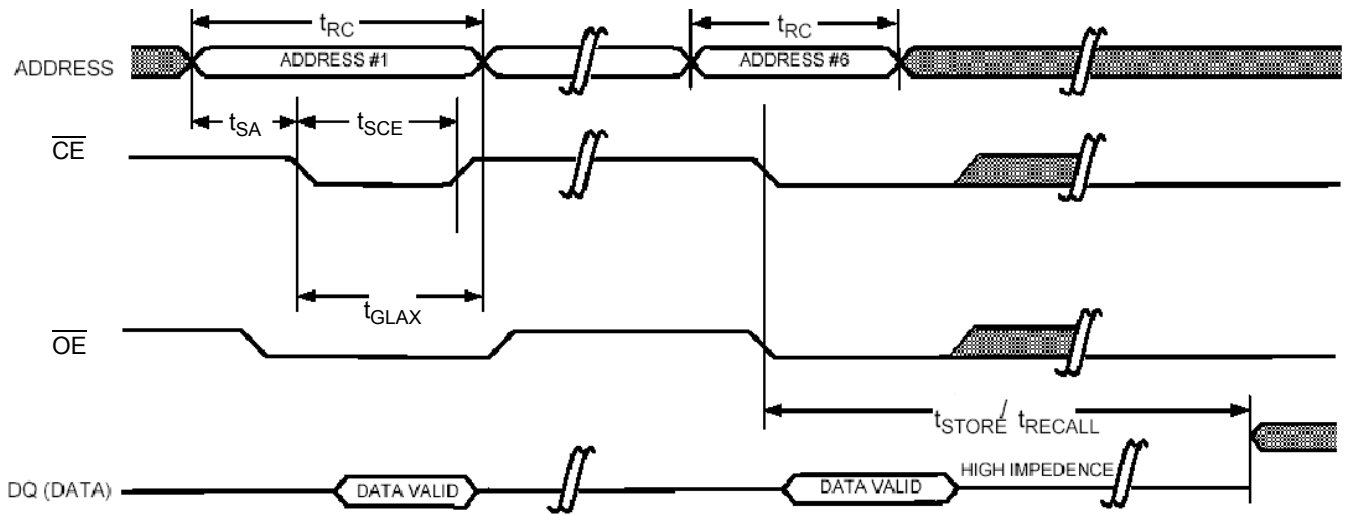


**Figure 6. SRAM Write Cycle #2:  $\overline{CE}$  Controlled**

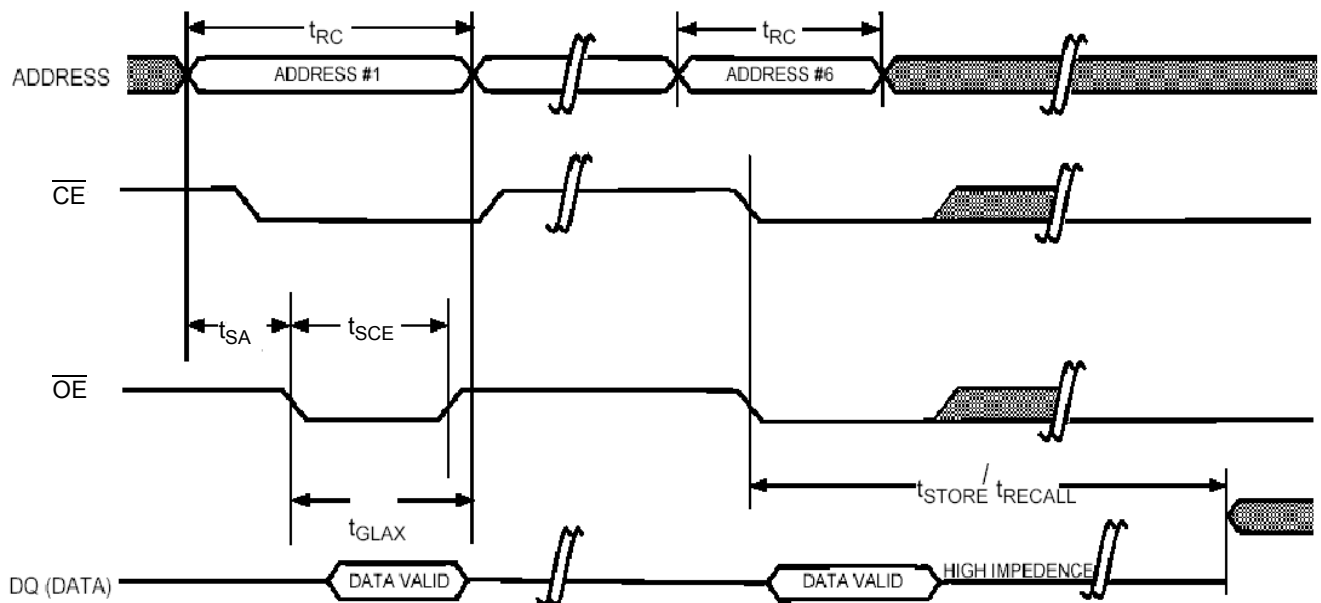


**Figure 7. AutoStore/Power-Up RECALL**

**Switching Waveforms** (continued)

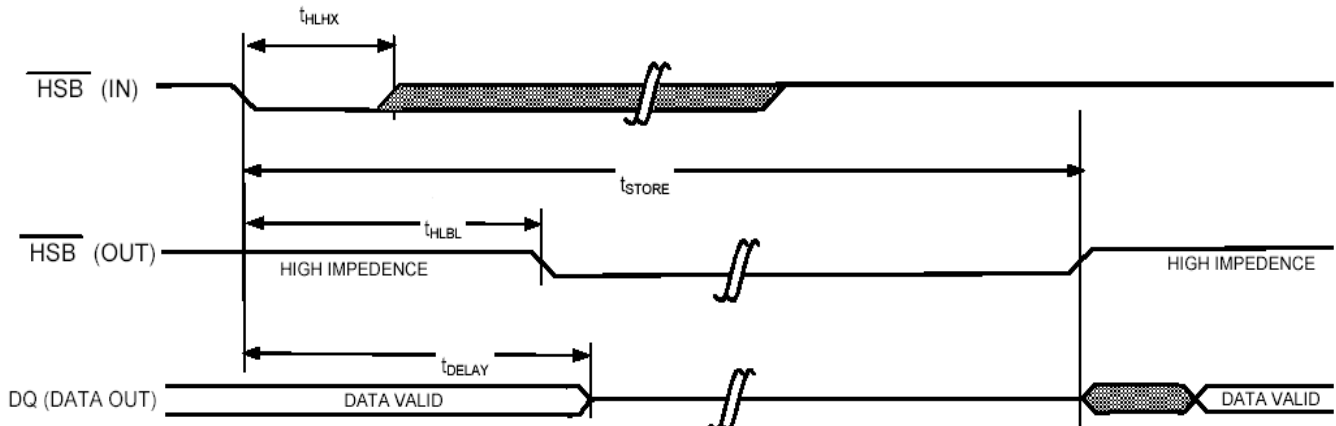


**Figure 8.  $\overline{\text{CE}}$ -controlled Software STORE/RECALL Cycle<sup>[14]</sup>**



**Figure 9.  $\overline{\text{OE}}$ -controlled Software STORE/RECALL Cycle<sup>[14]</sup>**

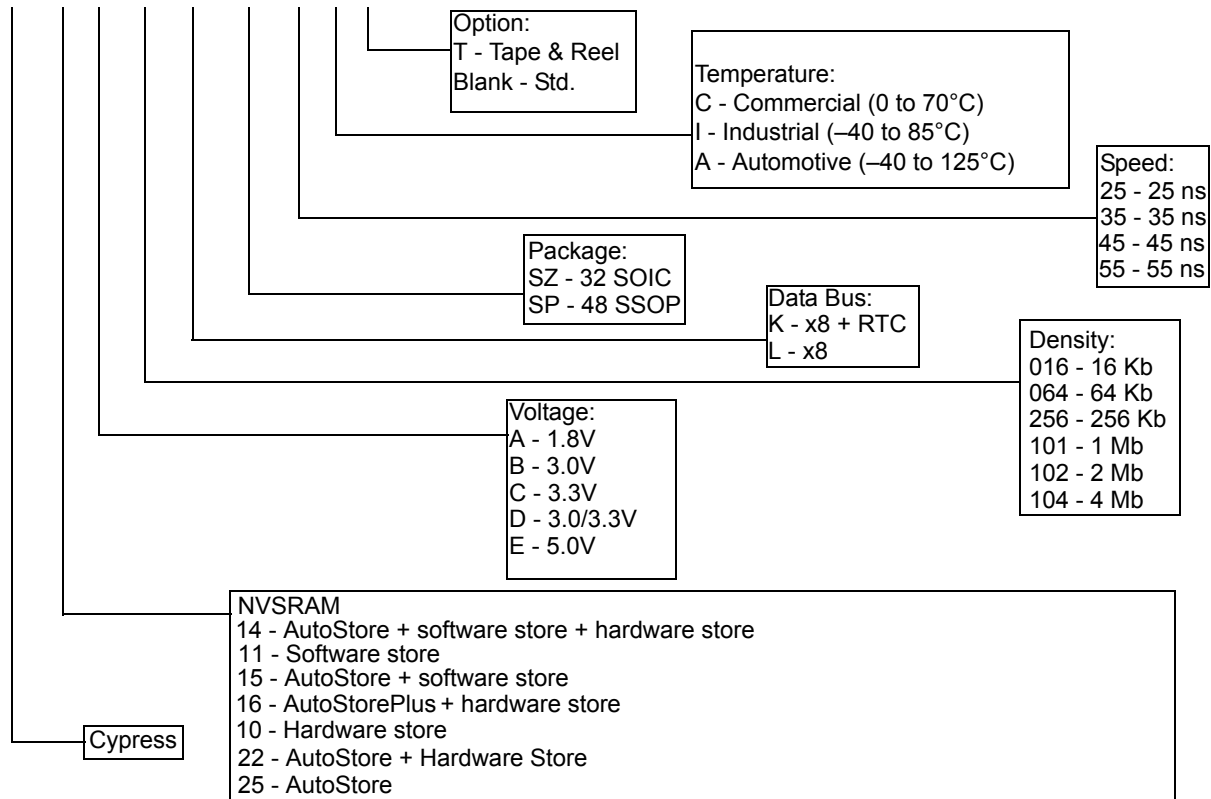
**Switching Waveforms** (continued)



**Figure 10. Hardware STORE Cycle**

**PART NUMBERING NOMENCLATURE**

**CY 14 B 101 L - SZ 25 C T**



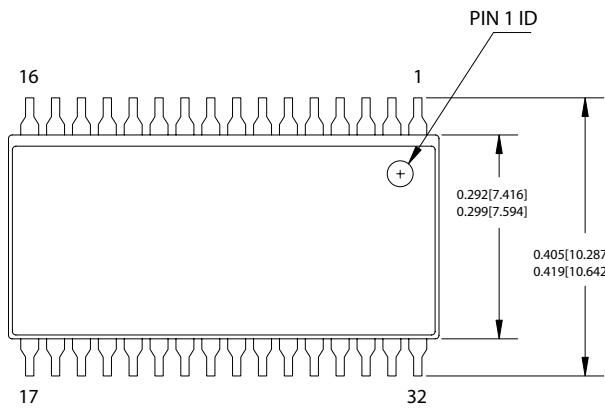
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
25	CY14B101L-SZ25CT	51-85127	32-pin SOIC Pb-Free	Commercial
	CY14B101L-SP25CT	51-85061	48-pin SSOP Pb-Free	
	CY14B101L-SZ25IT	51-85127	32-pin SOIC Pb-Free	Industrial
	CY14B101L-SP25IT	51-85061	48-pin SSOP Pb-Free	
	CY14B101L-SZ25I	51-85127	32-pin SOIC Pb-Free	
	CY14B101L-SP25I	51-85061	48-pin SSOP Pb-Free	
35	CY14B101L-SZ35CT	51-85127	32-pin SOIC Pb-Free	Commercial
	CY14B101L-SP35CT	51-85061	48-pin SSOP Pb-Free	
	CY14B101L-SZ35IT	51-85127	32-pin SOIC Pb-Free	Industrial
	CY14B101L-SP35IT	51-85061	48-pin SSOP Pb-Free	
	CY14B101L-SZ35I	51-85127	32-pin SOIC Pb-Free	
	CY14B101L-SP35I	51-85061	48-pin SSOP Pb-Free	

Shaded areas contain Advance information. Please contact your local Cypress sales representative for availability of these parts.

**Package Diagrams**

**32-Lead (300-Mil) SOIC (51-85127)**

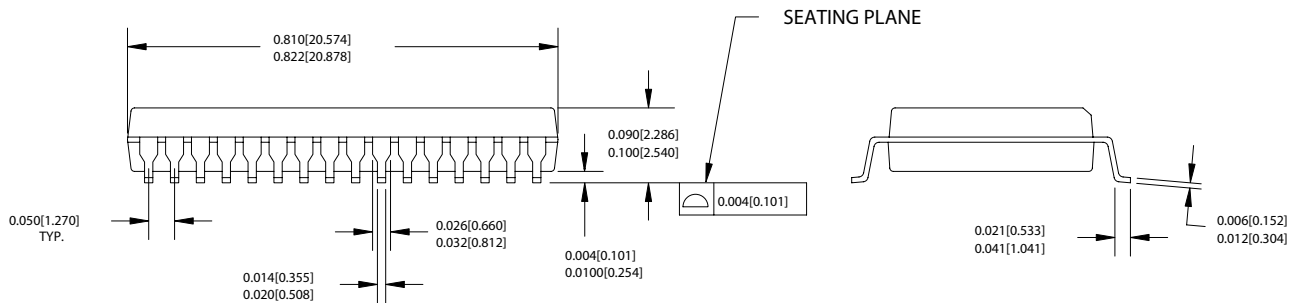


DIMENSIONS IN INCHES[MM]

MIN.  
MAX.

REFERENCE JEDEC MO-119

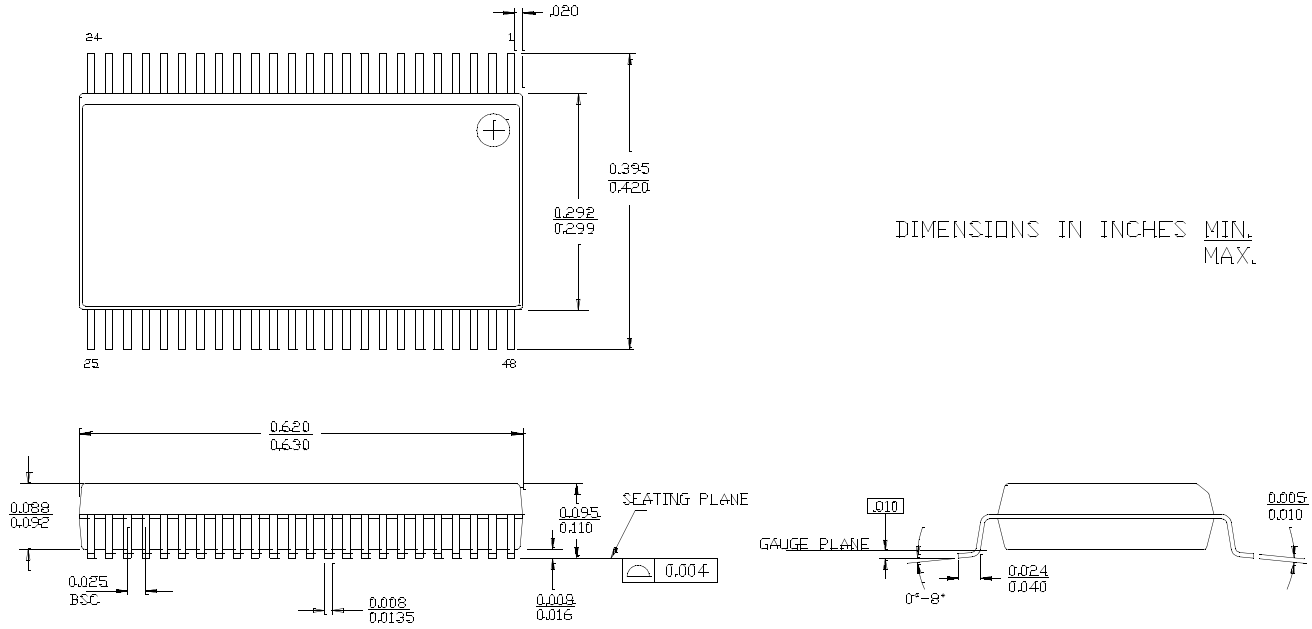
PART #	
S32.3	STANDARD PKG.
SZ32.3	LEAD FREE PKG.



51-85127-\*A

**Package Diagrams** (continued)

**48-Lead Shrunken Small Outline Package (51-85061)**



51-85061-1C

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**Document History Page**

<b>Document Title: CY14B101L 1-Mbit (128K x 8) nvSRAM</b> <b>Document Number: 001-06400</b>				
<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	425138	See ECN	TUP	New Data Sheet
*A	437321	See ECN	TUP	Show Data Sheet on external Web