FOR DETAILED INFORMATION SEE THE LATEST ISSUE OF HANDBOOK IC06 OR DATA SHEET

PHASE-LOCKED-LOOP WITH LOCK DETECTOR

FEATURES

- Low power consumption
- Centre frequency up to 17 MHz (typ.) at V_{CC} = 4.5 V
- Choice of two phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop;
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operation power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f_o	VCO centre frequency	C1 = 40 pF R1 = 3 kΩ V_{CC} = 5 V	19	19	MHz
C_I	input capacitance (pin 5)		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

GND = 0 V; T_{amb} = 25 °C

Notes

1. Applies to the phase comparator section only (VCO disabled).
   For power dissipation of VCO and demodulator sections see Figs 20, 21 and 22.
2. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$$ where:

f_i = input frequency in MHz
f_o = output frequency in MHz
$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
C_L = output load capacitance in pF
V_{CC} = supply voltage in V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38CP).
16-lead mini-pack; plastic (SO16; SOT109A).

GENERAL DESCRIPTION

The 74HC/HCT7046 are high-speed Si-gate CMOS devices and are specified in compliance with JEDEC standard no. 7.

The 74HC/HCT7046 are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and two different phase comparators (PC1 and PC2) with a common signal input amplifier and a common comparator input.

A lock detector is provided and this gives a HIGH level at pin 1 (LD) when the PLL is locked. The lock detector capacitor must be connected between pin 15 (C_{LD}) and pin 8 (GND). The value of the C_{LD} capacitor can be determined, using information supplied in Fig. 32

The input signal can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "7046" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

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APPLICATIONS

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control

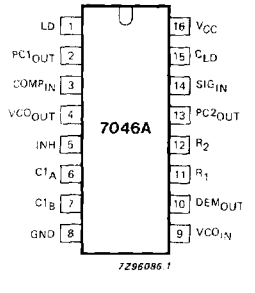

Fig. 1 Pin configuration.

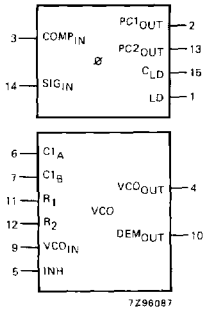

Fig. 2 Logic symbol.

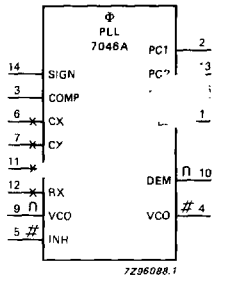

Fig. 3 IEC logic symbol.