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128K x 32 EEPROM Module

PUMA 68E4001/A-12/15/20

Issue 4.2 : November 1998

Description

The PUMA 68E4001/A is a 4Mbit CMOS EEPROM module in a JEDEC 68 pin surface mount PLCC. The plastic device is screened to ensure high reliability. Access times of 120, 150 and 200ns are available.The output width is user configurable as 8, 16, or 32 bits wide using $\overline{CS1}$-4 and is available in two pinout options, single $\overline{WE}$ or WE1-4 (version /A) . Page write (128 bytes) is performed in 5 ms (typical). The device also features both hardware and software data protection with DATA polling and Toggle bit indication of end of write . Write cycle endurance is 10,000 Erase/Write cycles with a data retention time of 10 years.

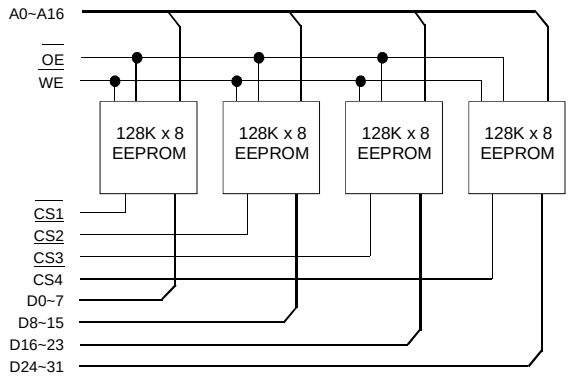
4,194,304 bit CMOS EEPROM Module

Features

- Access Times of 120/150/200 ns.
- User Configurable as 8 / 16 / 32 bit wide output.
- Commercial, Industrial, or Military grades.
- Operating Power 490 / 913 / 1760 mW (max).
- JEDEC 68 pin surface mount PLCC, available in two pinouts : Single $\overline{WE}$, $\overline{WE1}$~$\overline{4}$ is version A.
- High reliability plastic design
- Hardware and Software Data Protection.
- Endurance of 10^4 Erase/Write Cycles and Data Retention Time of 10 years.

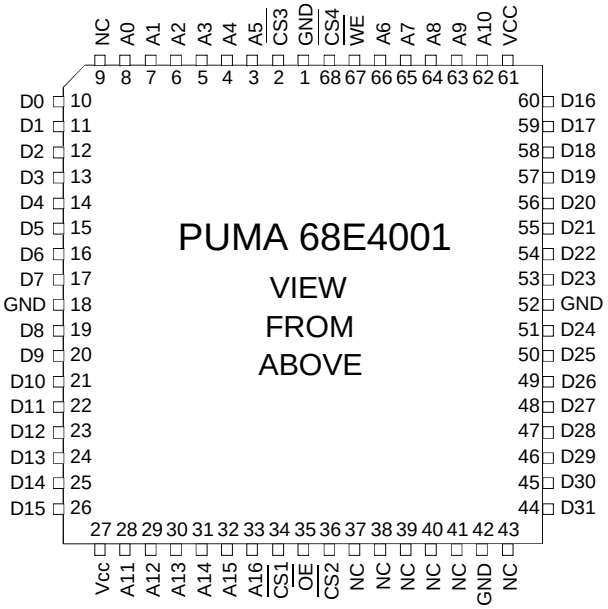
Block Diagram

(see page 11 for Block Diagram of option /A)



Pin Definition

(see page 11 for option /A Pinout)



Pin Functions

A0~16	Address Inputs	**D0~31**	Data Inputs/Outputs
$\overline{CS1}$~4	Chip Select	**$\overline{OE}$**	Output Enable
$\overline{WE}$	Write Enable (**$\overline{WE1}$~4** on version A)	**NC**	No Connect
V_{cc}	Power (+5V)	**GND**	Ground

DC OPERATING CONDITIONS

Absolute Maximum Ratings (1)

Operating Temperature	T_{OPR}	-55 to +125	˚C
Storage Temperature	T_{STG}	-65 to +150	˚C
Input voltages (including N.C. pins) with Respect to GND	V_{IN}	-0.6 to +6.25	V
Output voltages with respect to GND	V_{OUT}	-0.6 to V_{CC}+0.6	V

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

		min	*typ*	*max*	
DC Power Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+1	V
Operating Temp Range	T_A	0	-	70	˚C
	T_{AI}	-40	-	85	˚C (**I** Suffix)
	T_{AM}	-55	-	125	˚C (**M** Suffix)

DC Electrical Characteristics (T_A=-55°C to +125°C, V_{CC}=5V ± 10%)

Parameter		*Symbol*	*Test Condition*	*min*	*max*	*Unit*
Input Leakage Current		I_{LI1}	V_{IN} = GND to V_{CC} +1	-	40	µA
Output Leakage Current	32 bit	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CS}^{(1)}$=V_{IH}	-	40	µA
Operating Supply Current	32 bit	I_{CC32}	$\overline{CS}^{(1)}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, I_{OUT}=0mA, f=5MHz$^{(2)}$	-	320	mA
	16 bit	I_{CC16}	As above	-	166	mA
	8 bit	I_{CC8}	As above	-	89	mA
Standby Supply Current	TTL levels	I_{SB1}	$\overline{CS}^{(1)}$ = 2.0V to V_{CC}+1V	-	12	mA
	CMOS levels	I_{SB2}	$\overline{CS}^{(1)}$ = V_{CC}-0.3V to V_{CC}+1V	-	1.2	mA
Output Low Voltage		V_{OL}	I_{OL} = 2.1mA.	-	0.45	V
Output High Voltage		V_{OH}	I_{OH} = -400µA.	2.4	-	V

Notes (1) $\overline{CS}$ above are accessed through $\overline{CS1\text{-}4}$. These inputs must be operated simultaneously for 32 bit operation, in pairs in 16 bit mode and singly for 8 bit mode.

(2) Also for $\overline{WE1\sim4}$ on the PUMA 68E4001A version. Additionally, $\overline{WE1\sim4}$ are accessed as in note (1) above.

Capacitance (T_A=25°C, f=1MHz) Note: These parameters are calculated, not measured.

Parameter		*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance	$\overline{CS1\sim4}$, $\overline{WE1\sim4}$(1)	C_{IN1}	V_{IN}=0V	-	20	pF
	Other Inputs	C_{IN2}	V_{IN}=0V	-	22	pF
Output Capacitance		C_{OUT}	V_{OUT}=0V	-	22	pF

Notes: (1) On the PUMA 68E4001A version only.

AC OPERATING CONDITIONS

Read Cycle

		12		15		20		
Parameter	*Symnbol*	*min*	*max*	*min*	*max*	*min*	*max*	*Unit*
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
Chip Select Access Time	t_{CS}	-	120	-	150	-	200	ns
Output Enable Access Time	t_{OE}	0	60	0	70	0	80	ns
Chip Select High to High Z Output (1)	t_{HZ}	0	50	0	50	0	50	ns
Output Enable High to High Z Output (1)	t_{OHZ}	0	50	0	50	0	50	ns
Chip Select Low to Active Output (1)	t_{LZ}	0	-	0	-	0	-	ns
Output Enable Low to Active Output (1)	t_{OLZ}	0	-	0	-	0	-	ns
Output Hold from Address Change	t_{OH}	0	-	0	-	0	-	ns

Notes: (1) t_{HZ} max. and t_{OLZ} max. are measured with CL = 5pF, from the point when Chip Select or Output Enable return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} and t_{OHZ} are shown for reference only: they are characterized and not tested.

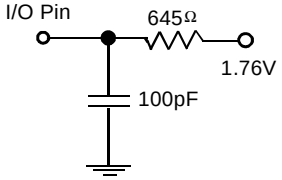
Write Cycle

Parameter	*Symbol*	*min*	*typ*	*max*	*Unit*
Write Cycle Time	t_{WC}	-	-	10	ms
Address Set-up Time	t_{AS}	0	-	-	ns
Address Hold Time	t_{AH}	50	-	-	ns
Output Enable Set-up Time	t_{OES}	0	-	-	ns
Output Enable Hold Time	t_{OEH}	0	-	-	ns
Chip Select Set-up Time	t_{CS}	0	-	-	ns
Chip Select Hold Time	t_{CH}	0	-	-	ns
Write Pulse Width	t_{WP}	100	-	-	ns
Write Enable High Recovery	t_{WPH}	50	-	-	ns
Data Set-up Time	t_{DS}	50	-	-	ns
Data Hold Time	t_{DH}	0	-	-	ns
Delay to Next Write	t_{DW}	10	-	-	µs
Byte Load Cycle	t_{BLC}	-	-	150	µs

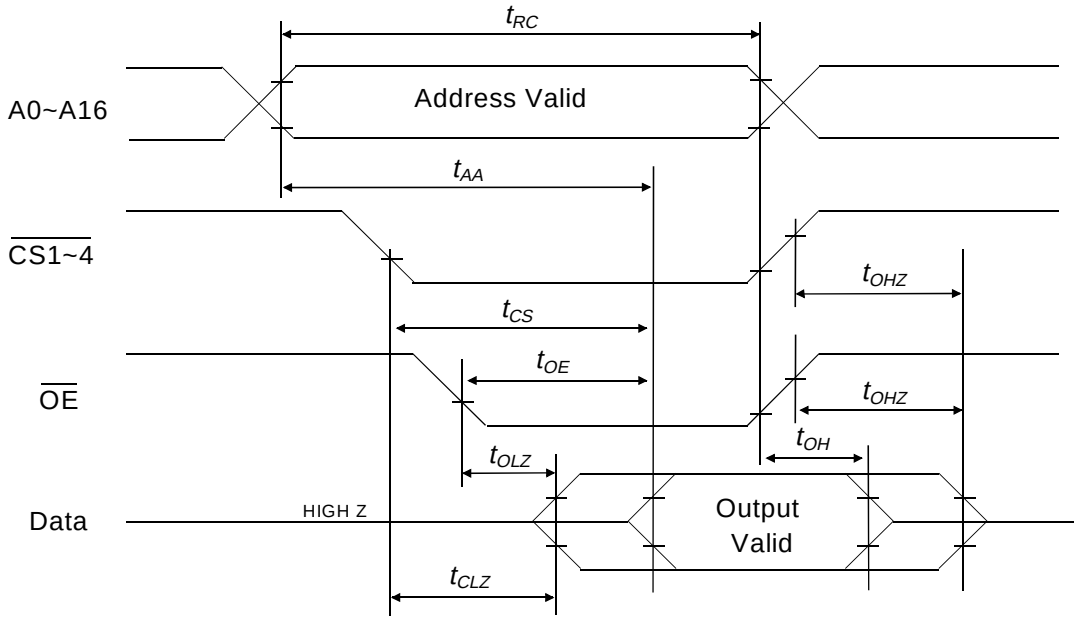
AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 10ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

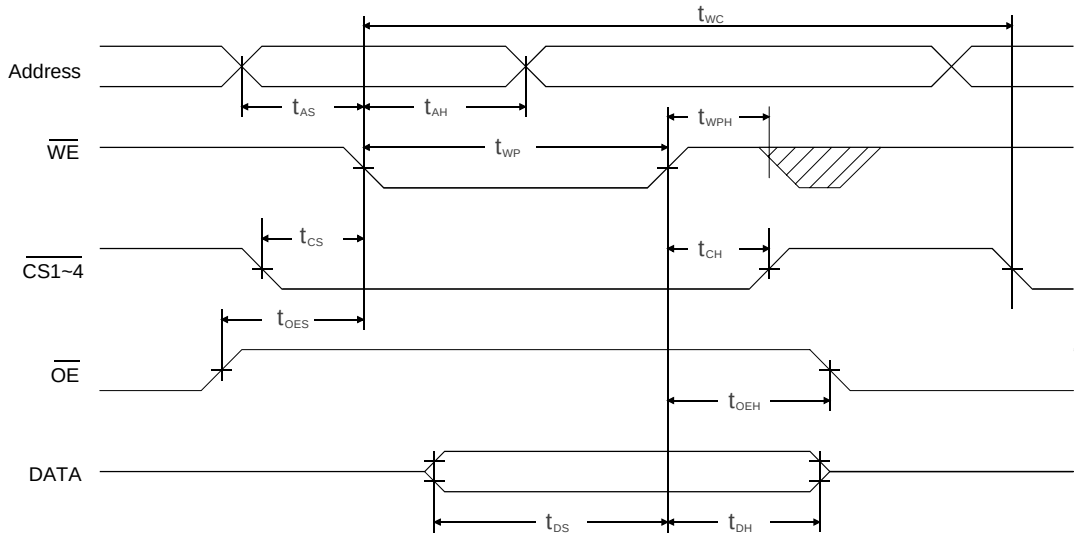
Output Test Load



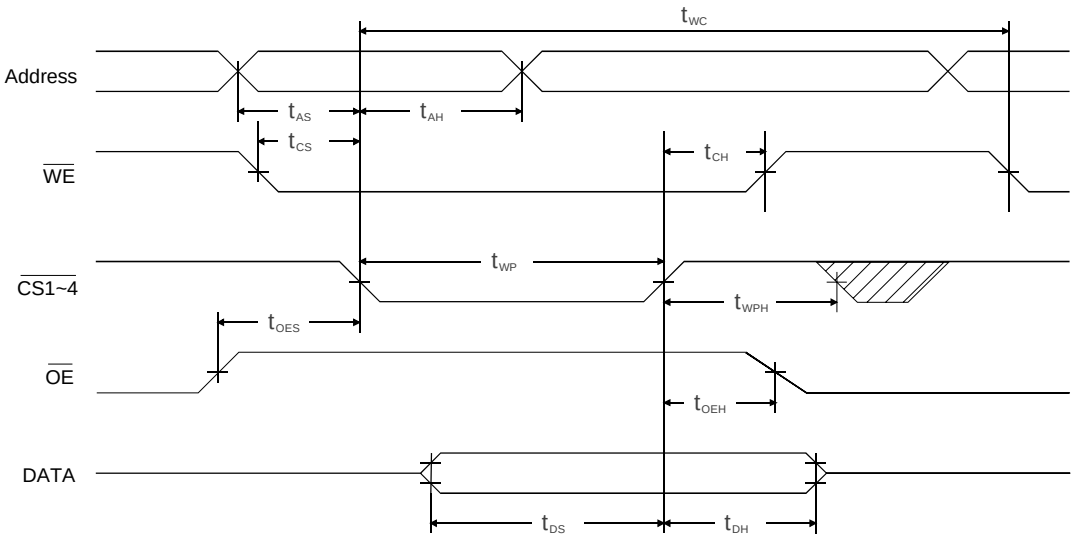
Read Cycle Timing Waveform



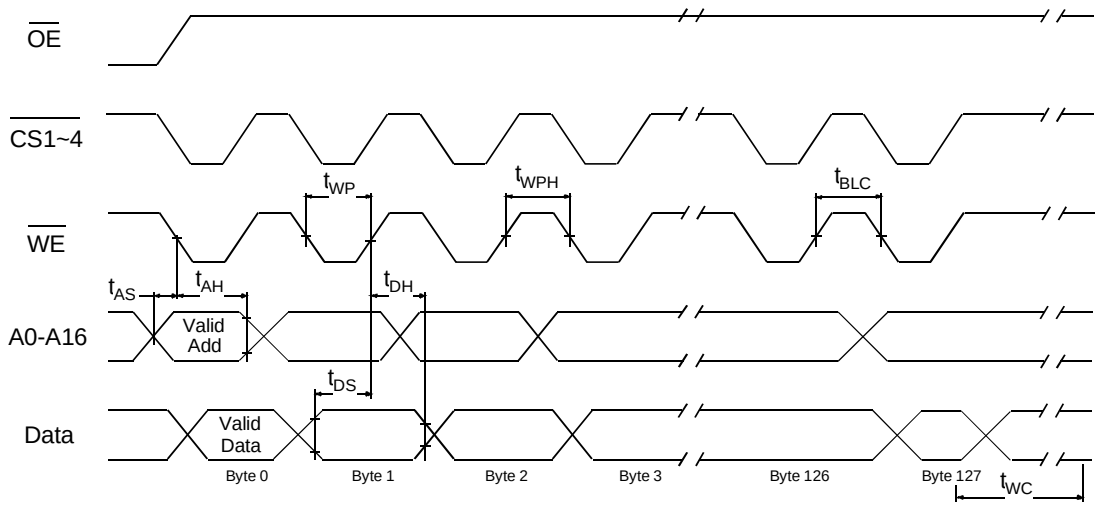
AC Write Waveform - $\overline{WE}$ Controlled



AC Write Waveform - $\overline{CS}$ Controlled

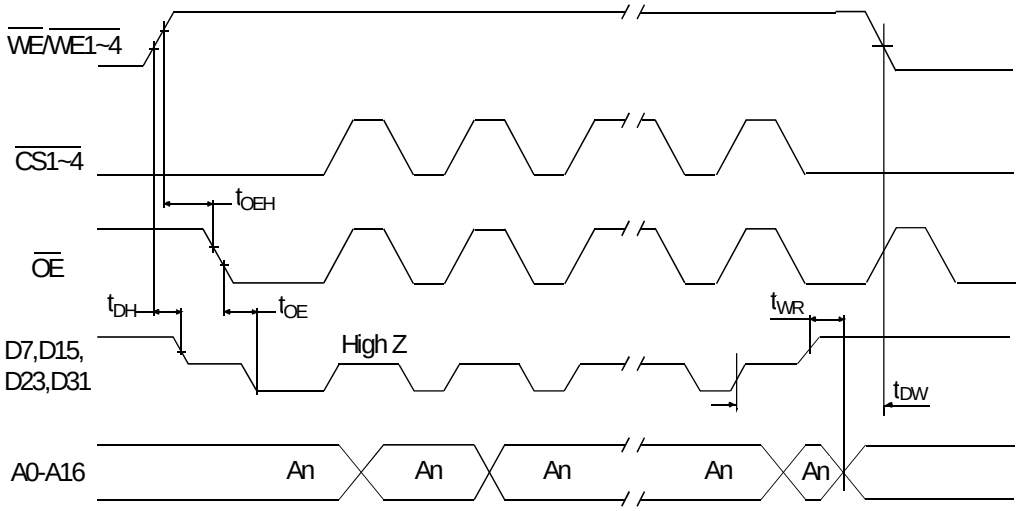


Page Mode Write Waveform

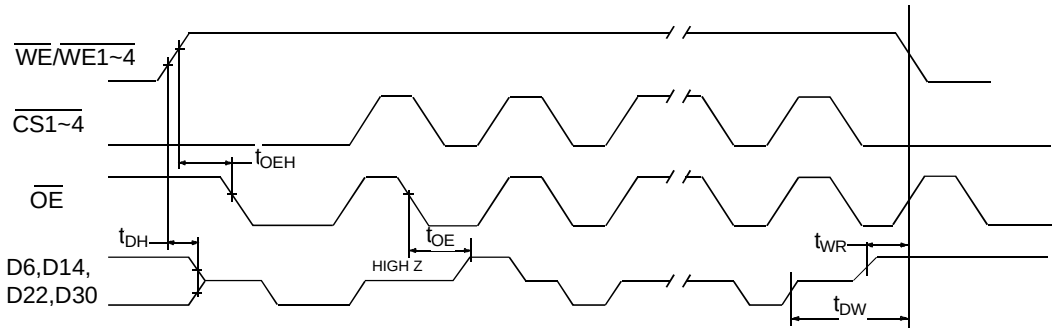


Note: A8 through A16 must specify the page address during each high to low transition of Write Enable (or Chip select). Output Enable must be high only when Write Enable and Chip Select are both low.

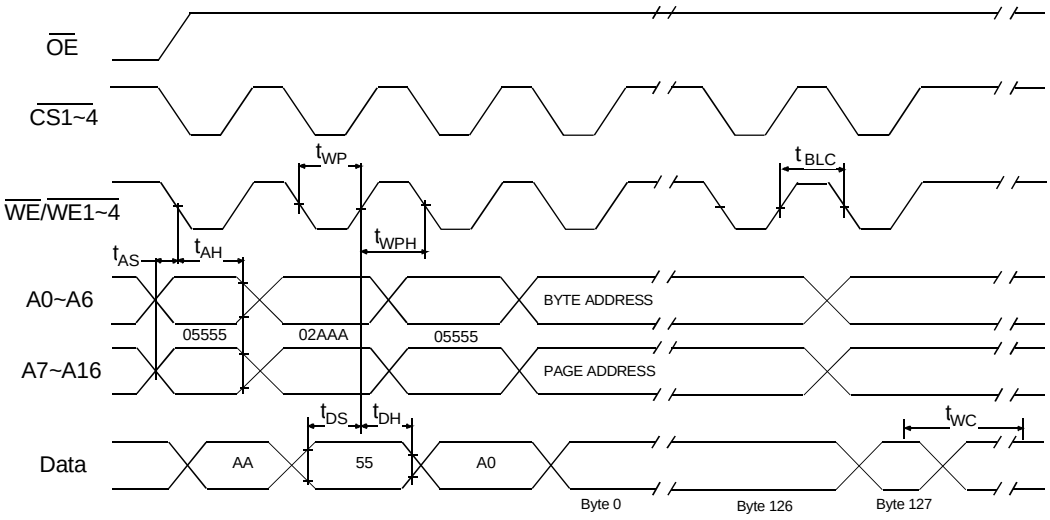
$\overline{\text{DATA}}$ Polling Waveform



Toggle Bit Waveform



Software Protected Write Waveform



Device Operation

The following description deals with the PUMA 68E4001 device, with the references to $\overline{WE}$ meaning $\overline{WE1{\sim}4}$ on the PUMA 68E4001A part.

Read

The PUMA 68E4001 read operations are initiated by both Output Enable and Chip Select LOW. The read operation is terminated by either Chip Select or Output Enable returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impendence state when either Output Enable or Chip Select is HIGH.

Write

Write operations are initiated when both Chip Select and Write Enable are LOW and Output Enable is HIGH. The PUMA 68E4001 supports both a Chip Select and Write Enable controlled write cycle. That is, the address is latched by the falling edge of either Chip Select or Write Enable, whichever occurs last. Similarly, the data is latched internally by the rising edge of either Chip Select or Write Enable, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Mode Write

The page write feature of the PUMA 68E4001 allows the entire memory to be written in 5 seconds. Page Write allows 128 bytes of data to be written prior to the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A8 through A16) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write up to 128 bytes in the same manner as the first byte written. Each successive byte load cycle, started by the Write Enable HIGH to LOW transition, must begin within 150 µs of the falling edge of the preceding Write Enable. If a subsequent Write Enable HIGH to LOW transition is not detected within 150 µs, the internal automatic programming cycle will commence.

DATA Polling

The PUMA 68E4001 features $\overline{DATA}$ Polling to indicate if the write cycle is completed. During the internal programming cycle, any attempt to read the last byte written will produce the compliment of that data on D7. Once the programming is complete, D7 will reflect the true data. Note: If the the PUMA 68E4001 is in a protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

TOGGLE bit

In addition to $\overline{DATA}$ polling, another method is provided to determine the end of a Write Cycle. During a write operation successive attempts to read data will result in D6 toggling between 1 and 0. Once a write is complete, this toggling will stop and valid data will be read.

Hardware Data Protection

The PUMA 68E4001 provides three hardware features to protect non-volalitile data from inadvertent writes.

- Noise Protection - A Write Enable pulse less than 15 ns will not initiate a write cycle.
- Default V_{CC} Sence - All functions are inhibited when V_{CC} < 3.6 V.
- Write Inhibit - Holding either Output Enable LOW, Write Enable HIGH or Chip Select HIGH will prevent an inadvertent write cycle during power on or power off, maintaining data integrity.

Software Data Protection

The PUMA 68E4001 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protect feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the PUMA 68E4001 is also protected against inadvertent and accidental writes in that, the software algorithm must be issued prior to writing additional data to the device.

Operating Modes

The table below shows the logic inputs required to control the operation of the PUMA 68E4001.

MODE	$\overline{CS1\sim4}$	$\overline{OE}$	$\overline{WE}$	OUTPUTS
Read	0	0	1	Data Out
Write	0	I	0	Data in
Standby	1	X	X	Floating
Write Inhibit	X	X	1	
	X	0	X	

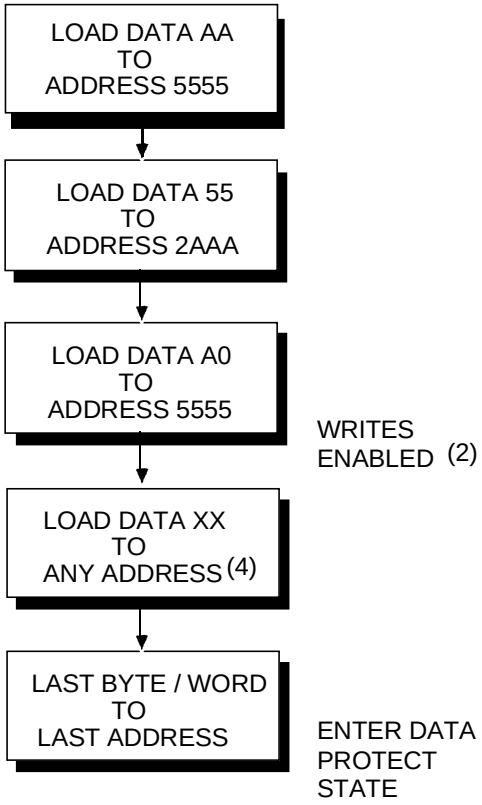
$0 = V_{IL}$: $1 = V_{IH}$: $X = V_{IH}$ or V_{IL}

Software Algorithms

Selecting the software data protection mode requires the host system to precede datawrite operations by a series of three write operations to three specfic addresses. The three byte sequence opens the page write window enabling the host to write from from 1 to 128 bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state

Software Data Protection Algorithm

Regardless of wheather the device has been protected or not, once the software data protected aglorithm is used and the data is written, the PUMA 68E4001 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the PUMA 68E4001 will be write protected during power-down and any subsequent power-up.



Notes:

(1) Data Format I/O7-I/O0 (Hex);
Once initiated, this sequence of write operations should not be interrupted.

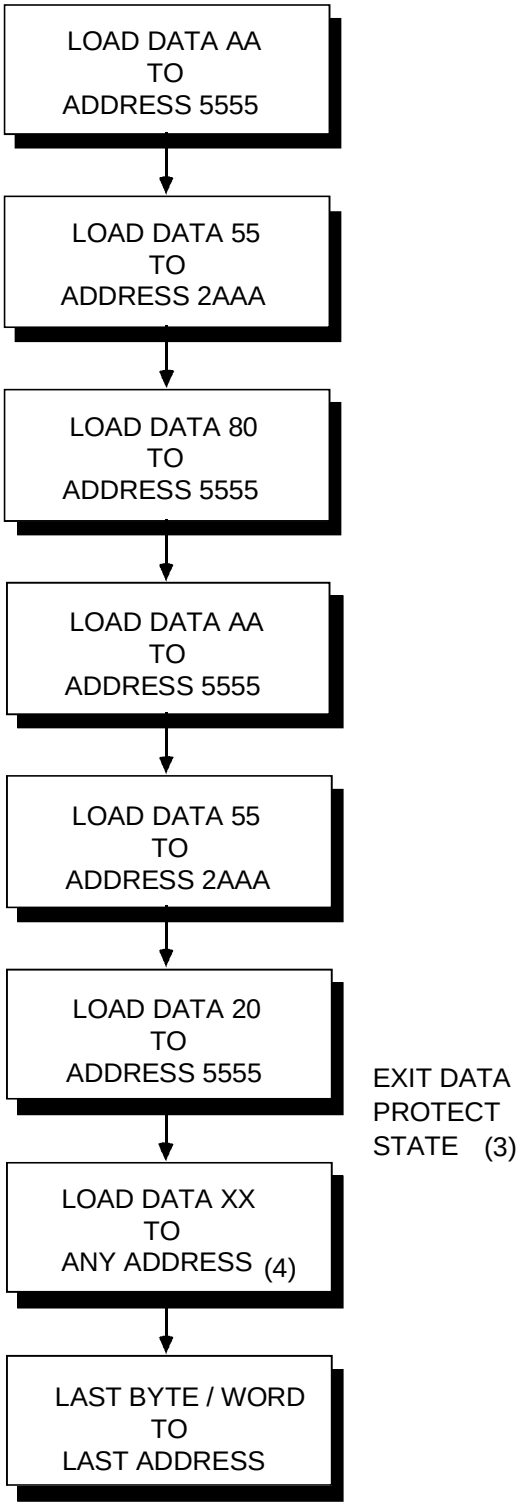
(2) Enable Write Protect state will be initiated at end of write even if no other data is loaded.

(3) Disable Write Protect state will be initiated at end of write period even if no other data is loaded.

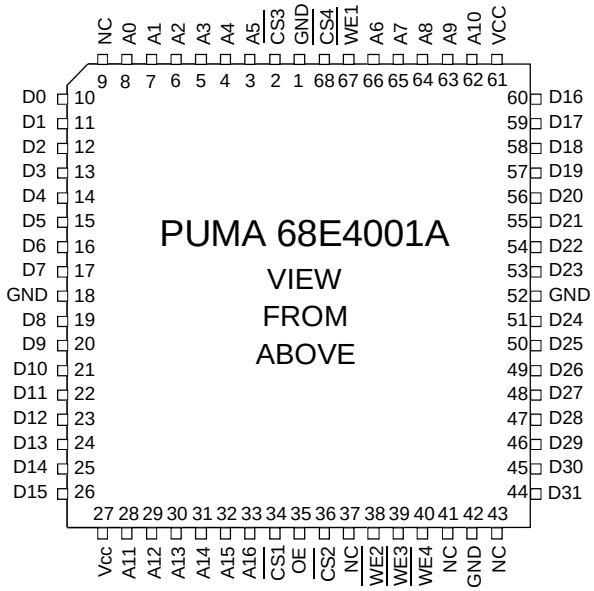
(4) 1 to 128 bytes of data may be loaded.

Software Data Protect Disable

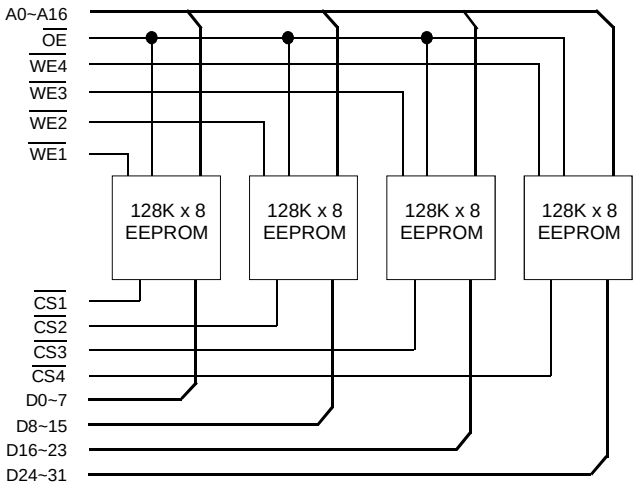
In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer. The following six step algorithm will reset the internal protection circuit. After t_{WC}, the PUMA 68E4001 will be in standard operating mode.



Pin Definifion 'A' version

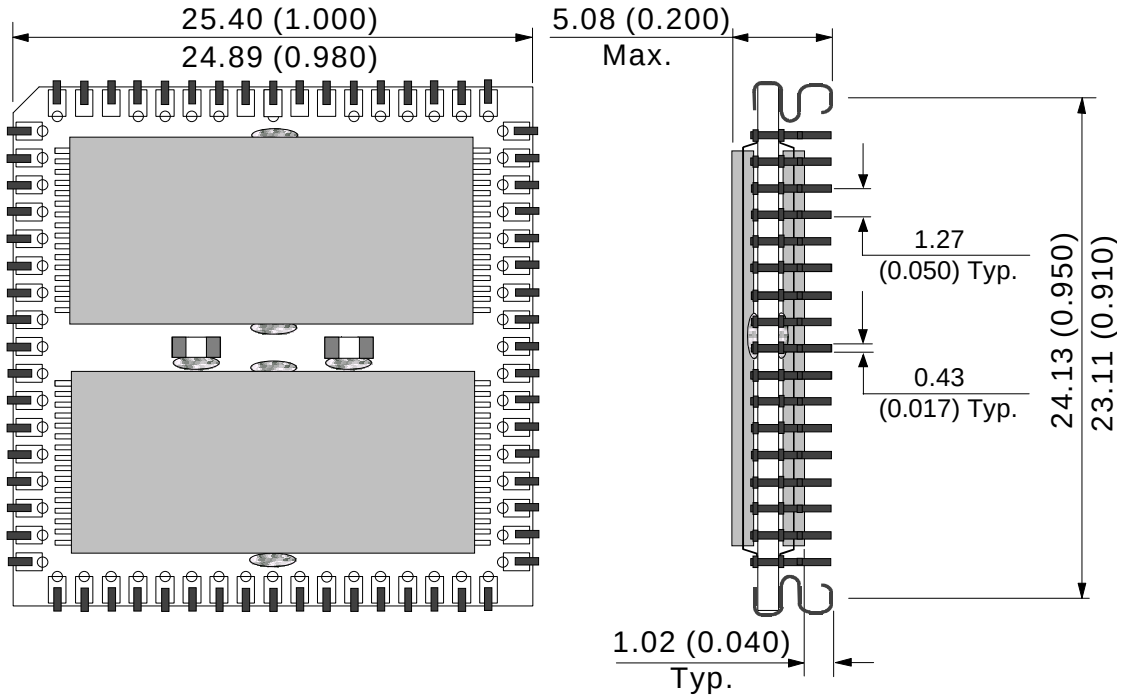


Block Diagram 'A' version



Package Information Dimensions in mm(inches)

Plastic 68 Pin JEDEC Surface mount PLCC



Ordering Information

PUMA 68E4001AM-15E

Endurance	Blank	=	10k Cycles
	E	=	100k Cycles
Speed	12	=	120ns
	15	=	150ns
	20	=	200ns
Temperature range	Blank	=	Commercial Temperature
	I	=	Industrial Temperature
	M	=	Military Temperature
Special Features	Blank	=	$\overline{WE}$
	A	=	$\overline{WE1}$~4
Organisation	4001	=	128K x 32, user configurable as 256K x 16 and 512K x 8
Memory Type	E	=	EEPROM
Package	PUMA 67	=	68 pin "J" Leaded PLCC

Soldering Recommendations

Bake

As specified on product packaging

If not specified HMPLtd recommend a minimum bake of 6 hours duration @ 125C if parts have been exposed to the atmosphere for 24hrs or more

Soldering

Must not exceed

VPR	215 - 219C, 60 secs

IR / Convection	Ramp rate 6C/sec max
	Temp maintained at 125C, 120secs max
	Temp exceeding 183C, 120-180secs
	Time at max temp 10-40secs
	Max temp 220 +5/-0 C
	Ramp down -6C/sec max