DRAM

16 MEG x 1 DRAM

5.0V FAST PAGE MODE

FEATURES

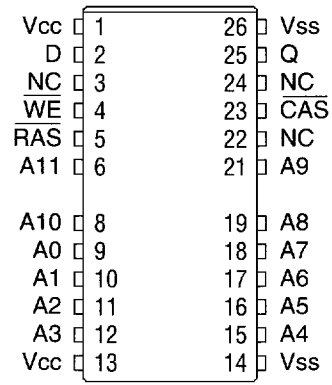
- Industry-standard x1 pinout, timing, functions and packages
- High-performance CMOS silicon-gate process
- Single power supply: +5V ±10%
- Low power, 4mW standby; 200mW active, typical
- All inputs, outputs and clocks are TTL-compatible
- Refresh modes: $\overline{RAS}$ ONLY, $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) and HIDDEN
- 4,096-cycle refresh distributed across 64ms

OPTIONS — MARKING

- Timing
  - 60ns access — -6
  - 70ns access — -7
- Packages
  - Plastic SOJ (300 mil) — DJ
- Part Number Example: MT4C16M1A1DJ-6

PIN ASSIGNMENT (Top View)

24/26-Pin SOJ
(DC-2)



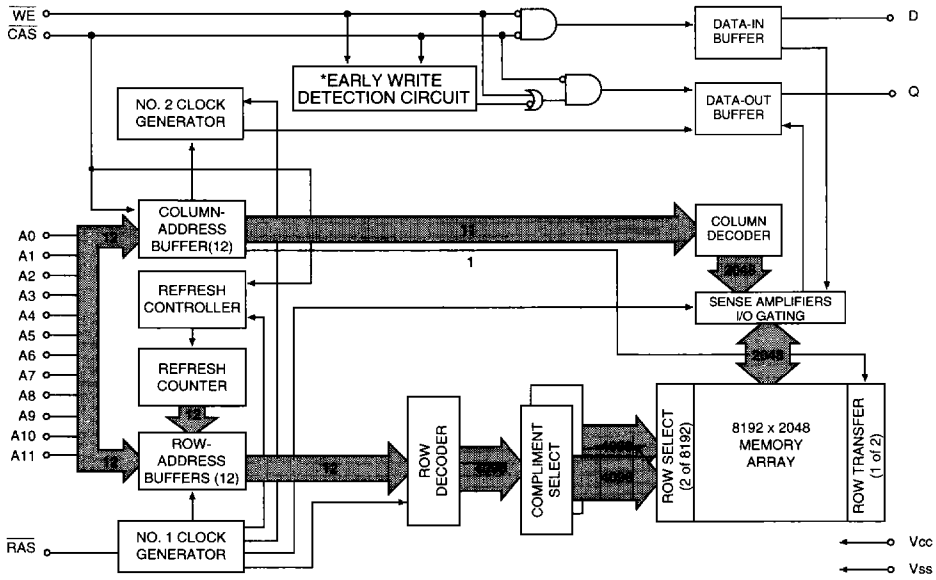
GENERAL DESCRIPTION

The MT4C16M1A1 is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x1 configuration. During READ and WRITE cycles, each bit is uniquely addressed through the 24 address bits, which are entered 12 bits (A0-A11) at a time. $\overline{RAS}$ is used to latch the first 12 bits and $\overline{CAS}$ the latter 12 bits. READ and WRITE cycles are selected with the $\overline{WE}$ input. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin remains open (High-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after data reaches the output pin, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ remains LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ WRITE cycle.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined (A0-A11) page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a column-address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminates the FAST PAGE MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and executing any $\overline{RAS}$ cycle (READ, WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ ONLY, CBR, or HIDDEN) so that all 4,096 combinations of $\overline{RAS}$ addresses (A0-A11) are executed at least every 64ms, regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE



***NOTE:** 1. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, EW detection circuit output is a HIGH (EARLY WRITE).
2. If $\overline{CAS}$ goes LOW prior to $\overline{WE}$ going LOW, EW detection circuit output is a LOW (LATE WRITE).

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDRESSES ^tR	ADDRESSES ^tC	DATA D (Data-In)	DATA Q (Data-Out)
Standby		H	H→X	X	X	X	"don't care"	High-Z
READ		L	L	H	ROW	COL	"don't care"	Data-Out
EARLY WRITE		L	L	L	ROW	COL	Data-In	High-Z
READ WRITE		L	L	H→L	ROW	COL	Data-In	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	H	ROW	COL	"don't care"	Data-Out
READ	2nd Cycle	L	H→L	H	n/a	COL	"don't care"	Data-Out
FAST-PAGE-MODE	1st Cycle	L	H→L	L	ROW	COL	Data-In	High-Z
EARLY-WRITE	2nd Cycle	L	H→L	L	n/a	COL	Data-In	High-Z
FAST-PAGE-MODE	1st Cycle	L	H→L	H→L	ROW	COL	Data-In	Data-Out
READ-WRITE	2nd Cycle	L	H→L	H→L	n/a	COL	Data-In	Data-Out
$\overline{RAS}$ ONLY REFRESH		L	H	X	ROW	n/a	"don't care"	High-Z
HIDDEN	READ	L→H→L	L	H	ROW	COL	"don't care"	Data-Out
REFRESH	WRITE	L→H→L	L	L	ROW	COL	Data-In	High-Z
CBR REFRESH		H→L	L	H	X	X	"don't care"	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to V_{SS} (5V) ..... -1V to +7V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 6.5V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5V ±10%)

PARAMETER/CONDITION	SYMBOL	MAX		UNITS	NOTES
		-6	-7		
STANDBY CURRENT: (TTL) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC1}	2	2	mA	
STANDBY CURRENT: (CMOS) ($\overline{RAS}$ = $\overline{CAS}$ = Other Inputs = V_{CC} -0.2V)	I_{CC2}	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC3}	90	80	mA	3, 4, 26
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: ^tPC = ^tPC [MIN])	I_{CC4}	70	60	mA	3, 4, 26
REFRESH CURRENT: $\overline{RAS}$ ONLY Average power supply current ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC5}	90	80	mA	3, 26
REFRESH CURRENT: CBR Average power supply current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: ^tRC = ^tRC [MIN])	I_{CC6}	90	80	mA	3, 5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A11, D	C_{I1}	5	pF	2
Input Capacitance: $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	7	pF	2
Output Capacitance: Q	C_O	7	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Random READ or WRITE cycle time	t_{RC}	110		130		ns	
READ WRITE cycle time	t_{RWC}	130		155		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	60		70		ns	
Access time from $\overline{RAS}$	t_{RAC}		60		70	ns	14
Access time from $\overline{CAS}$	t_{CAC}		15		20	ns	15
Access time from column-address	t_{AA}		30		35	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}		35		40	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	100,000	70	100,000	ns	
$\overline{RAS}$ pulse width (FAST PAGE MODE)	t_{RASP}	60	100,000	70	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	15		20		ns	
$\overline{RAS}$ precharge time	t_{RP}	40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	15	100,000	20	100,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	60		70		ns	
$\overline{CAS}$ precharge time	t_{CPN}	10		10		ns	16
$\overline{CAS}$ precharge time (FAST PAGE MODE)	t_{CP}	10		10		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	50	ns	17
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5		5		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Row-address hold time	t_{RAH}	10		10		ns	
$\overline{RAS}$ to column-address delay time	t_{RAD}	15	30	15	35	ns	18
Column-address setup time	t_{ASC}	0		0		ns	
Column-address hold time	t_{CAH}	10		15		ns	
Column-address hold time (referenced to $\overline{RAS}$)	t_{AR}	50		55		ns	
Column-address to $\overline{RAS}$ lead time	t_{RAL}	30		35		ns	
Read command setup time	t_{RCS}	0		0		ns	
Read command hold time (referenced to $\overline{CAS}$)	t_{RCH}	0		0		ns	19
Read command hold time (referenced to $\overline{RAS}$)	t_{RRH}	0		0		ns	19
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	3		3		ns	25
Output buffer turn-off delay	t_{OFF}	3	15	3	20	ns	20, 25
$\overline{WE}$ command setup time	t_{WCS}	0		0		ns	21

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

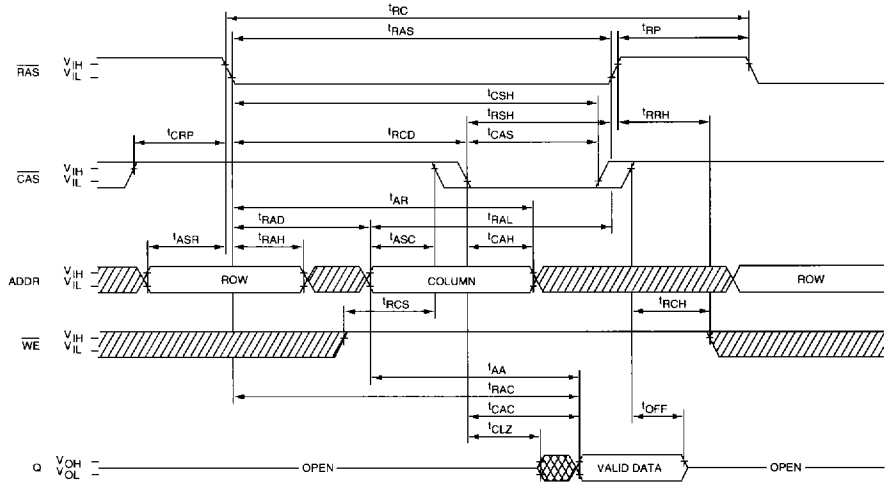
(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (V_{CC} = +5V ±10%)

AC CHARACTERISTICS		-6		-7			
PARAMETER	**SYM**	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**	**NOTES**
Write command hold time	t_{WCH}	10		15		ns	
Write command hold time (referenced to $\overline{RAS}$)	t_{WCR}	45		55		ns	
Write command pulse width	t_{WP}	10		15		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	15		20		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		20		ns	
Data-in setup time	t_{DS}	0		0		ns	22
Data-in hold time	t_{DH}	10		15		ns	22
Data-in hold time (referenced to $\overline{RAS}$)	t_{DHR}	45		55		ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	60		70		ns	21
Column-address to $\overline{WE}$ delay time	t_{AWD}	30		35		ns	21
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	15		20		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	ns	9, 10
Refresh period (4,096 cycles)	t_{REF}		64		64	ms	
$\overline{RAS}$ to $\overline{CAS}$ precharge time	t_{RPC}	0		0		ns	
$\overline{CAS}$ setup time (CBR REFRESH)	t_{CSR}	5		5		ns	5
$\overline{CAS}$ hold time (CBR REFRESH)	t_{CHR}	15		15		ns	5
$\overline{WE}$ hold time (CBR REFRESH)	t_{WRH}	10		10		ns	24
$\overline{WE}$ setup time (CBR REFRESH)	t_{WRP}	10		10		ns	24
$\overline{WE}$ hold time (WCBR test cycle)	t_{WTH}	10		10		ns	24
$\overline{WE}$ setup time (WCBR test cycle)	t_{WTS}	10		10		ns	24

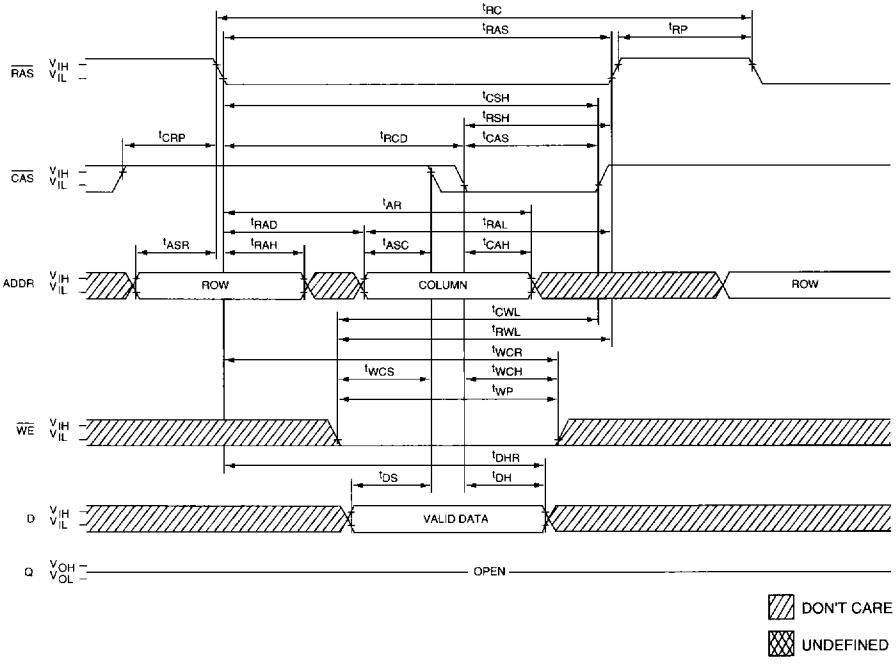
NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ±10%; f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the output open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$) is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ ONLY or CBR with $\overline{WE}$ HIGH) before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
8. AC characteristics assume ^tT = 5ns.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is High-Z.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with a load equivalent to two TTL gates and 100pF.
14. Assumes that $^tRCD < {}^tRCD$ (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
15. Assumes that $^tRCD \ge {}^tRCD$ (MAX).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed HIGH for ^tCPN.
17. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC.
18. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA.
19. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. ^tWCS, ^tRWD, ^tAWD and ^tCWD are restrictive operating parameters in LATE WRITE, READ WRITE and READ-MODIFY-WRITE cycles only. If $^tWCS \ge {}^tWCS$ (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If $^tRWD \ge {}^tRWD$ (MIN), $^tAWD \ge {}^tAWD$ (MIN) and $^tCWD \ge {}^tCWD$ (MIN), the cycle is a READ WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the cycle is a LATE WRITE and the state of data-out is indeterminate (at access time and until $\overline{CAS}$ goes back to V_{IH}).
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ WRITE cycles.
23. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{WE}$ = LOW.
24. ^tWTS and ^tWTH are set up and hold specifications for the $\overline{WE}$ pin being held LOW to enable the JEDEC test mode (with CBR timing constraints). These two parameters are the inverts of ^tWRP and ^tWRH in the CBR REFRESH cycle.
25. The 3ns minimum is a parameter guaranteed by design.
26. Column-address changed once each cycle.

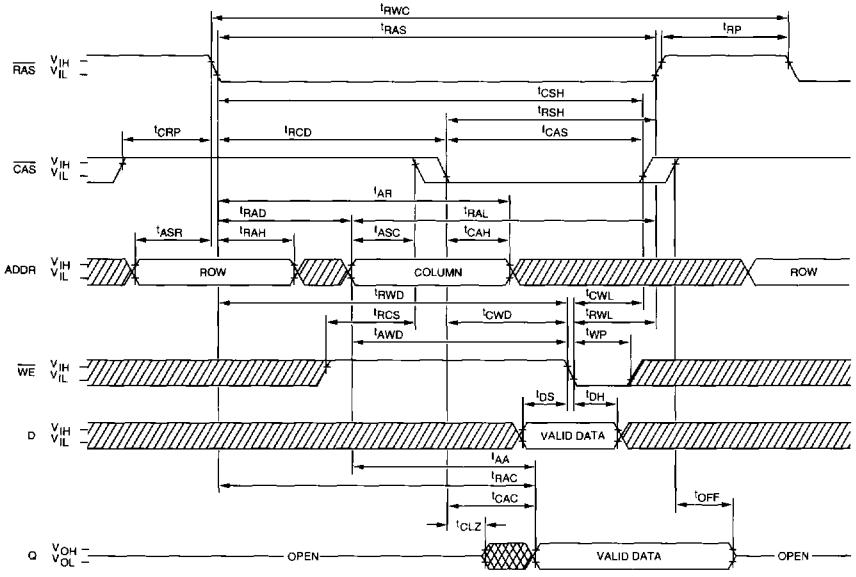
READ CYCLE



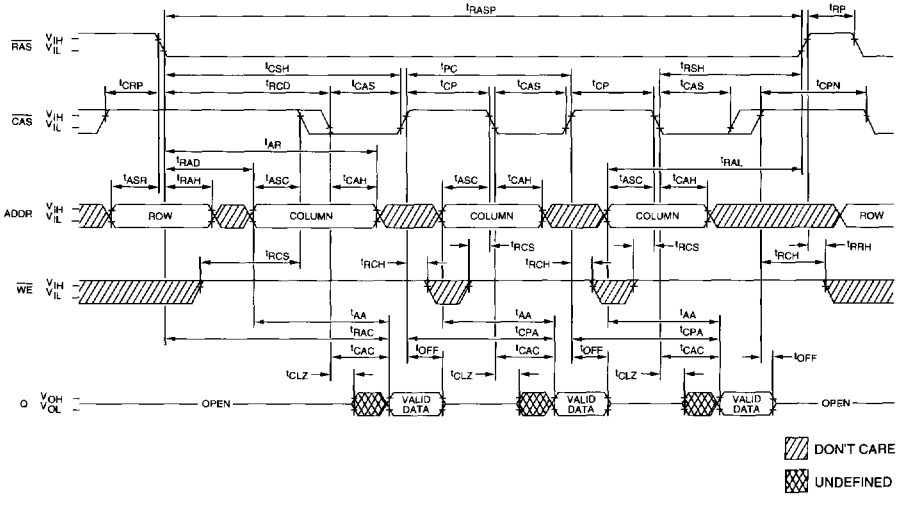
EARLY WRITE CYCLE



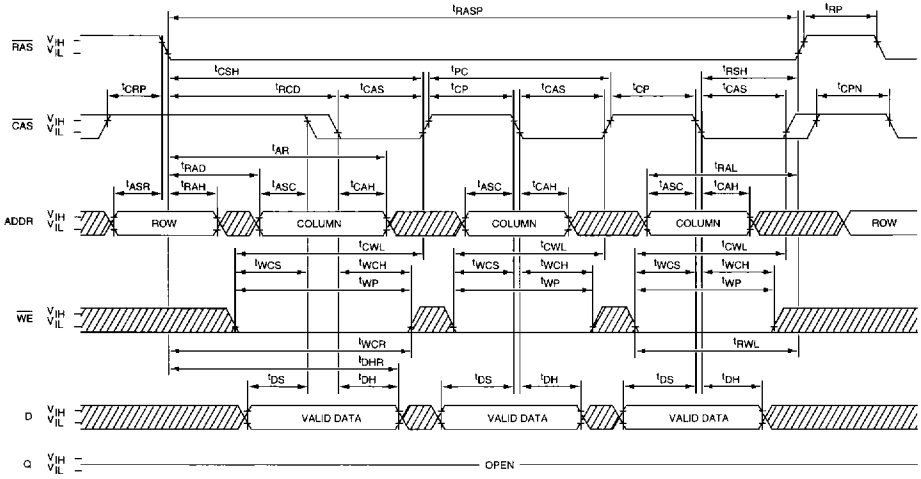
READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



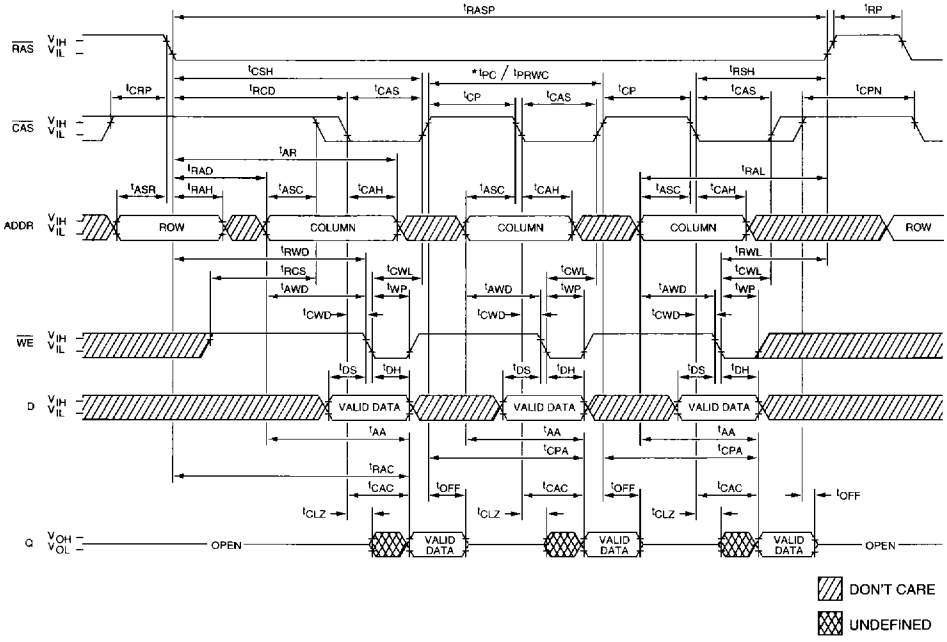
FAST-PAGE-MODE READ CYCLE



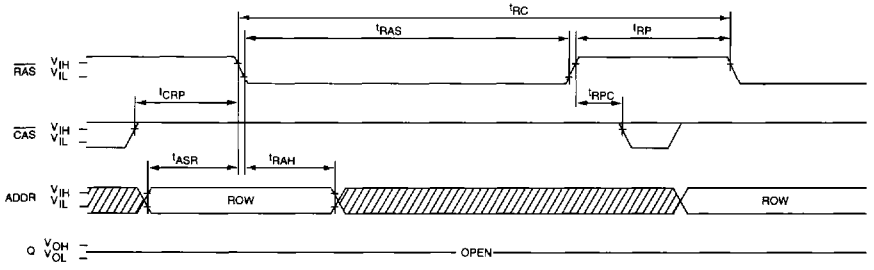
FAST-PAGE-MODE EARLY-WRITE CYCLE



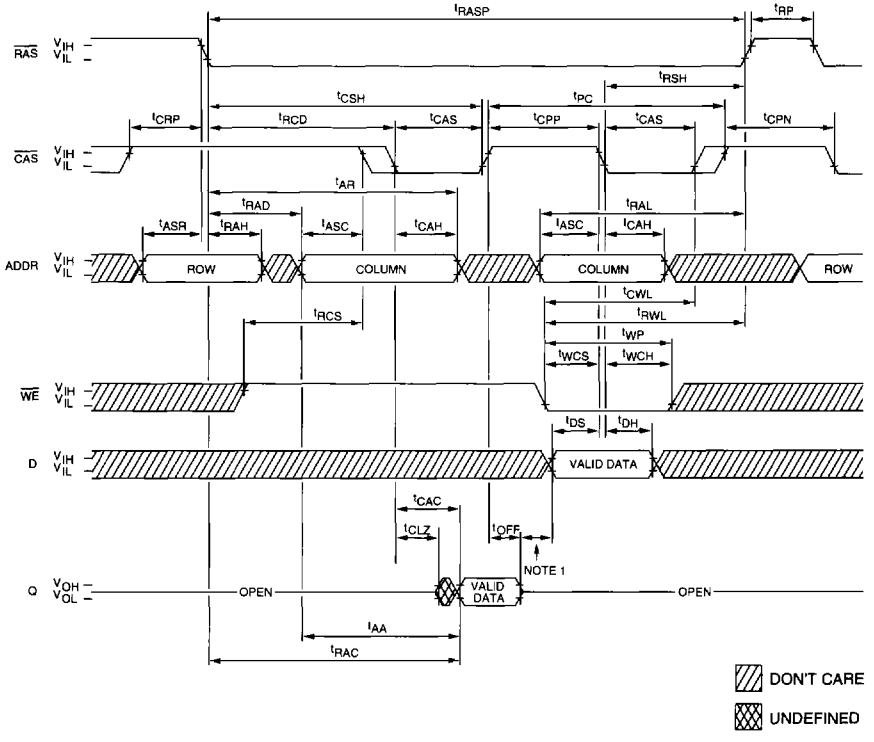
FAST-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE CYCLES)



$\overline{RAS}$ ONLY REFRESH CYCLE
(ADDR = A0-A11; $\overline{WE}$ = DON'T CARE)

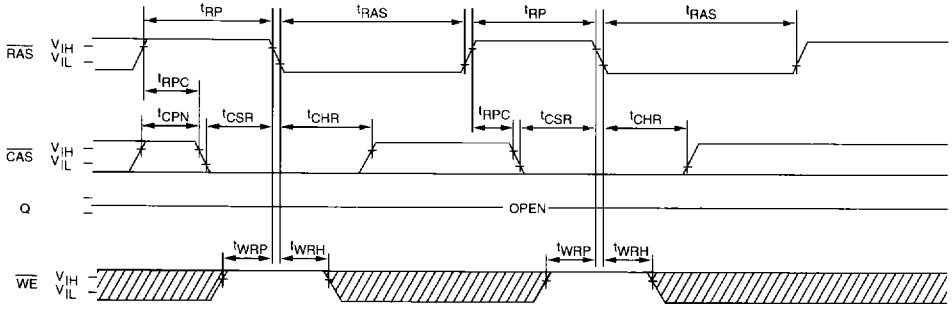


FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



NOTE: 1. Do not drive data prior to tristate: tCPP(MIN) or tCP(whichever is greater) + tDS(MIN) + any guardband between data-out and driving the bus with the new data-in.
2. Assumes D and Q are tied together.

CBR REFRESH CYCLE
(A0-A11 = DON'T CARE)



HIDDEN REFRESH CYCLE [23]
($\overline{WE}$ = HIGH)