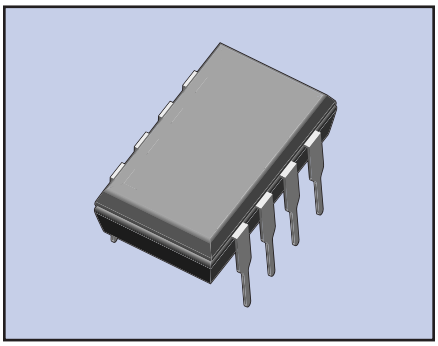
ECS-300CX SERIES DUAL OUTPUT CMOS CLOCK OSCILLATOR



The ECS-300CX utilizes a built in divider circuit to provide a second divided output. The CMOS based oscillator features low current consumption in a standard 8-pin DIP package.

FEATURES

- Low current consumption
- Built in divider circuit
- 8-pin DIP package
- PbFree/RoHS Compliant

PART NUMBERING GUIDE

SERIES		FREQUENCY (12.000 MHz)
ECS-300CX	–	120

Sample Part Number: ECS-300CX-120

STANDARD FREQUENCIES

12.000, 12.288, 12.800, 14.31818, 14.7456, 15.9744, 16.000, 16.384, 17.734476, 18.432, 19.6608, 20.000, 24.000, 24.576, 30.000 AND 32.000 MHz

OPERATING CONDITIONS/ELECTRICAL CHARACTERISTICS

PARAMETERS	CONDITIONS	MINIMUM	TYPICAL	MAXIMUM	UNITS
FREQUENCY RANGE	Primary Output	12.000		32.000	MHz
	Divided Output*	48.875 KHz		16.000 MHz	PPM
FREQUENCY STABILITY	All Conditions			±100*	PPM
OPERATING TEMPERATURE		-10˚		+70˚	˚C
STORAGE TEMPERATURE		-55˚		+125˚	˚C
INPUT VOLTAGE (V_{CC})		+3.0V	+5.0V	+5.5V	V DC
INPUT CURRENT				20	mA
OUTPUT SYMMETRY	Primary Output	40/60		60/40	%
	Divided Output	48/52		52/48	%
RISE AND FALL TIMES				15	ns
OUTPUT VOLTAGE	VOL			V_{CC} x 0.1	V DC
	VOH	V_{CC} x 0.9			V DC
OUTPUT LOAD	12.000 ~ 24.576 MHz			50	pF
	30.000 ~ 32.000 MHz			15	pF
START UP TIME	12.000 ~ 24.576 MHz			1.5	mS
	30.000 ~ 32.000 MHz			2.0	mS

**See Possible Frequency Divisions Table for example of divided frequencies.*

POSSIBLE FREQUENCY DIVISIONS BY PART NUMBER

ECS PART NUMBER	fo CLOCK PIN 1	fo/2^n (Divided Output) PIN 2							
		1/2^1	1/2^2	1/2^3	1/2^4	1/2^5	1/2^6	1/2^7	1/2^8
ECS-300CX-120	12.000 MHz	6.000 MHz	3.000 MHz	1.500 MHz	750 KHz	375 KHz	187.5 KHz	93.75 KHz	46.875 KHz
ECS-300CX-163	16.384 MHz	8.192 MHz	4.096 MHz	2.048 MHz	1.024 MHz	512 KHz	256 KHz	128 KHz	64 KHz
ECS-300CX-320	32.000 MHz	16.000 MHz	8.000 MHz	4.000 MHz	2.000 MHz	1.000 MHz	500 KHz	250 KHz	125 KHz

DIMENSIONS (mm)

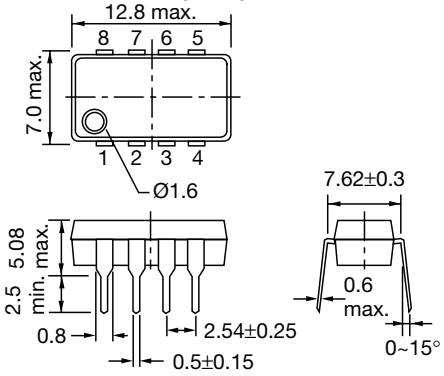


Figure 1) ECS-300CX Top and Side views

PIN CONNECTIONS	
#1	OUTPUT
#2	DIVIDED OUTPUT
#3	STANDBY
#4	GND
#5	A (Divider selection)
#6	B (Divider selection)
#7	C (Divider selection)
#8	Vcc

Figure 2) Pin Connections

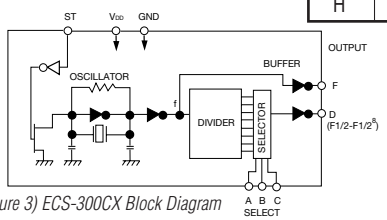


Figure 3) ECS-300CX Block Diagram

Input				Output	
Divider Selection			ST	PIN 1(Primary Output)	PIN 2(Divided Output)
C	B	A			
X	X	X	L	L	L
L	L	L	H	fo clock	fo 1/2^1 clock
L	L	H	H	fo clock	fo 1/2^2 clock
L	H	L	H	fo clock	fo 1/2^3 clock
L	H	H	H	fo clock	fo 1/2^4 clock
H	L	L	H	fo clock	fo 1/2^5 clock
H	L	H	H	fo clock	fo 1/2^6 clock
H	H	L	H	fo clock	fo 1/2^7 clock
H	H	H	H	fo clock	fo 1/2^8 clock

Figure 4) Divided Output Selection Table

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