CA3094

HARRIS SEMICONDUCTOR

Programmable Power Switch/Amplifier for Control and General Purpose Applications

March 1993

Features

- CA3094T, S, E, M for Operation Up to 24V
- CA3094AT, S, E, M for Operation Up to 36V
- CA3094BT, S, M for Operation Up to 44V
- Designed for Single or Dual Power Supply
- Programmable: Strobing, Gating, Squelching, AGC Capabilities
- Can Deliver 3W (Average) or 10W (Peak) to External Load (In Switching Mode)
- High Power, Single Ended Class A Amplifier will Deliver Power Output of 0.6W (1.6W Device Dissipation)
- Total Harmonic Distortion (THD) at 0.6W in Class A Operation 1.4% (Typ.)

Applications

- Error Signal Detector: Temperature Control with Thermistor Sensor; Speed Control for Shunt Wound DC Motor
- Over Current, Over Voltage, Over Temperature Protectors
- Dual Tracking Power Supply with CA3085
- Wide Frequency Range Oscillator
- Analog Timer
- Level Detector
- Alarm Systems
- Voltage Follower
- Ramp Voltage Generator
- High Power Comparator
- Ground Fault Interrupter (GFI) Circuits

Description

The CA3094 is a differential input power control switch/amplifier with auxiliary circuit features for ease of programmability. For example, an error or unbalance signal can be amplified by the CA3094 to provide an on-off signal or proportional control output signal up to 100mA. This signal is sufficient to directly drive high current thyristors, relays, dc loads, or power transistors. The CA3094 has the generic characteristics of the CA3080 operational amplifier directly coupled to an integral Darlington power transistor capable of sinking or driving currents up to 100mA.

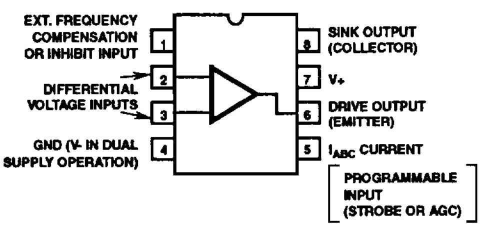
The gain of the differential input stage is proportional to the amplifier bias current (I_{ABC}), permitting programmable variation of the integrated circuit sensitivity with either digital and/or analog programming signals. For example, at an I_{ABC} of 100mA, a 1mV change at the input will change the output from 0 to 100mA (typical).

The CA3094 is intended for operation up to 24V and is especially useful for timing circuits, in automotive equipment, and in other applications where operation up to 24V is a primary design requirement (see Figures 28, 29 and 30 in Applications Section). The CA3094 and CA3094B are like the CA3094 but are intended for operation up to 36V and 44V, respectively (single or dual supply).

These types are available in 8 lead TO-5 style packages with standard leads ("T" suffix) and with dual-in-line formed leads "DIL-CAN" ("S" suffix). Type CA3094 is also available in an 8 lead dual-in-line plastic package "MINI-DIP" ("E" suffix), Small Outline Pakcage ("M" suffix), and in chip form ("H" suffix).

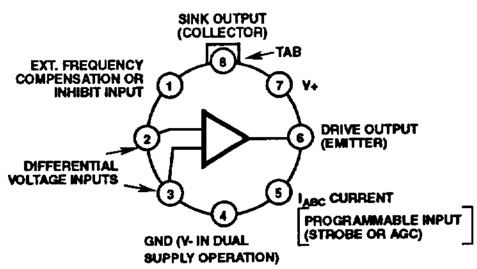
Pinouts

CA3094
(PDIP, SOIC)
TOP VIEW



NOTE: Pin 4 is connected to case

CA3094
(TO-5 CAN)
TOP VIEW



Absolute Maximum Ratings

Dual Supply Voltage
- CA3094 .... ±12V
- CA3094A .... ±18V
- CA3094B .... ±22V

Single Supply Voltage
- CA3094 .... 24V
- CA3094A 36V
- CA3094B 44V

Differential Input Voltage (Term. 2 and 3) Note 1 .... 5V
DC Input Voltage .... V+ to V-
Input Current (Term. 2 and 3) .... ±1mA
Amplifier Bias Current (Term. 5) 2mA
Output Current 300mA
Junction Temperature .... +175°C
Junction Temperature (Plastic Package) .... +150°C
Lead Temperature (Soldering 10 Sec.) .... +300°C

Operating Conditions

Operating Temperature Range .... -55°C to +125°C
Storage Temperature Range .... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100μA Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT PARAMETERS						
Input Offset Voltage	V_{IO}	T_A = +25°C	-	0.4	5.0	mV
		T_A = 0°C to +70°C	-	-	7.0	mV
Input Offset Voltage Change	$\|\Delta V_{IO}\|$	Change in V_{IO} between I_{ABC} = 100μA and I_{ABC} = 5μA	-	1	8.0	mV
Input Offset Current	I_{IO}	T_A = +25°C	-	0.02	0.2	μA
		T_A = 0°C to +70°C	-	-	0.3	μA
Input Bias Current	I_I	T_A = +25°C	-	0.2	0.50	μA
		T_A = 0°C to +70°C	-	-	0.70	μA
Device Dissipation	P_D	I_{OUT} = 0mA	8	10	12	mW
Common Mode Rejection Ratio	CMRR		70	110	-	dB
Common Mode Input Voltage Range	V_{ICR}	V+ = 30V (High)	27	28.8	-	V
		V- = 0V (Low)	1.0	0.5	-	V
		V+ = 15V	12	13.8	-	V
		V- = -15V	-14	-14.5	-	V
Unity Gain Bandwidth	f_T	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500μA	-	30	-	MHz
Open Loop Bandwidth at -3dB Point	BW_{OL}	I_C = 7.5mA, V_{CE} = 15V, I_{ABC} = 500μA	-	4	-	kHz
Total Harmonic Distortion (Class A Operation)	THD	P_D = 220mW	-	0.4	-	%
		P_D = 600mW	-	1.4	-	%
Amplifier Bias Voltage (Terminal 5 to Terminal 4)	V_{ABC}		-	0.68	-	V
Input Offset Voltage Temperature Coefficient	$\Delta V_{IO}/\Delta T$		-	4	-	μV/°C
Power Supply Rejection	$\Delta V_{IO}/\Delta V$		-	15	150	μV/V

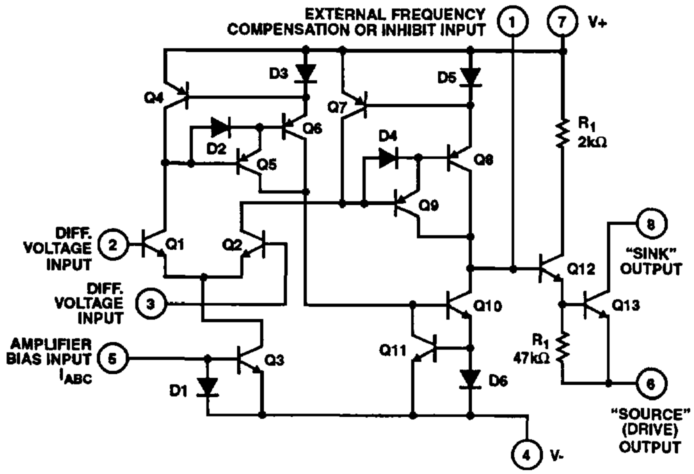
Electrical Specifications T_A = +25°C for Equipment Design. Single Supply V+ = 30V, Dual Supply V+ = 15V, V- = -15V, I_{ABC} = 100µA Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
INPUT PARAMETERS (Continued)						
1/F Noise Voltage	E_N	f = 10Hz, I_{ABC} = 50µA	-	18	-	$nV/\sqrt{Hz}$
1/F Noise Current	I_N	f = 10Hz, I_{ABC} = 50µA	-	1.8	-	$pA/\sqrt{Hz}$
Differential Input Resistance	R_I	I_{ABC} = 20µA	0.50	1.0	-	MΩ
Differential Input Capacitance	C_I	f = 1MHz, V+ = 30V	-	2.6	-	pF
OUTPUT PARAMETERS (Differential Input Voltage = 1V)						
Peak Output Voltage (Terminal 6)		V+ = 30V, R_L = 2kΩ to GND				
With Q13 "ON"	V+OM		26	27	-	V
With Q13 "OFF"	V-OM		-	0.01	0.05	V
Peak Output Voltage (Terminal 6)		V+ = 15V, V- = -15V, R_L = 2kΩ to -15V				
Positive	V+OM		11	12	-	V
Negative	V-OM		-	-14.99	-14.95	V
Peak Output Voltage (Terminal 8)		V+ = 30V, R_L = 2kΩ to 30V				
With Q13 "OFF"	V+OM		29.95	29.99	-	V
With Q13 "ON"	V-OM		-	0.040	-	V
Peak Output Voltage (Terminal 8)		V+ = 15V, V- = -15V, R_L = 2kΩ to 15V				
Positive	V+OM		14.95	14.99	-	V
Negative	V-OM		-	-14.96	-	V
Collector-to-Emitter Saturation Voltage (Terminal 8)	$V_{CE(SAT)}$	V+ = 30V, I_C = 50mA, Terminal 6 Grounded	-	0.17	0.80	V
Output Leakage Current (Terminal 6 to Terminal 4)		V+ = 30V	-	2	10	µA
Composite Small Signal Current Transfer Ratio (Beta) (Q12 and Q13)	h_{FE}	V+ = 30V, V_{CE} = 5V, I_C = 50mA	16,000	100,000	-	
Output Capacitance		f = 1MHz, All remaining Terminals Tied to Terminal 4				
Terminal 6	C_O		-	5.5	-	pF
Terminal 8	C_O		-	17	-	pF
TRANSFER PARAMETERS						
Voltage Gain	A	V+ = 30V, I_{ABC} = 100µA, ΔV_{OUT} = 20V, R_L = 2kΩ	20,000	100,000	-	V/V
			86	100	-	dB
Forward Transconductance to Terminal 1	g_M		1650	2200	2750	µmhos
Slew Rate (Open Loop)	SR	I_{ABC} = 500µA, R_L = 2kΩ				
Positive Slope			-	500	-	V/µs
Negative Slope			-	50	-	V/µs
Unity Gain (Non-Inverting Compensated)		I_{ABC} = 500µA, R_L = 2kΩ	-	0.70	-	V/µs

NOTE:

1. Exceeding this voltage rating will not damage the device unless the peak input signal current (1mA) is also exceeded.

Schematic Diagram



OUTPUT MODE	OUTPUT TERM	INPUTS	
		INV	NON-INV
"Source"	6	2	3
"Sink"	8	3	2

Typical Performance Curves

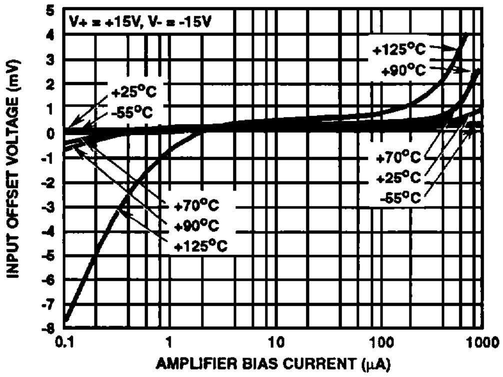


FIGURE 1. INPUT OFFSET VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

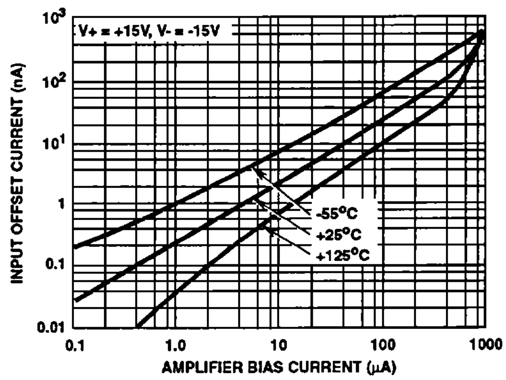


FIGURE 2. INPUT OFFSET CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

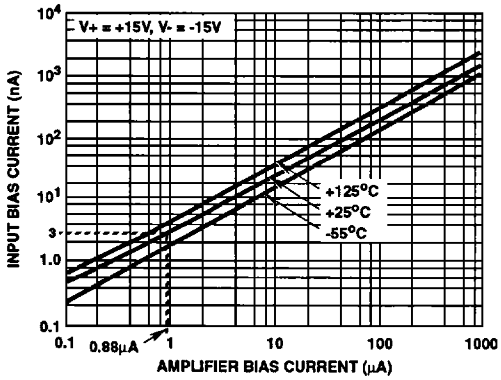


FIGURE 3. INPUT BIAS CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

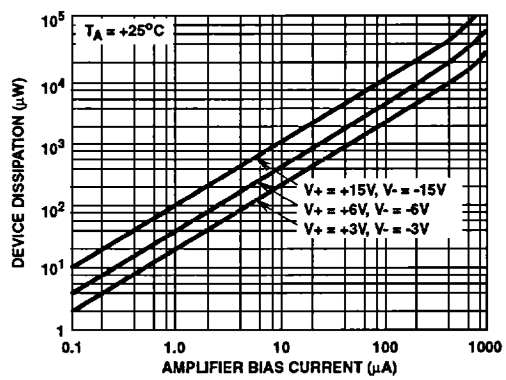


FIGURE 4. DEVICE DISSIPATION vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

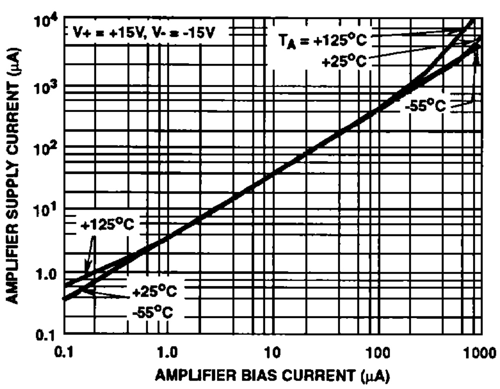


FIGURE 5. AMPLIFIER SUPPLY CURRENT vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

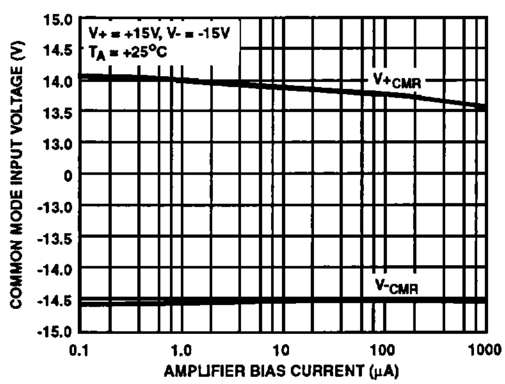


FIGURE 6. COMMON MODE INPUT VOLTAGE vs AMPLIFIER BIAS CURRENT (I_{ABC}, TERMINAL 5)

Typical Performance Curves (Continued)

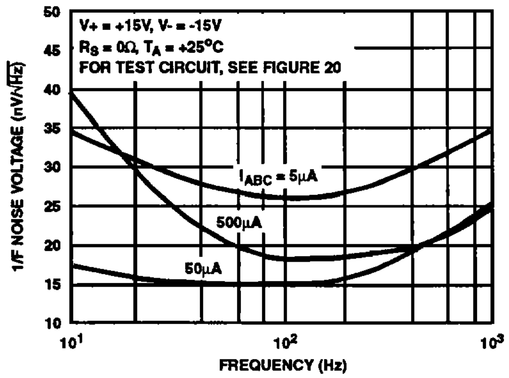


FIGURE 7. 1/F NOISE VOLTAGE vs FREQUENCY

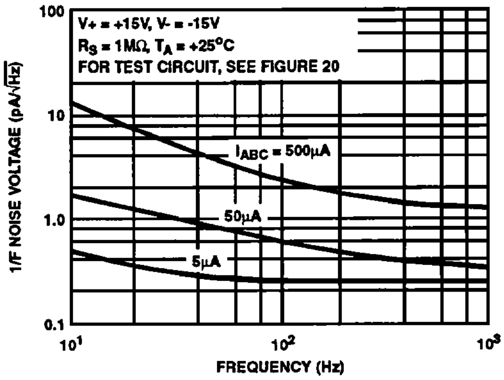


FIGURE 8. 1/F NOISE CURRENT vs FREQUENCY

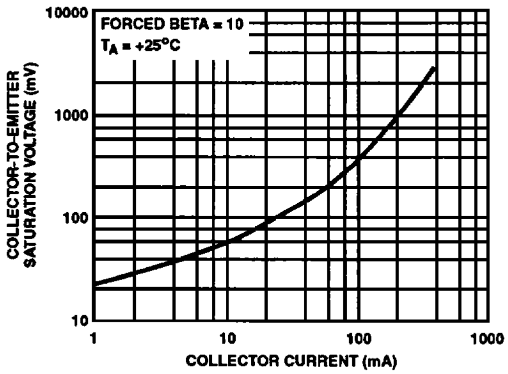


FIGURE 9. COLLECTOR EMITTER SATURATION VOLTAGE vs COLLECTOR CURRENT OF OUTPUT TRANSISTOR Q13

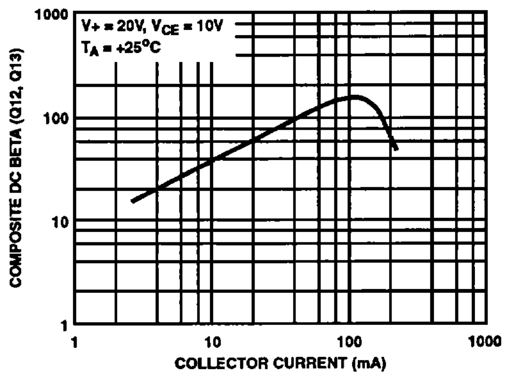


FIGURE 10. COMPOSITE DC BETA vs COLLECTOR CURRENT OF DARLINGTON CONNECTED OUTPUT TRANSISTORS (Q12, Q13)

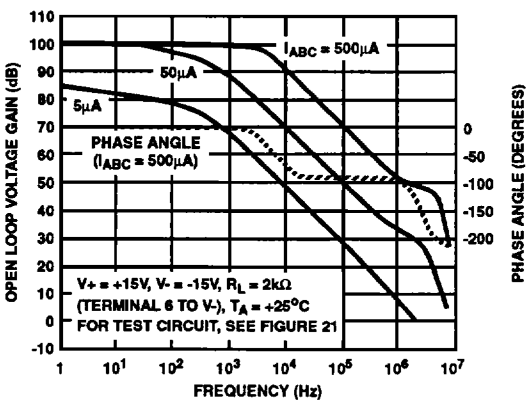


FIGURE 11. OPEN LOOP VOLTAGE GAIN vs FREQUENCY

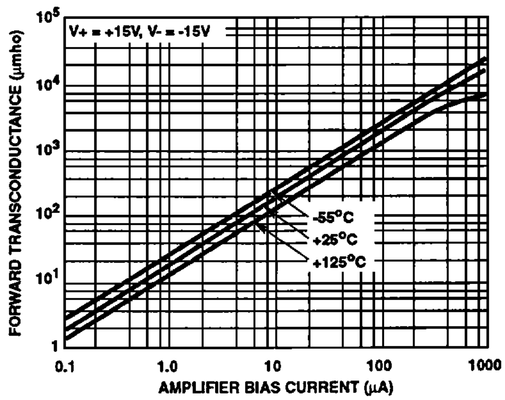


FIGURE 12. FORWARD TRANSCONDUCTANCE vs AMPLIFIER BIAS CURRENT

Typical Performance Curves (Continued)

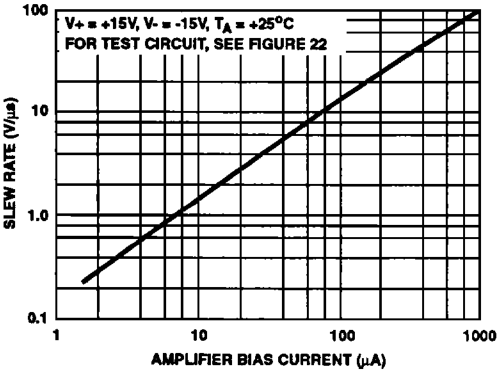


FIGURE 13. SLEW RATE vs AMPLIFIER BIAS CURRENT

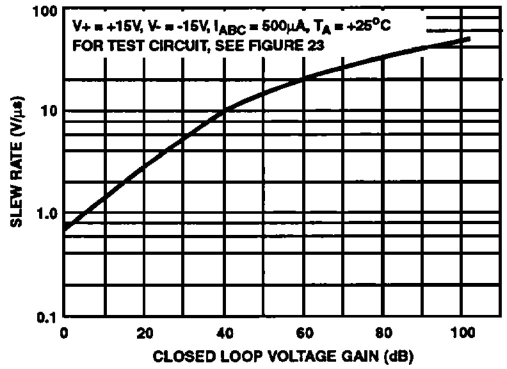


FIGURE 14. SLEW RATE vs CLOSED LOOP VOLTAGE GAIN

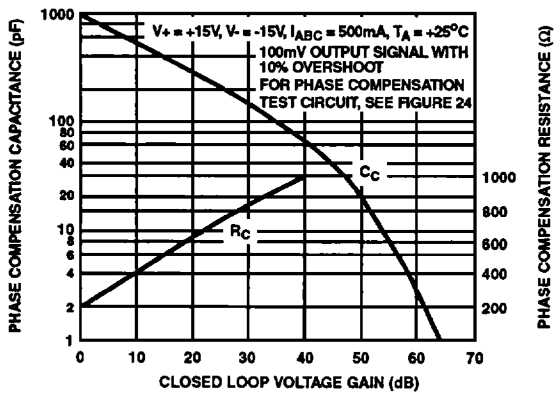


FIGURE 15. PHASE COMPENSATION CAPACITANCE AND RESISTANCE vs CLOSED LOOP VOLTAGE GAIN

Operating Considerations

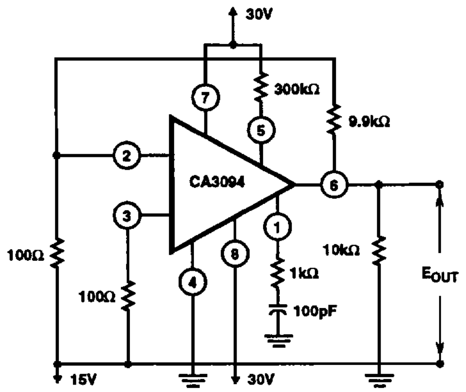
The "Sink" Output (Terminal 8) and the "Drive" Output (Terminal 6) of the CA3094 are not inherently current (or power) limited. Therefore, if a load is connected between Terminal 6 and Terminal 4 (V- or Ground), it is important to connect a current limiting resistor between Terminal 8 and Terminal 7 (V+) to protect transistor Q13 under shorted load conditions. Similarly, if a load is connected between Terminal 8 and Terminal 7 (V+), the current limiting resistor should be connected between Terminal 6 and Terminal 4 or ground. In circuit applications where the emitter of the output transistor is not connected to the most negative potential in the system, it is recommended that a 100Ω current limiting resistor be inserted between Terminal 7 and the V+ supply.

Test Circuits

1/F Noise Measurement Circuit

When using the CA3094, A, or B audio amplifier circuits, it is frequently necessary to consider the noise performance of the device. Noise measurements are made in the circuit shown in Figure 20. This circuit is a 30dB, non-inverting amplifier with emitter follower output and phase compensation from Terminal 2 to ground. Source resistors (R_S) are set to 0Ω or 1MΩ for E noise and I noise measurements, respectively. These measurements are made at frequencies of 10Hz, 100Hz and 1kHz with a 1Hz measurement bandwidth. Typical values for 1/f noise at 10Hz and 50μA I_{ABC} are $E_N = 18nV/\sqrt{Hz}$ and $I_N = 1.8pA/\sqrt{Hz}$.

Test Circuits



NOTES:

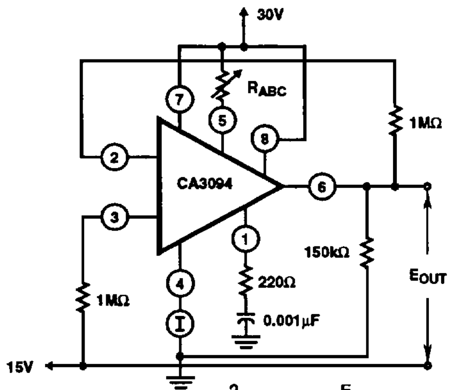
1. Input Offset Voltage: $V_{IO} = \frac{E_{OUT}}{100}$
2. For Power Supply Rejection Test: (1) vary V+ by -2V; then (2) vary V- by +2V
3. Equations:

   (1) V+ Rejection $= \frac{E_0OUT - E_1OUT}{200}$

   (2) V- Rejection $= \frac{E_0OUT - E_2OUT}{200}$
4. Power Supply Rejection: $(dB) = 20\log\frac{1}{V_{Rejection^*}}$

* Maximum Reading of Step 1 or Step 2

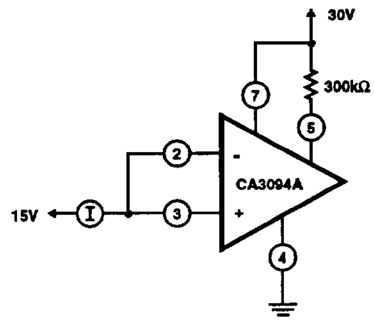
FIGURE 16. INPUT OFFSET VOLTAGE AND POWER SUPPLY REJECTION TEST CIRCUIT



NOTES:

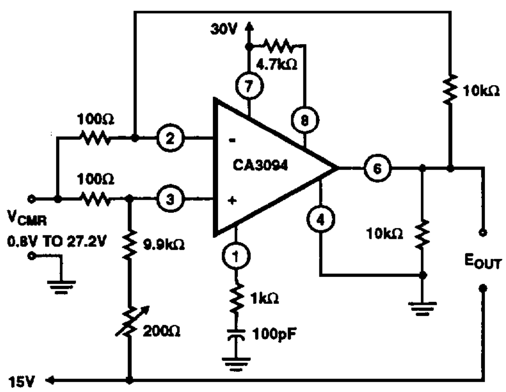
1. $P_{DISSIPATION} = (V+)(I)$
2. $I_{OS} = \frac{E_{OUT}}{10^6 \frac{VOLTS}{AMPS}}$

FIGURE 17. INPUT OFFSET CURRENT TEST CIRCUIT



NOTE: $I_I = \frac{I}{2}$

FIGURE 18. INPUT BIAS CURRENT TEST CIRCUIT

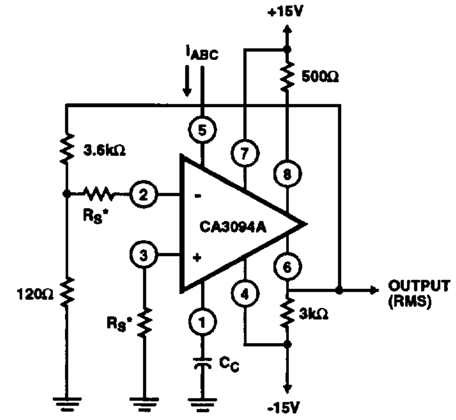


NOTES:

1. $CMRR = \left|\frac{100 \times 26V}{E_{2OUT} - E_{1OUT}}\right|$
2. Input Voltage Range for CMRR = 1V to 27V
3. $CMRR\ (dB) = 20\log\left|\frac{100 \times 26V}{E_{2OUT} - E_{1OUT}}\right|$

FIGURE 19. COMMON MODE RANGE AND REJECTION RATIO TEST CIRCUIT

Test Circuits (Continued)

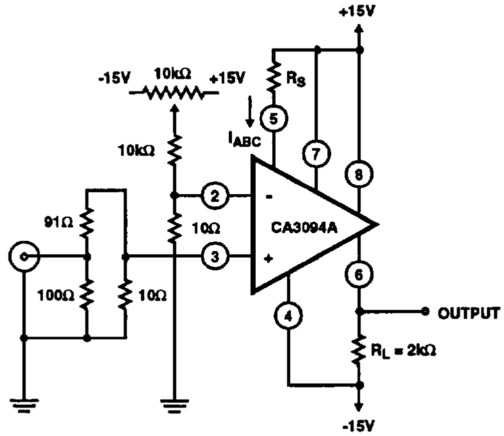


I_{ABC} (μA)	C_{COMP} (pF)
5	0
50	50
500	500

NOTES:

1. $R_S^* = 1M\Omega$ (1/F Noise Current Test)
2. $R_S = 0\Omega$ (1/F Noise Voltage Test)

FIGURE 20. 1/F NOISE TEST CIRCUIT



R_S (Ω)	I_{ABC} (μA)
56K	500
560K	50
56M	5

FIGURE 21. OPEN LOOP GAIN vs FREQUENCY TEST CIRCUIT

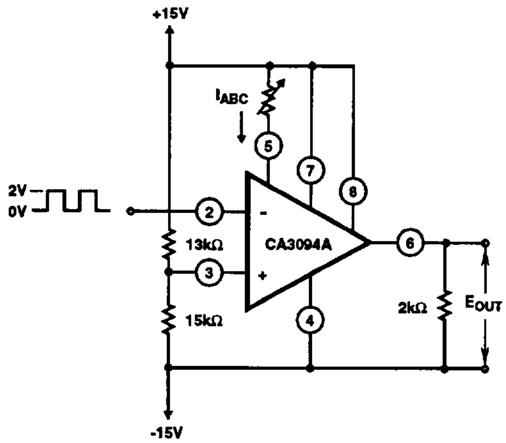


FIGURE 22. OPEN LOOP SLEW RATE vs I_{ABC} TEST CIRCUIT

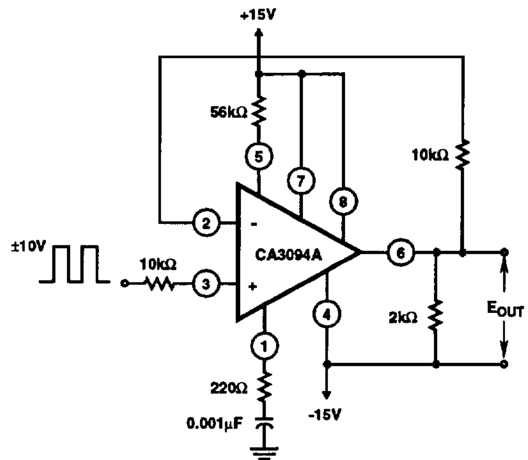
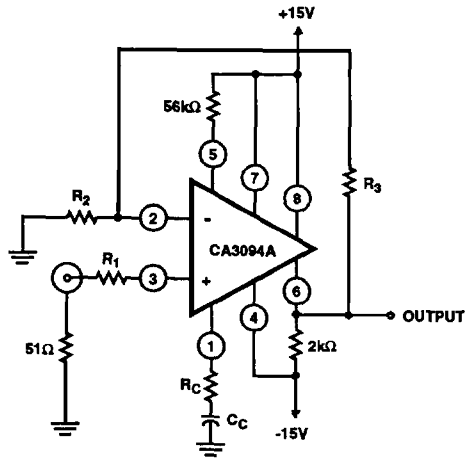


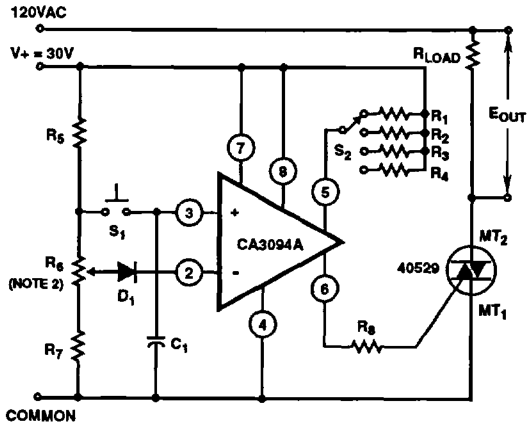
FIGURE 23. SLEW RATE vs NON-INVERTING UNITY GAIN TEST CIRCUIT

Test Circuits (Continued)



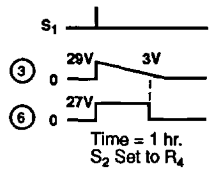
CLOSED LOOP GAIN (dB)	R_1 (kΩ)	R_2 (kΩ)	R_3 (kΩ)
0	10	∞	10
20	10	1	10
40	1	0.1	10

FIGURE 24. PHASE COMPENSATION TEST CIRCUIT



NOTES:

1. $C_1 = 0.5\mu F$
   D_1 = 1N914
   $R_1 = 0.51M\Omega$ = 3 min.
   $R_2 = 5.1M\Omega$ = 30 min.
   $R_3 = 22M\Omega$ = 2 hrs.
   $R_4 = 44M\Omega$ = 4 hrs.
   $R_5 = 1.5k\Omega$
   $R_6 = 50k\Omega$
   $R_7 = 5.1k\Omega$
   $R_8 = 1.5k\Omega$



2. Potentiometer required for initial time set to permit device interconnecting. Time variation with temperature < 0.3%/°C.

FIGURE 25. PRESETTABLE ANALOG TIMER

Typical Applications

For Additional Application Information, refer to Application Note ICAN-6048 "Some Applications of a Programmable Power/Switch Amplifier IC".

Design Considerations

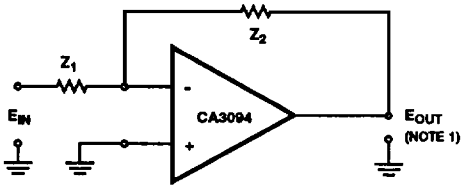
The selection of the optimum amplifier bias current (I_{ABC}) depends on:

1. The Desired Sensitivity - The higher the I_{ABC}, the higher the sensitivity, i.e., a greater drive current capability at the output for a specific voltage change at the input.
2. Required Input Resistance - The lower the I_{ABC}, the higher the input resistance.

If the desired sensitivity and required input resistance are not known and are to be experimentally determined, or the anticipated equipment design is sufficiently flexible to tolerate a wide range of these parameters, it is recommended that the equipment designer begin his calculations with an I_{ABC} of 100μA, since the CA3094 is characterized at this value of amplifier bias current.

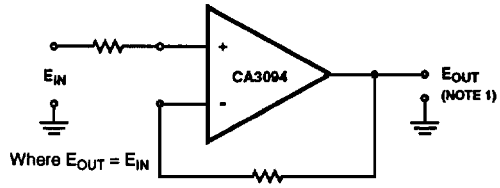
The CA3094 is extremely versatile and can be used in a wide variety of applications.

Typical Applications



Where $\frac{E_{OUT}}{E_{IN}} = f\left(\frac{Z_2}{Z_1}\right)$ depends on the characteristics of Z1 and Z2

(a)

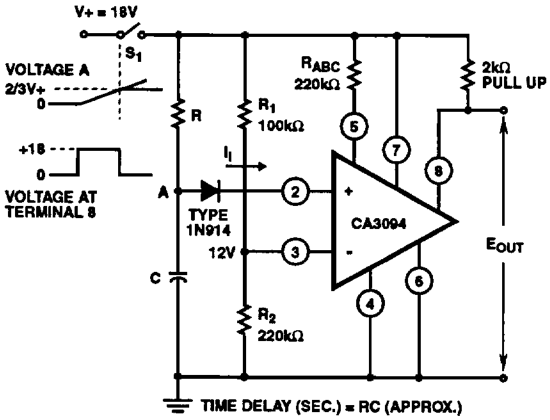


(b)

NOTE: 1. In single-ended output operation, the CA3094 may require a pull up or pull down resistor

FIGURE 26. APPLICATION OF THE CA3094: (a) AS AN INVERTING OP AMP AND (b) IN A NON-INVERTING MODE, AS A FOLLOWER

FIGURE 27. RC TIMER



Problem: To calculate the maximum value of R required to switch a 100mA output current comparator

Given: $I_{ABC} = 5\mu A$, $R_{ABC} = 3.6M\Omega \approx \frac{18V}{5\mu A}$

$I_I = 500nA$ at $I_{ABC} = 100\mu A$ (from Figure 3)

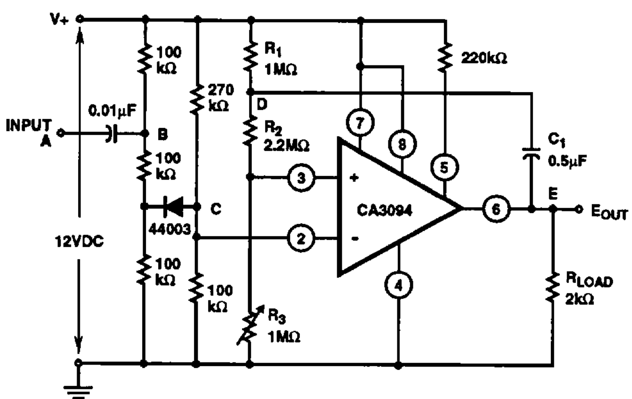
$I_I = 5\mu A$ can be determined by drawing a line on Figure 3 through $I_{ABC} = 100\mu A$ and $I_B = 500nA$ parallel to the typical $T_A = +25^oC$ curve.

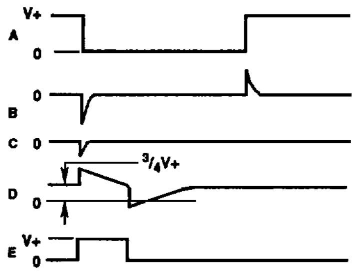
Then: $I_I = 33nA$ at $I_{ABC} = 5\mu A$

$$R_{MAX} = \frac{18V - 12V}{33nA} = 180M\Omega \text{ at } T_A = +25^oC$$

$$R_{MAX} = 180M\Omega \times 2/3^* = 120M\Omega \text{ at } T_A = -55^oC$$

* Ratio of I_I at $T_A = +25^oC$ to I_I at $T_A = -55^oC$ for any given value of I_{ABC}



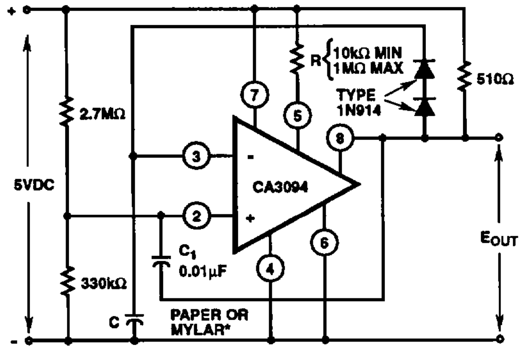


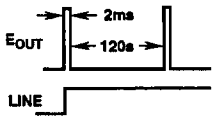
On a negative going transient at Input (A), a negative pulse at C will turn "on" the CA3094, and the output (E) will go from a low to a high level.

At the end of the time constant determined by C1, R1, R2, R3, the CA3094 will return to the "off" state and the output will be pulled low by R_{LOAD}. This condition will be independent of the interval when input (A) returns to a high level.

FIGURE 28. RC TIMER TRIGGERED BY EXTERNAL NEGATIVE PULSE

Typical Applications (Continued)





NOTES:

1. R = 1MΩ, C = 1μF
2. Time Constant: t ≈ RC x 120
3. Pulse Width: ω ≈ K(C_1/C)

* Trademark E.I. Dupont de Nemours

FIGURE 29. FREE RUNNING PULSE GENERATOR

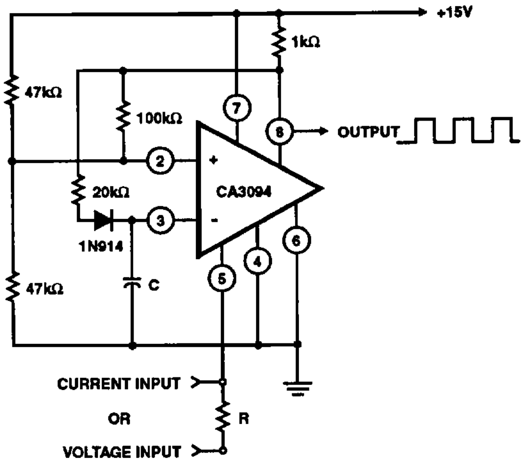


FIGURE 30. CURRENT OR VOLTAGE CONTROLLED OSCILLATOR

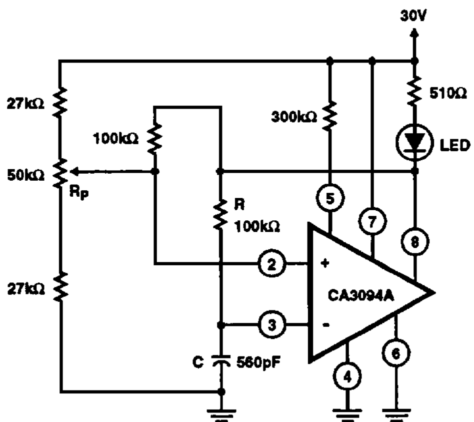
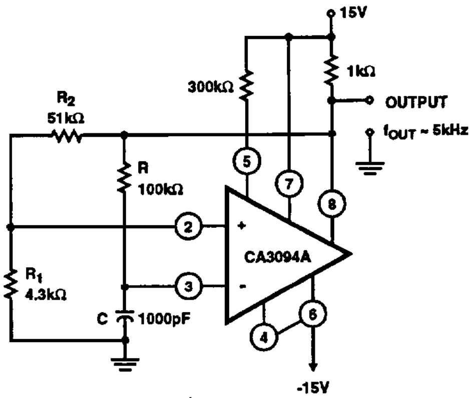


FIGURE 31. SINGLE SUPPLY ASTABLE MULTIVIBRATOR



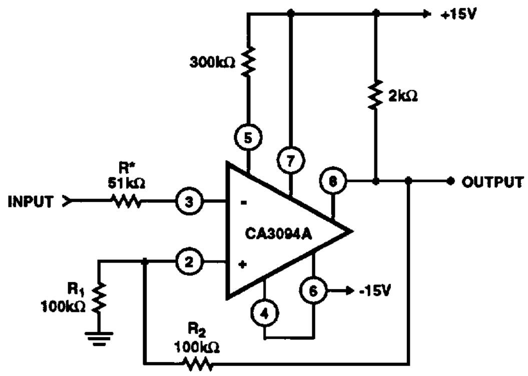
NOTE: $$f_{OUT} = \frac{1}{2RC \ln\left(\frac{2R_1}{R_2} + 1\right)}$$

If: $R_2 = 3.08R_1$, $f_{OUT} = \frac{1}{RC}$

FIGURE 32. DUAL SUPPLY ASTABLE MULTIVIBRATOR

2 OPERATIONAL AMPLIFIERS

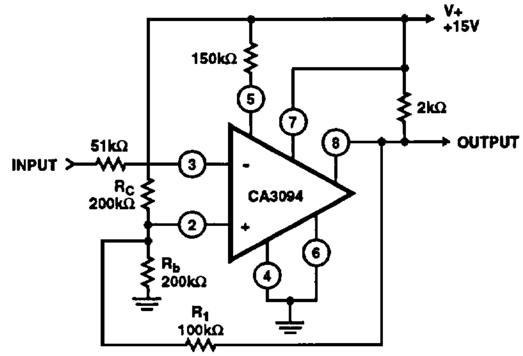
Typical Applications (Continued)



NOTES:

1. $R^* = \frac{R_1 R_2}{R_1 + R_2}$
2. $\pm\text{Threshold} = [\pm\text{Supply}]\left[\frac{R_1}{R_1 + R_2}\right]$

(a) Dual Supply

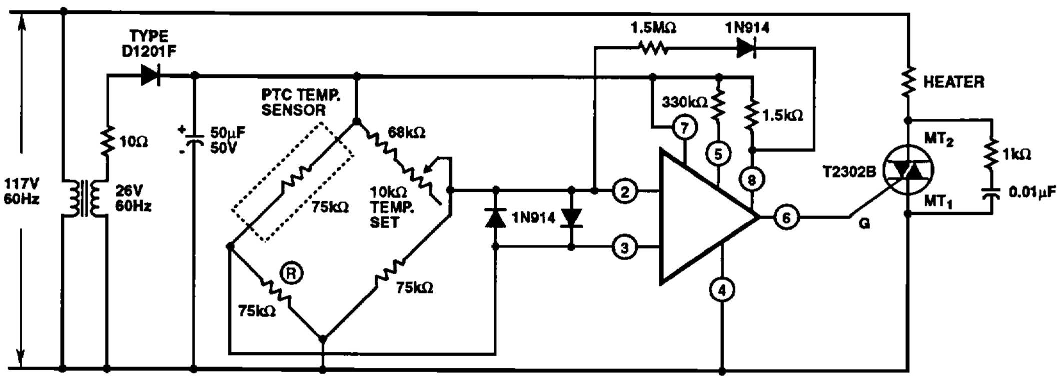


NOTES:

1. $\text{Upper Threshold} = [V+]\left[\frac{R_b}{\left(\frac{R_1 R_a}{R_1 + R_a}\right) + R_b}\right]$
2. $\text{Lower Threshold} = [V+]\left[\frac{\frac{R_1 R_b}{R_1 + R_b}}{\left(\frac{R_1 R_b}{R_1 + R_b}\right) + R_a}\right]$

(b) Single Supply

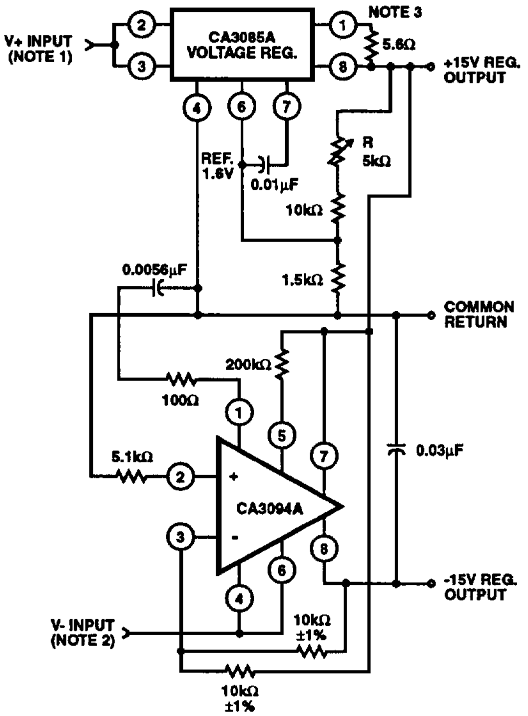
FIGURE 33. COMPARATORS (THRESHOLD DETECTORS) DUAL AND SINGLE SUPPLY TYPES



NOTE: All Resistors are 1/2W.

FIGURE 34. TEMPERATURE CONTROLLER

Typical Applications (Continued)



NOTES:

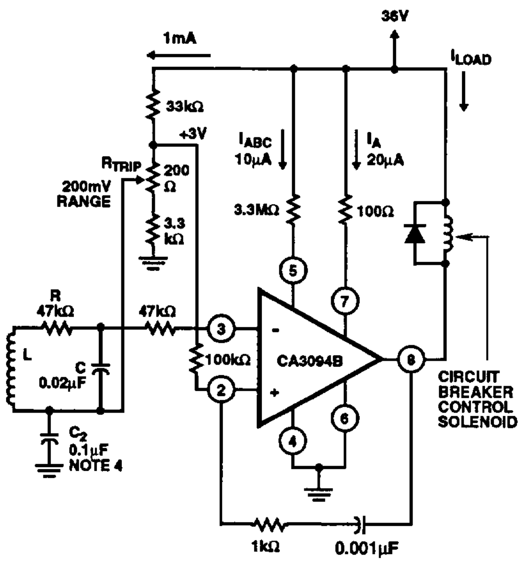
1. V+ Input Range = 19V to 30V for 15V output
2. V- Input Range = -16V to -30V for -15V output
3. Max I_{OUT} = ±100mA
4. Regulation:

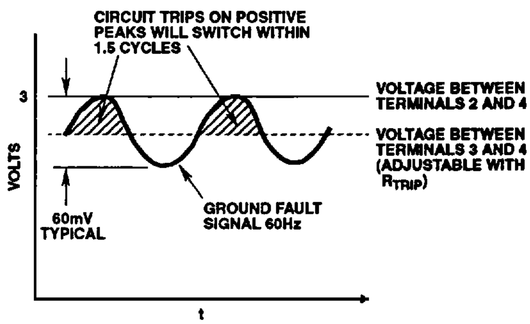
$$\text{Max Line} = \frac{\Delta V_{OUT}}{[V_{OUT}(\text{Initial})]\,\Delta V_{IN}} \times 100 = 0.075\%/V$$

$$\text{Max. Load} = \frac{\Delta V_{OUT}}{V_{OUT}(\text{Initial})} \times 100 = 0.075\%\ V_{OUT}$$

(IL from 1mA to 50mA)

FIGURE 35. DUAL VOLTAGE TRACKING REGULATOR



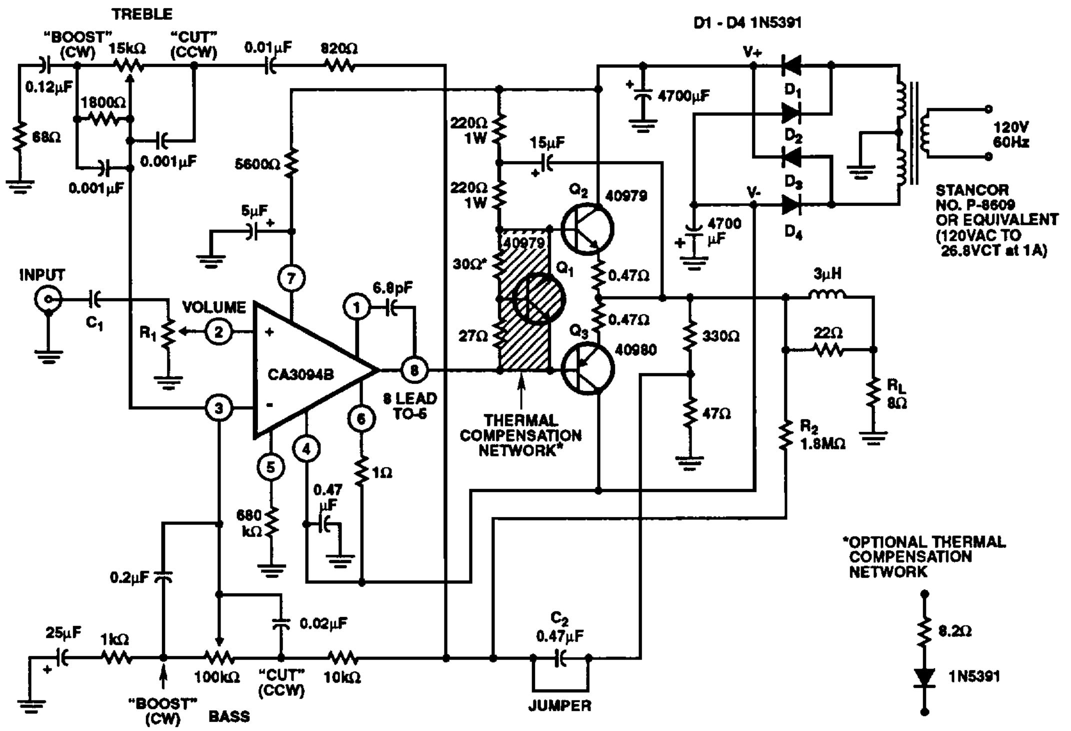


NOTES:

1. Differential current sensor provides 60mV signal ≈ 5mA of unbalance (Trip) current
2. All Resistors are 1/2 Watt, ±10%
3. RC selected for 3dB point at 200Hz
4. C_2 = AC by-pass
5. Offset adj. included in R_{TRIP}
6. Input impedance from 2 to 3 = 800kΩ
7. With no input signal Terminal 8 (output) at 36V

FIGURE 36. GROUND FAULT INTERRUPTER (GFI) AND WAVEFORMS PERTINENT TO GROUND FAULT DETECTOR

Typical Applications (Continued)



TYPICAL PERFORMANCE DATA
For 12W Audio Amplifier Circuit

Power Output (8Ω load, Tone Control set at "Flat")
- Music (at 5% THD, regulated supply) 15W
- Continuous (at 0.2% IMD, 60Hz and 2kHz mixed in a 4:1 ratio, unregulated supply) See Figure 8 in AN6048............................ 12W

Total Harmonic Distortion
- At 1W, unregulated supply.......................... 0.05%
- At 12W, unregulated supply......................... 0.57%

Voltage Gain 40dB
Hum and Noise (below continuous power output)........... 83dB
Input Resistance 250kΩ
Tone Control Range................... See Figure 9 in AN6048

NOTES:

1. For standard input: Short C_2; R_1 = 250kΩ, C_1 = 0.047µF; remove R_2
2. For ceramic cartridge input: C_1 = 0.0047µF, R_1 = 2.5MΩ, remove jumper from C_2; leave R_2

FIGURE 37. 12W AUDIO AMPLIFIER CIRCUIT FEATURING TRUE COMPLEMENTARY SYMMETRY OUTPUT STAGE WITH CA3094 IN DRIVER STAGE