Am7961

StarLAN Coded Data Transceiver

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

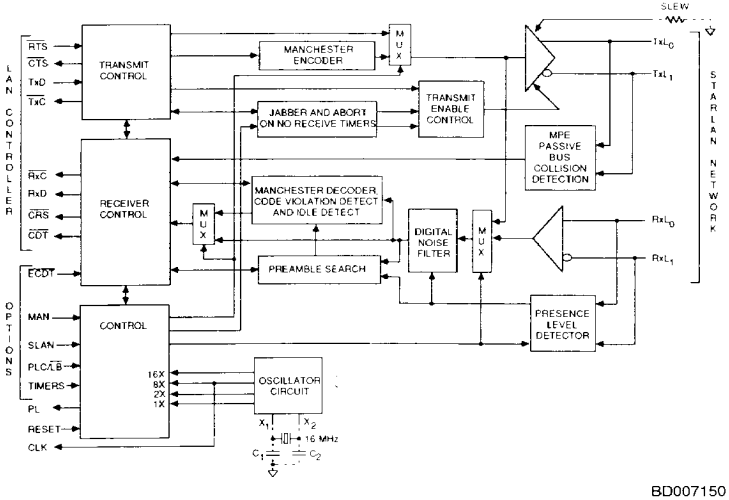
- Single-Chip Transceiver for StarLAN Networks (proposed IEEE 802.3 1BASE5)
- Direct Interface to Am7990, 82586, 82588 and 68802 LAN Controllers
- Digital Receiver Noise Filter
- Manchester Encoder/Decoder may be disabled by an external control pin (MAN)
- External pin selects two different receiver input thresholds (±700 mV or ±300 mV)
- Multipoint Extension (Daisychain) Collision Detection Circuit
- Transmit Slew Rate Controlled with a Single External Resistor
- Optional Fault Detection Modes
  - Transmit Jabber Control
  - Abort On No Receive of Carrier after transmit
  - Loopback Testing Capability
- Oscillator Circuit
  - Can be driven by a Crystal or External Clock
  - 8-MHz Output Clock is provided to Drive LAN Controller and System Clock (No LAN Controller Crystal Required)
- Fault Detection Output to Drive LED
  - Indicates that Jabber or Abort on No Receive timers have expired

GENERAL DESCRIPTION

The Am7961 is a single-chip transceiver which meets all physical layer requirements specified by the StarLAN network standard (proposed IEEE 802.3 1BASE5 Specification). This +5-volt device directly interfaces to most Local Area Network (LAN) Controllers. The StarLAN Coded Data Transceiver (SCDT) has two major operating modes: Manchester encoder and decoder active, or Manchester encoder and decoder bypassed. This means the SCDT can operate with Manchester-formatted data or as a simple transceiver. In either mode, the transmit slew rate and receiver presence level may be adjusted by external control pins. The SCDT has an internal digital receive filter which removes the need for external discrete filters. The SCDT is guaranteed to drive StarLAN transmit voltage levels of 2 V minimum and 3.65 V maximum into IEEE 802.3 1BASE5 heavy and light loads. This allows the SCDT to drive StarLAN hubs or operate in Multipoint Extension (daisychain) mode without a StarLAN Hub.

Used with two StarLAN isolation transformers and a LAN controller, the Am7961 is a complete solution which operates between a personal computer bus and a StarLAN network. This network is intended for office environments with either installed telephone wire or with user-installed twisted pair wire.

BLOCK DIAGRAM



BD007150

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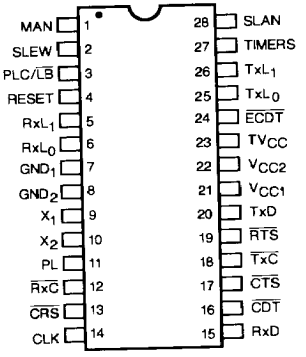
RELATED AMD PRODUCTS

Part No.	Description
Am7960	Coded Data Transceiver
Am7990	Local Area Network Controller for Ethernet
Am7992B	Serial Interface Adapter
Am7996	Ethernet Transceiver
AmZ8530	Serial Communications Controller

CONNECTION DIAGRAMS

Top View

DIP



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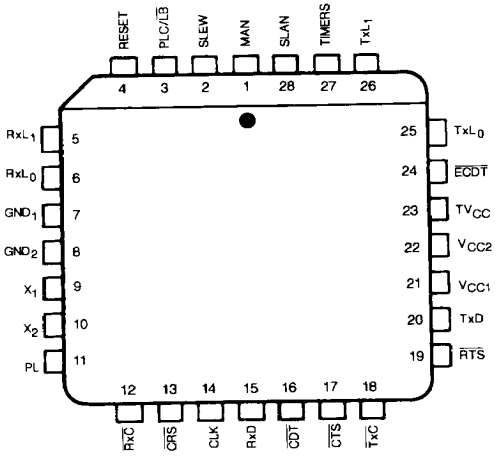
PLCC



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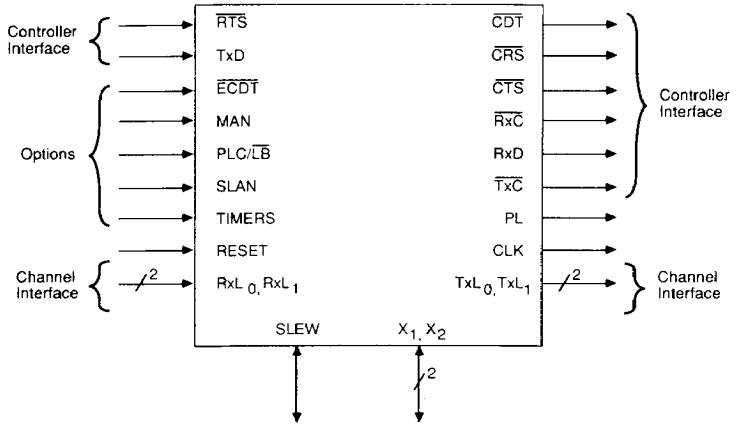
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM7961 D C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)
M = Military* (−55 to +125°C)

c. PACKAGE TYPE
D = 28-Pin Ceramic DIP (CD 028)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am7961
StarLAN Coded Data Transceiver

Valid Combinations	
AM7961	DC, DCB, DE, DMB, JC, JCB

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

LAN Controller Signals

$\overline{CDT}$ $\overline{Collision\ Detection}$ (Output; Active LOW)
The polarity of this signal can be reversed if SLAN is made LOW; SLAN is normally HIGH. This signal will go active when any of the following conditions occur:

1) A Manchester code violation is detected on the receive data, or End Of Message (EOM) is detected.

2) Presence Level is reset after assertion.

3) Daisychain Collision (ECDT) goes active while $\overline{CRS}$ is asserted.

4) Abort On No Receive goes active, $\overline{CRS}$ is de-asserted, and $\overline{RTS}$ is enabled.

5) External Collision ($\overline{ECDT}$) goes active while $\overline{CRS}$ is asserted.

$\overline{CRS}$ $\overline{Carrier\ Sense}$ (Output; Active LOW)
The polarity of this signal can be reversed if SLAN is made LOW; SLAN is normally HIGH. This signal indicates that valid data is being received from the differential receive channel. $\overline{CRS}$ is qualified by two circuits: 1) Presence Level Detect senses the receive signal for threshold voltages for signals greater than ±(700 + 100) mV if PLC/$\overline{LB}$ = 1, or ±(300 + 50) mV if PLC/$\overline{LB}$ = 0, and greater than 100-ns duration, and 2) Preamble Search circuit must detect preamble before $\overline{CRS}$ is asserted LOW. De-assertion of $\overline{CRS}$ indicates that IDLE has been detected, the presence level has gone inactive for 16 $\overline{TxC}$, or that a Manchester coding violation has been detected.

$\overline{CTS}$ $\overline{Clear\ To\ Send}$ (Output; Active LOW)
This signal line is an output from SCDT. When the StarLAN Controller asserts $\overline{RTS}$ and the SCDT is ready to receive data on the transmit serial data line (TxD), the SCDT asserts $\overline{CTS}$.

$\overline{RTS}$ $\overline{Request\ To\ Send}$ (Input; Active LOW)
The polarity of this input can be reversed if SLAN is made LOW; SLAN is normally HIGH. When this pin is driven active the StarLAN Controller is ready to output data on its TxD pin. When driven inactive, the SCDT will append IDLE to the end of message and then disable the transmitter.

$\overline{RxC}$ $\overline{Receive\ Clock}$ (Output; Active LOW)
The polarity of this signal can be reversed if SLAN is made LOW; SLAN is normally HIGH. Receive Clock is a MOS level output voltage. $\overline{RxC}$ is used to strobe out RxD on a HIGH to LOW clock transition if $\overline{CRS}$ = 0 (regardless of whether MAN is tied to V_{CC}, GND, or left open). When $\overline{CRS}$ is HIGH, $\overline{RxC}$ is also held HIGH.

RxD Receive Serial Data (Output)
Receive data output to the StarLAN Controller. RxD has MOS level output voltages. (See V_{OH} spec.)

$\overline{TxC}$ $\overline{Transmit\ Clock}$ (Output; Active LOW)
This timing signal is the 1-MHz transmit bit rate clock. This signal has MOS-level output voltages (see V_{OH} spec). The polarity of this signal can be reversed if SLAN is made LOW; SLAN is normally HIGH.

TxD Transmit Serial Data (Input)
Transmit data input from the StarLAN Controller should be either Manchester or NRZ coded depending on the logical state of the MAN pin.

Option Signals

$\overline{ECDT}$ $\overline{External\ Collision\ Detect}$ (Input; Active LOW)
This input is active LOW and provides an auxiliary external collision detect if $\overline{CRS}$ is asserted. This signal must be present for a miminum of 15 ns. This pin has an internal pull-up resistor.

MAN Manchester Mode (Input)
This input has three input logic levels: V_{CC}, open circuit, and ground. This input enables and disables the Manchester encoder and decoder. If MAN = V_{CC}, the internal Manchester encoder/decoder is enabled. If MAN = open circuit, the Manchester encoder/decoder is enabled and the PL output will latch to a logic 0 if either (Jabber or Abort On No Receive) timer expires. If MAN = Ground, the Manchester encoder/decoder is disabled.

PL Presence Level (Output; Active HIGH)
This signal has two modes controlled by the state of MAN. Mode one is when MAN is at V_{CC} or GND; in Mode one the Presence Level signal will be logic 1 when the differential signal on the $RxL_0 - RxL_1$ pair has been accepted for amplitude and minimum time duration. This mode supports daisychain options. Mode two is when the MAN = open circuit. In this mode, the PL signal will latch to logic 0 whenever the Jabber or Abort on No Receive timers expire. This output can be used to directly drive an LED and a series limiting resistor to V_{CC1}.

PLC/$\overline{LB}$ Presence Level Control/$\overline{Loopback}$ (Input)
This input has three states: V_{CC}, ground, and open circuit. When this input is tied to V_{CC}, the presence level is set to ±(700±100) mV and the differential receiver complies with the StarLAN IEEE 802.3 1BASE5 specifications. When this input is open circuit, the presence level is decreased to ±(300±50) mV, which extends dynamic transmission range in low-noise applications. When PLC/$\overline{LB}$ is tied to ground (GND), loopback is active and the SCDT will process TxD and then loop the data back as if it were received data. Then the chip outputs RxD with the following support signals: $\overline{RxC}$, $\overline{CDT}$ and $\overline{CRS}$.

SLAN Control Circuit Option Pin (Input; Active HIGH)
This input, when tied HIGH or left open, will maintain the active states as defined in the Functional Pin Description. When this signal is tied LOW the following signal active states are inverted: $\overline{RTS}$, $\overline{TxC}$, $\overline{CRS}$, $\overline{CDT}$ and $\overline{RxC}$.This pin has an internal pull-up resistor.

TIMERS Timers (Input; Active HIGH)
This input, when driven to a logic 1, will enable both the Jabber timer and the Abort On No Receive timer. The Jabber timer limits the maximum transmitted data message to 16 ms which is longer than the maximum StarLAN packet size. If this value is exceeded, then the SCDT transmitter is three-stated until $\overline{RTS}$ goes inactive and then returns to an active logic level. The Abort On No Receive timer ensures that the SCDT is connected to the network. When the SCDT transmits a packet, differential receive channel data must be detected within 384 μs or the transmitter circuit is disabled. When TIMERS is a logic 0, both timers are disabled and therefore the differential transmitter will be active when $\overline{CTS}$ is active. This pin has an internal pull-up resistor.

System Signals

CLK Clock (Output)
This clock output is 8 MHz which is synchronous with the 16-MHz internal clock oscillator circuit. This signal has MOS output voltage levels and can be used to drive the StarLAN Controller system clock.

RESET Reset (Input; Active HIGH)
RESET is active HIGH and can be used asynchronously. It resets all internal flip-flops and three-states TxL_0 and TxL_1. $\overline{TxC}$ and CLK outputs continue to operate when RESET is active.

SLEW Slew Rate Control (Input/Output)
This pin is used to control the transmit slew rate with an external resistor to ground. External slew rate resistor of 2K will cause the rise and fall times to be approximately equal to 100 ns from zero crossing to +2.0 volts.

X_1, X_2 Crystal Oscillator Connections (Input/Output)
X_1 and X_2 are connections for an external crystal. X_1 may be driven by a MOS or TTL level clock, but X_2 must be left open in this mode.

StarLAN Network Signals

RxL_0, RxL_1 Receive Data (Inputs)
RxL_0 and RxL_1 form a differential receive data input pair.

TxL_0, TxL_1 Transmit Data (Outputs)
TxL_0 and TxL_1 form a differential transmit data pair. (The external resistor connected to the SLEW pin controls the slew rate).

Power Supply Pins

GND_1 Ground
This pin is power-supply return for TTL and the differential transmit circuit.

GND_2 Ground
This pin is power-supply return for the internal logic circuits.

V_{CC1} Power Supply
This pin is nominally 5.0 Volts and powers the TTL circuitry.

V_{CC2} Power Supply
This pin is nominally 5.0 Volts and powers the internal logic circuitry.

V_{CCT} Transmit Power Supply
The differential transmitter circuit has a separate +5-volt power supply pin. This pin also controls Test Mode; if V_{CCT} is tied to 0 volts while V_{CC1} and V_{CC2} are connected to 5 V, the $\overline{TxC}$ output will stay in a logic-1 state (assuming SLAN is HIGH). In addition, if $\overline{RTS}$ is LOW and TIMER is HIGH, the Abort On No Receive and Jabber counters will run at a rate 16 times faster than normal (i.e., Abort will time out in 24 μs and Jabber at 1 ms).

FUNCTIONAL DESCRIPTION

The Am7961 StarLAN Coded Data Transceiver (SCDT) is a single-chip transceiver for StarLAN (proposed IEEE 802.3 1BASE5 Specification). This chip links LAN controllers to StarLAN and provides advanced networking features while reducing the cost of interfacing Data Terminal Equipment (DTE) to StarLAN. This chip integrates the following functions: differential transmitter, differential receiver, Manchester encoder, Manchester decoder, digital noise filter, watchdog timer (jabber), diagnostic features (abort on no receive and loopback), presence level detection circuit (squelch), crystal oscillator, and daisychain collision detection. It allows the designer to build a two-chip solution for StarLAN by using existing LAN controllers (e.g., 82586), SCDT, a 16-MHz crystal, and two StarLAN isolation transformers. The SCDT replaces more than 10 discrete parts, reduces printed-circuit board area, and includes advanced StarLAN networking features.

Transmitter

The SCDT block diagram is shown on page 1. The Transmit Control circuit receives Request-To-Send ($\overline{RTS}$) and responds by sending back Clear-To-Send ($\overline{CTS}$). The Transmit Enable Control activates the differential transmit circuit. If the LAN controller outputs Non-Return to Zero (NRZ) data, then the option pin (MAN) should be held HIGH. This places the internal Manchester encoder into the signal path. When the LAN controller outputs Manchester encoded data, then the MAN pin should be held LOW. This disables the internal Manchester encoder output and allows TxD to drive the transmit circuit. In either mode, the SCDT differential transmitter directly drives the primary of the StarLAN isolation transformer. The transmit circuit matches the rise and fall times to minimize transmitter jitter. An external resistor connected to the transmit slew rate control pin adjusts the rise and fall times of the differential line driver to minimize higher-order harmonics, thus reducing EMI and RFI.

The transmitter circuit has two optional timers: Jabber, and Abort On No Receive (AONR). Both of these timers are enabled if the option pin (TIMERS) is HIGH. During normal operation these two timers will not expire. If a LAN controller tries to send a message much longer than the maximum StarLAN packet length, the Jabber timer will disable the differential transmitter until the $\overline{RTS}$ signal has gone inactive (HIGH). This ensures that one DTE station cannot lock up the whole StarLAN network and isolates the failure to the transmitting DTE. This ability gives greater network efficiency, by detecting and isolating the faulty DTE at the SCDT instead of at the StarLAN hub. The Abort On No Receive (AONR) timer, if enabled, monitors whether Carrier Sense ($\overline{CRS}$) goes active after each transmission. Failure to go active within 384 μs indicates a fault in one of the following: SCDT transmitter, SCDT receiver, twisted pair wiring, connectors, hub receiver, or hub transmitter. If this condition exists, the differential output driver is disabled which prevents the DTE from randomly transmitting onto a busy network, thereby improving network efficiency. If either timer expires, the chip is capable of directly driving the PL output pin to an LED indicator. This indicator is helpful for user installation and diagnostic testing.

Receiver

The input pins of the differential receiver circuit are driven by a StarLAN isolation transformer. To be accepted, the received data must be qualified by the two following conditions: the protection time has expired, and both the positive and negative Presence Level Detectors have been asserted. Protection time is the minimum time from the end of the last message to the time the next message can be received. This parameter is not to be confused with the interframe gap which is also defined by the StarLAN specification.

The Am7961 supports three levels of signal qualification. First, the Presence Level Control option pin (PLC/$\overline{LB}$) sets the signal threshold qualification level at the receiver input to a nominal ±700 mV or ±300 mV. The higher value supports the proposed IEEE 802.3 1BASE5 StarLAN specification for signals on twisted pairs in bundled telephone cables. The lower value supports networks which use user-installed wiring which has comparatively greater noise margins and which permits extended communication distances. The receive differential signal must be above the positive presence level for a

minimum of 100 ns and then go below the negative presence level for a minimum of 100 ns to qualify for reception. The Presence Level Detector, when enabled, allows data to pass through the Digital Noise Filter.

Second, the output of the Digital Noise Filter drives the Preamble Search, Manchester Decoder and the Receiver Control. When Manchester mode is disabled (MAN = 0), the data flows directly from the digital noise filter to the Receiver Control and out to the Receive Data pin (RxD). When Manchester mode is enabled (MAN = 1), the Preamble Search and Manchester decoder paths are active. First, the Preamble Search circuit has to detect 500-KHz StarLAN preamble, at the completion of which data is synchronized and decoding commences. The Manchester decoder separates data into NRZ received data (RxD) and received clock ($\overline{RxC}$). This Manchester decoder has a digital phase-locked-loop which operates at sixteen times the received data rate and lengthens or shortens its cycle to track the incoming data. This decoder can successfully track the received Manchester data with enhanced jitter performance.

Finally, the Manchester Decoder examines the data stream for Manchester coding violations and reports their presence to the LAN controller through the Collision Detect ($\overline{CDT}$) pin. At the end of message, the Manchester decoder detects the start of the IDLE condition, which is the time when the transmitter output is driven HIGH for 2μs to 3μs (End of Message) and then released to a three-state condition. When IDLE goes active, the protection timer is started which inhibits the Presence Level Detector during the end-of-message transients.

The Receiver Control circuit interfaces the SCDT to its controller. LAN controllers fall into two main categories which support either active-LOW signals or active-HIGH signals. The option pin (SLAN) in the Control circuit of the SCDT is used to select appropriate signal polarity of $\overline{CTS}$, $\overline{TxC}$, $\overline{CRS}$, $\overline{CDT}$ and $\overline{RxC}$. Two other input pins to the Control circuit are used in the following way: the Manchester Mode Pin (MAN) controls whether the encoder and decoder are active; Presence Level and Loopback (PLC/$\overline{LB}$) controls whether the presence level is ±700 mV or ±300 mV, or if loopback mode is provided as a diagnostic tool. Loopback Mode allows the LAN controller to send transmit data (TxD) to the SCDT, which then processes the data and loops it back to the LAN controller as received data (RxD). The loopback point is just prior to the differential transmitter and after the differential receiver circuits, which are disabled in this mode. This test can be performed with Manchester mode enabled or disabled.

Oscillator

The Oscillator Circuit can either be driven with an external 16-MHz source or a 16-MHz crystal can be connected between pins X_1 and X_2. The SCDT divides the 16-MHz signal and outputs an 8-MHz clock which can directly drive the system clock of some LAN Controllers. This eliminates the need to have separate crystals for the LAN controller and the SCDT.

Multipoint Extension Option

The SCDT supports the daisychain option, presently one of the Multipoint Extension Options (MPE) being considered by the IEEE 802.3 1BASE5 committee. The SCDT detects a collision at the transmitter circuit output and asserts the collision detection line ($\overline{CDT}$) when a collision occurs. This allows DTEs to be connected together without the use of a StarLAN hub.

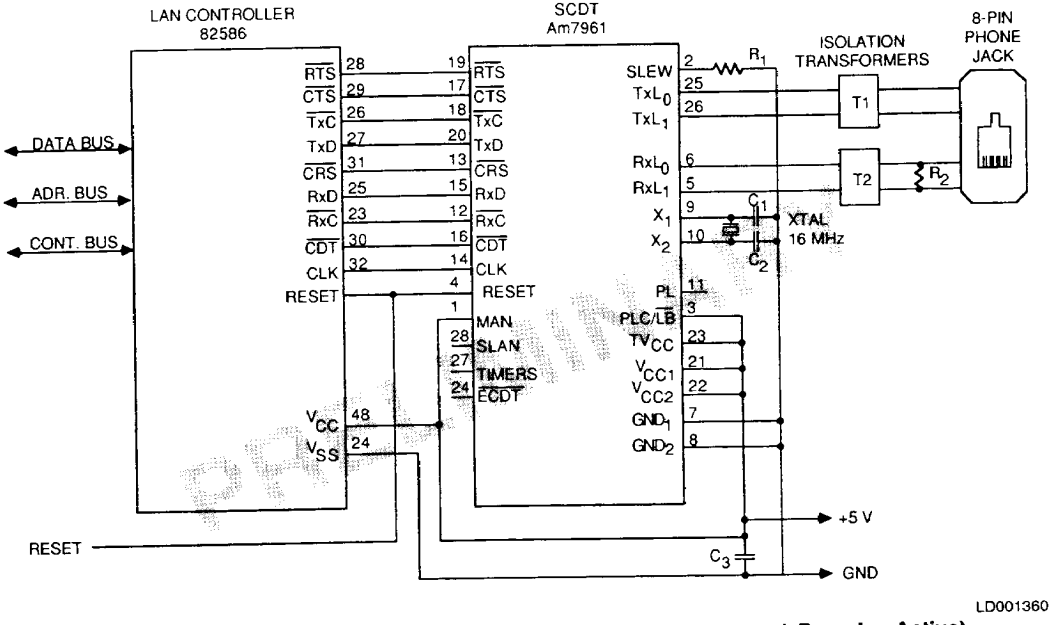


Figure 1. SCDT and the 82586 (SCDT Internal Manchester Encoder and Decoder Active)

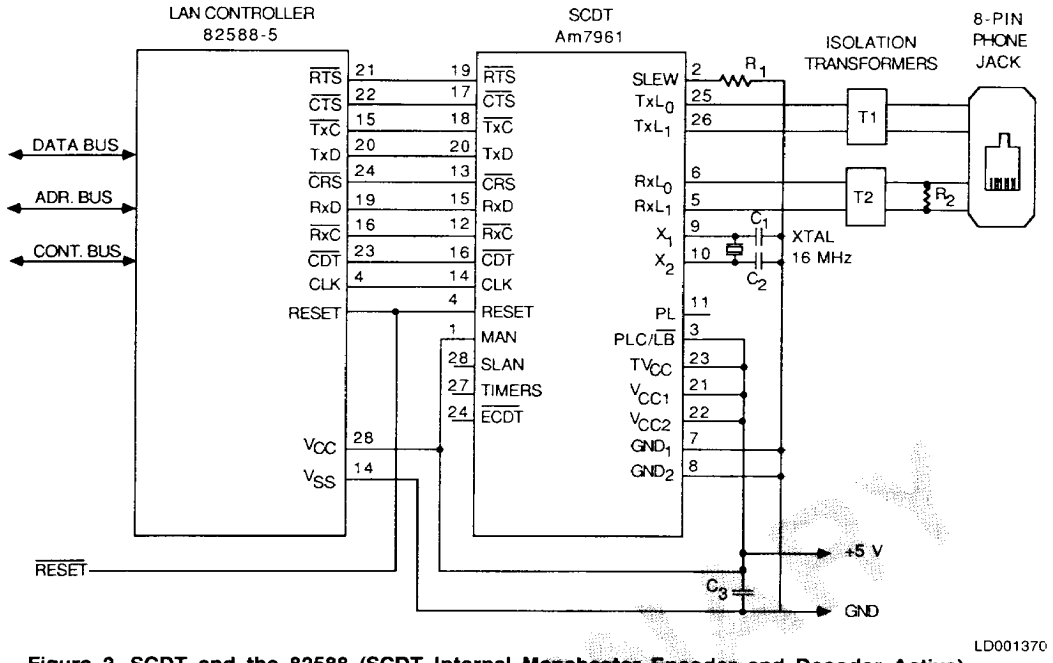


Figure 2. SCDT and the 82588 (SCDT Internal Manchester Encoder and Decoder Active)

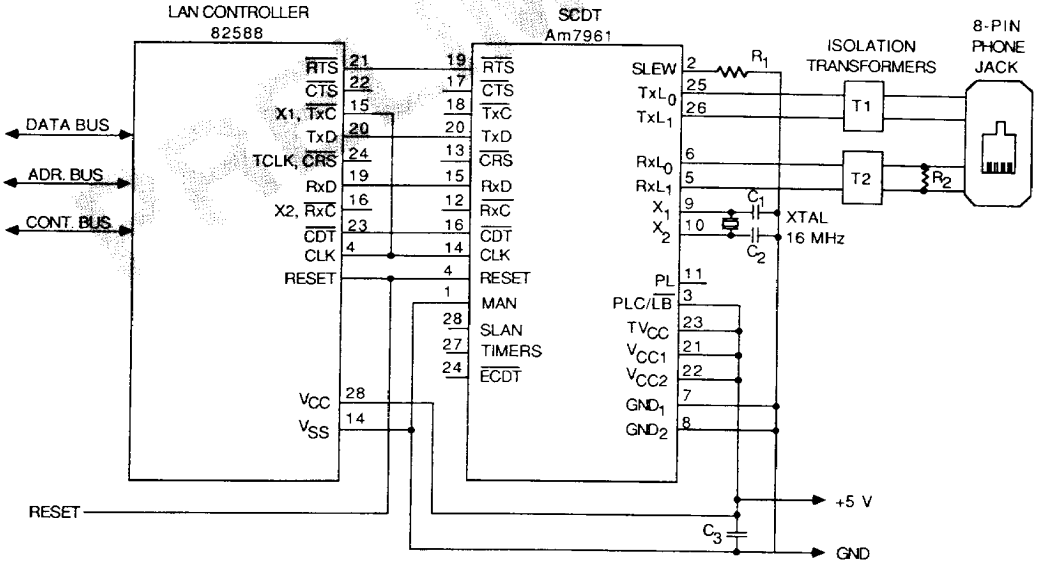


Figure 3. SCDT and the 82588 (82588 Internal Manchester Encoder and Decoder Active)

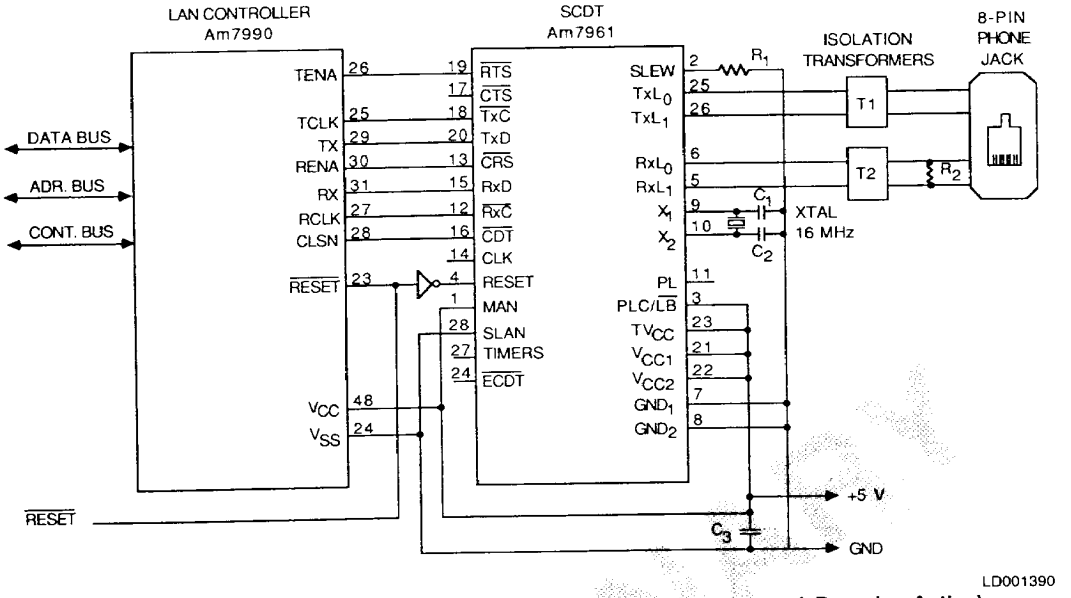


Figure 4. SCDT and the Am7990 (SCDT Internal Manchester Encoder and Decoder Active)

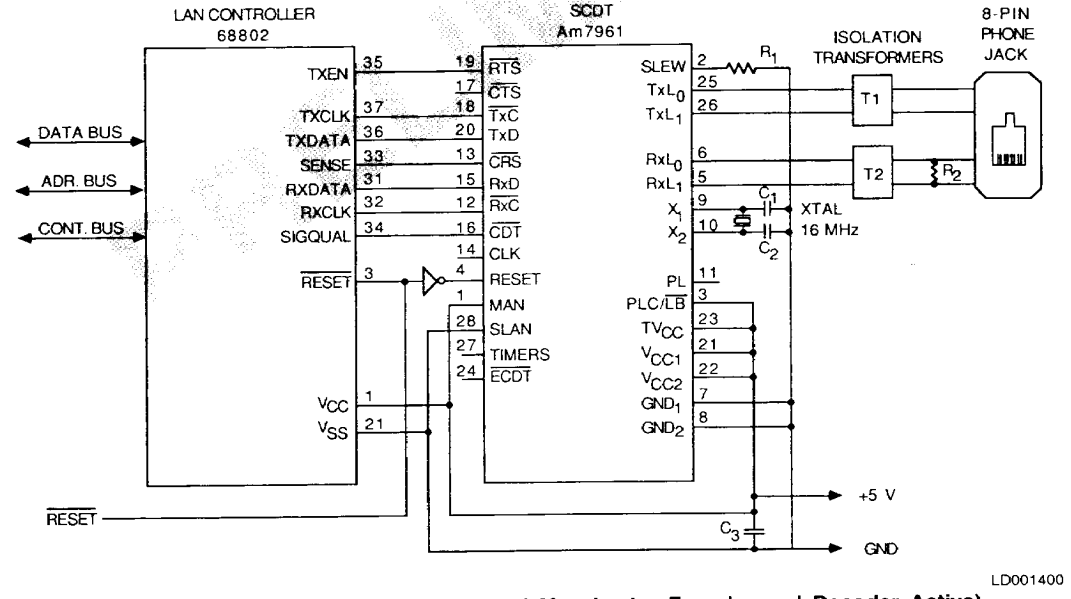


Figure 5. SCDT and the 68802 (SCDT Internal Manchester Encoder and Decoder Active)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Temperature Under Bias ..... −55 to +125°C
Supply Voltage Above Ground Potential. −0.5 V to +7.0 V
Receiver Common Mode Voltage ..... −10.0 V to +6.0 V
Transmitter Common Mode Voltage ..... −0.5 V to +5.5 V
DC Output Current
into Outputs (Logic Outputs) ..... 30 mA
DC Input Voltage (Logic Inputs) ..... −0.5 V to +5.5 V
DC Input Current (Logic Inputs) ..... −30 mA to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5V

DC CHARACTERISTICS over operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V_{OH}	Output HIGH Voltage (Notes 1 & 2)	I_{OH} = −1 mA	2.4		V
		I_{OH} = −0.4 mA	3.9		
V_{OL}	Output LOW Voltage (Notes 1 & 2)	I_{OL} = +8 mA		0.45	V
V_{IH}	Input HIGH Voltage (TTL)	(Note 3)	2.0		V
		(Note 5)	V_{CC} − 0.1		
V_{IL}	Input LOW Voltage (TTL)	(Note 3)		0.8	V
		(Note 5)		0.1	
$\overline{V_T}$	Differential Transmit Output Voltage	R_L = 40 or 115 Ω	−2.0	−3.65	V
V_T			+2.0	+3.65	
V_{TO}	Matching of Differential Output Voltage (Note 4)	R_L = 40 or 115 Ω	−75	+75	mV
I_{OSC}	Transmit Output Short-Circuit Current	V_{CC} = Max.		−300	mA
I_{OX}	Transmit Off-State Leakage Current	V_{CC} = Max., V_{OX} = V_{CC} ÷ 2	−100	+100	μA
V_{TH}	Differential Receiver Offset Voltage	0 < V_{CM} < +5	−100	+100	mV
R_R	Differential Receiver Input Resistance		13.5		KΩ
I_{SC}	TTL/MOS Output Short-Circuit Current (Note 6)	V_{CC} = Max.	−40	−240	mA
R_{PV}	Receiver Positive Presence Voltage Level	PLC/$\overline{LB}$ = V_{CC} or GND	600	800	mV
		PLC/$\overline{LB}$ Open	250	350	
R_{NV}	Receiver Negative Presence Voltage Level	PLC/$\overline{LB}$ = V_{CC} or GND	−600	−800	mV
		PLC/$\overline{LB}$ Open	−250	−350	
T_{CM}	Transmit Common Mode Output Voltage			200	mV
I_{CC}	V_{CC} = 5.5 V, Transmit Outputs Open Circuit (Unloaded)			192	mA

Input Capacitance*

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C_R	Differential Receiver Input Capacitance	$\overline{RTS} = V_{CC}$	4	pF
C_T	Differential Transmit Voltage Capacitance		6	

* Parameters are not Tested

Notes: 1. TTL output signals $\overline{CTS}$, $\overline{CDT}$, $\overline{CRS}$.
2. MOS output signals $\overline{TxC}$, $\overline{RxC}$, RxD, CLK.
3. TTL inputs TxD, $\overline{RTS}$, $\overline{ECDT}$.
4. V_T and $\overline{V_T}$ are the differential output signals $TxL_0 - TxL_1$ depending upon signal polarity.
5. Three-level input signals: MAN and PLC/$\overline{LB}$.
6. No more than one TTL or MOS output may be shorted at a time, and short-circuit duration shall not exceed 1 second.

SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified

Transmit Specifications

No.	Parameter Symbol	Parameter Descriptions (Note 5)	Min.	Nom.	Max.	Unit
Transmit (Beginning of Packet) (Refer to Timing Diagrams 1A & 1B)						
1	t_{PW}	CLK HIGH Time (Notes 1 & 6)	57	62.5	68	ns
2	t_{PW}	CLK LOW Time (Notes 1 & 6)	57	62.5	68	ns
3	t_F	CLK Fall Time (Notes 1 & 3)			10	ns
4	t_R	CLK Rise Time (Notes 1 & 3)			10	ns
5	t_{PD}	CLK LOW to $\overline{TxC}$ LOW (Notes 1 & 6)			15	ns
6	t_{PW}	$\overline{TxC}$ HIGH Time (Notes 1 & 6)	485	500	515	ns
7	t_{PW}	$\overline{TxC}$ LOW Time (Notes 1 & 6)	485	500	515	ns
8	t_R	$\overline{TxC}$ Rise Time (Notes 1 & 3)			10	ns
9	t_F	$\overline{TxC}$ Fall Time (Notes 1 & 3)			10	ns
10	t_S	$\overline{RTS}$ LOW to $\overline{TxC}$ HIGH (Notes 1 & 6)	300	500	700	ns
11	t_P	X_1 Input Period at 16 MHz (Notes 1 & 6)	62.5		62.5	ns
12	t_{PD}	$\overline{RTS}$ LOW to $\overline{CTS}$ LOW (Notes 1 & 6)			50	ns
13	t_{PD}	$\overline{TxC}$ HIGH to TxD Valid (Data Start Inhibit Period) (Notes 1 & 6)	2200			ns
14	t_{PD}	$\overline{TxC}$ HIGH to $\overline{TxL_0}$, $\overline{TxL_1}$ Active (Notes 1, 2, & 7)	2200	2300	2570	ns
15A	t_S	TxD Valid to $\overline{TxC}$ HIGH (MAN = 1) (Notes 1 & 6)	50			ns
15B	t_H	$\overline{TxC}$ HIGH to TxD Valid (MAN = 1) (Notes 1 & 6)	50			ns
16	t_{PD}	$\overline{TxC}$ HIGH to TxL_{0-1} Transition (MAN = 0) (Notes 6 & 7)		750		ns
17A	t_S	TxD Valid to CLK LOW (Edge 2) (MAN = 0) (Notes 1 & 6)	50			ns
17B	t_H	CLK LOW (Edge 2) to TxD Valid (MAN = 0) (Notes 1 & 6)	50			ns
19	t_R	$TxL_0 - TxL_1$ Rise Time (Notes 2 & 8)			100	ns
20	t_F	$TxL_0 - TxL_1$ Fall Time (Notes 2 & 8)			100	ns
Transmit (End of Packet) (Refer to Timing Diagram 2)						
21	t_{PD}	$\overline{RTS}$ HIGH to $\overline{CTS}$ HIGH (Notes 1 & 6)			50	ns
23	t_{H2}, t_{L2}	$\overline{TxC}$ HIGH to TxL_0, TxL_1 Three-State (Notes 1, 2, 6 & 9)		2800		ns
26	t_S	$\overline{RTS}$ HIGH to $\overline{TxC}$ HIGH (Notes 1 & 6)	300	500	700	ns

SWITCHING CHARACTERISTICS (Cont'd.)
Transmit and Receiver Specifications

No.	Parameter Symbol	Parameter Description	Min.	Nom.	Max.	Units
Receiver (Beginning of Packet) (Refer to Timing Diagram 3)						
30	t_{PD}	$RxL_0 - RxL_1$ to $\overline{CRS}$ LOW (Notes 1, 6, & 7)	1250		5500	ns
31	t_{PD}	$\overline{CRS}$ LOW to $\overline{RxC}$ LOW (Notes 1 & 6)			1200	ns
Receiver (Middle of Packet) (Refer to Timing Diagram 4)						
34	t_P	$\overline{RxC}$ Period (Notes 1 & 6)	920		1080	ns
35	t_R	$\overline{RxC}$ Rise Time (Notes 1 & 3)			10	ns
36	t_F	$\overline{RxC}$ Fall Time (Notes 1 & 3)			10	ns
37	t_{PW}	$\overline{RxC}$ LOW Time (Notes 1 & 6)	420		580	ns
38	t_{PW}	$\overline{RxC}$ HIGH Time (Notes 1 & 6)	420		580	ns
39	t_S	RxD Valid Before $\overline{RxC}$ LOW (Notes 1 & 6)	100	300		ns
40	t_H	RxD Valid After $\overline{RxC}$ LOW (Notes 1 & 6)	100	690		ns
41	t_R	RxD Rise Time (Notes 1 & 3)			10	ns
42	t_F	RxD Fall Time (Notes 1 & 3)			10	ns
Receiver (End of Packet) (Refer to Timing Diagram 5)						
51	t_{PD}	$\overline{RxC}$ HIGH to $\overline{CRS}$ HIGH (Notes 1 & 6)	100	405		ns
52	t_{PD}	$\overline{CRS}$ HIGH to $\overline{RxC}$ HIGH (Notes 1 & 6)	100	600		ns
60		$RxL_0 - RxL_1$ Three-State to $\overline{CRS}$ HIGH (Notes 1, 6, & 10)		380		ns
61	t_{PD}	$\overline{CDT}$ LOW to $\overline{CRS}$ HIGH (Notes 1 & 6)		940		ns
62	t_{PD}	RxD LOW to $\overline{CRS}$ HIGH (Notes 1 & 6)		160		ns
63	t_{PD}	$\overline{RxC}$ HIGH to $\overline{CDT}$ LOW (Notes 1 & 6)	470	520	550	ns
Receiver (End of Packet) (Refer to Timing Diagram 6)						
65	t_P	$\overline{CRS}$ HIGH to Receiver Active for Next Packet Reception (Protection Time) (Notes 1 & 6)		20		$\overline{TxC}$
Loopback Test (Refer to Timing Diagram 7)						
70	t_D	$\overline{CRS}$ HIGH to $\overline{CDT}$ LOW (Notes 1 & 6)		7		$\overline{TxC}$
71	t_D	$\overline{CRS}$ HIGH to $\overline{CDT}$ HIGH (Notes 1 & 6)		14		$\overline{TxC}$
72	t_D	$\overline{CRS}$ HIGH to End of Protection Time		20		$\overline{TxC}$

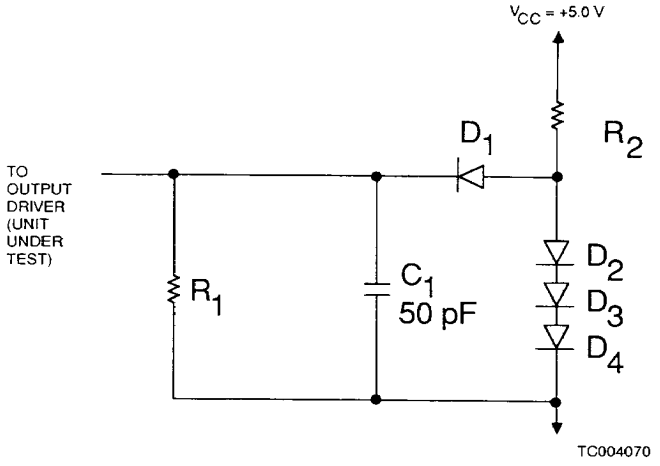
SWITCHING CHARACTERISTICS (Cont'd.)

Miscellaneous Timing Specifications

No.	Parameter Symbol	Parameter Description	Min.	Nom.	Max.	Units
75	SR	Transmit Slew Rate (Note 11)	±20			mV/ns
76	TJT	Transmit Jitter Tolerance			±10	ns
77	TID	Transmit IDLE HIGH Time	1.9		3	μs
78	RJT	Receiver Jitter Tolerance	±125			ns
79	RID	Receiver IDLE Detect	1.3		1.8	μs
80	RTP	Receiver Time Required at Positive Presence Voltage Level	100			ns
81	RTN	Receiver Time Required at Negative Presence Voltage	100			ns
82	RPP	Receiver Protection Time Start of IDLE to Presence Level Detect (See Timing Diagram 8)	19	20	21	μs
84	AB	Abort On No Receive Counter		384		μs
85	JT	Jabber Timer		16		ms
	CF	Crystal Frequency (Note 12)		16		MHz
86	t_{PW}	Master Reset Pulse Width	3			μs

Notes:
1. See Test Circuit for TTL and MOS Output Drivers (See Switching Test Circuit).
2. Differential Heavy Load Specification IEEE 802.3 1BASE5.
3. Rise and Fall Times measured from 0.6 V to 3.6 V ($\overline{TxC}$, $\overline{RxC}$, RxD, and CLK).
4. Rise and Fall Times measured from 0.8 V to 2.0 V ($\overline{CTS}$, $\overline{CDT}$, $\overline{CRS}$, and PL).
5. SLAN pin equals V_{CC} or open circuit for all measurements.
6. Times for all single-ended signals are measured at 1.5-volt points.
7. Times for all differential signals are measured at 50% points.
8. Transition time to be measured from 0 to 2 volts differential.
9. Three-state level of TxL_0-TxL_1 at start of IDLE is defined as 1.1 volt differential.
10. Three-state level of RxL_0-RxL_1 at start of IDLE is defined as 300 mV differential.
11. With Heavy Load = 180 Ω in parallel with series circuit (0.022 μF and 150 Ω).
12. The frequency tolerance will be within +0.01% if a Crystek series resonant crystal, Part Number CY16B with variable load capacitor, or with Crystek MF10 ±0.005% with two-load capacitors (capacitor values to be determined) or equivalent is connected to pins X_1 and X_2. With this connection, the Am7961 shall be capable of obtaining a tolerance of $\overline{TxC}$ period of 1 MHz ±0.1%.

SWITCHING TEST CIRCUIT

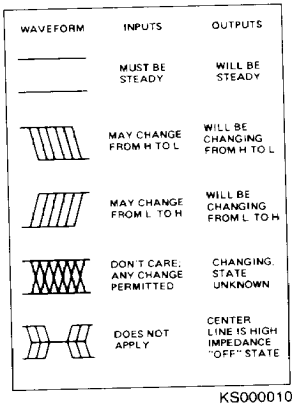


Notes: 1. All diodes are 1N914.
2. All resistors are 0.25 W.
3. Table of Resistor Values:

Outputs	R_1 (Ω)	R_2 (Ω)
MOS	10 K	450
TTL	2.4 K	620

SWITCHING WAVEFORMS

Key to Switching Waveforms



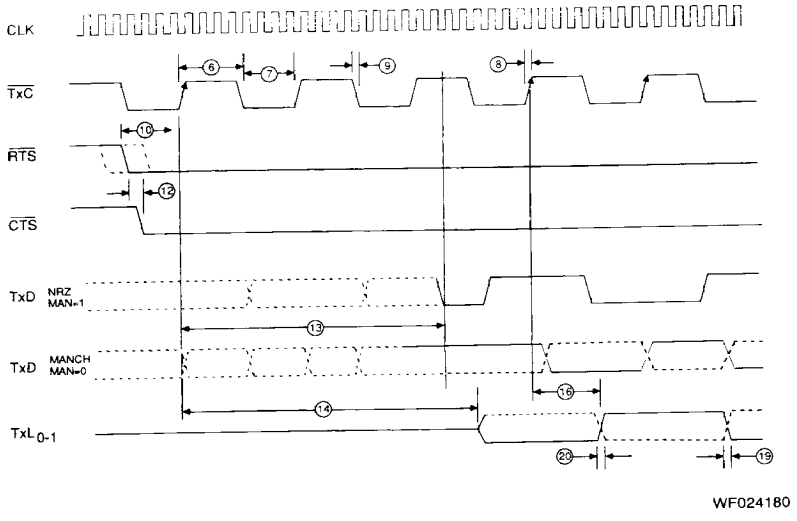


Diagram 1A. Transmit (Beginning of Packet)

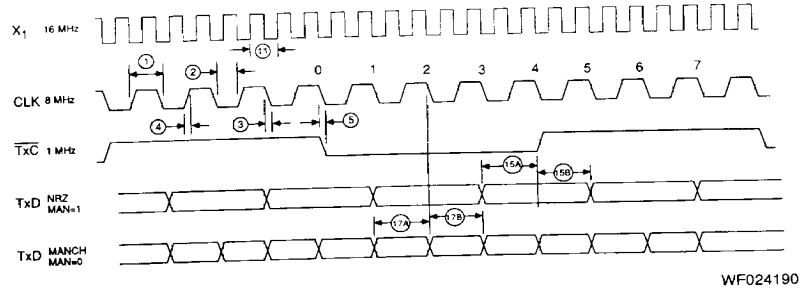


Diagram 1B. Transmit (Beginning of Packet)

SWITCHING WAVEFORMS (Cont'd.)

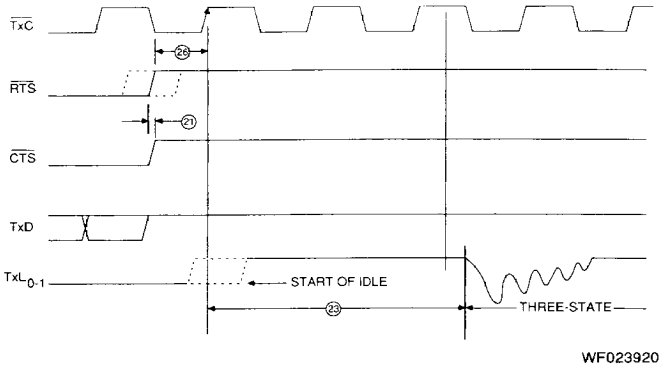


Diagram 2. Transmit (End of Packet)

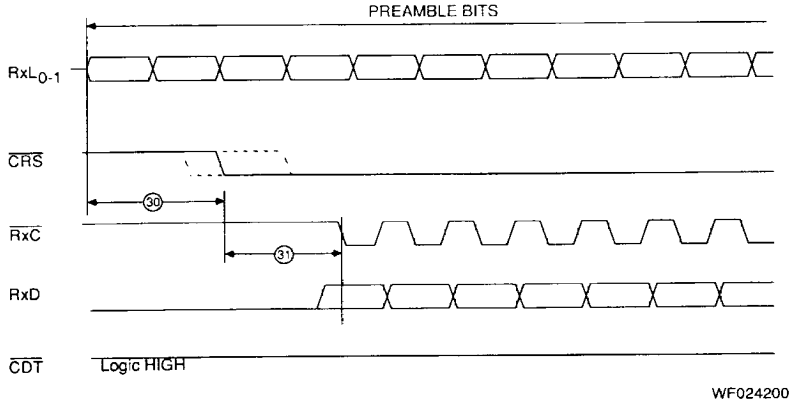


Diagram 3. Receiver (Beginning of Packet)

SWITCHING WAVEFORMS (Cont'd.)

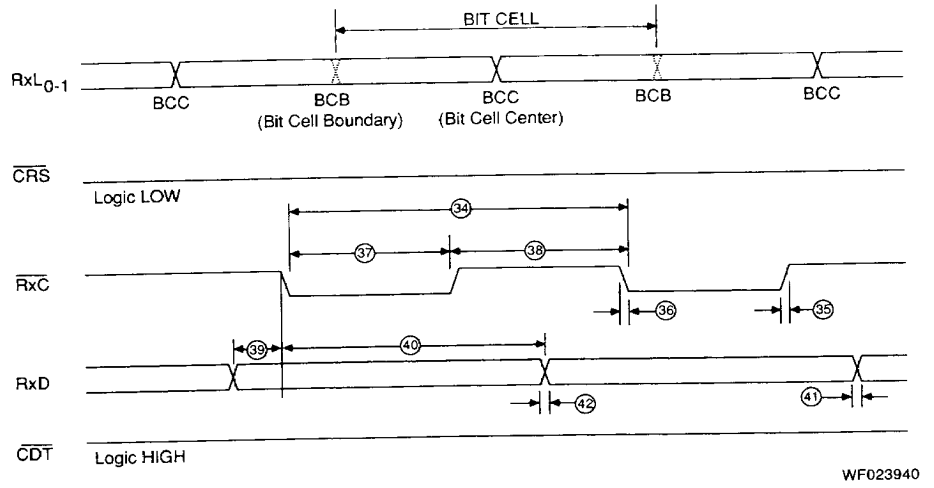
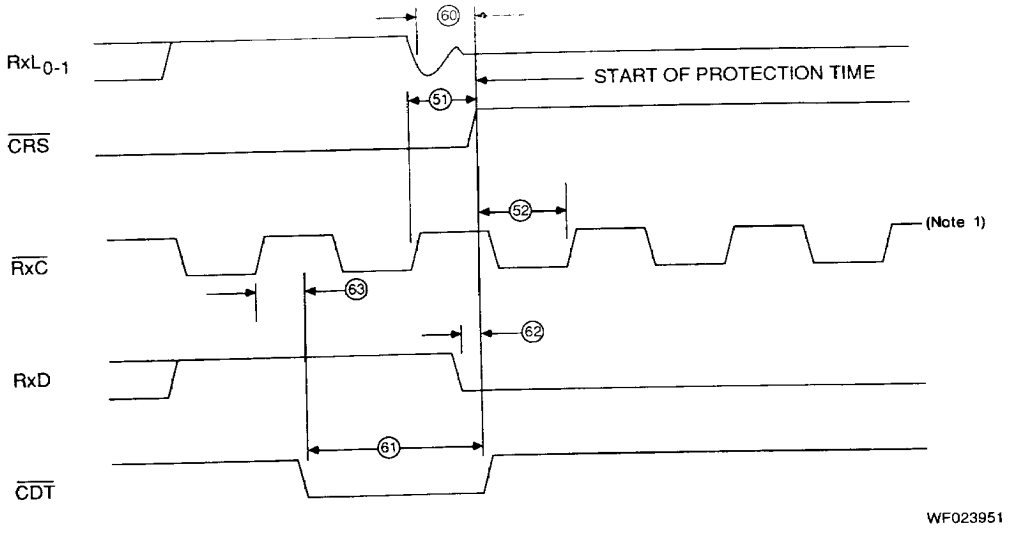


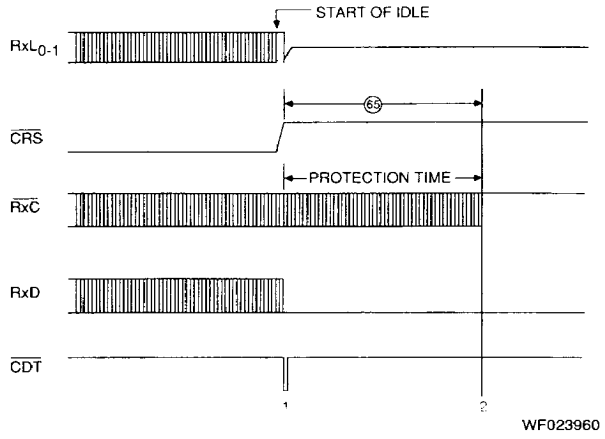
Diagram 4. Receiver (Middle of Packet)



Notes: 1. $\overline{RxC}$ remains until end of protection time (see Diagram 6).

Diagram 5. Receiver (End of Packet)

SWITCHING WAVEFORMS (Cont'd.)



Notes: 1. $\overline{CDT}$ responses to IDLE detection.
2. Receiver circuit enabled for next packet reception.

Diagram 6. Receiver (Start of IDLE)

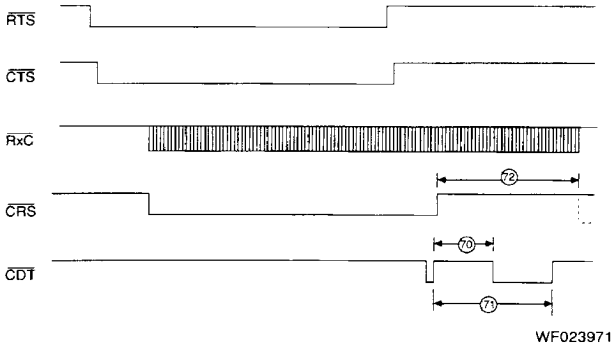
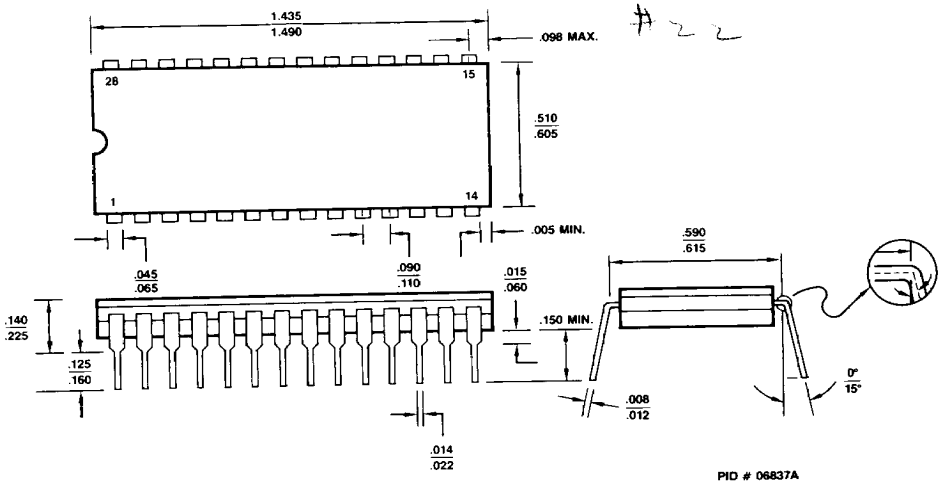


Diagram 7. Loopback Test (PLC/$\overline{LB}$ = 0)

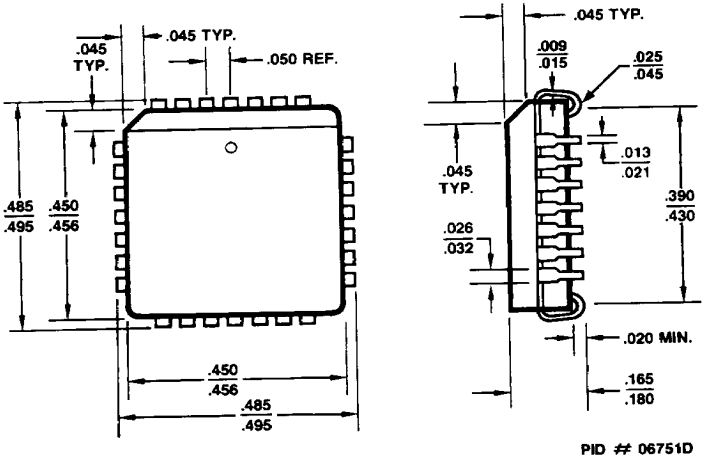
PHYSICAL DIMENSIONS*

CD 028



PID # 06837A

PL 028



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*For reference only.

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