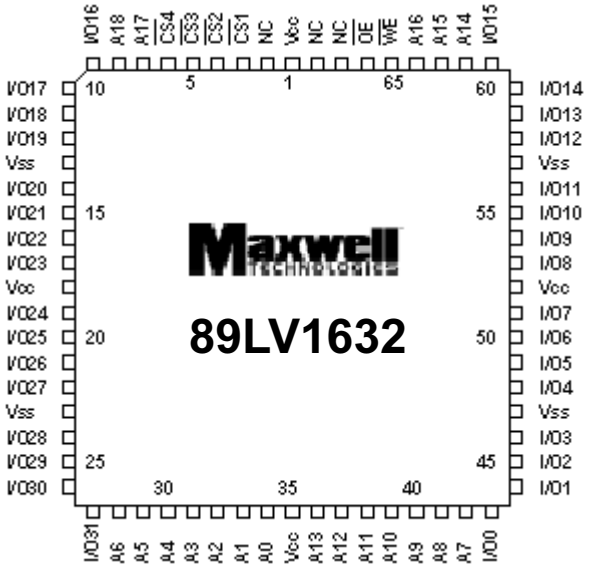
89LV1632
16 Megabit (512K x 32-Bit) Low Voltage MCM SRAM



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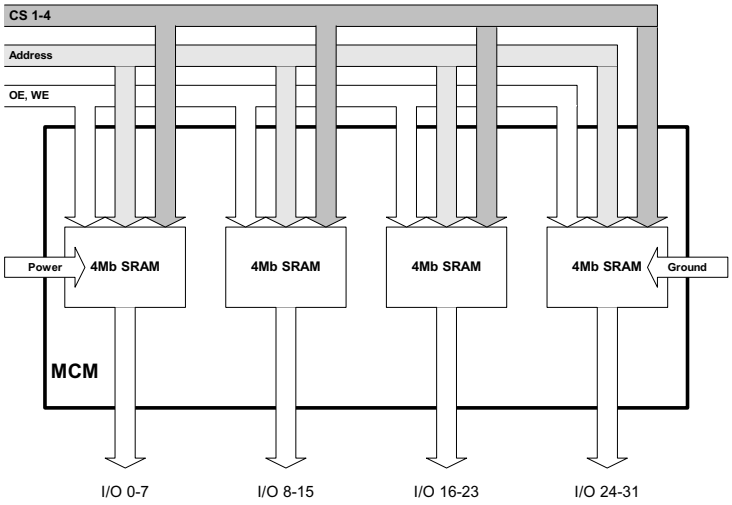

Logic Diagram

FEATURES:

- Four 512k x 8 SRAM die
- RAD-PAK® Technology radiation-hardend against natural space radiation
- Total dose hardness:
  - > 100 krad (Si), depending upon space mission
- Excellent Single Event Effects:
  - SEL > 101MeV-cm^2/mg
  - SEU threshold = 3 MeV-cm^2/mg
  - SEU saturated cross section: 6E-9 cm^2/bit
- Package: 68-pin quad flat package
- Completely static memory - no clock or timing strobe required
- Fast Access Time:
- -20, 25, 30 ns Access Times
- Internal bypass capacitor
- High-speed silicon-gate CMOS Technology
- 3.3 V ± 10% power supply
- Equal address and chip enable access times
- Three-state outputs
- All inputs and outputs are TTL compatible

DESCRIPTION:

Maxwell Technologies' 89LV1632 high-performance 16 Megabit Multi-Chip Module (MCM) Static Random Access Memory features a greater than 100 krad(Si) total dose tolerance, depending upon space mission. The four 4-Megabit SRAM die and bypass capacitors are incorporated into a high-reliable hermetic quad flat-pack ceramic package. With high-performance silicon-gate CMOS technology, the 89LV1632 reduces power consumption and eliminates the need for external clocks or timing strobes. It is equipped with output enable ($\overline{OE}$) and four byte chip enables ($\overline{CS1}$ - $\overline{CS4}$) inputs to allow greater system flexibility. When $\overline{OE}$ input is high, the output is forced to high impedance.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package.It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or a space mission. In a GEO orbit, RAD-PAK® packaging provides greater than 100 krad(Si) total radiation dose tolerance. This product is available with screening up to Maxwell Technologies self-defined Class K.

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TABLE 1. PINOUT DESCRIPTION

PIN	SYMBOL	DESCRIPTION
34-28, 42-36, 62-64, 7, 8	A0-A18	Address Enable
65	$\overline{WE}$	WriteEnable
66	$\overline{OE}$	Output Enable
3-6	$\overline{CS1}$ - $\overline{CS4}$	Chip Enable
43-46, 48-51,53-56, 58-61, 9-12, 14-17, 19-22, 24-27	I/O0-I/O31	Data Input/Output
2, 67, 68	NC	No Connection
1, 18, 35, 52	V_{CC}	+3.3V Power Supply
13, 23, 47, 57	V_{SS}	Ground

TABLE 2. 89LV1632 ABSOLUTE MAXIMUM RATINGS

(VOLTAGE REFERENCED TO V_{SS} = 0V)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Power Supply Voltage Relative to V_{SS}	V_{CC}	-0.5	+4.6	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	-0.5	V_{CC}+0.5	V
Weight			42	Grams
Thermal Resistance	T_{JC}		3.6	˚C/W
Power Dissipation	P_D	--	4.0	W
Operating Temperature	T_A	-55	+125	˚C
Storage Temperature	T_S	-65	+150	˚C

TABLE 3. 89LV1632 RECOMMENDED OPERATING CONDITIONS

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Supply Voltage, (Operating Voltage Range)	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.5 (1)	V
Input Low Voltage	V_{IL}	-0.5 (2)	0.8	V

1. V_{IH} (max) = V_{CC} + 2V ac (pulse width ≤ 10ns) for I ≤ 80 mA.
2. V_{IL} (min) = -2.0V ac; (pulse width ≤ 20 ns) for I ≤ 80 mA.

TABLE 4. 89LV1632 DELTA LIMITS

PARAMETER	VARIATIONL
I_{CC}	±10% of stated value in table 5
I_{SB}	±10% of stated value in table 5
I_{SB1}	±10% of stated value in table 5
I_{LI}	±10% of stated value in table 5

TABLE 5. 89LV1632 DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}	1, 2, 3	-8.0	--	+8.0	uA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, V_{OUT} = V_{SS} to V_{CC}	1, 2, 3	-8.0	--	+8.0	uA
Operating Current : -20 -25 -30	I_{CC}	Min. Cycle, 100% Duty, $\overline{CS}$ = V_{IL}, I_{OUT} = 0 mA V_{IN} = V_{IH} or V_{IL}	1, 2, 3	 - - -	 - - -	 330 320 310	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$= V_{IH}, Min Cycle	1, 2, 3	--	--	240	mA
CMOS Standby Power Supply Current	I_{SB1}	$\overline{CS}$ ≥ V_{CC} - 0.2V, f = 0 MHz, V_{IN} ≥ V_{CC} - 0.2V or V_{IN} < 0.2V	1, 2, 3	--	--	40	mA
Output Low Voltage	V_{OL}	I_{OL} = + 8.0 mA	1, 2, 3	--	--	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	2.4	--	--	V
Input Capacitance[1] $\overline{CS1}$ - $\overline{CS4}$, $\overline{OE}$, $\overline{WE}$ I/O0-7, I/O8-15, I/O16-23, I/O24-31 A0 - A18	C_{IN}	V_{IN} = 0 V	4, 5, 6			 7 28 7 7 32	pF
Output Capacitance[1]	C_{OUT}	$V_{I/O}$ = 0 V	4, 5, 6			8	pF

1. Guaranteed by design.

TABLE 6. 89LV1632 AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	MIN	TYP	MAX	UNITS
Input Pulse Level	0.0	--	3.0	V

TABLE 6. 89LV1632 AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	MIN	TYP	MAX	UNITS
Output Timing Measurement Reference Level	--	--	1.5	V
Input Rise/Fall Time	--	--	3.0	ns
Input Timing Measurement Reference Level	--	--	1.5	V

TABLE 7. 89LV1632 AC CHARACTORISTICS FOR READ CYCLE

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 ˚C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNITS
Read Cycle Time	t_{RC}	9, 10, 11				ns
-20			20	--	--	
-25			25	--	--	
-30			30	--	--	
Address Access Time	t_{AA}	9, 10, 11				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Chip Select Access Time	t_{CO}	9, 10, 11				ns
-20			--	--	20	
-25			--	--	25	
-30			--	--	30	
Output Enable to Output Valid	t_{OE}	9, 10, 11				ns
-20			--	--	10	
-25			--	--	12	
-30			--	--	14	
Chip Enable to Low-Z Output	t_{OLZ}	9, 10, 11				ns
-20			--	3	--	
-25			--	3	--	
-30			--	3	--	
Output Enable to Low-Z Output	t_{LZ}	9, 10, 11				ns
-20			--	0	--	
-25			--	0	--	
-30			--	0	--	
Chip Enable Deselect to High-Z Output	t_{OHZ}	9, 10, 11				ns
-20			--	5	--	
-25			--	6	--	
-30			--	8	--	
Output Enable Deselect to High-Z Output	t_{HZ}	9, 10, 11				ns
-20			--	5	--	
-25			--	6	--	
-30			--	8	--	

TABLE 7. 89LV1632 AC CHARACTORISTICS FOR READ CYCLE

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNITS
Output Hold from Address Change	t_{OH}	9, 10, 11				ns
-20			3	--	--	
-25			5	--	--	
-30			6	--	--	
Chip Select to Power Up Time	T_{PU}	9, 10, 11				ns
-20			--	0	--	
-25			--	0	--	
-30			--	0	--	
Chip Select to Power DownTime	T_{PD}	9, 10, 11				ns
-20			--	10	--	
-25			--	15	--	
-30			--	20	--	

TABLE 8. 89LV1632 FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O PIN	SUPPLY CURRENT
H	X[1]	X[1]	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X[1]	Write	D_{IN}	I_{CC}

1. X = don't care.

TABLE 9. 89LV1632 AC CHARACTORISTICS FOR WRITE CYCLE

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNITS
Write Cycle Time	t_{WC}	9, 10, 11				ns
-20			20	--	--	
-25			25	--	--	
-30			30	--	--	
Chip Select to End of Write	t_{CW}	9, 10, 11				ns
-20			14	--	--	
-25			15	--	--	
-30			17	--	--	
Address Set-up Time	t_{AS}	9, 10, 11				ns
-20			0	--	--	
-25			0	--	--	
-30			0	--	--	

TABLE 9. 89LV1632 AC CHARACTORISTICS FOR WRITE CYCLE

(V_{CC} = 3.3± 10%, T_A = -55 TO +125 °C, UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNITS
Address Valid to End of Write	t_{AW}	9, 10, 11				ns
-20			14	--	--	
-25			15	--	--	
-30			17	--	--	
Write Pulse Width ($\overline{OE}$ High)	t_{WP}	9, 10, 11				ns
-20			14	--	--	
-25			15	--	--	
-30			17	--	--	
Write Pulse Width ($\overline{OE}$ Low)	t_{WP1}	9, 10, 11				ns
-20			20	--	--	
-25			25	--	--	
-30			30	--	--	
Write Recovery Time	t_{WR}	9, 10, 11				ns
-20			0	--	--	
-25			0	--	--	
-30			0	--	--	
Write to Output High-Z	t_{WHZ}	9, 10, 11				ns
-20			--	5	-	
-25			--	5	--	
-30			--	6	--	
Data to Write Time Overlap	t_{DW}	9, 10, 11				ns
-20			9	--	--	
-25			10	--	--	
-30			11	--	--	
Data Hold from Write Time	t_{DH}	9, 10, 11				ns
-20			0	--	--	
-25			0	--	--	
-30			0	--	--	
End Write to Output Low-Z	t_{OW}	9, 10, 11				ns
-20			--	6	--	
-25			--	7	--	
-30			--	8	--	

FIGURE 1. AC TEST LOADS

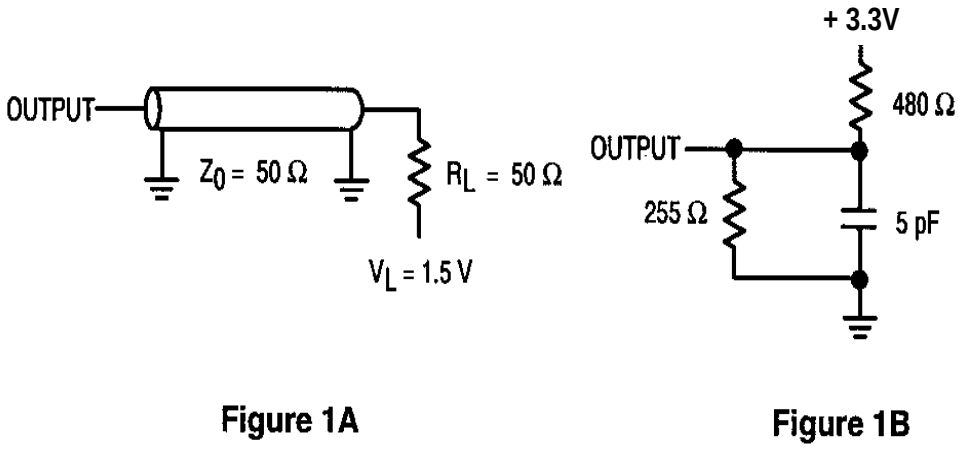


Figure 1A **Figure 1B**

FIGURE 2. TIMING WAVEFORM OF READ CYCLE (1) (ADDRESS CONTROLLED)

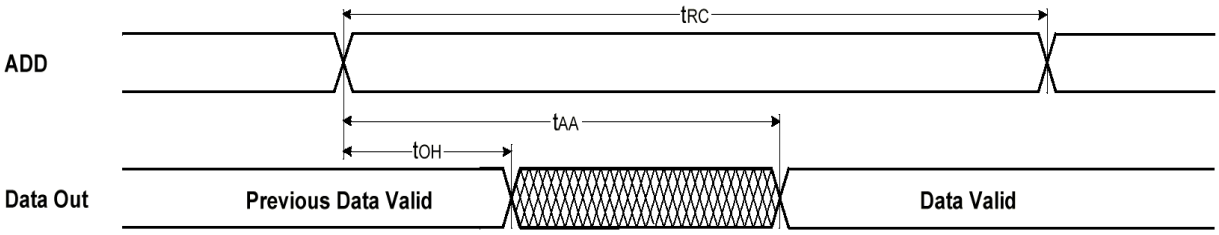
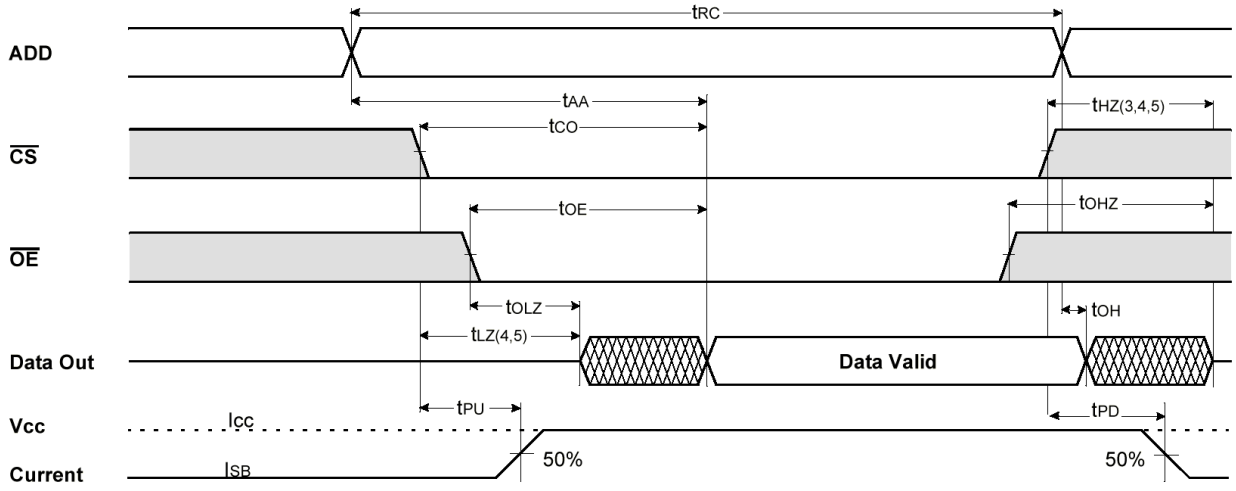


FIGURE 3. TIMING WAVEFORM OF READ CYCLE (2) ($\overline{WE}$ = V_{IH})



1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.

3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage conditions, t_{HZ} (max) is less than t_{LZ} (min) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ = V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

FIGURE 4. TIMING WAVEFORM OF WRITE CYCLE (1) ($\overline{OE}$ CLOCK)

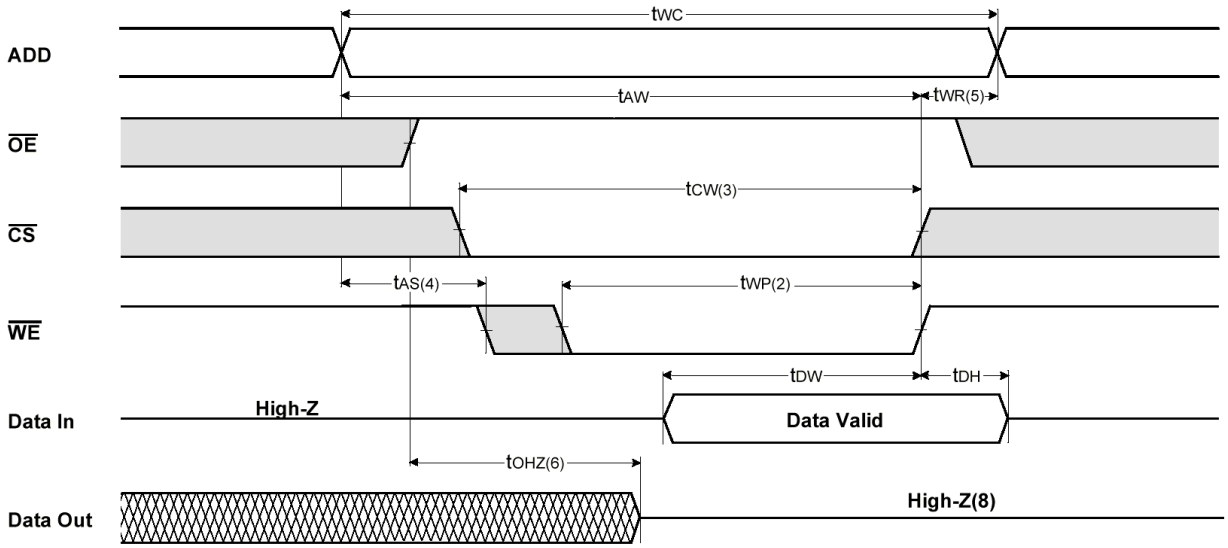


FIGURE 5. TIMING WAVEFORM OF WRITE CYCLE (2) ($\overline{OE}$ LOW FIIXED)

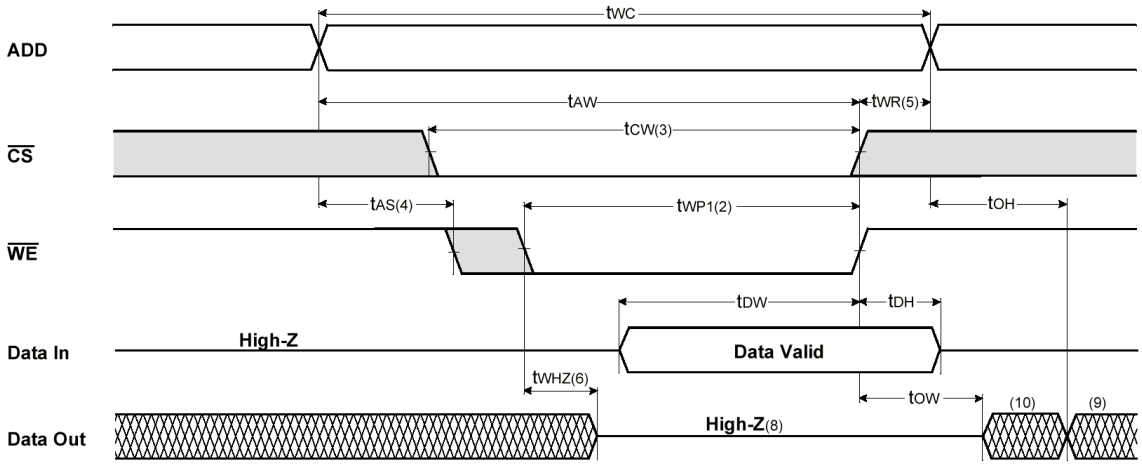
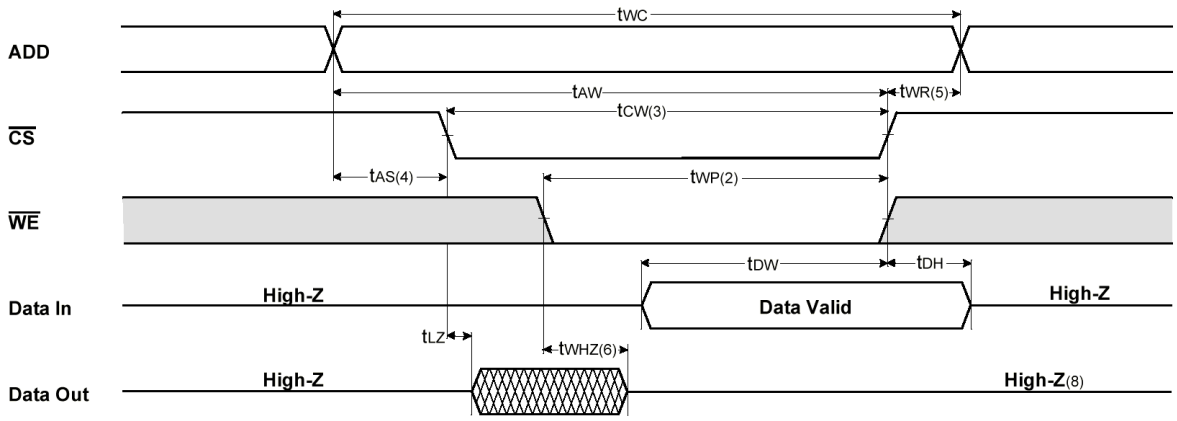
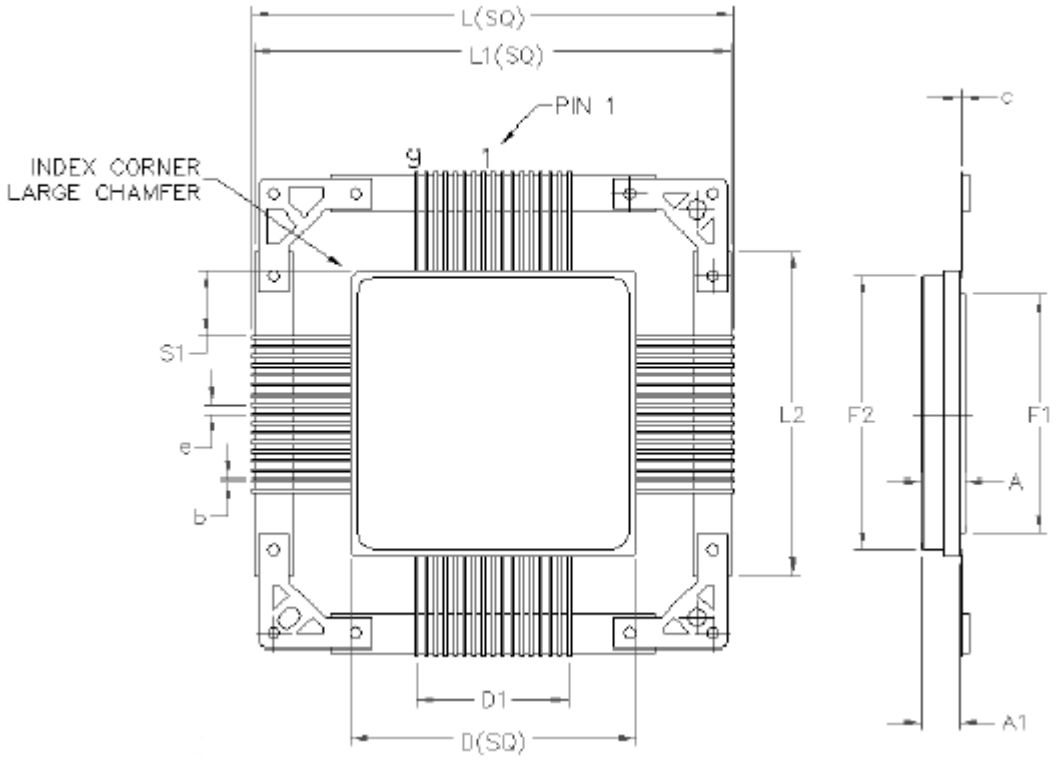


FIGURE 6. TIMING WAVEFORM OF WRITE CYCLE (3) ($\overline{CS}$ CONTROLLED)



1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low. A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization of elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low, I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.



68 PIN RAD-PAK® QUAD FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.206	0.225	0.244
b	0.015	0.017	0.018
c	0.008	0.009	0.12
D	1.479	1.494	1.509
D1		0.800	
e		0.050 BSC	
S1	--	0.339	--
F1	1.239	1.244	1.249
F2	1.429	1.434	1.439
L	2.485	2.510	2.545
L1	2.485	2.500	2.505
L2	1.690	1.700	1.710
A1	0.180	0.195	0.210
N		68	

Note: All dimensions in inches

Important Notice:

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