54AC/74AC138 • 54ACT/74ACT138

1-of-8 Decoder/Demultiplexer

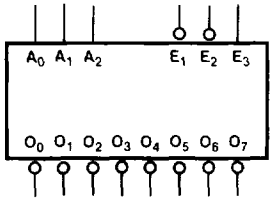
Description

The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

- **Demultiplexing Capability**
- **Multiple Input Enable for Easy Expansion**
- **Active LOW Mutually Exclusive Outputs**
- **Outputs Source/Sink 24 mA**
- **'ACT138 has TTL-Compatible Inputs**

Ordering Code: See Section 6

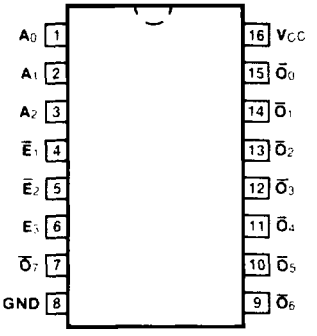
Logic Symbol



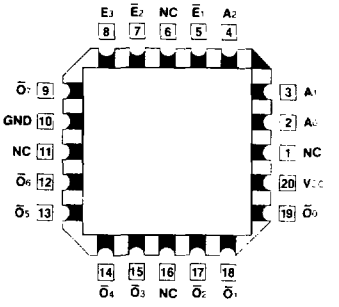
Pin Names

A_0 - A_2	Address Inputs
$\overline{E}_1$ - $\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$ - $\overline{O}_7$	Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

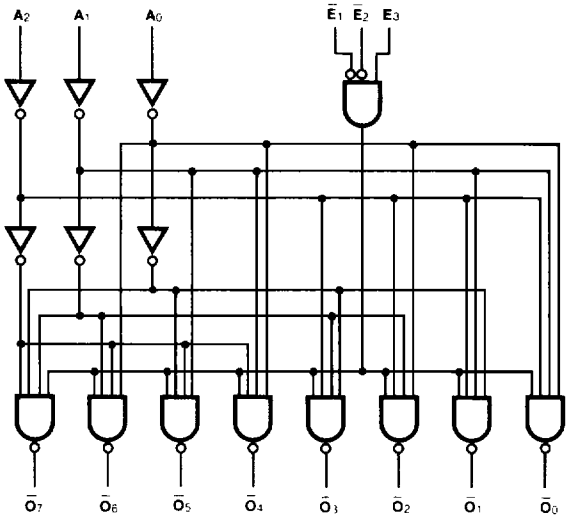
The 'AC/'ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0, A_1, A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O}_0$ - $\overline{O}_7$). The 'AC/'ACT138 features three Enable inputs, two active-LOW ($\overline{E}_1$, $\overline{E}_2$) and one active-HIGH (E_3). All outputs will be HIGH unless $\overline{E}_1$ and $\overline{E}_2$ are LOW and E_3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/'ACT138 devices and one inverter (See Figure a). The 'AC/'ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Truth Table

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

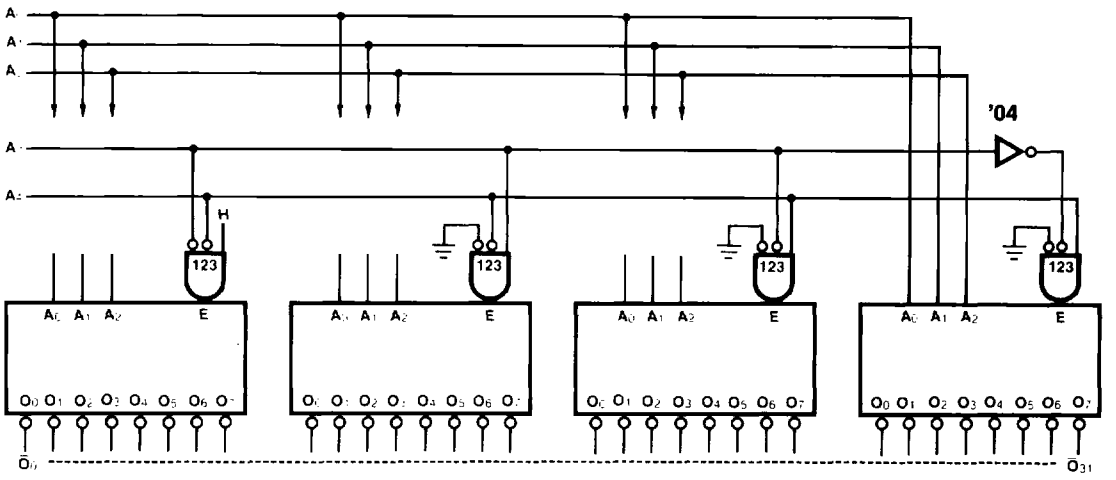
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure a: Expansion to 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT138)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.5 6.5	13.0 9.5	1.0 1.0	16.0 12.0	1.0 1.0	15.0 10.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.0 6.0	12.5 9.0	1.0 1.0	15.0 11.5	1.0 1.0	14.0 10.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	11.0 8.0	15.0 11.0	1.0 1.0	16.5 13.0	1.0 1.0	16.0 12.0	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	3.3 5.0	1.0 1.0	9.5 7.0	13.5 9.5	1.0 1.0	15.5 12.0	1.0 1.0	15.0 10.5	ns	3-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	3.3 5.0	1.0 1.0	11.0 8.0	15.5 11.0	1.0 1.0	17.0 13.5	1.0 1.0	16.5 12.5	ns	3-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	3.3 5.0	1.0 1.0	8.5 6.0	13.0 8.0	1.0 1.0	15.0 11.0	1.0 1.0	14.0 9.5	ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

5

AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay A_n to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	8.0	11.5	1.0	13.5	1.0	12.5	ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	5.0	1.0	7.5	11.5	1.0	12.5	1.0	12.5	ns	3-6
t_{PLH}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	8.0	12.0	1.0	14.0	1.0	13.0	ns	3-6
t_{PHL}	Propagation Delay E_3 to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.0	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	60.0	pF	$V_{CC} = 5.5$ V