

54AC/74AC138 • 54ACT/74ACT138

1-of-8 Decoder/Demultiplexer

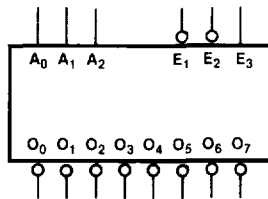
Description

The 'AC/'ACT138 is a high-speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high-speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three 'AC/'ACT138 devices or a 1-of-32 decoder using four 'AC/'ACT138 devices and one inverter.

- Demultiplexing Capability
- Multiple Input Enable for Easy Expansion
- Active LOW Mutually Exclusive Outputs
- Outputs Source/Sink 24 mA
- 'ACT138 has TTL-Compatible Inputs

Ordering Code: See Section 6

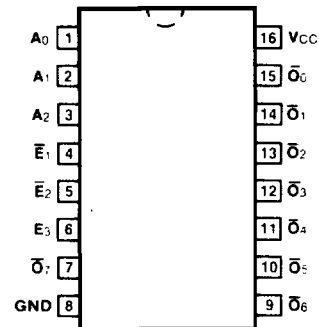
Logic Symbol



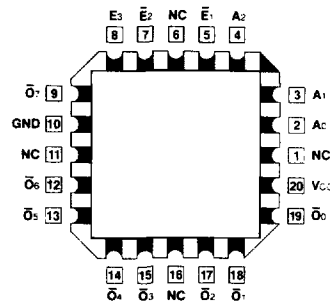
Pin Names

- A₀ - A₂ Address Inputs
- \bar{E}_1 - \bar{E}_2 Enable Inputs
- E₃ Enable Input
- \bar{O}_0 - \bar{O}_7 Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/ACT138 high-speed 1-of-8 decoder/demultiplexer accepts three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provides eight mutually exclusive active-LOW outputs (\bar{O}_0 - \bar{O}_7). The 'AC/ACT138 features three Enable inputs, two active-LOW (\bar{E}_1 , \bar{E}_2) and one active-HIGH (E_3). All outputs will be HIGH unless \bar{E}_1 and \bar{E}_2 are LOW and E_3 is HIGH. This multiple

enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 'AC/ACT138 devices and one inverter (See Figure a). The 'AC/ACT138 can be used as an 8-output demultiplexer by using one of the active LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

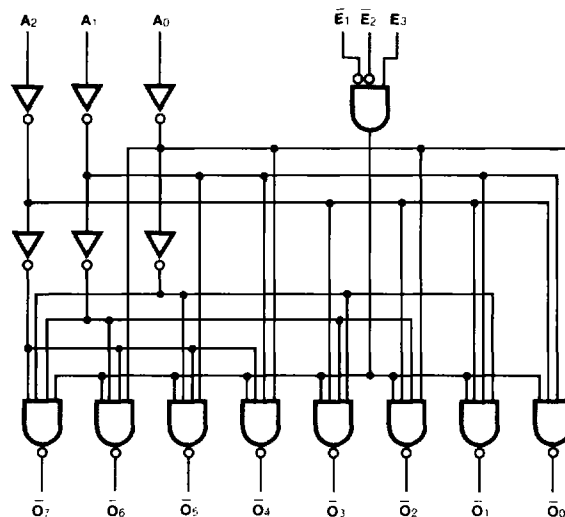
Truth Table

Inputs						Outputs							
\bar{E}_1	\bar{E}_2	E_3	A_0	A_1	A_2	\bar{O}_0	\bar{O}_1	\bar{O}_2	\bar{O}_3	\bar{O}_4	\bar{O}_5	\bar{O}_6	\bar{O}_7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

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H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

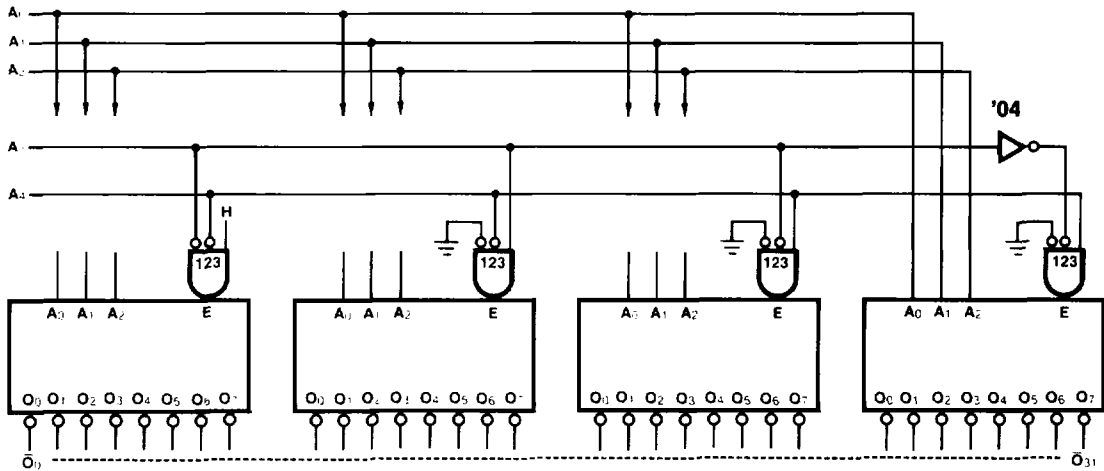
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

AC138 • ACT138

Figure a: Expansion to 1-of-32 Decoding



DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input ('ACT138)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V, V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay An to \bar{O}_n	3.3	1.0	8.5	13.0	1.0	16.0	1.0	15.0	ns	3-6
		5.0	1.0	6.5	9.5	1.0	12.0	1.0	10.5		
tPHL	Propagation Delay An to \bar{O}_n	3.3	1.0	8.0	12.5	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	6.0	9.0	1.0	11.5	1.0	10.5		
tPLH	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	3.3	1.0	11.0	15.0	1.0	16.5	1.0	16.0	ns	3-6
		5.0	1.0	8.0	11.0	1.0	13.0	1.0	12.0		
tPHL	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	3.3	1.0	9.5	13.5	1.0	15.5	1.0	15.0	ns	3-6
		5.0	1.0	7.0	9.5	1.0	12.0	1.0	10.5		
tPLH	Propagation Delay E3 to \bar{O}_n	3.3	1.0	11.0	15.5	1.0	17.0	1.0	16.5	ns	3-6
		5.0	1.0	8.0	11.0	1.0	13.5	1.0	12.5		
tPHL	Propagation Delay E3 to \bar{O}_n	3.3	1.0	8.5	13.0	1.0	15.0	1.0	14.0	ns	3-6
		5.0	1.0	6.0	8.0	1.0	11.0	1.0	9.5		

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
tPLH	Propagation Delay An to \bar{O}_n	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-6
tPHL	Propagation Delay An to \bar{O}_n	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
tPLH	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	5.0	1.0	8.0	11.5	1.0	13.5	1.0	12.5	ns	3-6
tPHL	Propagation Delay \bar{E}_1 or \bar{E}_2 to \bar{O}_n	5.0	1.0	7.5	11.5	1.0	12.5	1.0	12.5	ns	3-6
tPLH	Propagation Delay E3 to \bar{O}_n	5.0	1.0	8.0	12.0	1.0	14.0	1.0	13.0	ns	3-6
tPHL	Propagation Delay E3 to \bar{O}_n	5.0	1.0	6.5	10.5	1.0	12.0	1.0	11.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5 V
C _{PD}	Power Dissipation Capacitance	60.0	pF	V _{CC} = 5.5 V