SYM53C895
PCI-Ultra2 SCSI
I/O Processor with LVDlink
Universal Transceivers

Data Manual
Version 3.0

SCSI LVD/SE

M59983I

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Preface

This manual assumes some prior knowledge of current and proposed SCSI and PCI standards. For background information, please contact:

ANSI
11 West 42nd Street
New York, NY 10036
(212) 642-4900
Ask for document number X3.131-1994 (SCSI-2)

Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
(800) 854-7179 or (303) 7956 (outside U.S.) FAX (303) 397-2740
Ask for document number X3.131-1994 (SCSI-2) or X3.253 *(SCSI-3 Parallel Interface)*

ENDL Publications
14426 Black Walnut Court
Saratoga, CA 95070
(408) 867-6642
Document names: *SCSI Bench Reference, SCSI Encyclopedia, SCSI Tutor*

Prentice Hall
113 Sylvan Avenue
Englewood Cliffs, NJ 07632
(800) 947-7700
Ask for document number ISBN 0-13-796855-8, *SCSI: Understanding the Small Computer System Interface*

Symbios Electronic Bulletin Board
(719) 533-7235

SCSI Electronic Bulletin Board
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Symbios Internet Anonymous FTP Site
ftp.symbios.com (204.131.200.1)
Directory: /pub/symchips/scsi

Symbios World Wide Web Home Page
www.symbios.com/t10

PCI Special Interest Group
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SYM53C8XX Family Programming Guide

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Chapter 1
Introduction

What is Covered in This Manual

This manual provides reference information on the SYM53C895 PCI-SCSI I/O Processor. It is intended for system designers and programmers who are using this device to design a SCSI port for PCI-based personal computers, workstations, or embedded applications.

- This chapter includes general information about the SYM53C895 and other members of the SYM53C8XX family of PCI-SCSI I/O Processors.
- Chapter 2 describes the main functional areas of the chip in more detail, including the interfaces to the SCSI bus and external memory.
- Chapter 3 describes the chip's connection to the PCI bus, including the PCI commands and configuration registers supported.
- Chapter 4 contains the pin diagrams and definitions of each signal.
- Chapter 5 describes each bit in the operating registers, organized by address.
- Chapter 6 defines all of the SCSI SCRIPTS instructions that are supported by the SYM53C895.
- Chapter 7 contains the electrical characteristics and AC timings for the chip.
- The appendixes contain a register summary, a mechanical drawing of the SYM53C895, and several example interface drawings to connect the SYM53C895 to an external ROM.

This data manual assumes the user is familiar with the current and proposed standards for SCSI and PCI. For additional background information on these topics, please refer to the list of reference materials provided in the Preface of this document.

General Description

The SYM53C895 PCI-SCSI I/O Processor brings Ultra2 SCSI performance to host adapter, workstation, and general computer designs, making it easy to add a high-performance SCSI bus to any PCI system. It supports Ultra2 SCSI transfer rates and allows you to increase SCSI connectivity and cable length with Low Voltage Differential (LVD) signaling for SCSI.

The SYM53C895 has a local memory bus for local storage of the device's BIOS ROM in flash memory or standard EPROMs. The SYM53C895 supports Big and Little Endian byte addressing to accommodate a variety of data configurations. The SYM53C895 supports programming of local FLASH memory for updates to BIOS or SCRIPTS programs. The chip is packaged in a 208-pin quad flat pack or a 292-ball BGA. System diagrams showing the connections of the SYM53C895 with an external ROM or flash memory are pictured in Appendix C. A block diagram of the SYM53C895 is pictured in Figure 1-1 on page 1-6.

Symbios LVDlink™ technology is the Symbios implementation of LVD. LVDlink transceivers allow the SYM53C895 to perform single-ended and low voltage differential transfers, and support external high voltage differential transceivers. The SYM53C895 integrates a high-performance SCSI core, a PCI bus master DMA core, and the Sym-

bios SCSI SCRIPTS™ processor to meet the flexibility requirements of SCSI-3 and Ultra2 SCSI standards. It is designed to implement multi-threaded I/O algorithms with a minimum of processor intervention, solving the protocol overhead problems of previous intelligent and non-intelligent adapter designs.

New Features in the SYM53C895

The SYM53C895 is functionally similar to the SYM53C875 PCI-SCSI I/O processor, with added support for Ultra2 SCSI. Some software enhancements, and use of low voltage differential, are needed to enable the chip to transfer data at Ultra2 SCSI transfer rates. Most of the feature enhancements in the SYM53C895 are included to enable the chip to take advantage of Ultra2 SCSI transfer rates.

- Optional 816-byte DMA FIFO supports large block transfers at Ultra2 SCSI speeds. The default FIFO size is 112 bytes.
- Thirty-one levels of SCSI Synchronous Offset increases the pace of synchronous transfers to match Ultra2 SCSI transfer speeds.
- On-chip LVDlink transceivers allow increased connectivity, longer cable length, and improved performance. They also automatically sense the type of device connected to the SCSI bus and switch as needed to single-ended, LVD, or high voltage differential mode (if the chip is connected to external transceivers).
- On-chip SCSI clock quadrupler can achieve 160 MHz frequency with an external 40MHz oscillator.
- Supports Subsystem ID and Subsystem Vendor ID registers in PCI configuration space.
- Support for serial EEPROM interface.

Benefits of LVDlink

The SYM53C895 supports Low Voltage Differential (LVD) for SCSI, a signaling technology that increases the reliability of SCSI data transfers over longer distances than supported by single-ended SCSI. The low current output of LVD allows the I/O transceivers to be integrated directly onto the chip. LVD provides the reliability of high voltage differential SCSI without the added cost of external differential transceivers. Ultra2 SCSI with LVD allows a longer SCSI cable and more devices on the bus, with the same cables defined in the SCSI-3 Parallel Interface standard for Ultra SCSI. LVD provides a long-term migration path to even faster SCSI transfer rates without compromising signal integrity, cable length, or connectivity.

For backward compatibility to existing single-ended devices, the SYM53C895 features universal LVDlink transceivers that can switch between LVD SCSI and single-ended modes. The LVDlink technology also supports high-power differential signaling in legacy systems, when external transceivers are connected to the SYM53C895. This allows the SYM53C895 to be used in both legacy and Ultra2 SCSI applications.

Benefits of Ultra2 SCSI

Ultra2 SCSI is an extension of the SPI-2 draft standard that allows faster synchronous SCSI transfer rates and defines a new physical layer, LVD SCSI, that provides an incremental evolution from SCSI-2 and Ultra SCSI. When enabled, Ultra2 SCSI performs 40 megatransfers per second, which results in approximately double the synchronous transfer rates of Ultra SCSI. The SYM53C895 can perform 16-bit, Ultra2 SCSI synchronous transfers as fast as 80 MB/s. This advantage is most noticeable in heavily loaded systems, or large-block size applications such as video on-demand and image processing.

One advantage of Ultra2 SCSI is that it significantly improves SCSI bandwidth while preserving existing hardware and software investments. The primary software changes required are to enable the chip to perform synchronous negotiations for Ultra2 SCSI rates, and to enable the clock quadrupler. Ultra2 SCSI uses the same connectors as Ultra SCSI, but can operate with longer cables and more devices on the bus. Chapter 2 contains more information on migrating from an Ultra SCSI design to support Ultra2 SCSI.

TolerANT Technology

The SYM53C895 features TolerANT® technology, which includes active negation on the SCSI drivers and input signal filtering on the SCSI receivers. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively driven high rather than passively pulled up by terminators. Active negation is enabled by setting bit 7 in the STEST3 register.

TolerANT receiver technology improves data integrity in unreliable cabling environments, where other devices would be subject to data corruption. TolerANT receivers filter the SCSI bus signals to eliminate unwanted transitions, without the long signal delay associated with RC-type input filters. This improved driver and receiver technology helps eliminate double clocking of data, the single biggest reliability issue with SCSI operations. TolerANT input signal filtering is a built in feature of the SYM53C895 and all Symbios Fast SCSI, Ultra SCSI, and Ultra2 SCSI devices. On the SYM53C895, the user can select a filtering period of 30 or 60 ns, with bit 1 in the STEST2 register.

The benefits of TolerANT include increased immunity to noise when the signal is going high, better performance due to balanced duty cycles, and improved fast SCSI transfer rates. In addition, TolerANT SCSI devices do not cause glitches on the SCSI bus at power up or power down, so other devices on the bus are also protected from data corruption. When it is used with the LVDlink transceivers, TolerANT provides excellent signal quality and data reliability in real world cabling environments. TolerANT is compatible with both the Alternative One and Alternative Two termination schemes proposed by the American National Standards Institute.

SYM53C895 Benefits Summary

SCSI Performance

- Integrated LVDlink universal transceivers
  - Support single ended, LVD, and high voltage differential signals (with external transceivers)
  - Allow greater device connectivity and longer cable length
  - LVDlink transceivers save cost of external differential transceivers
  - Support a long-term performance migration path
- With 816-byte FIFO, chip can burst up to 512 bytes across the PCI bus
- Performs wide, Ultra2 SCSI synchronous transfers as fast as 80 MB/s
- On-chip SCSI clock quadrupler allows the chip to achieve Ultra2 SCSI transfer rates with 40 MHz clock
- Includes 4 KB internal RAM for SCRIPTS instruction storage
- Thirty-one levels of SCSI synchronous offset
- Supports variable block size and scatter/gather data transfers.
- Performs sustained memory-to-memory DMA transfers faster than 47 MB/s (@ 33 MHz)
- Minimizes SCSI I/O start latency
- Performs complex bus sequences without interrupts, including restore data pointers
- Reduces ISR overhead through a unique interrupt status reporting method
- Load and Store SCRIPTS instruction increases performance of data transfers to and from chip registers
- Supports target disconnect and later reconnect with no interrupt to the system processor
- Supports multi-threaded I/O algorithms in SCSI SCRIPTS with fast I/O context switching
- Expanded Register Move instruction supports additional arithmetic capability

PCI Performance

- Complies with PCI 2.1 specification
- 32-bit 33 MHz PCI interface
- Bursts 2, 4, 8, 16, 32, 64, or 128 dwords across PCI bus
- Supports 32-bit word data bursts with variable burst lengths
- Pre-fetches up to 8 dwords of SCRIPTS instructions
- Bursts SCRIPTS op code fetches across the PCI bus
- Performs zero wait-state bus master data bursts faster than 110 MB/s (@ 33 MHz)
- Supports PCI Cache Line Size register
- Supports PCI Write and Invalidate, Read Line, and Read Multiple commands

Integration

- Integrated LVD transceivers
- Full 32-bit PCI DMA bus master
- Can be used as a third-party PCI bus DMA controller by using Memory to Memory Move instructions
- High performance SCSI core
- Integrated SCRIPTS processor

Ease of Use

- Up to one megabyte of add-in memory support for BIOS and SCRIPTS storage
- Direct PCI-to-SCSI connection

- Reduced SCSI development effort
- Compiler-compatible with existing SYM53C7XX and SYM53C8XX family SCRIPTS
- Direct connection to PCI, and SCSI single-ended and differential buses
- Development tools and sample SCSI SCRIPTS available
- Maskable and pollable interrupts
- Wide SCSI, A or P cable, and up to 16 devices supported
- Three programmable SCSI timers: Select/ Reselect, Handshake-to-Handshake, and General Purpose. The time-out period is programmable from 100 µs to greater than 25.6 seconds
- Software for PC-based operating system support
- Support for relative jumps
- SCSI Selected As ID bits for responding with multiple IDs

Flexibility

- Universal LVD transceivers are backward compatible with single-ended or high-power differential devices
- High level programming interface (SCSI SCRIPTS)
- Programs local memory bus FLASH memory
- Big/Little Endian support
- Selectable 112- or 816-byte DMA FIFO for backward compatibility
- Tailored SCSI sequences execute from main system RAM or internal SCRIPTS RAM
- Flexible programming interface to tune I/O performance or to adapt to unique SCSI devices
- Support for changes in the logical I/O interface definition
- Low level access to all registers and all SCSI bus signals
- Fetch, Master, and Memory Access control pins
- Separate SCSI and system clocks
- SCSI clock quadrupler bits enable Ultra2 SCSI transfer rates with a 40 MHz SCSI clock
- Selectable IRQ pin disable bit
- Ability to route system clock to SCSI clock

Reliability

- 2 KV ESD protection on SCSI signals
- Protection against bus reflections due to impedance mismatches
- Controlled bus assertion times (reduces RFI, improves reliability, and eases FCC certification)
- Latch-up protection greater than 150 mA
- Voltage feed through protection (minimum leakage current through SCSI pads)
- More than 25% of pins are power and ground
- Power and ground isolation of I/O pads and internal chip logic
- TolerANT technology provides:
  - Active negation of SCSI Data, Parity, Request, and Acknowledge signals for improved fast SCSI transfer rates
  - Input signal filtering on SCSI receivers improves data integrity, even in noisy cabling environments

Testability

- All SCSI signals accessible through programmed I/O
- SCSI loopback diagnostics
- SCSI bus signal continuity checking
- Support for single-step mode operation
- Test mode (AND tree) to check pin continuity to the board

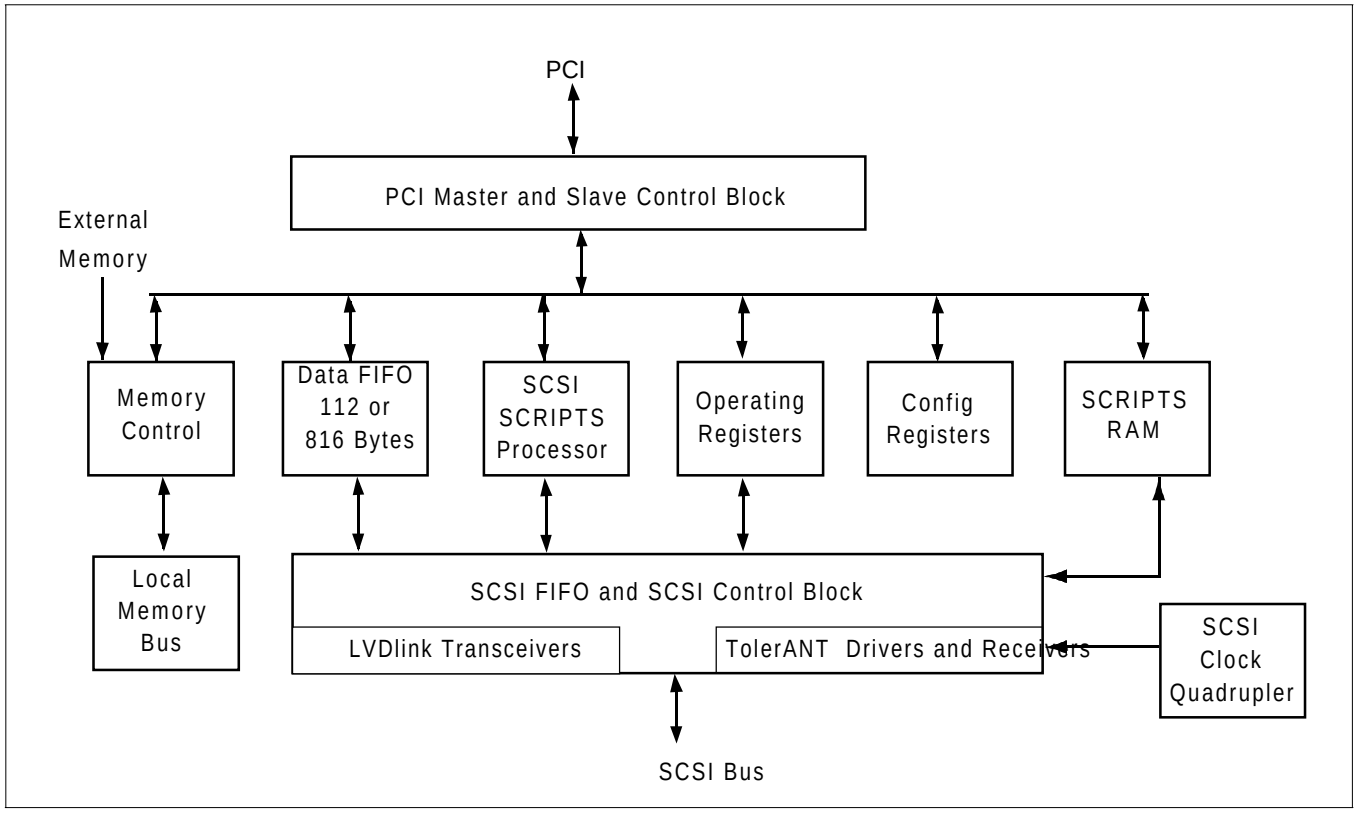

Figure 1-1: SYM53C895 Chip Block Diagram

Chapter 2
Functional Description

The SYM53C895 contains three functional blocks: the SCSI Core, the DMA Core, and the SCRIPTS Processor. Symbios supplies software that supports the SYM53C895 and the entire Symbios product line of SCSI processors and controllers.

SCSI Core

The SCSI core supports an 8- or 16-bit data bus. It supports Ultra2 SCSI synchronous transfer rates up to 80 MB/s on a 16-bit, Low Voltage Differential (LVD) SCSI bus. The SCSI core can be programmed with SCSI SCRIPTS, making it easy to "fine tune" the system for specific mass storage devices or SCSI-3 requirements.

The SCSI core offers low-level register access or a high-level control interface. Like first generation SCSI devices, the SYM53C895 SCSI core can be accessed as a register-oriented device. The ability to sample and/or assert any signal on the SCSI bus can be used in error recovery and diagnostic procedures. In support of loopback diagnostics, the SCSI core may perform a self-selection and operate as both an initiator and a target.

The integrated SCRIPTS processor controls the SYM53C895 SCSI core through a high-level logical interface. Commands controlling the SCSI core are fetched out of the main host memory or local memory. These commands instruct the SCSI core to transfer information, change bus phases and, in general, implement all aspects of the SCSI protocol. The SCRIPTS processor is a special high-speed processor optimized for SCSI protocol.

DMA Core

The DMA core is a bus master DMA device that attaches directly to the industry standard PCI Bus. The DMA core is tightly coupled to the SCSI core through the SCRIPTS processor, which supports uninterrupted scatter/gather memory operations.

The SYM53C895 supports 32-bit memory and automatically supports misaligned DMA transfers. A 112- or 816-byte FIFO allows the SYM53C895 to support 2, 4, 8, 16, 32, 64, or 128 dword bursts across the PCI bus interface.

SCRIPTS Processor

The SCSI SCRIPTS processor allows both DMA and SCSI commands to be fetched from host memory or internal SCRIPTS RAM. Algorithms written in SCSI SCRIPTS control the actions of the SCSI and DMA cores and are executed from 32-bit system RAM or internal SCRIPTS RAM. The SCRIPTS processor executes complex SCSI bus sequences independently of the host CPU.

The SCRIPTS processor can begin a SCSI I/O operation in approximately 500 ns. Algorithms may be designed to tune SCSI bus performance to adjust to new bus device types (such as scanners, communication gateways, etc.), or to incorporate changes in the SCSI-2 or SCSI-3 logical bus definitions without sacrificing I/O performance. SCSI SCRIPTS are hardware independent, so they can be used interchangeably on any host or CPU system bus.

Internal SCRIPTS RAM

The SYM53C895 has 4 KB (1024 x 32 bits) of internal, general purpose RAM. The RAM is designed for SCRIPTS program storage, but is not limited to this type of information. When the chip fetches SCRIPTS instructions or Table Indirect information from the internal RAM, these fetches remain internal to the chip and do not use the PCI bus. Other types of access to the RAM by the SYM53C895 use the PCI bus as if they were external accesses. The MAD5 pin enables the 4K internal RAM, when it is connected to V_{DD} through a 4.7 KΩ resistor. To disable the internal RAM, connect a 4.7 KΩ resistor between the MAD5 pin and V_{SS}.

The RAM can be relocated by the PCI system BIOS anywhere in 32-bit address space. The RAM Base Address register in PCI configuration space contains the base address of the internal RAM. This register is similar to the ROM Base Address register in PCI configuration space. To simplify loading of SCRIPTS instructions, the base address of the RAM will appear in the SCRATCHB register when bit 3 of the CTEST2 register is set. The RAM is byte-accessible from the PCI bus and will be visible to any bus-mastering device on the bus. External accesses to the RAM (that is, by the CPU) follow the same timing sequence as a standard slave register access, except that the target wait states required will drop from 5 to 3.

A complete set of development tools is available for writing custom drivers with SCSI SCRIPTS. For more information on the SCSI SCRIPTS instructions supported by the SYM53C895, see Chapter 6, “Instruction Set of the I/O Processor.”

Designing an Ultra2 SCSI System

Since Ultra2 SCSI is based on existing SCSI standards, it can use existing driver programs as long as the software is able to negotiate for Ultra2 SCSI synchronous transfer rates. Additional software modifications may be needed to take advantage of the new features in the SYM53C895.

In the area of hardware, LVD SCSI is required to achieve Ultra2 SCSI transfer rates and to support the longer cable and additional devices on the bus. All devices on the bus must have LVD SCSI to guarantee Ultra2 SCSI transfer rates. For additional information on Ultra2 SCSI, refer to the SPI-2 working document which is available from the SCSI BBS referenced at the beginning of this manual. Chapter 7 contains Ultra2 SCSI timing information. In addition to the guidelines in the draft standard, make the following software and hardware adjustments to accommodate Ultra2 SCSI transfers:

1. Set the Ultra Enable bit to enable Ultra2 SCSI transfers.
2. Set the TolerANT Enable bit, bit 7 in the STEST3 register, whenever the Ultra Enable bit is set.
3. Do not extend the SREQ/SACK filtering period with STEST2 bit 1. When the Ultra Enable bit is set, the filtering period will be fixed at 8 ns for Ultra2 SCSI or 15 ns for Ultra SCSI, regardless of the value of the SREQ/SACK Filtering bit.
4. Use the SCSI clock quadrupler.

Using the SCSI Clock Quadrupler

The SYM53C895 can quadruple the frequency of a 40 MHz SCSI clock, allowing the system to perform Ultra2 SCSI transfers. This option is user-selectable with bit settings in the STEST1, STEST3, and SCNTL3 registers. At power-on or reset, the quadrupler is disabled and powered down. Follow these steps to use the clock quadrupler:

1. Set the SCLK Quadrupler Enable bit (STEST1, bit 3).
2. Poll bit 5 of the STEST4 register. The SYM53C895 sets this bit as soon as it locks in the 160 MHz frequency. The frequency lockup takes approximately 100 microseconds.
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (STEST3 bit 5)
4. Set the clock conversion factor using the SCF and CCF fields in the SCNTL3 register
5. Set the SCLK Quadrupler Select bit (STEST1, bit 2)
6. Clear the Halt SCSI Clock bit

Prefetching SCRIPTS Instructions

When enabled (by setting the Prefetch Enable bit in the DCNTL register), the prefetch logic in the SYM53C895 fetches 8 dwords of instructions. The prefetch logic automatically determines the maximum burst size that it can perform, based on the burst length as determined by the values in the DMODE register. If the burst size is less than four dwords, the SYM53C895 performs normal instruction fetches. While the SYM53C895 is prefetching SCRIPTS instructions, the PCI Cache Line Size register value does not have any effect and the Read Line, Read Multiple, and Write and Invalidate commands will not be used.

The SYM53C895 may flush the contents of the prefetch buffer under certain conditions, listed below, to ensure that the chip always operates from the most current version of the software. When one of these conditions apply, the contents of the prefetch buffer are flushed automatically.

1. On every Memory Move instruction. The Memory Move instruction is often used to place modified code directly into memory. To make sure that the chip executes all recent modifications, the prefetch buffer flushes its contents and loads the modified code every time an instruction is issued. To avoid inadvertently flushing the prefetch buffer contents, use the No Flush option for all Memory Move operations that do not modify code within the next 8 dwords. For more information on this instruction, refer to Chapter 6.
2. On every Store instruction. The Store instruction may also be used to place modified code directly into memory. To avoid inadvertently flushing the prefetch buffer contents, use the No Flush option for all Store operations that do not modify code within the next 8 dwords.

3. On every write to the DSP.
4. On all Transfer Control instructions when the transfer conditions are met. This is necessary because the next instruction to be executed is not the sequential next instruction in the prefetch buffer.
5. When the Pre-Fetch Flush bit (DCNTL bit 6) is set. The buffer flushes whenever this bit is set. The bit is self-clearing.

Op Code Fetch Burst Capability

Setting the Burst Op Code Fetch Enable bit in the DMODE register (38h) causes the SYM53C895 to burst in the first two dwords of all instruction fetches. If the instruction is a Memory-to-Memory move, the third dword will be accessed in a separate ownership. If the instruction is an indirect type, the additional dword will be accessed in a subsequent bus ownership. If the instruction is a table indirect block move, the SYM53C895 will use two accesses to obtain the four dwords required, in two bursts of two dwords each.

Note: This feature only works if pre-fetching is disabled.

Parallel ROM Interface

The SYM53C895 supports up to one megabyte of external memory in binary increments from 16 KB, to allow the use of expansion ROM for add-in PCI cards. The device also supports flash ROM updates through the add-in interface and the GPIO4 pin (used to control V_{PP}, the power supply for programming external memory). This interface is designed for low-speed operations such as downloading instruction code from ROM; it is not intended for dynamic activities such as executing instructions.

System requirements include the SYM53C895, two or three external 8-bit address holding registers (HCT273 or HCT374), and the appropriate memory device. The 4.7 KΩ resistors on the memory address/data (MAD) bus require HC or HCT external components to be used. If in-system flash ROM updates are required, a 7406 (high voltage open collector inverter), an MTD4P05, and several passive components are also needed. The memory size and speed is determined by pull-up/pull-down configuration on the 8-bit bidirectional memory bus at power up. The SYM53C895 senses this bus shortly after the release of the Reset signal and configures the ROM Base Address register and the memory cycle state machines for the appropriate conditions.

The SYM53C895 supports a variety of sizes and speeds of expansion ROM, using pull-up and pull-down resistors on the MAD(3-0) pins. The encoding of pins MAD(3-1) allows the user to define how much external memory is available to the SYM53C895. Table 2-1 shows the memory space associated with the possible values of MAD(3-1). The MAD(3-1) pins are fully defined in Chapter 4, “Signal Descriptions.” Appendix C shows an example set of interface drawings.

Table 2-1: External Memory Support

MAD(3-1)	Available Memory Space
000	16 KB
001	32 KB
010	64 KB
011	128 KB
100	256 KB
101	512 KB
110	1024 KB
111	no external memory present

To use one of the configurations mentioned above in a host adapter board design, put 4.7 KΩ pull-up and pull-down resistors on the appropriate MAD pins, corresponding to the available memory space. For example, to connect to a 32 KB external ROM, use pull-downs on MAD(3) and MAD(2) and a pull-up on MAD(1).

Note: The SYM53C875 contains internal pull-ups on the MAD bus. The SYM53C895 requires external resistors to pull up the MAD bus to V_{DD}.

The SYM53C895 allows the system to determine the size of the available external memory using the Expansion ROM Base Address register in PCI configuration space. For more information on how this works, refer to the PCI specification or the Expansion ROM Base Address register description in Chapter 3.

MAD(0) is the slow ROM pin. When pulled down, it enables two extra clock cycles of data access time to allow use of slower memory devices.

The external memory interface also supports updates to flash memory. The 12 volt power supply for flash memory, V_{PP}, is enabled and disabled with the GPIO4 pin and the GPIO4 control bit. For more information on the GPIO4 pin, refer to Chapter 4, "Signal Descriptions."

Serial EEPROM Interface

The SYM53C895 implements an interface which allows attachment of a serial EEPROM device to the GPIO0 and GPIO1 pins. Four different modes of operation are possible; each one relates to different values for the serial EEPROM interface, the Subsystem ID Register, and the Subsystem Vendor ID register. The modes are programmable through the MAD6 and MAD7 pins, which are sampled at power-up or hard reset.

Mode A: 4.7 KΩ pull-ups on MAD6 and MAD7

In this mode, GPIO0 is the serial data signal (SDA) and GPIO1 is the serial clock signal (SCL). Certain data in the serial EEPROM is automatically loaded into chip registers at power-up or hard reset.

The format of the serial EEPROM data is defined in Table 2-2. If the EEPROM is not present, or the checksum fails, the Subsystem ID and Subsystem Vendor ID registers read back all zeroes. At power-up or hard reset, only five bytes are loaded into the chip from locations 00h through 04h.

Table 2-2: Mode A Serial EEPROM Data Format

Byte	Description
00h	Subsystem Vendor ID, LSB. This byte is loaded into the least significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
01h	Subsystem Vendor ID, MSB. This byte is loaded into the most significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
02h	Subsystem ID, LSB. This byte is loaded into the least significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
03h	Subsystem ID, MSB. This byte is loaded into the most significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
04h	Checksum. This 8-bit checksum is formed by adding, bytewise, each byte contained in locations 00h-03h to the seed value 55h, and then taking the 2's compliment of the result.
05h - FFh	Reserved
100h-EOM	User Data

Mode B: 4.7 KΩ pull-down on MAD6, 4.7 KΩ pull-up on MAD7

In this mode, GPIO0 and GPIO1 are each defined as either the serial data signal (SDA) or the serial clock signal (SCL), since both pins are controlled through software.

No data is automatically loaded into chip registers at power-up or hard reset. The Subsystem ID register and Subsystem Vendor ID registers are read/write, in violation of the PCI specification, with a default value of all zeroes.

Mode C: 4.7 KΩ pull-downs on MAD6 and MAD7

In this mode, GPIO1 is the serial data signal (SDA) and GPIO0 is the serial clock signal (SCL). Certain data in the serial EEPROM is automatically loaded into chip registers at power-up or hard reset.

The format of the serial EEPROM data is defined in Table 2-3. If the EEPROM is not present, or the checksum fails, the Subsystem ID and Subsystem Vendor ID registers read back all zeroes. At power-up or hard reset, only five bytes are loaded into the chip from locations FBh through FFh.

Table 2-3: Mode C Serial EEPROM Data Format

Byte	Description
00h - FAh	User Data
FBh	Subsystem Vendor ID, LSB. This byte is loaded into the least significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
FCh	Subsystem Vendor ID, MSB. This byte is loaded into the most significant byte of the Subsystem Vendor ID register in PCI configuration space at chip power-up or hard reset.
FDh	Subsystem ID, LSB. This byte is loaded into the least significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
FEh	Subsystem ID, MSB. This byte is loaded into the most significant byte of the Subsystem ID register in PCI configuration space at chip power-up or hard reset.
FFh	Checksum. This 8-bit checksum is formed by adding, bytewise, each byte contained in locations FBh-FEh to the seed value 55h, and then taking the 2's compliment of the result.
100h-EOM	User Data

Mode D: 4.7 KΩ pull-up on MAD6, 4.7 KΩ pull-down on MAD7

This is a reserved mode and should not be used. It may be redefined in future devices.

PCI Cache Mode

The SYM53C895 supports the PCI specification for an 8-bit Cache Line Size register located in PCI configuration space. The Cache Line Size register provides the ability to sense and react to non-aligned addresses corresponding to cache line boundaries. In conjunction with the Cache Line Size register, the PCI commands Read Line, Read Multiple, and Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands. For more information on PCI cache mode operations, refer to Chapter 3, "PCI Functional Description."

Big and Little Endian Support

The SYM53C895 supports both Big and Little Endian byte ordering through pin selection. In Big Endian mode, the first byte of an aligned SCSI-to-PCI transfer will be routed to lane three and succeeding transfers will be routed to descending lanes. This mode of operation also applies to data transfers over the add-in ROM interface. The byte of data accessed at location 0000h from memory is routed to lane three, and the data at location 0003h is routed to byte lane 0. In Little Endian mode, the first byte of an aligned SCSI to PCI transfer will be routed to lane zero and succeeding transfers will be routed to ascending lanes. This mode of operation also applies to the add-in ROM interface. The byte of data accessed at location 0000h from memory is routed to lane zero, and the data at location 0003h is routed to byte lane 3.

The Big_Lit pin gives the SYM53C895 the flexibility of operating with either Big or Little Endian byte orientation. Internally, in either mode, the actual byte lanes of the DMA FIFO and registers are not modified. The SYM53C895 supports slave accesses in Big or Little Endian mode.

When a dword is accessed, no repositioning of the individual bytes is necessary since dwords are addressed by the address of the least significant byte. SCRIPTS always uses dwords in 32-bit systems, so compatibility is maintained between systems using different byte orientations. When less than a dword is accessed, individual bytes must be repositioned. Internally, the SYM53C895 adjusts the byte control logic of the DMA FIFO and register decodes to access the appropriate byte lanes. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Big and Little Endian mode selection has the most effect on individual byte access. Internally, the SYM53C895 adjusts the byte control logic of the DMA FIFO and register decodes to enable the appropriate byte lane. The registers will always appear on the same byte lane, but the address of the register will be repositioned.

Data to be transferred between system memory and the SCSI bus always starts at address zero and continues through address ‘n’ - there is no byte ordering in the chip. The first byte in from the SCSI bus goes to address 0, the second to address 1, etc. Going out onto the SCSI bus, address zero is the first byte out on the SCSI bus, address 1 is the second byte, etc. The only difference is that in a Little Endian system, address 0 will be on byte lane 0, and in Big Endian mode address 0 will be on byte lane 3.

Correct SCRIPTS will be generated if the SCRIPTS compiler is run on a system that has the same byte ordering as the target system. Any SCRIPTS patching in memory must patch the instruction with the byte ordering that the SCRIPTS processor expects.

Software drivers for the SYM53C895 should access registers by their logical name (that is, SCNTL0) rather than by their address. The logical name should be equated to the register’s Big Endian address in Big Endian mode (SCNTL0 = 03h), and its Little Endian address in Little Endian Mode (SCNTL0 = 00h). This way, there is no change to the software when moving from one mode to the other; only the equate statement setting the operating modes needs to be changed.

Addressing of registers from within a SCRIPTS instruction is independent of bus mode. Internally, the SYM53C895 always operates in Little Endian mode.

Loopback Mode

The SYM53C895 loopback mode allows testing of both initiator and target functions and, in effect, lets the chip communicate with itself. When the Loopback Enable bit is set in the STEST1 register, the SYM53C895 allows control of all SCSI signals, whether the SYM53C895 is operating in initiator or target mode. For more information on this mode of operation, refer to the *Symbios PCI-SCSI Programming Guide*.

Parity Options

The SYM53C895 implements a flexible parity scheme that allows control of the parity sense, allows parity checking to be turned on or off, and has the ability to deliberately send a byte with bad parity over the SCSI bus to test parity error recovery procedures. Table 2-4 defines the bits that are involved in parity control and observation.
Table 2-5 describes the parity control function of the Enable Parity Checking and Assert SCSI Even Parity bits in the SCNTL0 register. Table 2-6 describes the options available when a parity error occurs.

Table 2-4: Bits Used for Parity Control and Generation

Bit Name	Location	Description
Assert SATN/ on Parity Errors	SCNTL0, Bit 1	Causes the SYM53C895 to automatically assert SATN/ when it detects a parity error while operating as an initiator.
Enable Parity Checking	SCNTL0, Bit 3	Enables the SYM53C895 to check for parity errors. The SYM53C895 checks for odd parity.
Assert Even SCSI Parity	SCNTL1, Bit 2	Determines the SCSI parity sense generated by the SYM53C895 to the SCSI bus.
Disable Halt on SATN/ or a Parity Error (Target Mode Only)	SCNTL1, Bit 5	Causes the SYM53C895 not to halt operations when a parity error is detected in target mode.
Enable Parity Error Interrupt	SIEN0, Bit 0	Determines whether the SYM53C895 will generate an interrupt when it detects a SCSI parity error.
Parity Error	SIST0, Bit 0	This status bit is set whenever the SYM53C895 has detected a parity error on the SCSI bus.
Status of SCSI Parity Signal	SSTAT0, Bit 0	This status bit represents the active high current state of the SCSI SDP0 parity signal.
SCSI SDP1 Signal	SSTAT2, Bit 0	This bit represents the active high current state of the SCSI SDP1 parity signal.
Latched SCSI Parity	SSTAT 2, Bit 3 and SSTAT1, Bit 3	These bits reflect the SCSI odd parity signal corresponding to the data latched into the SIDL register
Master Parity Error Enable	CTEST4, Bit 3	Enables parity checking during master data phases.
Master Data Parity Error	DSTAT, Bit 6	Set when the SYM53C895 as a master detects that a target device has signalled a parity error during a data phase.
Master Data Parity Error Interrupt Enable	DIEN, Bit 6	By clearing this bit, a Master Data Parity Error will not cause IRQ/ to be asserted, but the status bit will be set in the DSTAT register.
Enable Parity Error Response	Command, bit 6	Parity checking and parity error reporting are enabled on the PCI bus.

Table 2-5: SCSI Parity Control

EPC	AESP	Description
0	0	Will not check for parity errors. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
0	1	Will not check for parity errors. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.
1	0	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts odd parity when sending SCSI data.
1	1	Checks for odd parity on SCSI data received. Parity is generated when sending SCSI data. Asserts even parity when sending SCSI data.

Key:
EPC = Enable Parity Checking (bit 3 SCNTL0)
ASEP = Assert SCSI Even Parity (bit 2 SCNTL1)

This table only applies when the Enable Parity Checking bit is set.

Table 2-6: SCSI Parity Errors and Interrupts

DHP	PAR	Description
0	0	Will halt when a parity error occurs in target or initiator mode and will NOT generate an interrupt.
0	1	Will halt when a parity error occurs in target mode and will generate an interrupt in target or initiator mode.
1	0	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will not be generated.
1	1	Will not halt in target mode when a parity error occurs until the end of the transfer. An interrupt will be generated.

Key: DHP = Disable Halt on SATN/ or Parity Error (bit 5 SCNTL1) PAR = Parity Error (bit 0 SIEN0)

DMA FIFO

The DMA FIFO is 4-bytes wide and 28 or 204 transfers deep. The DMA FIFO is illustrated in Figure 2-1. To assure compatibility with older products in the SYM53C8XX family, the user may set the DMA FIFO size to 112 bytes by clearing the DMA FIFO Size bit, bit 5 in the CTEST5 register.

The 816-byte FIFO size is related to the SYM53C895 FIFO architecture. It does not reflect any specific system design parameters or expectations.

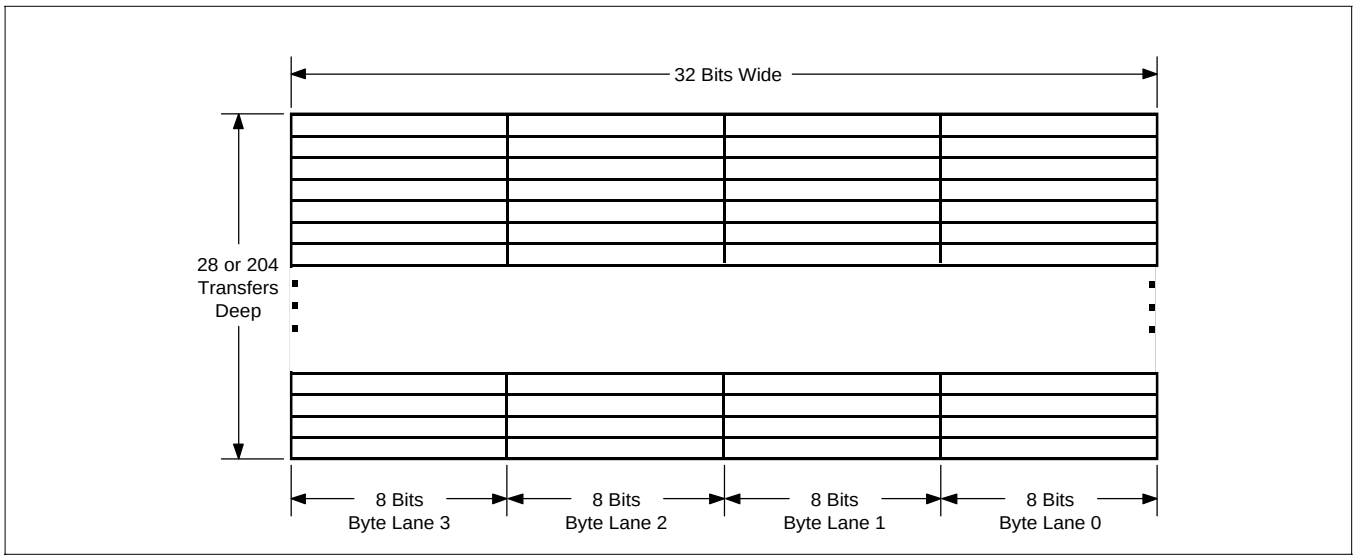

Figure 2-1: DMA FIFO Sections

Data Paths

The data path through the SYM53C895 is dependent on whether data is being moved into or out of the chip, and whether SCSI data is being transferred asynchronously or synchronously.

Figure 2-2 shows how data is moved to/from the SCSI bus in each of the different modes.

The following steps determine if any bytes remain in the data path when the chip halts an operation:

Asynchronous SCSI Send

1. If the DMA FIFO size is set to 112 bytes, look at the DFIFO and DBC registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 112.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the CTEST5 register), subtract the 10 least significant bits of the DBC register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits 1-0 in the CTEST5 register and bits 7-0 of the DMA FIFO register. AND the result with 3FFh for a byte count between 0 and 816.

2. Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODL register is full, respectively. Checking this bit also reveals bytes left in the SODL register from a Chained Move operation with an odd byte count.

Synchronous SCSI Send

1. If the DMA FIFO size is set to 112 bytes, look at the DFIFO and DBC registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between zero and 112.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the CTEST5 register), subtract the 10 least significant bits of the DBC register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits 1-0 in the CTEST5 register and bits 7-0 of the DMA FIFO register. AND the result with 3FFh for a byte count between 0 and 816.

2. Read bit 5 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODL register. If bit 5 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODL register is full, respectively. Checking this bit also reveals bytes left in the SODL register from a Chained Move operation with an odd byte count.

3. Read bit 6 in the SSTAT0 and SSTAT2 registers to determine if any bytes are left in the SODR register. If bit 6 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte in the SODR register is full, respectively.

Asynchronous SCSI Receive

1. If the DMA FIFO size is set to 112 bytes, look at the DFIFO and DBC registers and calculate if there are bytes left in the DMA FIFO. To make this calculation, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 112.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the CTEST5 register), subtract the 10 least significant bits of the DBC register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits 1-0 in the CTEST5 register and bits 7-0 of the DMA FIFO register. AND the result with 3FFh for a byte count between 0 and 816.

2. Read bit 7 in the SSTAT0 and SSTAT2 register to determine if any bytes are left in the SIDL register. If bit 7 is set in the SSTAT0 or SSTAT2, then the least significant byte or the most significant byte is full, respectively.

3. If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCNTL2, bit 0) to determine whether a byte is left in the SWIDE register.

Synchronous SCSI Receive

1. If the DMA FIFO size is set to 112 bytes, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register. AND the result with 7Fh for a byte count between 0 and 112.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the CTEST5 register), subtract the 10 least significant bits of the DBC register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits 1-0 in the CTEST5 register and bits 7-0 of the DMA FIFO register. AND the result with 3FFh for a byte count between 0 and 816.

2. Read bits 7-4 of the SSTAT1 register and bit 4 of the SSTAT2 register, the binary representation of the number of valid bytes in the SCSI FIFO, to determine if any bytes are left in the SCSI FIFO.
3. If any wide transfers have been performed using the Chained Move instruction, read the Wide SCSI Receive bit (SCNTL2, bit 0) to determine whether a byte is left in the SWIDE register.

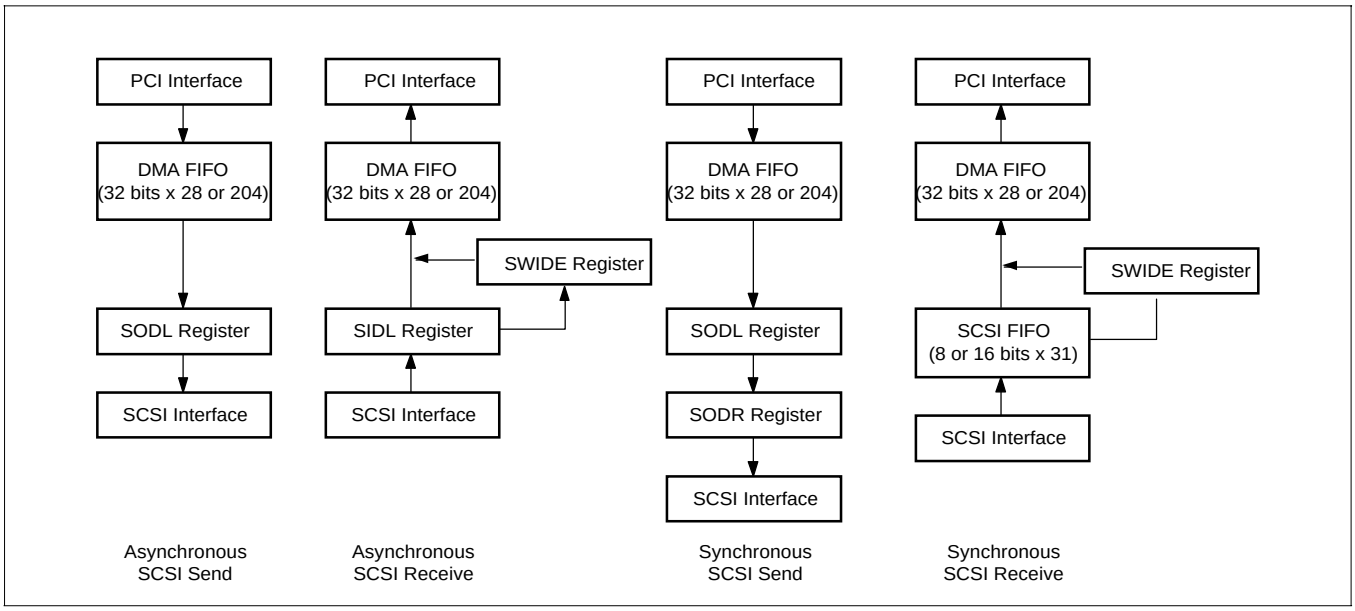

Figure 2-2: SYM53C895 Host Interface Data Paths

SCSI Bus Interface

The SYM53C895 performs single-ended and low voltage differential (LVD) transfers, and supports traditional (high-power) differential operation when the chip is connected to external high-power differential transceivers.

To support LVD SCSI, all SCSI data and control signals have a positive and a negative signal line, as in high voltage differential. In single-ended and high voltage differential operation, the negative signals perform the SCSI data and control function. In high voltage differential mode, the positive signals provide directional control and in single-ended mode they are virtual ground drivers. TolerANT technology provides signal filtering at the inputs of SREQ/ and SACK/ to increase immunity to signal reflections.

LVDlink Technology

To support greater device connectivity and a longer SCSI cable, the SYM53C895 features LVDlink technology, the Symbios implementation of LVD SCSI. LVDlink transceivers provide the inherent reliability of differential SCSI, and a long-term migration path of faster SCSI transfer rates.

LVDlink technology is based on current drive; its low output current reduces the power needed to drive the SCSI bus, so that the I/O drivers can be integrated directly onto the chip. This reduces the cost and complexity compared to traditional (high power) differential designs. LVDlink lowers the amplitude of noise reflections and allows higher transmission frequencies.

The Symbios LVDlink transceivers operate in LVD and single-ended modes. They allow the chip to detect a high voltage differential signal when the chip is connected to external high voltage differential transceivers. The SYM53C895 automatically detects which type of signal is connected, based on voltage detected by the DIFFSENS pin. Bits 7 and 6 of the STEST4 register contain the encoded value for the type of signal that is detected (LVD, single-ended, or high voltage differential). Please see the STEST4 register description for encoding and other bit information.

High Voltage Differential Mode(HVD)

To maintain backward compatibility with legacy systems, the SYM53C895 can operate in high voltage differential mode (when the chip is connected to external differential transceivers). In high voltage differential mode, the SD+ (15-0), SDP+ (1-0), REQ+, ACK+, RST+, BSY+, and SEL+ signals control the direction of external differential-pair transceivers. The SYM53C895 is placed in differential mode by setting the DIF bit, bit 5 of the STEST2 register (4Eh). Setting this bit tri-states the BSY-, SEL-, and RST- pads so they can be used as pure input pins. In addition to the standard SCSI lines, the following signals are used by the SYM53C895 during high voltage differential operation:

Signal	Function
BSY+, SEL+, RST+	Active high signals used to enable the differential drivers as outputs for SCSI signals BSY-, SEL-, and RST-, respectively
SD+(15-0), SDP+(1-0)	Active high signals used to control direction of the differential drivers for SCSI data and parity lines, respectively
ACK+	Active high signal used to control direction of the differential driver for initiator group signals ATN- and ACK-
REQ+	Active high signal used to control direction of the differential drivers for target group signals MSG-, C/D-, I/O- and REQ-/
DIFFSENS	Input to the SYM53C895 used to detect the voltage level of a SCSI signal to determine whether it is a single-ended, LVD, or high-power differential signal. The result is displayed in STEST4 bits 7-6.

In the differential wiring diagram example shown in Figure 2-3, the SYM53C895 is connected to the TI SN75976A2 differential transceiver for Ultra SCSI operation. The recommended value of the pull-up resistor on the REQ-, ACK-, MSG-, C/D-, I/O-, ATN-, SD0-7-, and SDP0- lines is 680Ω when the Active Negation portion of Symbios TolerANT technology is not enabled. When TolerANT is enabled, the recommended resistor value on the REQ-, ACK-, SD7-0-, and SDP0- signals is 1.5 KΩ The electrical characteristics of these pins change when TolerANT is enabled, permitting a higher resistor value.

To interface the SYM53C895 to the SN75976A2, connect the positive pins in the SCSI LVD pair of the SYM53C895 directly to the transceiver enables (nDE/RE/). These signals control the direction of the channels on the SN75976A2.

The SCSI bidirectional control and data pins (SD7-0- SDP0-, REQ-, ACK-, MSG-, I_O-, C_D, and ATN-) of the SYM53C895 connect to the bidirectional data pins (nA) of the SN75976A2 with a pull-up resistor. The pull-up value should be no lower than the transceiver I_{OL} can tolerate, but not so high as to cause RC timing problems. The three remaining pins, SEL-, BSY,- and RST-, are connected to the SN75976A2 with a pull-down resistor. The pull-down resistors are required when the pins (nA) of the SN75976A2 are configured as inputs. When the data pins are inputs, the resistors provide a bias voltage to both the SYM53C895 pins (SEL-, BSY-, and RST-) and the SN75976A2 data pins. Because the SEL-, BSY-, and RST- pins on the SYM53C895 are inputs only, this configuration allows for the SEL-, BSY-, and RST- SCSI signals to be asserted on the SCSI bus. The differential pairs on the SCSI bus are reversed when connected to the SN75976A2, due to the active low nature of the SCSI bus.

8-bit/16-bit SCSI and the high voltage differential interface

In an 8-bit SCSI bus, the SD15-8 pins on the SYM53C895 should be pulled up with a 1.5 KΩ resistor or terminated like the rest of the SCSI bus lines. This is very important, as errors may occur during reselection if these lines are left floating.

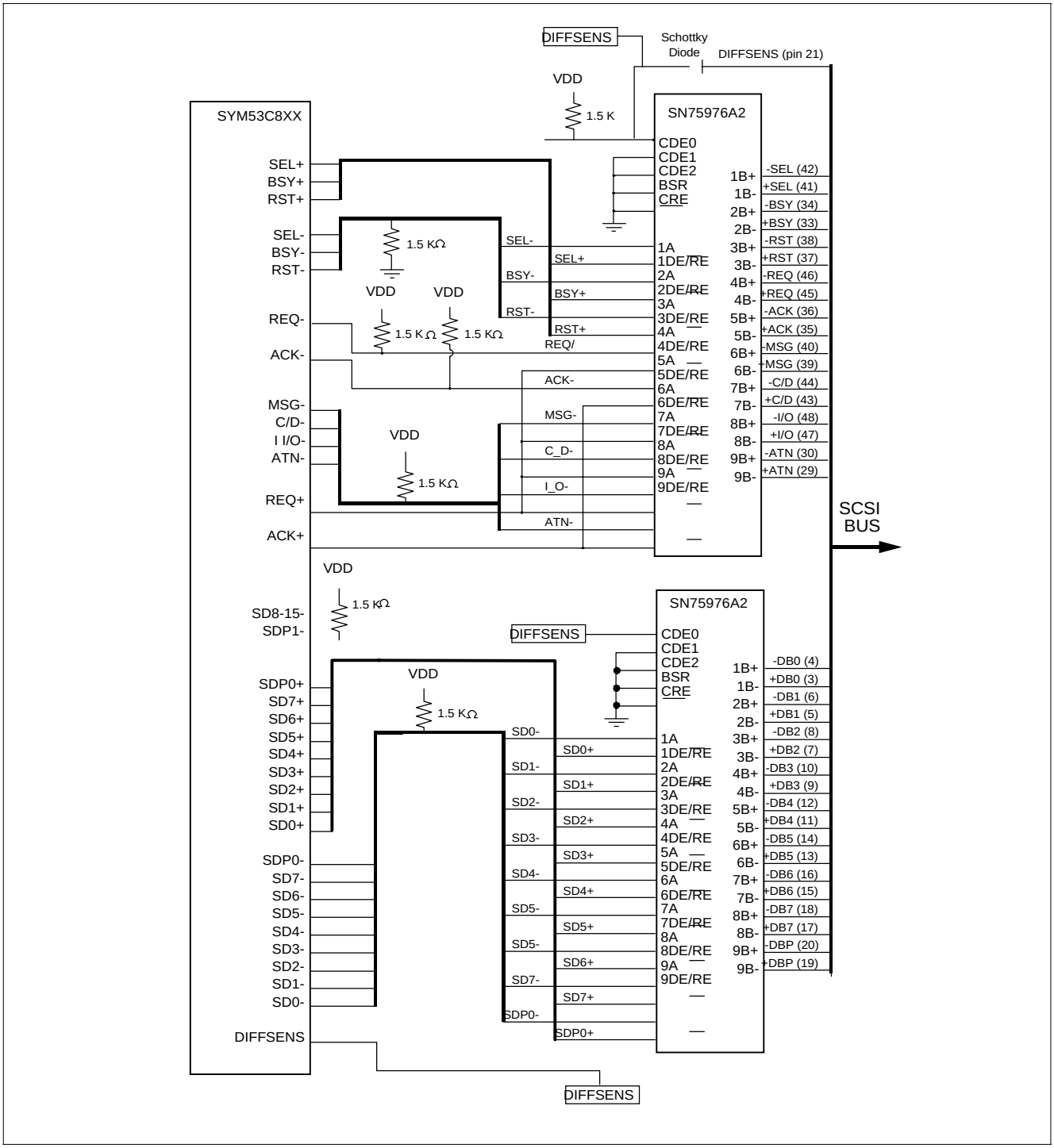

Figure 2-3: High Voltage Differential Wiring Diagram for Ultra SCSI

SCSI Termination

The terminator networks provide the biasing needed to pull signals to an inactive voltage level, and to match the impedance seen at the end of the cable with the characteristic impedance of the cable. Terminators must be installed at the extreme ends of the SCSI chain, and only at the ends; no system should ever have more or less than two terminators installed and active. SCSI host adapters should provide a means of accommodating terminators. The terminators should be socketed, so that if not needed they may be removed, or there should be a means of disabling them with software.

Single-ended cables can use a 220 Ω pull-up to the terminator power supply (Term-Power) line and a 330 Ω pull-down to Ground. Because of the high-performance nature of the SYM53C895, Regulated (or Active) termination is recommended. Figure 2-4 shows a Unitrode active terminator. For additional information, refer to the SCSI-2 Specification. TolerANT active negation can be used with either termination network.

For information on terminators that support LVD, refer to the SPI-2 draft standard.

Note: If the SYM53C895 is to be used in a design with only an 8-bit SCSI bus, all 16 data lines still must be terminated or pulled high.

System Engineering Note

In the SYM53C895, transmission mode detection for single-ended (SE), high voltage differential (HVD), and low voltage differential (LVD) is implemented by using the DIFFSENS line. Table 2-7 shows the corresponding voltages and what mode they indicate.

Table 2-7: Transmission Mode

Mode	SE	LVD	HVD
Voltage	-0.35 to +0.5	0.7 to 1.9	2.4 to 5.5

The SPI-2 (SCSI Parallel Interconnect 2) Specification, Revision 1.1, requires that a bus mode change must be sensed for at least a continuous 100 ms to be valid. Additionally, the signal drivers should remain in a high impedance state at power up until the device is capable of full logical operation for at least 100 ms and the bus mode detected by the DIFFSENS line has remained stable for at least another 100 ms after that. In order to achieve the sufficient 100 ms delay required by the standard, the following steps should be taken when a mode change is detected.

At power-up:

1. Set bit 3 in STEST2 (register 4Eh), to place the SCSI drivers in a high impedance state.
2. Enable the SBMC (SCSI Bus Mode Change) interrupt by setting bit 4 in SIEN1 (register 41h).
3. If a SCSI bus mode change is detected, then SIST1 (register 43h), bit 4 will indicate a SBMC interrupt.
4. Clear the interrupt by reading SIST0 (register 42h) and SIST1.
5. Wait 100 ms.
6. Check that no more SBMC interrupts have occurred. If not, the DIFFSENS line has not changed voltage levels and the bus mode is stable. Read bits 7-6 in STEST4 (register 52h). Write these two bits to STEST0 (register 4Ch), bits 5-4. This will force the SCSI bus

mode to the correct operating mode. (If a SBMC interrupt occurs between steps 4 and 6, handle the interrupt and return to step 3.)

Note that bits 5-4 in STEST0 are normally used as part of the SSAID and are read only. These bits may be written as part of a special test mode that forces the SCSI bus mode to one of three operating modes: single-ended, LVD, or high voltage differential. The bit encoding is the same that is shown in the table under STEST4 for bits 7-6.

7. Clear bit 3 in STEST2 to remove the SCI drivers from the high impedance state.

During normal operation:

1. Enable the SBMC (SCSI Bus Mode Change) interrupt. Bit 4 in SIEN1 should be set.
2. If a SCSI bus mode change is detected, SIST1, bit 4 will indicate a SBMC interrupt.
3. Clear the interrupt by reading SIST0 and SIST1.
4. Wait 100 ms.
5. Check that no more SBMC interrupts have occurred. If not, the DIFFSENS line has not changed voltage levels and the bus mode is stable. Read bits 7-6 in STEST4. Write two bits 5 and 4 to STEST0.

   Note that bits 5-4 in STEST0 are normally used as part of the SSAID and are read only. These bits may be written as part of a special test mode that forces the SCSI bus mode to one of three operating modes: single-ended, LVD, or high voltage differential. The bit encoding is the same that is shown in the table under STEST4 for bits 7-6. This will force the SCSI bus to the correct operating mode.

   If a SBMC interrupt did occur between steps 3 and 5, handle the interrupt and return to step 3.

The SCSI Bus Mode Change (SBMC) interrupt can cause a problem in systems that use multiple software drivers, where the drivers pass control to one another after a chip reset. This problem occurs when the SYM53C895 is connected to a single-ended SCSI bus, because the SBMC interrupt is generated after each reset. In particular, this problem occurs with NetWare when control is passed between the NetWare and DOS drivers. After a soft reset, the SYM53C895 defaults to LVD mode. If single-ended devices are on the bus, causing the DIFFSENS line to be pulled low, a SBMC interrupt will be generated and the driver will need to respond to it.

One solution is to use a soft abort by writing a one to bit 7 in the ISTAT register, instead of a soft reset to stop current SCSI transactions. This would halt current transactions without altering chip settings such as the clock quadrupler and the clock divider setup. The pending transactions would then be started over.

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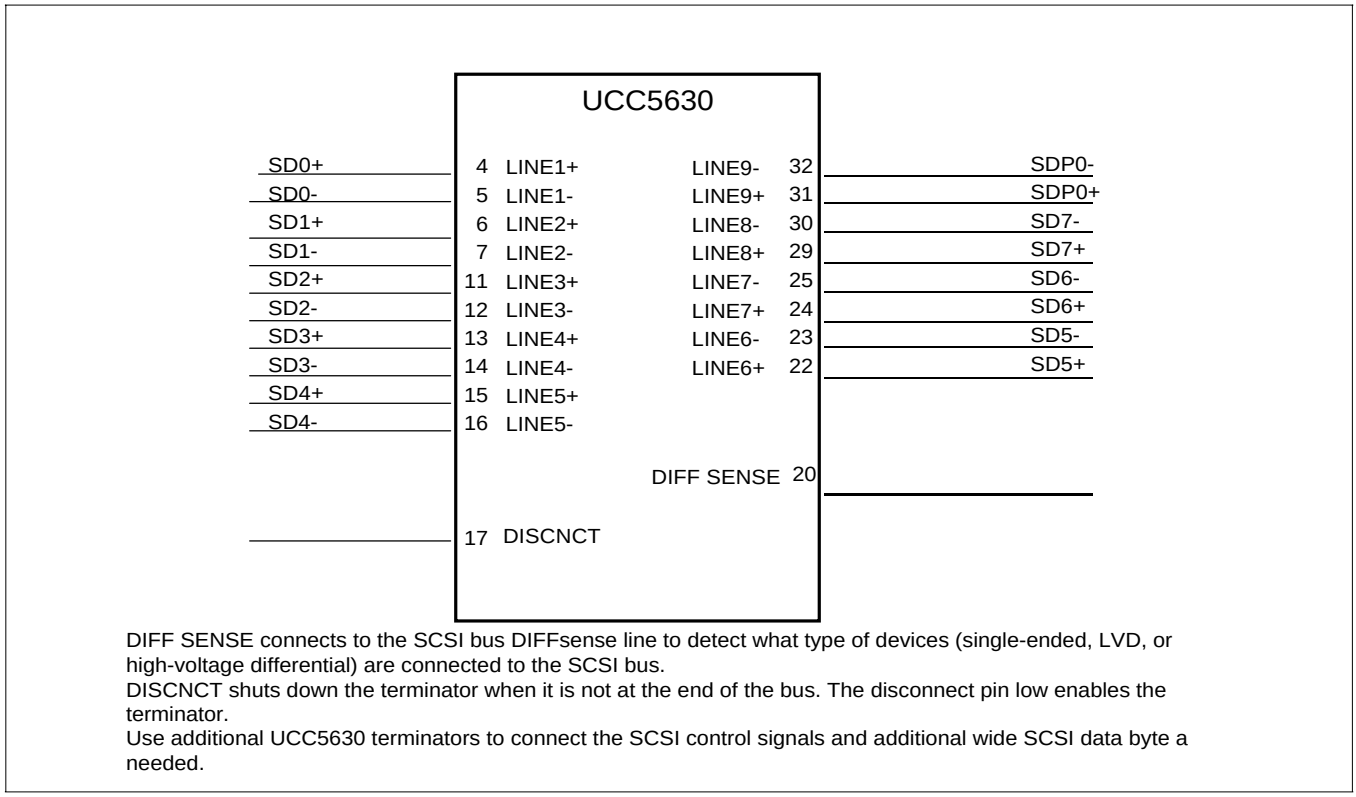


Figure 2-4: Regulated Termination for Ultra2 SCSI

(Re)Select During (Re)Selection

In multi-threaded SCSI I/O environments, it is not uncommon to be selected or reselected while trying to perform selection/reselection. This situation may occur when a SCSI controller (operating in initiator mode) tries to select a target and is reselected by another. The Select SCRIPTS instruction has an alternate address to which the SCRIPTS will jump when this situation occurs. The analogous situation for target devices is being selected while trying to perform a reselection.

Once a change in operating mode occurs, the initiator SCRIPTS should start with a Set Initiator instruction or the target SCRIPTS should start with a Set Target instruction. The Selection and Reselection Enable bits (SCID bits 5 and 6, respectively) should both be asserted so that the SYM53C895 may respond as an initiator or as a target. If only selection is enabled, the SYM53C895 cannot be reselected as an initiator. There are also status and interrupt bits in the SIST0 and SIEN0 registers, respectively, indicating that the SYM53C895 has been selected (bit 5) and reselected (bit 4).

Synchronous Operation

The SYM53C895 can transfer synchronous SCSI data in both initiator and target modes. The SXFER register controls both the synchronous offset and the transfer period. It may be loaded by the CPU before SCRIPTS execution begins, from within SCRIPTS via a Table Indirect I/O instruction, or with a Read-Modify-Write instruction.

The SYM53C895 can receive data from the SCSI bus at a synchronous transfer period as short as 25 ns, regardless of the transfer period used to send data. The SYM53C895 can receive data at one-fourth of the divided SCLK frequency. Depending on the SCLK frequency, the negotiated transfer period, and the synchronous clock divider, the SYM53C895 can send synchronous data at intervals as short as 25 ns for Ultra2 SCSI, 50 ns for Ultra SCSI, 100 ns for fast SCSI and 200 ns for SCSI-1.

Determining the Data Transfer Rate

Synchronous data transfer rates are controlled by bits in two different registers of the SYM53C895. A brief description of the bits is provided below. Figure 2-5 illustrates the clock division factors used in each register, and the role of the register bits in determining the transfer rate.

SCNTL3 Register, bits 6–4 (SCF2–0)

The SCF2-0 bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The output from this divider controls the rate at which data can be received; this rate must not exceed 160 MHz. The receive rate of synchronous SCSI data is 1/4 of the SCF divider output. For example, if SCLK is 160 MHz and the SCF value is set to divide by one, then the maximum rate at which data can be received is 40 MHz (160/(1*4) = 40).

SCNTL3 Register, bits 2–0 (CCF2–0)

The CCF2-0 bits select the factor by which the frequency of SCLK is divided before being presented to the asynchronous SCSI core logic. This divider must be set according to the input clock frequency in the table.

SXFER Register, bits 7–5 (TP2–0)

The TP2-0 divider bits determine the SCSI synchronous transfer period when sending synchronous SCSI data in either initiator or target mode. This value further divides the output from the SCF divider.

Ultra2 SCSI Synchronous Data Transfers

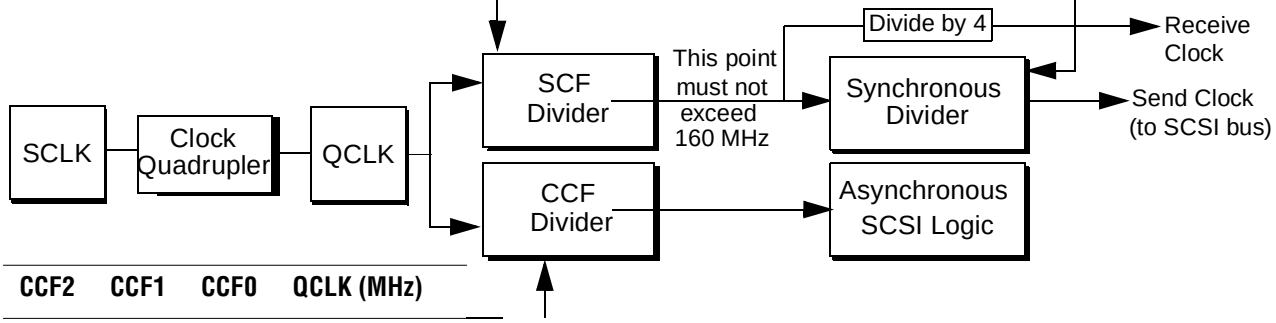
Ultra2 SCSI is an extension of current Ultra SCSI synchronous transfer specifications. It allows synchronous transfer periods to be negotiated down as low as 25 ns, which is half the 50 ns period allowed under Ultra SCSI. This will allow a maximum transfer rate of 80 MB/s on a 16-bit, LVD SCSI bus. The SYM53C895 has a SCSI clock quadrupler that must be enabled for the chip to perform Ultra2 SCSI transfers with a 40 MHz oscillator. In addition, the following bit values affect the chip's ability to support Ultra2 SCSI synchronous transfer rates:

1. Clock Conversion Factor bits, SCNTL3 register bits 2-0 and Synchronous Clock Conversion Factor bits, SCNTL3 register bits 6-4. These fields support a value of 111 (binary), allowing the 160 MHz SCLK frequency to be divided down by 8 for the asynchronous logic.
2. Ultra2 SCSI Enable bit, SCNTL 3 register bit 7. Setting this bit enables Ultra2 SCSI synchronous transfers in systems that use the internal SCSI clock quadrupler.
3. TolerANT Enable bit, STEST3 register bit 7. Active negation must be enabled for the SYM53C895 to perform Ultra2 SCSI transfers.

Note: The clock quadrupler requires a 40 MHz external clock. Symbios software assumes that the SYM53C895 is connected to a 40 MHz external clock, which is quadrupled to achieve Ultra2 SCSI transfer rates.

SCF2	SCF1	SCF0	SCF Divisor
0	0	1	1
0	1	0	1.5
0	1	1	2
1	0	0	3
0	0	0	3
1	0	1	4
1	1	0	6
1	1	1	8

TP2	TP1	TP0	XFERP Divisor
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11



CCF2	CCF1	CCF0	QCLK (MHz)
0	0	0	50.1-66.00
0	0	1	16.67-25.00
0	1	0	25.01-37.50
0	1	1	37.51-50.00
1	0	0	50.01-66.00
1	0	1	75.01-80.00
1	1	0	120
1	1	1	160

Example:

QCLK (Quadrupled SCSI Clock)=160 MHz, SCF=1(/1), XFERP=0(/4),
CCF=7 (/8)
Synchronous send rate = (QCLK/SCF)/XFERP= (160/1)/4=40MB/s
Synchronous receive rate=(QCLK/SCF)/4=(160/1)/4=40MB/s

Figure 2-5: Determining the Synchronous Transfer Rate

Interrupt Handling

The SCRIPTS processor in the SYM53C895 performs most functions independently of the host microprocessor. However, certain interrupt situations must be handled by the external microprocessor. This section explains all aspects of interrupts as they apply to the SYM53C895.

Polling and Hardware Interrupts

The external microprocessor is informed of an interrupt condition by polling or hardware interrupts. Polling means that the microprocessor must continually loop and read a register until it detects a bit set that indicates an interrupt. This method is the fastest, but it wastes CPU time that could be used for other system tasks. The preferred method of detecting interrupts in most systems is hardware interrupts. In this case, the SYM53C895 will assert the Interrupt Request (IRQ/) line that will interrupt the microprocessor, causing the microprocessor to execute an interrupt service routine. A hybrid approach would use hardware interrupts for long waits, and use polling for short waits.

Registers

The registers in the SYM53C895 that are used for detecting or defining interrupts are: ISTAT, SIST0, SIST1, DSTAT, SIEN0, SIEN1, DCNTL, and DIEN registers.

ISTAT

The ISTAT is the only register that can be accessed as a slave during SCRIPTS operation, therefore it is the register that is polled when polled interrupts are used. It is also the first register that should be read when the IRQ/ pin has been asserted in association with a hardware interrupt. The INTF (Interrupt on the Fly) bit should be the first interrupt serviced. It must be written to one to be cleared. This interrupt must be cleared before servicing any other interrupts. If the SIP bit in the ISTAT register is set, then a SCSI-type interrupt has occurred and the SIST0 and SIST1 registers should be read. If the DIP bit in the ISTAT register is set, then a DMA-type interrupt has occurred and the DSTAT register should be read. SCSI-type and DMA-type interrupts may occur simultaneously, so in some cases both SIP and DIP may be set.

SIST0 and SIST1

The SIST0 and SIST1 registers contain the SCSI-type interrupt bits. Reading these registers will determine which condition or conditions caused the SCSI-type interrupt, and will clear that SCSI interrupt condition. If the SYM53C895 is receiving data from the SCSI bus and a fatal interrupt condition occurs, the SYM53C895 will attempt to send the contents of the DMA FIFO to memory before generating the interrupt. If the SYM53C895 is sending data to the SCSI bus and a fatal SCSI interrupt condition occurs, data could be left in the DMA FIFO. If this situation occurs, the DMA FIFO Empty (DFE) bit in DSTAT should be checked. If this bit is clear, set the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits before continuing. The CLF bit is bit 2 in CTEST3. The CSF bit is bit 1 in STEST3.

DSTAT

The DSTAT register contains the DMA-type interrupt bits. Reading this register will determine which condition or conditions caused the DMA-type interrupt, and will clear that DMA interrupt condition. Bit 7 in DSTAT, DFE, is purely a status bit; it will not generate an interrupt under any circumstances and will not be cleared when read. DMA interrupts will flush neither the DMA nor SCSI FIFOs before generating the interrupt, so the DFE bit in the DSTAT register should be checked after any DMA interrupt. If the DFE bit is clear, then the FIFOs must be cleared by setting the CLF (Clear DMA FIFO) and CSF (Clear SCSI FIFO) bits, or flushed by setting the FLF (Flush DMA FIFO) bit.

SIEN0 and SIEN1

The SIEN0 and SIEN1 registers are the interrupt enable registers for the SCSI interrupts in SIST0 and SIST1.

DIEN

The DIEN register is the interrupt enable register for DMA interrupts in DSTAT.

DCNTL

When bit 1 in this register is set, the IRQ/ pin will not be asserted when an interrupt condition occurs. The interrupt is not lost or ignored, but merely masked at the pin. Clearing this bit when an interrupt is pending will immediately cause the IRQ/ pin to assert. As with any register other than ISTAT, this register cannot be accessed except by a SCRIPTS instruction during SCRIPTS execution.

Fatal vs. Non-Fatal Interrupts

A fatal interrupt, as the name implies, always causes SCRIPTS to stop running. All non-fatal interrupts become fatal when they are enabled by setting the appropriate interrupt enable bit. Interrupt masking will be discussed later in this section. All DMA interrupts (indicated by the DIP bit in ISTAT and one or more bits in DSTAT being set) are fatal.

Some SCSI interrupts (indicated by the SIP bit in the ISTAT and one or more bits in SIST0 or SIST1 being set) are non-fatal. When the SYM53C895 is operating in Initiator mode, only the Function Complete (CMP), Selected (SEL), Reselected (RSL), General Purpose Timer Expired (GEN), and Handshake to Handshake Timer Expired (HTH) interrupts are non-fatal. When operating in Target mode CMP, SEL, RSL, Target mode: SATN/ active (M/A), GEN, and HTH are non-fatal. Refer to the description for the Disable Halt on a Parity Error or SATN/ active (Target Mode Only) (DHP) bit in the SCNTL1 register to configure the chip's behavior when the SATN/ interrupt is enabled during Target mode operation. The Interrupt on the Fly interrupt is also non-fatal, since SCRIPTS can continue when it occurs.

The reason for non-fatal interrupts is to prevent SCRIPTS from stopping when an interrupt occurs that does not require service from the CPU. This prevents an interrupt when arbitration is complete (CMP set), when the SYM53C895 has been selected or reselected (SEL or RSL set), when the initiator has asserted ATN (target mode: SATN/ active), or when the General Purpose or Handshake to Handshake timers expire. These interrupts are not needed for events that occur during high-level SCRIPTS operation.

Masking

Masking an interrupt means disabling or ignoring that interrupt. Interrupts can be masked by clearing bits in the SIEN0 and SIEN1 (for SCSI interrupts) registers or DIEN (for DMA interrupts) register. How the chip will respond to masked interrupts depends on: whether polling or hardware interrupts are being used; whether the interrupt is fatal or non-fatal; and whether the chip is operating in Initiator or Target mode.

If a non-fatal interrupt is masked and that condition occurs, SCRIPTS will not stop, the appropriate bit in the SIST0 or SIST1 will still be set, the SIP bit in the ISTAT will not be set, and the IRQ/ pin will not be asserted. See the section on fatal vs. non-fatal interrupts for a list of the non-fatal interrupts.

If a fatal interrupt is masked and that condition occurs, then SCRIPTS will still stop, the appropriate bit in the DSTAT, SIST0, or SIST1 register will be set, and the SIP or DIP bits in the ISTAT will be set, but the IRQ/ pin will not be asserted.

When the chip is initialized, enable all fatal interrupts if you are using hardware interrupts. If a fatal interrupt is disabled and that interrupt condition occurs, SCRIPTS will halt and the system will never know it unless it times out and checks the ISTAT after a certain period of inactivity.

If you are polling the ISTAT instead of using hardware interrupts, then masking a fatal interrupt will make no difference since the SIP and DIP bits in the ISTAT inform the system of interrupts, not the IRQ/ pin.

Masking an interrupt after IRQ/ is asserted will not cause IRQ/ to be deasserted.

Stacked Interrupts

The SYM53C895 stacks interrupts if they occur one after the other. If the SIP or DIP bits in the ISTAT register are set (first level), then there is already at least one pending interrupt, and any future interrupts will be stacked in extra registers behind the SIST0, SIST1, and DSTAT registers (second level). When two interrupts have occurred and the two levels of the stack are full, any further interrupts will set additional bits in the extra registers behind SIST0, SIST1, and DSTAT. When the first level of interrupts are cleared, all the interrupts that came in afterward will move into the SIST0, SIST1, and DSTAT. After the first interrupt is cleared by reading the appropriate register, the IRQ/ pin will be deasserted for a minimum of three CLKs; the stacked interrupt(s) will move into the SIST0, SIST1, or DSTAT; and the IRQ/ pin will be asserted once again.

Since a masked non-fatal interrupt will not set the SIP or DIP bits, interrupt stacking will not occur. A masked, non-fatal interrupt will still post the interrupt in SIST0, but will not assert the IRQ/ pin. Since no interrupt is generated, future interrupts will move right into the SIST0 or SIST1 instead of being stacked behind another interrupt. When another condition occurs that generates an interrupt, the bit corresponding to the earlier masked non-fatal interrupt will still be set.

A related situation to interrupt stacking is when two interrupts occur simultaneously. Since stacking does not occur until the SIP or DIP bits are set, there is a small timing window in which multiple interrupts can occur but will not be stacked. These could be multiple SCSI interrupts (SIP set), multiple DMA interrupts (DIP set), or multiple SCSI and multiple DMA interrupts (both SIP and DIP set).

As previously mentioned, DMA interrupts will not attempt to flush the FIFOs before generating the interrupt. It is important to set either the Clear DMA FIFO (CLF) and Clear SCSI FIFO (CSF) bits if a DMA interrupt occurs and the DMA FIFO Empty (DFE) bit is not set. This is because any future SCSI interrupts will not be posted until the DMA FIFO is clear of data. These 'locked out' SCSI interrupts will be posted as soon as the DMA FIFO is empty.

Halting in an Orderly Fashion

When an interrupt occurs, the SYM53C895 will attempt to halt in an orderly fashion.

- If the interrupt occurs in the middle of an instruction fetch, the fetch will be completed, except in the case of a Bus Fault. Execution will not begin, but the DSP will point to the next instruction since it is updated when the current instruction is fetched.
- If the DMA direction is a write to memory and a SCSI interrupt occurs, the SYM53C895 will attempt to flush the DMA FIFO to memory before halting. Under any other circumstances only the current cycle will be completed before halting, so the DFE bit in DSTAT should be checked to see if any data remains in the DMA FIFO.
- SCSI SREQ/SACK handshakes that have begun will be completed before halting.
- The SYM53C895 will attempt to clean up any outstanding synchronous offset before halting.
- In the case of Transfer Control Instructions, once instruction execution begins it will continue to completion before halting.
- If the instruction is a JUMP/CALL WHEN/IF <phase>, the DSP will be updated to the transfer address before halting.
- All other instructions may halt before completion.

Sample Interrupt Service Routine

The following is a sample of an interrupt service routine for the SYM53C895. It can be repeated if polling is used, or should be called when the IRQ/ pin is asserted if hardware interrupts are used.

1. Read ISTAT.
2. If the INTF bit is set, it must be written to a one to clear this status.
3. If only the SIP bit is set, read SIST0 and SIST1 to clear the SCSI interrupt condition and get the SCSI interrupt status. The bits in the SIST0 and SIST1 tell which SCSI interrupt(s) occurred and determine what action is required to service the interrupt(s).
4. If only the DIP bit is set, read the DSTAT to clear the interrupt condition and get the DMA interrupt status. The bits in the DSTAT will tell which DMA interrupt(s) occurred and determine what action is required to service the interrupt(s).
5. If both the SIP and DIP bits are set, read SIST0, SIST1, and DSTAT to clear the SCSI and DMA interrupt condition and get the interrupt status. If using 8-bit reads of the SIST0, SIST1, and DSTAT registers to clear interrupts, insert a 12 CLK delay between the consecutive reads to ensure that the interrupts clear properly. Both the SCSI and DMA interrupt conditions should be handled before leaving the interrupt service routine. It is recommended that the DMA interrupt be serviced before the SCSI interrupt, because a serious DMA interrupt condition could influence how the SCSI interrupt is acted upon.
6. When using polled interrupts, go back to step 1 before leaving the interrupt service routine, in case any stacked interrupts moved in when the first interrupt was cleared. When using hardware interrupts, the IRQ/ pin will be asserted again if there are any stacked interrupts. This should cause the system to re-enter the interrupt service routine.

Chained Block Moves

Since the SYM53C895 has the capability to transfer 16-bit wide SCSI data, a unique situation occurs when dealing with odd bytes. The chained move (CHMOV) SCRIPTS instruction along with the Wide SCSI Send (WSS) and Wide SCSI Receive (WSR) bits in the SCNTL2 register are used to facilitate these situations. The Chained Block Move instruction is illustrated in Figure 2-6.

Wide SCSI Send Bit (WSS)

The WSS bit is set whenever the SCSI core is sending data (Data Out for initiator or Data In for target) and the core detects a partial transfer at the end of a chained Block Move SCRIPTS instruction (this flag will not be set if a normal Block Move instruction is used). Under this condition, the SCSI core does not send the low-order byte of the last partial memory transfer across the SCSI bus. Instead, the low-order byte is temporarily stored in the lower byte of the SODL register and the WSS flag is set. The hardware uses the WSS flag to determine what behavior must occur at the start of the next data send transfer. When the WSS flag is set at the start of the next transfer, the first byte (the high-order byte) of the next data send transfer is “married” with the stored low-order byte in the SODL register; and the two bytes are sent out across the bus, regardless of the type of Block Move instruction (normal or chained). The flag is automatically cleared when the “married” word is sent. The flag can alternately be cleared through SCRIPTS or by the microprocessor.

Additionally, this bit can be used by the microprocessor or SCRIPTS for error detection and recovery purposes.

Wide SCSI Receive Bit (WSR)

The WSR bit is set whenever the SCSI core is receiving data (Data In for initiator or Data Out for target) and the core detects a partial transfer at the end of a block move or chained block move SCRIPTS instruction. When WSR is set, the high order byte of the last SCSI bus transfer is not transferred to memory. Instead, the byte is temporarily stored in the SWIDE register. The hardware uses the WSR bit to determine what behavior must occur at the start of the next data receive transfer. The bit is automatically cleared at the start of the next data receive transfer. The bit can alternatively be cleared by the microprocessor or through SCRIPTS. The bit can also be used by the microprocessor or SCRIPTS for error detection and recovery purposes.

SWIDE Register

This register stores data for partial byte data transfers. For receive data, the SWIDE register holds the high-order byte of a partial SCSI transfer which has not yet been transferred to memory. This stored data may be a residue byte (and therefore ignored) or it may be valid data that will be transferred to memory at the beginning of the next Block Move instruction.

SODL Register

For send data, the low-order byte of the SODL register holds the low-order byte of a partial memory transfer which has not yet been transferred across the SCSI bus. This stored data is usually “married” with the first byte of the next data send transfer, and both bytes are sent across the SCSI bus at the start of the next data send block move command.

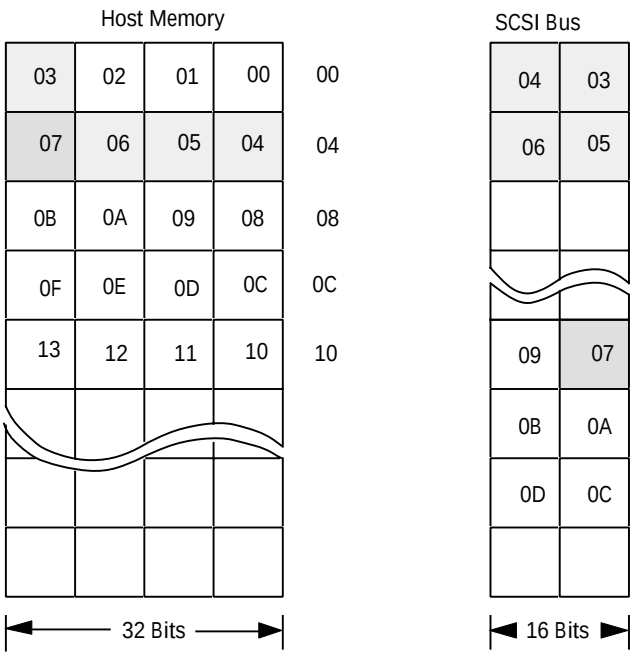
Chained Block Move SCRIPTS Instruction

A chained Block Move SCRIPTS instruction is primarily used to transfer consecutive data send or data receive blocks. Using the chained block move instruction facilitates partial receive transfers and allows correct partial send behavior without additional op code overhead. Behavior of the chained Block Move instruction varies slightly for sending and receiving data.

For receive data (Data In for initiator or Data Out for target), a chained Block Move instruction indicates that if a partial transfer occurred at the end of the instruction, the WSR flag is set.The high order byte of the last SCSI transfer is stored in the SWIDE register rather than transferred to memory. The contents of the SWIDE register should be the first byte transferred to memory at the start of the chained block move data stream. Since the byte count always represents data transfers to/from memory (as opposed to the SCSI bus), the byte transferred out of the SWIDE register is one of the bytes in the byte count. If the WSR bit is clear when a receive data chained Block Move instruction is executed, the data transfer occurs similar to that of the regular block move instruction. Whether the WSR bit is set or clear, when a normal block move instruction is executed, the contents of the SWIDE register will be ignored and the transfer takes place normally. For “N” consecutive wide data receive Block Move instructions, the 2nd through the Nth Block Move instructions should be chained block moves.

For send data (Data Out for initiator or Data In for target), a chained Block Move instruction indicates that if a partial transfer terminates the chained block move instruction, the last low-order byte (the partial memory transfer) should be stored in the lower byte of the SODL register and not sent across the SCSI bus. Without the chained block move instruction, the last low-order byte would be sent across the SCSI bus. The starting byte count represents data bytes transferred from memory but not to the SCSI bus when a partial transfer exists.

For example, if the instruction is an Initiator chained Block Move Data Out of five bytes (and WSS is not previously set), five bytes will be transferred out of memory to the SCSI core, four bytes will be transferred from the SCSI core across the SCSI bus, and one byte will be temporarily stored in the lower byte of the SODL register waiting to be married with the first byte of the next block move instruction. Regardless of whether a chained Block Move or normal Block Move instruction is used, if the WSS bit is set at the start of a data send command, the first byte of the data send command is assumed to be the high-order byte and is "married" with the low-order byte stored in the stored in the lower byte of the SODL register before the two bytes are sent across the SCSI bus. For "N" consecutive wide data send Block Move commands, the first through the (Nth - 1) Block Move instructions should be Chained Block Moves.



Notes: CHMOV 5, 3 when DATA_OUT: *Moves five bytes from address 03 in the host memory to the SCSI bus (bytes 03, 04, 05, and 06 are moved and byte 07 remains in the low order byte of the SCSI Output Data Latch register and is married with the first byte of the following MOVE instruction).*

MOVE 5, 9 when DATA_OUT: *Moves five bytes from address 09 in the host memory to the SCSI bus.*

Figure 2-6: Block Move and Chained Block Move Instructions

Chapter 3
PCI Functional Description

PCI Addressing

There are three types of PCI-defined address spaces:

1. Configuration space
2. Memory space
3. I/O space

Configuration space is a contiguous 256 x 8-bit set of addresses dedicated to each “slot” or “stub” on the bus. Decoding C_BE/(3-0) determines if a PCI cycle is intended to access configuration register space. The IDSEL bus signal is a “chip select” that allows access to the configuration register space only. A configuration read/write cycle without IDSEL will be ignored. The eight lower order addresses are used to select a specific 8-bit register. AD(10-8) are decoded as well, but they must be zero or the SYM53C895 will not respond. According to the PCI specification, AD(10-8) are to be used for multifunction devices. The host processor uses the PCI configuration space to initialize the SYM53C895.

The lower 128 bytes of the SYM53C895 configuration space holds system parameters while the upper 128 bytes map into the SYM53C895 operating registers. For all PCI cycles except configuration cycles, the SYM53C895 registers are located on the 256-byte block boundary defined by the base address assigned through the configured register. The SYM53C895 operating registers are available in both the upper and lower 128-byte portions of the 256-byte space selected.

At initialization time, each PCI device is assigned a base address (in the case of the SYM53C895, the upper 24 bits of the address are selected) for memory accesses and I/O accesses. On every access, the SYM53C895 compares its assigned base addresses with the value on the Address/Data bus during the PCI address phase. If there is a match of the upper 24 bits, the access is for the SYM53C895 and the low order eight bits define the register to be accessed. A decode of C_BE/ (3-0) determines which registers and what type of access is to be performed.

PCI defines memory space as a contiguous 32-bit memory address that is shared by all system resources, including the SYM53C895. Base Address Register One determines which 256-byte memory area this device will occupy.

PCI defines I/O space as a contiguous 32-bit I/O address that is shared by all system resources, including the SYM53C895. Base Address Register Zero determines which 256-byte I/O area this device will occupy.

PCI Bus Commands and Functions Supported

Bus commands indicate to the target the type of transaction the master is requesting. Bus commands are encoded on the C_BE/(3-0) lines during the address phase. PCI bus command encoding and types appear in Table 3-1.

The I/O Read command is used to read data from an agent mapped in I/O address space. All 32 address bits are decoded.

The I/O Write command is used to write data to an agent when mapped in I/O address space. All 32 address bits are decoded.

The Memory Read, Memory Read Multiple, and Memory Read Line commands are used to read data from an agent mapped in memory address space. All 32 address bits are decoded.

The Memory Write and Memory Write and Invalidate commands are used to write data to an agent when mapped in memory address space. All 32 address bits are decoded.

Table 3-1: PCI Bus Commands Supported

C_BE(3-0)	Command Type	Supported as Master	Supported as Slave
0000	Special Interrupt Acknowledge	No	No
0001	Special Cycle	No	No
0010	I/O Read Cycle	Yes	Yes
0011	I/O Write Cycle	Yes	Yes
0100	Reserved	n/a	n/a
0101	Reserved	n/a	n/a
0110	Memory Read	Yes	Yes
0111	Memory Write	Yes	Yes
1000	Reserved	n/a	n/a
1001	Reserved	n/a	n/a
1010	Configuration Read	No	Yes
1011	Configuration Write	No	Yes
1100	Memory Read Multiple	Yes**	No (defaults to 0110)
1101	Dual Address Cycle	No	No
1110	Memory Read Line	Yes*	No (defaults to 0110)
1111	Memory Write and Invalidate	Yes***	No (defaults to 0111)

** This operation is selectable by bit 3 in the DMODE operating register*
*** This operation is selectable by bit 2 in the DMODE operating register*
****This operation is selectable by bit 0 in the CTEST3 operating register*

PCI Cache Mode

The SYM53C895 supports the PCI specification for an 8-bit Cache Line Size register located in PCI configuration space. The Cache Line Size register provides the ability to sense and react to non-aligned addresses corresponding to cache line boundaries. In conjunction with the Cache Line Size register, the PCI commands Read Line, Read Multiple, and Write and Invalidate are each software enabled or disabled to allow the user full flexibility in using these commands.

Support for PCI Cache Line Size Register

The SYM53C895 supports the PCI specification for an 8-bit Cache Line Size register in PCI configuration space; it can sense and react to non-aligned addresses corresponding to cache line boundaries.

Selection of Cache Line Size

The cache logic will select a cache line size based on the values for the burst size in the DMODE register, bit 2 in the CTEST5 register, and the PCI Cache Line Size register.

Note: The SYM53C895 will not automatically use the value in the PCI Cache Line Size register as the cache line size value. The chip scales the value of the Cache Line Size register down to the nearest binary burst size allowed by the chip (2, 4, 8, 16, 32, 64, or 128), compares this value to the burst size defined by the values of the DMODE register and bit 2 of the CTEST5 register, then selects the smallest as the value for the cache line size. The SYM53C895 will use this value for all burst data transfers.

Alignment

The SYM53C895 uses the calculated line size value to monitor the current address for alignment to the cache line size. When it is not aligned, the chip attempts to align to the cache boundary by using a "smart aligning" scheme. This means that it will attempt to use the largest burst size possible that is less than the cache line size, to reach the cache boundary quickly with no overflow. This process is a stepping mechanism that will step up to the highest possible burst size based on the current address.

The stepping process begins at a 4-dword boundary. The SYM53C895 will first try to align to a 4-dword boundary (0x0000, 0x0010, etc.) by using single dword transfers (no bursting). Once this boundary has been reached the chip will evaluate the current alignment to various burst sizes allowed, and will select the largest possible as the next burst size, while not exceeding the cache line size. The chip will then issue this burst, and re-evaluate the alignment to various burst sizes, again selecting the largest possible while not exceeding the cache line size, as the next burst size. This stepping process continues until the chip reaches the cache line size boundary or runs out of data. Once a cache line boundary is reached, the chip will use the cache line size as the burst size from then on, except in the case of multiples (explained below). The alignment process is finished at this point.

Example: Cache Line Size - 16, Current Address = 0x01

The chip is not aligned to a 4-dword cache boundary (the stepping threshold), so it issues four single-dword transfers (the first is a 3-byte transfer). At address 0x10, the chip is aligned to a 4-dword boundary, but not aligned to any higher burst size boundaries that are less than the cache line size. So, the SYM53C895 will issue a burst of 4. At this point, the address is 0x20, and the chip will evaluate that it is aligned not only to a 4-dword boundary, but also to an 8-dword boundary. It will select the highest, 8, and burst 8 dwords. At this point, the address is 0x40, which is a cache line size boundary. Alignment stops, and the burst size from then on is switched to 16.

Memory Move Misalignment

The SYM53C895 will not operate in a cache alignment mode when a Memory Move instruction type is issued and the read and write addresses are different distances from the nearest cache line boundary. For example, if the read address is 0x21F and the write address is 0x42F, and the cache line size is eight (8), the addresses are byte aligned, but they are not the same distance from the nearest cache boundary. The read address is 1 byte from the cache boundary 0x220 and the write address is 17 bytes from the cache boundary 0x440. In this situation, the chip will not align to cache boundaries and will operate as an SYM53C825.

Memory Write and Invalidate Command

The Memory Write and Invalidate command is identical to the Memory Write command, except that it additionally guarantees a minimum transfer of one complete cache line; that is, the master intends to write all bytes within the addressed cache line in a single PCI transaction unless interrupted by the target. This command requires implementation of the PCI Cache Line Size regis-

ter at address 0Ch in PCI configuration space. The SYM53C895 enables Memory Write and Invalidate cycles when bit 0 in the CTEST3 register (WRIE) and bit 4 in the PCI Command register are set. This will cause Memory Write and Invalidate commands to be issued when the following conditions are met:

1. The CLSE bit, WRIE bit, and PCI configuration Command register, bit 4 must be set.
2. The cache line size register must contain a legal burst size (2, 4, 8, 16, 32, 64, or 128) value AND that value must be less than or equal to the DMODE burst size.
3. The chip must have enough bytes in the DMA FIFO to complete at least one full cache line burst.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the SYM53C895 will issue a Write and Invalidate command instead of a Memory Write command during all PCI write cycles.

Multiple Cache Line Transfers

The Write and Invalidate command can write multiple cache lines of data in a single bus ownership. The chip issues a burst transfer as soon as it reaches a cache line boundary. The size of the transfer will not automatically be the cache line size, but rather a multiple of the cache line size as allowed for in the Revision 2.1 of the PCI specification. The logic will select the largest multiple of the cache line size based on the amount of data to transfer, with the maximum allowable burst size being that determined from the DMODE Burst Size bits and CTEST 5, bit 2. If multiple cache line size transfers are not desired, the DMODE burst size can be set to exactly the cache line size and the chip will only issue single cache line transfers.

After each data transfer, the chip re-evaluates the burst size based on the amount of remaining data to transfer and again selects the highest possible multiple of the cache line size, no larger than the DMODE burst size. The most likely scenario of this scheme is that the chip will select the DMODE burst size after alignment, and issue bursts of this size. The burst size will, in effect, throttle down toward the end of a long Memory Move or Block Move transfer until only the cache line size burst size is left; the chip will finish the transfer with this burst size.

Latency

In accordance with the PCI specification, the chip's latency timer will be ignored when issuing a Write and Invalidate command such that when a latency time-out has occurred, the SYM53C895 will continue to transfer up until a cache line boundary. At that point, the chip will relinquish the bus and finish the transfer at a later time using another bus ownership. If the chip is transferring multiple cache lines it will continue to transfer until the next cache boundary is reached.

PCI Target Retry

During a Write and Invalidate transfer, if the target device issues a retry (STOP with no TRDY, indicating that no data was transferred), the SYM53C895 will relinquish the bus and immediately try to finish the transfer on another bus ownership. The chip will issue another Write and Invalidate command on the next ownership, in accordance with the PCI specification.

PCI Target Disconnect

During a Write and Invalidate transfer, if the target device issues a disconnect the SYM53C895 will relinquish the bus and immediately try to finish the transfer on another bus ownership. The chip will not issue another Write and Invalidate command on the next ownership unless the address is aligned.

Memory Read Line Command

This command is identical to the Memory Read command, except that it additionally indicates that the master intends to fetch a complete cache line. This command is intended to be used with bulk sequential data transfers where the memory system and the requesting master might gain some performance advantage by reading up to a cache line boundary rather than a single memory cycle.The Read Line Mode function that exists in the previous SYM53C8XX chips has been modified in the SYM53C895 to reflect the PCI Cache Line Size register specifications. The functionality of the Enable Read Line bit (bit 3 in DMODE) has been modified to more resemble the Write and Invalidate mode in terms of conditions that must be met before a Read Line command will be issued. However, the Read Line option will operate exactly like the previous SYM53C8XX chips when cache mode has been disabled by a CLSE bit reset or when certain conditions exist in the chip (explained below).

The Read Line mode is enabled by setting bit 3 in the DMODE register. If cache mode is disabled, Read Line commands will be issued on every read data transfer, except op code fetches, as in previous SYM53C8XX chips.

If cache mode has been enabled, a Read Line command will be issued on all read cycles, except op code fetches, when the following conditions have been met:

1. The CLSE and Enable Read Line bits must be set.
2. The Cache Line Size register must contain a legal burst size value (2, 4, 8, 16, 32, 64, or 128) AND that value must be less than or equal to the DMODE burst size.
3. The number of bytes to be transferred at the time a cache boundary has been reached must be equal to or greater than the DMODE burst size.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip will issue a Read Line command instead of a Memory Read during all PCI read cycles. Otherwise, it will issue a normal Memory Read command.

Memory Read Multiple Command

This command is identical to the Memory Read command except that it additionally indicates that the master may intend to fetch more than one cache line before disconnecting. The SYM53C895 supports PCI Read Multiple functionality and will issue Read Multiple commands on the PCI bus when the Read Multiple Mode is enabled. This mode is enabled by setting bit 2 of the DMODE register (ERMP). If cache mode has been enabled, a Read Multiple command will be issued on all read cycles, except op code fetches, when the following conditions have been met:

1. The CLSE and ERMP bits must be set.
2. The Cache Line Size register must contain a legal burst size value (2, 4, 8, 16, 32, 64, or 128) AND that value must be less than or equal to the DMODE burst size.
3. The number of bytes to be transferred at the time a cache boundary has been reached must be at least twice the full cache line size.
4. The chip must be aligned to a cache line boundary.

When these conditions have been met, the chip will issue a Read Multiple command instead of a Memory Read during all PCI read cycles.

Burst Size Selection

The Read Multiple command reads in multiple cache lines of data in a single bus ownership. The number of cache lines to be read is a multiple of the cache line size as allowed for in the PCI Specification, Revision 2.1. The logic will select the largest multiple of the cache line size based on the

amount of data to transfer, with the maximum allowable burst size being determined from the DMODE Burst Size bits and CTEST 5, bit 2.

Read Multiple with Read Line Enabled

When both the Read Multiple and Read Line modes have been enabled, the Read Line command will not be issued if the above conditions are met. Instead, a Read Multiple command will be issued, even though the conditions for Read Line have been met.

If the Read Multiple mode is enabled and the Read Line mode has been disabled, Read Multiple commands will still be issued if the Read Multiple conditions are met.

Unsupported PCI Commands

The SYM53C895 does not respond to reserved commands, special cycle, dual address cycle, or interrupt acknowledge commands as a slave. It will never generate these commands as a master.

Configuration Registers

The Configuration registers are accessible only by the system BIOS during PCI configuration cycles, and are not available to the user at any time. No other cycles, including SCRIPTS operations, can access these registers. The lower 128 bytes hold configuration data while the upper 128 bytes hold the SYM53C895 operating registers, which are described in Chapter Five, “Operating Registers.” These registers can be accessed by SCRIPTS or the host processor.

Note: The configuration register descriptions provide general information only to indicate which PCI configuration addresses are supported in the SYM53C895. For detailed information, refer to the PCI Specification.

Table 3-2 shows the PCI configuration registers implemented by the SYM53C895. Addresses 40h through 7Fh are not defined.

All PCI-compliant devices, such as the SYM53C895, must support the Vendor ID, Device ID, Command, and Status Registers. Support of other PCI-compliant registers is optional. In the SYM53C895, registers that are not supported are not writable and will return all zeroes when read. Only those registers and bits that are currently supported by the SYM53C895 are described in this chapter. For more detailed information on PCI registers, please see the PCI Specification.

Table 3-2: PCI Configuration Register Map

31	16	15	0	
Device ID = 000Ch		Vendor ID = 1000h		00h
Status		Command		04h
Class Code = 010000h			Rev ID = 0Xh	08h
Not Supported	Header Type	Latency Timer	Cache Line Size	0Ch
Base Address Zero (I/O)[1]				10h
Base Address One (Memory)[2]				14h
RAM Base Address[3]				18h
Not Supported				1Ch
Not Supported				20h
Not Supported				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address[4]				30h
Reserved				34h
Reserved				38h
Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	3Ch

[1]I/O Base is supported
[2]Memory Base is supported
Note: Addresses 40h to 7Fh are not defined. All unsupported registers are not writable and will return all zeroes when read. Reserved registers will also return zeroes when read.
[3]This register powers up enabled and can be disabled by pull-down resistors on the MAD5 pin
[4]If expansion memory is enabled through pull-down resistors on the MAD(7-0) bus.

Register 00h
Vendor ID
Read Only

This field identifies the manufacturer of the device. The Symbios Vendor ID is 1000h.

Register 02h
Device ID
Read Only

This field identifies the particular device. The SYM53C895 device ID is 0Ch.

Register 04h
Command
Read/Write

The Command Register, illustrated in Figure 3-1, provides coarse control over a device's ability to generate and respond to PCI cycles. When a zero is written to this register, the SYM53C895 is logically disconnected from the PCI bus for all accesses except configuration accesses.

In the SYM53C895, bits 3, 5, 7, and 9 are not implemented. Bits 10 through 15 are reserved.

Bits 15-9 Reserved

Bit 8 SERR/ Enable
This bit enables the SERR/ driver. SERR/ is disabled when this bit is clear. The default value of this bit is zero. Bit 8 and bit 6 must be set to report address parity errors.

Bit 7 Reserved

Bit 6 Enable Parity Error Response
This bit allows the SYM53C895 to detect parity errors on the PCI bus and report these errors to the system. Only data parity checking is enabled. The SYM53C895 always generates parity for the PCI bus.

Bit 5 Reserved

Bit 4 Write and Invalidate Mode
Setting this bit will cause Memory Write and Invalidate cycles to be issued on the PCI bus after certain conditions have been met. For more information on these conditions, refer to the section "Memory Write and Invalidate Command". To enable Write and Invalidate Mode, bit 0 in the CTEST3 register (operating register set) must also be set.

Bit 3 Reserved

Bit 2 Enable Bus Mastering
This bit controls the SYM53C895's ability to act as a master on the PCI bus. A value of zero disables the device from generating PCI bus master accesses. A value of one allows the SYM53C895 to behave as a bus master. The SYM53C895 must be a bus master in order to fetch SCRIPTS instructions and transfer data.

Bit 1 Enable Memory Space
This bit controls the SYM53C895's response to Memory Space accesses. A value of zero disables the device response. A value of one allows the SYM53C895 to respond to Memory Space accesses at the address specified by Base Address One.

Bit 0 Enable I/O Space
This bit controls the SYM53C895's response to I/O space accesses. A value of zero disables the response. A value of one allows the SYM53C895 to respond to I/O space accesses at the address specified in Base Address Zero.

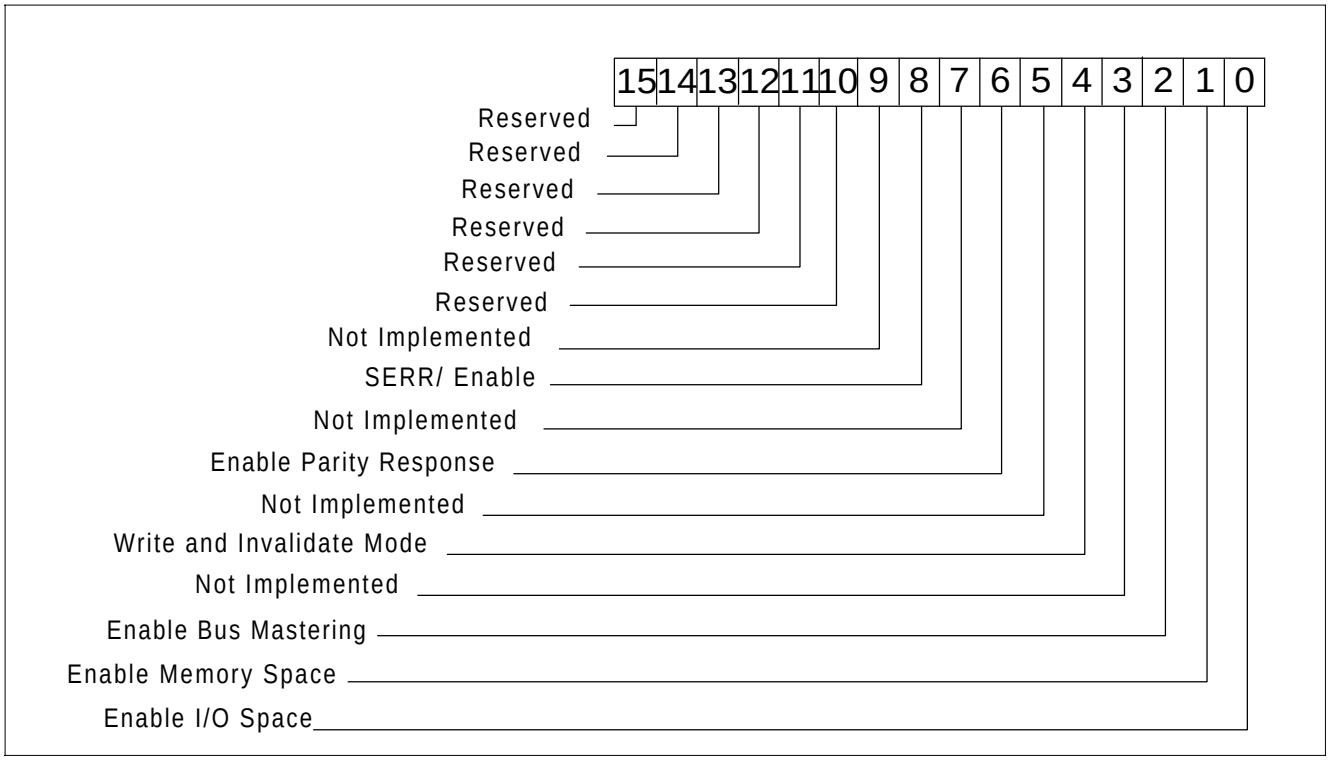


Figure 3-1: Command Register Layout

Register 06h
Status
Read/Write

The Status Register, illustrated in Figure 3-2, is used to record status information for PCI bus-related events.

In the SYM53C895, bits 0 through 4 are reserved and bits 5, 6, 7, and 11 are not implemented by the SYM53C895.

Reads to this register behave normally. Writes are slightly different in that bits can be cleared, but not set. A bit is reset whenever the register is written, and the data in the corresponding bit location is a one. For instance, to clear bit 15 and not affect any other bits, write the value 8000h to the register.

Bit 15 Detected Parity Error (from Slave)
This bit will be set by the SYM53C895 whenever it detects a data parity error, even if parity error handling is disabled.

Bit 14 Signaled System Error
This bit is set whenever a device asserts the SERR/ signal.

Bit 13 Master Abort (from Master)
This bit should be set by a master device whenever its transaction (except for Special Cycle) is terminated with master abort. All master devices should implement this bit.

Bit 12 Received Target Abort (from Master)
This bit should be set by a master device whenever its transaction is terminated with a target abort. All master devices should implement this bit.

Bit 11 Reserved

Bits 10-9 DEVSEL/ Timing

These bits encode the timing of DEVSEL/. These are encoded as 00b for fast, 01b for medium, 10b for slow with 11b reserved. These bits are read-only and should indicate the slowest time that a device asserts DEVSEL/ for any bus command except Configuration Read and Configuration Write. In the SYM53C895, 01b is supported.

Bit 8 Data Parity Reported

This bit is set when the following three conditions are met: 1) The bus agent asserted PERR/ itself or observed PERR/ asserted; 2) The agent setting this bit acted as the bus master for the operation in which the error occurred; 3) The Parity Error Response bit in the Command register is set.

Bits 7-0 Reserved

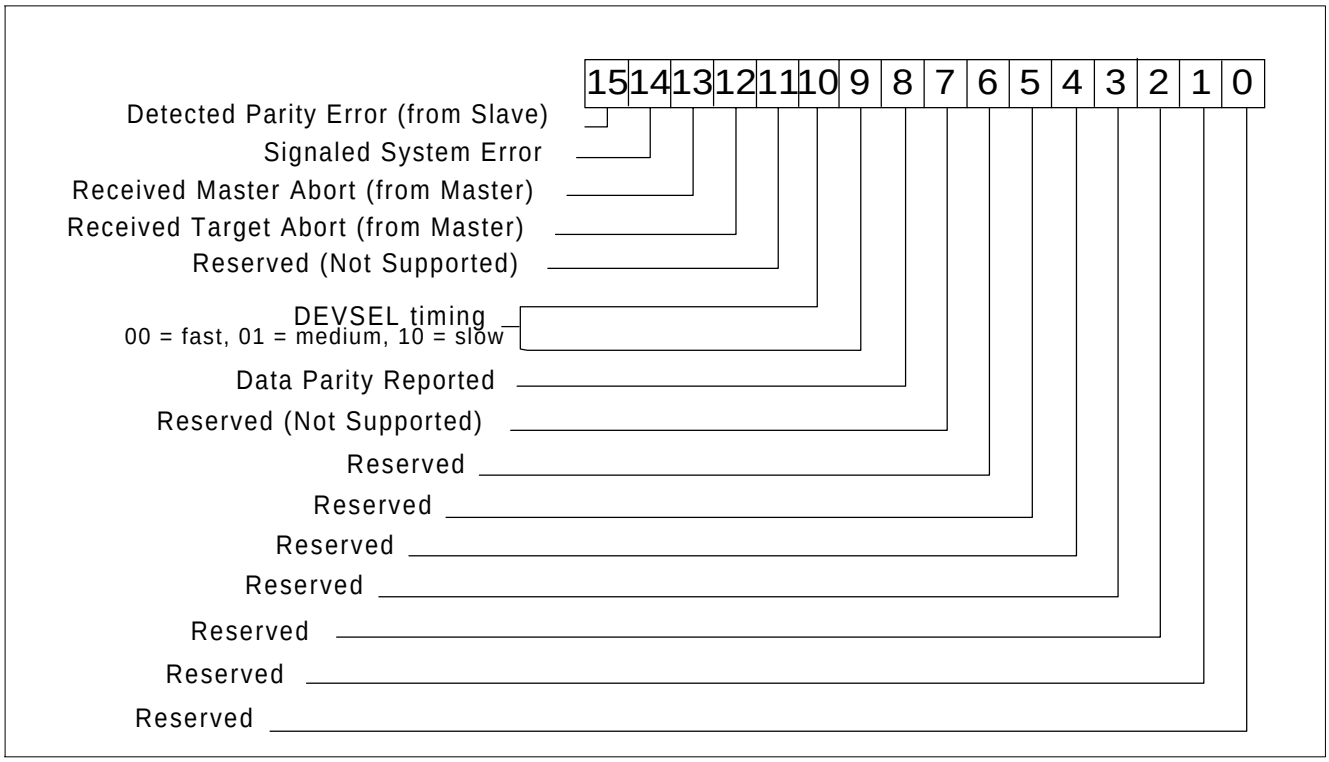


Figure 3-2: Status Register Layout

Register 08h
Revision ID
Read Only

This register specifies device and revision identifiers. In the SYM53C895, the upper nibble will be 0000b. The lower nibble reflects the current revision level of the device. It should have the same value as the Chip Revision Level bits in the CTEST3 register.

Register 09h
Class Code
Read Only

This register identifies the generic function of the device. The upper byte of this register is a base class code, the middle byte is a subclass code, and the lower byte identifies a specific register-level programming interface. The value of this register is 010000h, which indicates a SCSI controller.

Register 0Ch
Cache Line Size
Read/Write

This register specifies the system cache line size in units of 32-bit words. Cache mode is enabled and disabled by the Cache Line Size Enable (CLSE) bit, bit 7 in the DCNTL register. Setting this bit causes the SYM53C895 to align to cache line boundaries before allowing any bursting, except during Memory Moves in which the read and write addresses are not aligned to a burst size boundary. For more information on this register, see the section "Support for PCI Cache Line Size Register".

Register 0Dh
Latency Timer
Read/Write

The Latency Timer register specifies, in units of PCI bus clocks, the value of the Latency Timer for this PCI bus master. The SYM53C895 supports this timer. All eight bits are writable, allowing latency values of 0-255 PCI clocks. Use the following equation to calculate an optimum latency value for the SYM53C895:

Latency = 2 + (Burst Size * (typical wait states +1)).

Values greater than optimum are also acceptable.

Register 0Eh
Header Type
Read Only

This register identifies the layout of bytes 10h through 3Fh in configuration space and also whether or not the device contains multiple functions. The value of this register is 00h.

Register 10h
Base Address Zero (I/O)
Read/Write

This 32-bit register has bit zero hardwired to one. Bit 1 is reserved and must return a zero on all reads, and the other bits are used to map the device into I/O space.

Register 14h
Base Address One (Memory)
Read/Write

This register has bit 0 hardwired to zero. For detailed information on the operation of this register, refer to the PCI Specification.

Register 18h
RAM Base Address
Read/Write

This register holds the memory base address of the 4 KB internal RAM. The user can read this register through the SCRATCHB register in the operating register set when bit 3 of the CTEST2 register is set.

Register 2C-2D
Subsystem Vendor ID
Read Only

This register uniquely identifies the vendor manufacturing the add-in board or subsystem where the SYM53C895 resides. It provides a mechanism for an add-in card vendor to distinguish its cards from another vendor's cards, even if the cards use the same PCI controller (and therefore have the same Vendor ID and Device ID). See the Serial EEPROM Interface section in Chapter 2 for information about the values to load in this register. If the external serial EEPROM interface is enabled, this register is automatically loaded at power-up from the EEPROM. All of the bits in this register are cleared if serial EEPROM access is not enabled.

Register 2E-2F
Subsystem ID
Read Only

This register uniquely identifies the board or subsystem where the SYM53C895 resides. It provides a mechanism for an add-in card vendor to distinguish between its cards that use the same PCI controller (and therefore have the same vendor ID, Device ID, and Subsystem Vendor ID). See the Serial EEPROM Interface section in Chapter 2 for information about the values to load in this register. If the external serial EEPROM interface is enabled, this register is automatically loaded at powerup from the EEPROM. All of the bits in this register are cleared if serial EEPROM access is not enabled.

In some operating system implementations, Bit 15 of this register indicates whether the SYM53C895 is being controlled by Symbios software or by a different device driver. A value of 0 indicates that the Symbios software controls the chip, and a value of 1 indicates another driver.

Register 30h
Expansion ROM Base Address
Read/Write

This four-byte register handles the base address and size information for expansion ROM. It functions exactly like the Base Address Zero and Base Address One registers, except that the encoding of the bits is different. The upper 21 bits correspond to the upper 21 bits of the expansion ROM base address.

The Expansion ROM Enable bit, bit 0, is the only bit defined in this register. This bit is used to control whether or not the device accepts accesses to its expansion ROM. When the bit is set, address decoding is enabled, and a device can be used with or without an expansion ROM depending on the system configuration. To access the external memory interface, the Memory Space bit in the Command register must also be set.

The host system detects the size of the external memory by first writing the Expansion ROM Base Address register with all ones and then reading back the register. The SYM53C895 will respond with zeros in all don't care locations. The ones in the remaining bits represent the binary version of the external memory size. For example, to indicate an external memory size of 32 KB, this register, when written with ones and read back, will return ones in the upper 17 bits.

Register 3Ch
Interrupt Line
Read/Write

This register communicates interrupt line routing information. POST software will write the routing information into this register as it initiates and configures the system. The value in this register tells which input of the system interrupt controller(s) the device's interrupt pin has been connected to. Values in this register are specified by system architecture.

Register 3Dh
Interrupt Pin
Read Only

This register tells which interrupt pin the device uses. Its value is set to 01h, for the INTA/ signal.

Register 3Eh
Min_Gnt
Read Only

Register 3Fh
Max_Lat
Read Only

These registers specify the desired settings for Latency Timer values. Min_Gnt specifies how long a burst period the device needs. Max_Lat specifies how often the device needs to gain access to the PCI bus. The value specified in these registers is in units of 0.25 microseconds. Values of zero indicate that the device has no major requirements for the settings of Latency Timers. The SYM53C895 sets the Min_Gnt register to 11h and the Max_Lat register to 40h.

Chapter 4
Signal Descriptions

This chapter presents the SYM53C895 pin configuration and signal definitions using tables and illustrations. Figure 4-1 through Figure 4-3 are the pin diagrams for the SYM53C895 and Figure 4-4 is the functional signal grouping. Table 4-1 and Table 4-2 list the BGA ball assignments by location and signal name. The pin definitions are in Table 4-3 through Table 4-14. The pin definitions are organized into the following functional groups: System, Address/Data, Interface Control, Arbitration, Error Reporting, SCSI, and Optional Interface. A slash (/) at the end of the signal name indicates that the active state occurs when the signal is at a low voltage. When the slash is absent, the signal is active at a high voltage.

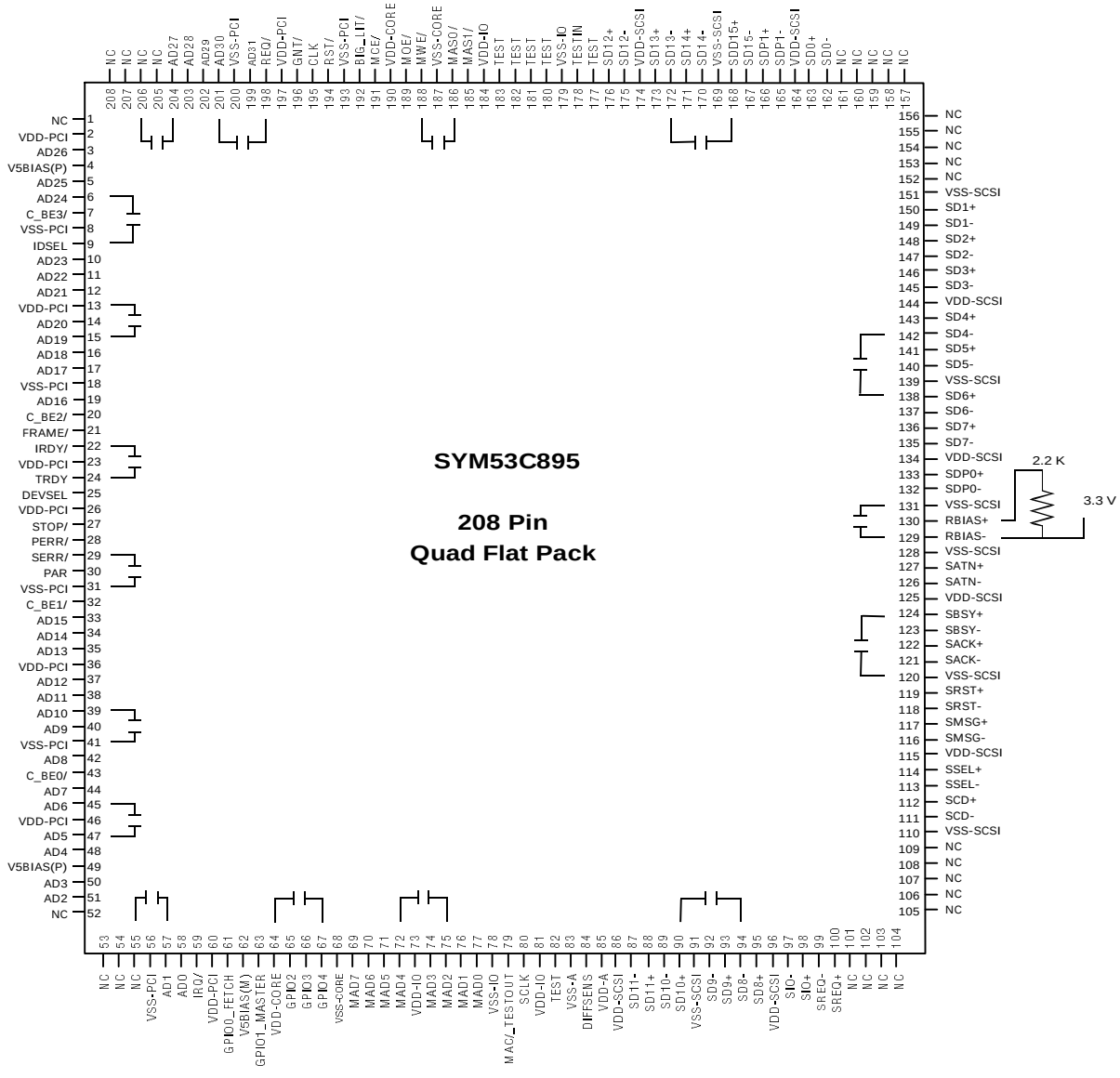
There are four signal type definitions:

I	Input, a standard input-only signal
O	Totem Pole Output, a standard output driver
T/S	Tri-State, a bi-directional, tri-state input/output pin
S/T/S	Sustained tri-state, an active low tri-state signal owned and driven by one and only one agent at a time

Voltage Capabilities and Limitations

The SYM53C895 uses 5 Volt biasing pins to allow the device to handle up to 5 Volt input voltage to the PCI and external memory interface pins. When the SYM53C895 is used in a 5 Volt PCI system, the biasing pins (V5BIAS(P)) must be supplied with 5 Volts; when they are used in a 3 Volt only PCI environment, they must be supplied with 3.3 Volts. The external memory pins (GPIO pins and MAD7-0) also use 5 Volt-tolerant I/O pads. They also have a 5 Volt biasing pin (V5BIAS(M)). These pins should be supplied with 5 Volts when using 5 Volt memory devices, and with 3.3 Volts when using 3.3 Volt memory devices. The SCLK input is also a 5V-tolerant input pin.

The chip cannot operate normally if the 5 Volt biasing pins are grounded or disconnected. In addition, the PCI biasing pins should not be shorted to the memory bias pin if mixed voltage environments (such as 5 Volt PCI with 3 Volt memories) are possible. All other V_{DD} supplies to the SYM53C895 must be set for 3.3 Volt operation. In addition, the chip will only drive 3.3 Volts on any of the pins when they operate as outputs.



The decoupling capacitor arrangement shown above is recommended to maximize the benefits of the internal split ground system. Capacitor values between 0.01 and 0.1µF should provide adequate noise isolation. Because of the number of high current drivers on the SYM53C895, a multi-layer PC board with power and ground planes is required.

Figure 4-1: SYM53C895 Pin Diagram, 208-pin QFP

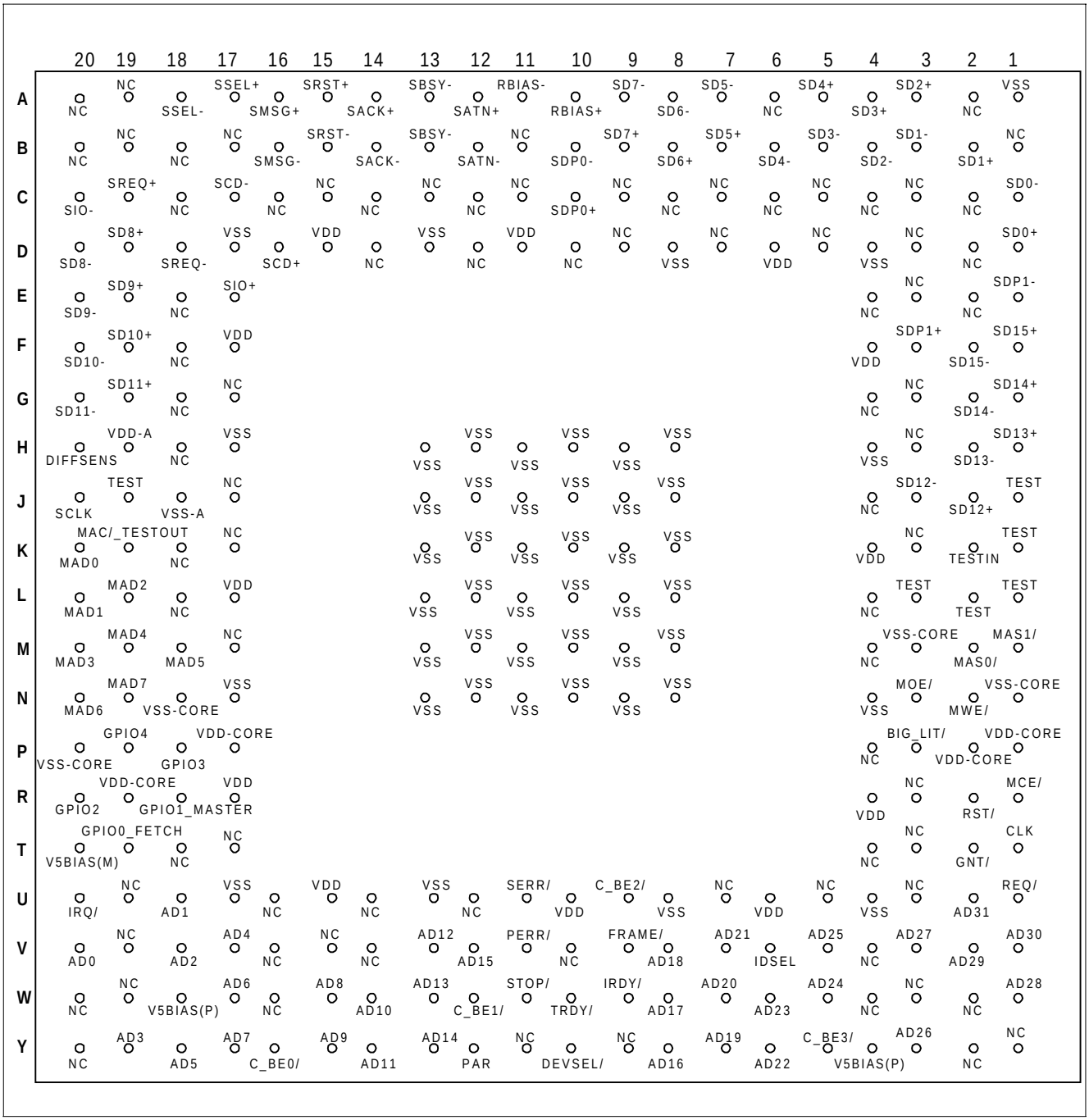


Figure 4-2: SYM53C895 Pin Diagram, 292-ball BGA (bottom view)

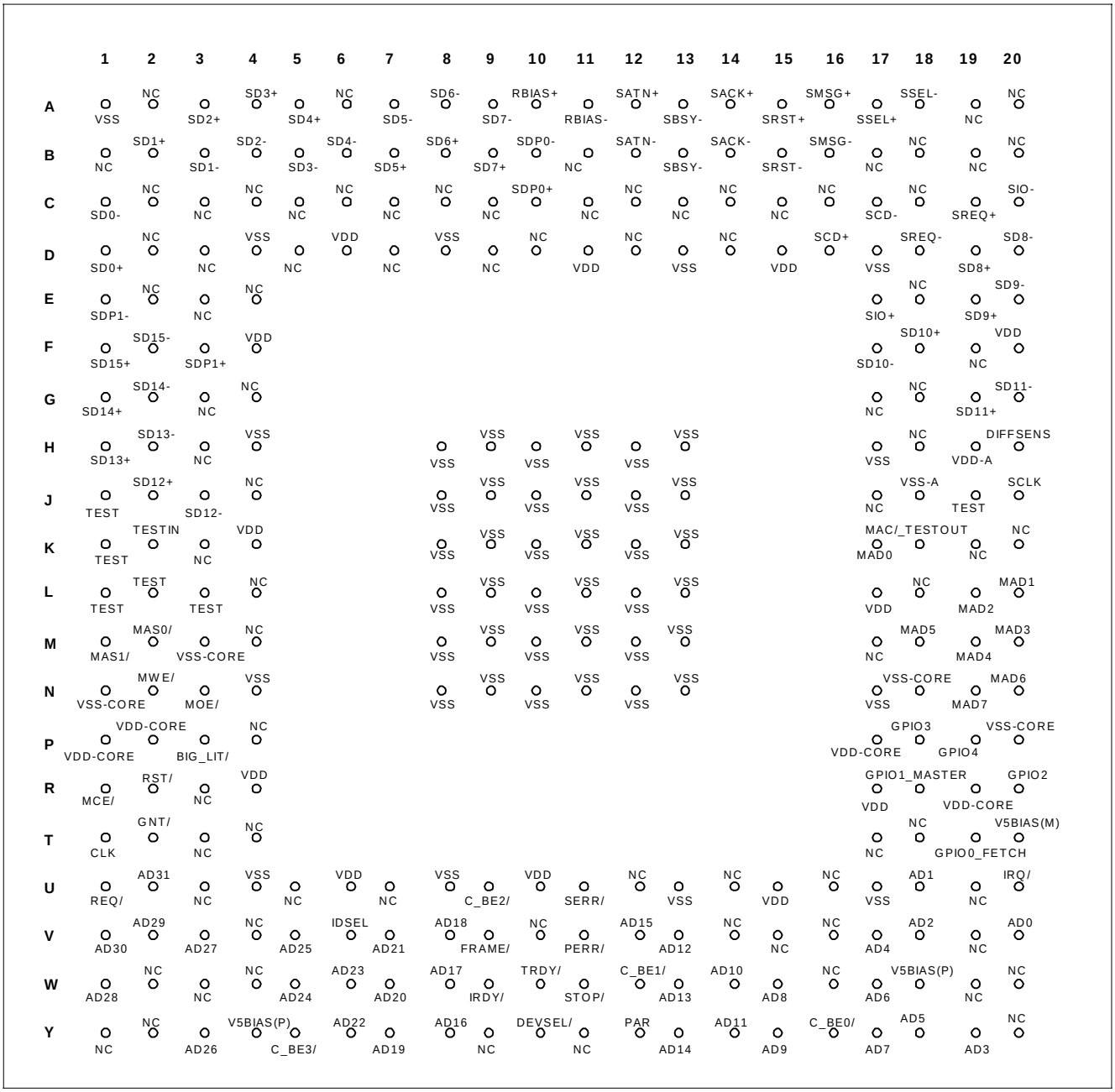


Figure 4-3: SYM53C895 Pin Diagram, 292-ball BGA (top view)

Table 4-1: BGA Listing Location

A3	SD2+
A4	SD3+
A5	SD4+
A7	SD5-
A8	SD6-
A9	SD7-
A10	RBIAS+
A11	RBIAS-
A12	SATN+
A13	SBSY+
A14	SACK+
A15	SRST+
A16	SMSG+
A17	SSEL+
A18	SSEL-
B2	SD1+
B3	SD1-
B4	SD2-
B5	SD3-
B6	SD4-
B7	SD5+
B8	SD6+
B9	SD7+
B10	SDP0-
B12	SATN-
B13	SBSY-
B14	SACK-
B15	SRST-
B16	SMSG-
C1	SD0-
C10	SDP0+
C17	SCD-
C19	SREQ+
C20	SIO-
D1	SD0+
D16	SCD+
D18	SREQ-
D19	SD8+
D20	SD8-
E1	SDP1-
E17	SIO+
E19	SD9+
E20	SD9-
F1	SD15+
F2	SD15-
F3	SDP1+
F19	SD10+
F20	SD10-
G1	SD14+/
G2	SD14-
G19	SD11+
G20	SD11-
H1	SD13+
H2	SD13-
H20	DIFFSENS
J1	TEST
J2	SD12+
J3	SD12-
J19	TEST
J20	SCLK
K1	TEST
K2	TESTIN
K19	MAC/ _TESTOUT
K20	MAD0
L1	TEST
L2	TEST
L3	TEST
L19	MAD2
L20	MAD1
M1	MAS1/
M2	MAS0/
M18	MAD5
M19	MAD4
M20	MAD3
N2	MWE/
N3	MOE/
N19	MAD7
N20	MAD6
P3	BIG_LIT/
P18	GPIO3
P19	GPIO4
R1	MCE/
R2	RST/
R18	GPIO1_MASTER
R20	GPIO2
T1	CLK
T2	GNT/
T19	GPIO0_FETCH
U1	REQ/
U2	AD31
U9	C_BE2/
U11	SERR/
U18	AD1
U20	IRQ/
V1	AD30
V2	AD29
V3	AD27
V5	AD25
V6	IDSEL
V7	AD21
V8	AD18
V9	FRAME/
V11	PERR/
V12	AD15
V13	AD12
V17	AD4
V18	AD2
V20	AD0
W1	AD28
W5	AD24
W6	AD23
W7	AD20
W8	AD17
W9	IRDY/
W10	TRDY/
W11	STOP
W12	C_BE1/
W13	AD13
W14	AD10
W15	AD8
W17	AD6
Y3	AD26
Y5	C_BE3/
Y6	AD22
Y7	AD19
Y8	AD16
Y10	DEVSEL/
Y12	PAR
Y13	AD14
Y14	AD11
Y15	AD9
Y16	C_BE0/
Y17	AD7
Y18	AD5
Y19	AD3

Table 4-2: BGA Listing by Name

AD0	V20
AD1	U18
AD10	W14
AD11	Y14
AD12	V13
AD13	W13
AD14	Y13
AD15	V12
AD16	Y8
AD17	W8
AD18	V8
AD19	Y7
AD2	V18
AD20	W7
AD21	V7
AD22	Y6
AD23	W6
AD24	W5
AD25	V5
AD26	Y3
AD27	V3
AD28	W1
AD29	V2
AD3	Y19
AD30	V1
AD31	U2
AD4	V17
AD5	Y18
AD6	W17
AD7	Y17
AD8	W15
AD9	Y15
BIG_LIT/	P3
C_BE0/	Y16
C_BE1/	W12
C_BE2/	U9
C_BE3/	Y5
CLK	T1
DEVSEL/	Y10
DIFFSENS	H20
FRAME/	V9
GNT/	T2
GPIO0_FETCH	T19
GPIO1_MASTER	R18
GPIO2	R20
GPIO3	P18
GPIO4	P19
IDSEL	V6
IRDY/	W9
IRQ/	U20
MAC/_TESTOUT	K19
MAD0	K20
MAD1	L20
MAD2	L19
MAD3	M20
MAD4	M19
MAD5	M18
MAD6	N20
MAD7	N19
MAS0/	M2
MAS1/	M1
MCE/	R1
MOE/	N3
MWE/	N2
PAR	Y12
PERR/	V11
RBIAS+	A10
RBIAS-	A11
REQ/	U1
RST/	R2
SACK+	A14
SACK-	B14
SATN+	A12
SATN-	B12
SBSY+	A13
SBSY-	B13
SCD+	D16
SCD-	C17
SCLK	J20
SD0+	D1
SD0-	C1
SD1+	B2
SD1-	B3
SD10+	F19
SD10-	F20
SD11+	G19
SD11-	G20
SD12+	J2
SD12-	J3
SD13+	H1
SD13-	H2
SD14+/	G1
SD14-	G2
SD15+	F1
SD15-	F2
SD2+	A3
SD2-	B4
SD3+	A4
SD3-	B5
SD4+	A5
SD4-	B6
SD5+	B7
SD5-	A7
SD6+	B8
SD6-	A8
SD7+	B9
SD7-	A9
SD8+	D19
SD8-	D20
SD9+	E19
SD9-	E20
SDP0+	C10
SDP0-	B10
SDP1+	F3
SDP1-	E1
SERR/	U11
SIO+	E17
SIO-	C20
SMSG+	A16
SMSG-	B16
SREQ+	C19
SREQ-	D18
SRST+	A15
SRST-	B15
SSEL+	A17
SSEL-	A18
STOP	W11
TEST	J1
TEST	J19
TEST	K1
TEST	L1
TEST	L2
TEST	L3
TESTIN	K2
TRDY/	W10

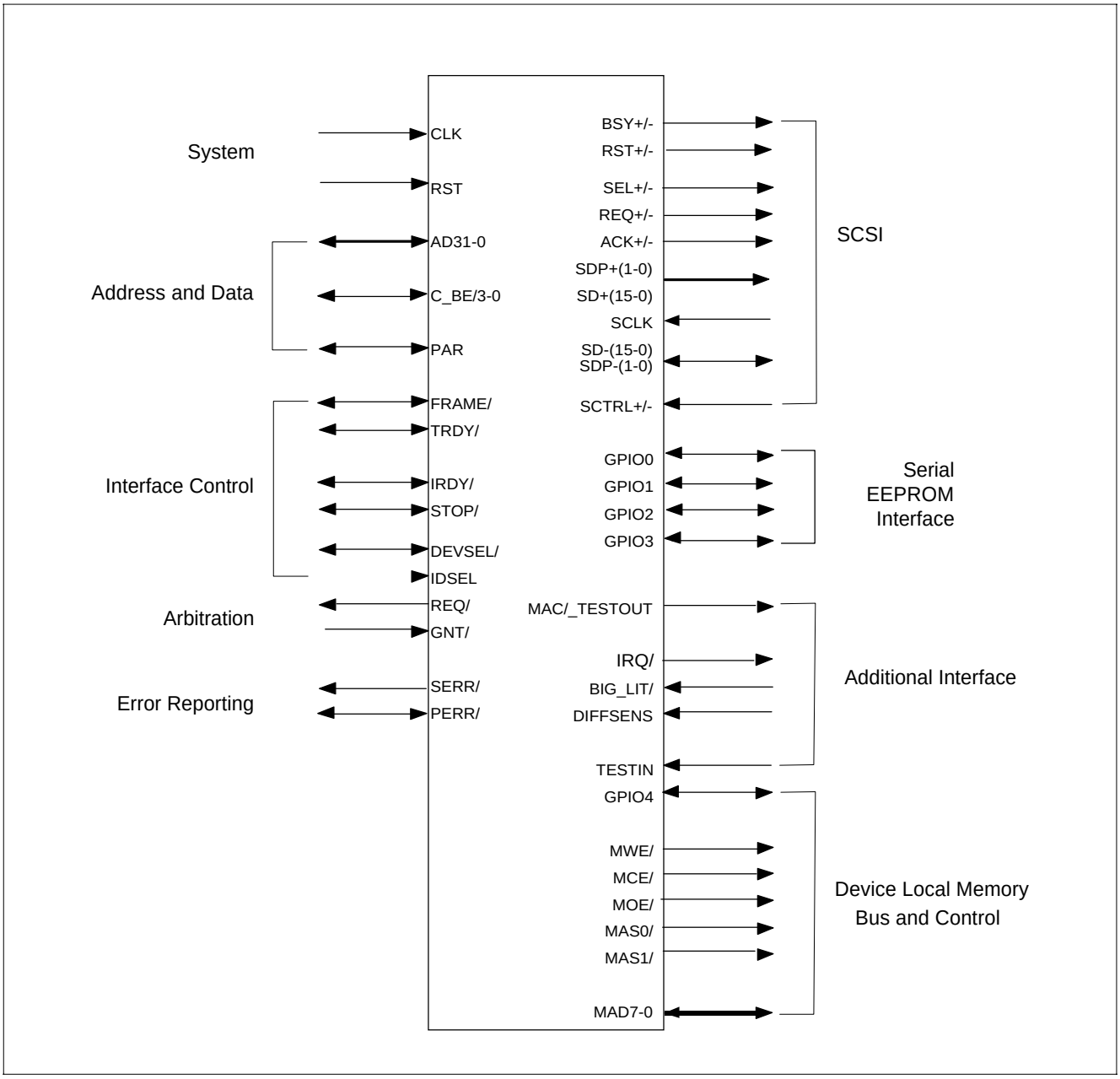


Figure 4-4: SYM53C895 Functional Signal Grouping

Internal Pull-ups on SYM53C895 Pins

Several pins on the SYM53C895 use internal pull-ups. Table 4-3 describes the conditions under which these pull-ups are enabled or disabled.

Table 4-3: SYM53C895 Internal Pull-ups

Pin Name	Pull-up current	Conditions for pull-up
PCI pins except IRQ, CLK and RST	25 µA	Pull-ups enabled when and-tree mode is enabled by driving TESTIN low
IRQ	25 µA	Pull-up enabled when and-tree mode is enabled by driving TESTIN low or when the IRQ mode bit (bit 3 of DCNTL (3Bh)) is cleared*
RST, CLK	n/a	No pull-up
MAD (7-0)	n/a	No pull-ups
MAS/(1-0), MCE/, MOE/, MWE/	25 µA	Pull-up enabled when and-tree mode is enabled by driving TESTIN low or if the ZMODE bit (bit7 of CTEST4 (21h)) is set
GPIO(4-0)	n/a	No pull-ups
SCSI pads and SCLK	n/a	No pull-ups
RBIAS+, RBIAS-	n/a	No pull-ups
DIFFSENS	n/a	No pull-up, analog input protect pin
BIG_LIT/	25 µA	Pull-up enabled when and-tree mode is enabled by driving TESTIN low
MAC/_TESTOUT	n/a	No pull-up, output only
TEST pin 82	25 µA	Pull-up all the time
TEST pin 177	25 µA	Pull-up all the time
TESTIN	25 µA	Pull-up all the time
TEST pins 180, 181, 182, 183	25 µA	Pull-up enabled when and-tree mode is enabled by driving TESTIN low or if a hidden bit (bit7 of STEST0 (4Ch)) is cleared (default = cleared)

**When bit 3 of DCNTL is set, the pad becomes a totem pole output pad and will drive both high and low.*

Pin Descriptions

Table 4-4: SYM53C895 Power and Ground Pins

Symbol	Pin No. Ball No.	Description
V_{SS-PCI}*	8, 18, 31, 41, 56, 193, 200 (Pins)	Power supplies to the PCI I/O pins
V_{DD-PCI}*	2, 13, 23, 26, 36, 46, 60, 197 (Pins)	Power supplies to the PCI I/O pins
$V_{SS-SCSI}$*	91, 110, 120, 128, 131, 139, 151, 169 (Pins)	Power supplies to the SCSI bus I/O pins
$V_{DD-SCSI}$*	86, 96, 115, 125, 134, 144, 164, 174 (Pins)	Power supplies to the SCSI bus I/O pins
V_{SS-IO}*	78, 179	Power supplies to the external memory interface
V_{DD-IO}*	73, 81, 184	Power supplies to the external memory interface
$V_{SS-CORE}$	68, 187 N18, P20, N1, M3	Power supplies to the internal logic core
$V_{DD-CORE}$	64, 190 P17, R19, P2, P1	Power supplies to the internal logic core
V_{SS-A}	83 J18	Power pins used by analog circuitry
V_{DD-A}	85 H19	Power pins used by analog circuitry Note: The V_{DD-A} pin is sensitive to noise above 90 mV at frequencies above 140 MHz. Refer to ** for information on filtering schemes to protect this pin and the phase locked loop from high frequency noise.
V5BIAS(P)	4, 49 W18, Y4	5 Volt biasing pins for PCI signals. These pins must be supplied with 5V in a 5V PCI environment, or 3.3V when used in a 3V only PCI environment.
V5BIAS(M)	62 T20	5 Volt biasing pin for external memory interface signals. When using 5V memory devices, this pin should be supplied with 5V. When using 3.3V memory devices, it should be supplied with 3.3V.

All V_{DD} pins must be supplied 3.3 Volts. The SYM53C895 output signals drive 3.3V.

**In the BGA option, $V_{DD-SCSI}$, V_{DD-PCI}, and V_{DD-IO} are connected together and $V_{SS-SCSI}$, V_{SS-PCI} and V_{SS-IO} are connected together at package.*

***Optional ground pins*

Table 4-4: SYM53C895 Power and Ground Pins (Continued)

Symbol	Pin No. Ball No.	Description
V_{SS}*	A1, D4, H4, N4, UR, D8, H8**, J8, K8**, L8**, M8**, N8**, U8, H9**, J9**, K9**, L9**, M9**, N9**, H10**, J10**, K10**, L10**, M10**, N10**, H11**, J11**, K11**, L11**, M11**, N11**, H12**, J12**, K12**, L12**, M12**, N12**, D13, H13**, J13**, K13**, L13**, M13**, N13, U13, D17, H17, N17, U17	Power pins
V_{DD}*	F4, K4, R4, D6, U6, D11, U10, D15, U15, F17, L17, R17	Power supplies

All V_{DD} pins must be supplied 3.3 Volts. The SYM53C895 output signals drive 3.3V.

**In the BGA option, $V_{DD-SCSI}$, V_{DD-PCI}, and V_{DD-IO} are connected together and $V_{SS-SCSI}$, V_{SS-PCI} and V_{SS-IO} are connected together at package.*

***Optional ground pins*

Note: If you apply separate power supplies to the V_{DD-IO} and $V_{DD-CORE}$ pins in a chip testing environment, either power up the pins simultaneously or power up $V_{DD-CORE}$ before V_{DD-IO}. The V_{DD-IO} pins must always power down before $V_{DD-CORE}$.

Table 4-5: System Pins

Symbol	Pin No. Ball No.	Type	Description
CLK	195 T1	I	Clock provides timing for all transactions on the PCI bus and is an input to every PCI device. All other PCI signals are sampled on the rising edge of CLK, and other timing parameters are defined with respect to this edge. This clock can optionally be used as the SCSI core clock; however, the SYM53C895 will not be able to achieve Fast SCSI-2 (or faster) transfer rates.
RST/	194 R2	I	Reset forces the PCI sequencer of each device to a known state. All T/S and S/T/S signals are forced to a high impedance state, and all internal logic is reset. The RST/ input is synchronized internally to the rising edge of CLK. The CLK input must be active while RST/ is active to properly reset the device.

Table 4-6: Address and Data Pins

Symbol	Pin No. Ball No.	Type	Description
AD(31-0)	199, 201-204, 3, 5, 6, 10-12, 14-17, 19, 33-35, 37-40, 42, 44, 45, 47, 48, 50, 51, 57, 58 U2, V1, V2, W1, V3, Y3, V5, W5, W6, Y6, V7, W7, Y7, V8, W8, Y8, V12, Y13, W13, V13, Y14, W14, Y15, W15, Y17, W17, V17, Y19, V18, U18, V20	T/S	Physical longword address and data are multiplexed on the same PCI pins. During the first clock of a transaction, AD(31-0) contain a physical address. During subsequent clocks, AD(31-0) contain data. A bus transaction consists of an address phase, followed by one or more data phases. PCI supports both read and write bursts. AD(7-0) define the least significant byte, and AD(31-24) define the most significant byte.

Table 4-6: Address and Data Pins (Continued)

Symbol	Pin No. Ball No.	Type	Description
C_BE(3-0)/	7, 20, 32, 43 Y5, U9, W12, Y16	T/S	Bus commands and byte enables are multiplexed on the same PCI pins. During the address phase of a transaction, C_BE(3-0)/ define the bus command. During the data phase, C_BE(3-0)/ are used as byte enables. The byte enables determine which byte lanes carry meaningful data. C_BE(0)/ applies to byte 0, and C_BE(3)/ applies to byte 3.
PAR	30 Y12	T/S	Parity is the even parity bit that protects the AD(31-0) and C_BE(3-0)/ lines. During address phase, both the address and command bits are covered. During data phase, both data and byte enables are covered.

Table 4-7: Interface Control Pins

Symbol	Pin No. Ball No.	Type	Description
FRAME/	21 V9	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access. FRAME/ is asserted to indicate a bus transaction is beginning. While FRAME/ is asserted, data transfers continue. When FRAME/ is deasserted, the transaction is in the final data phase or the bus is idle.
TRDY/	24 W10	S/T/S	Target Ready indicates the selected device's ability to complete the current data phase of the transaction. TRDY/ is used with IRDY/. A data phase is completed on any clock when both TRDY/ and IRDY/ are sampled asserted. During a read, TRDY/ indicates that valid data is present on AD(31-0). During a write, it indicates the target is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
IRDY/	22 W9	S/T/S	Initiator Ready indicates the bus master's ability to complete the current data phase of the transaction. This signal is used with TRDY/. A data phase is completed on any clock when both IRDY/ and TRDY/ are sampled asserted. During a write, IRDY/ indicates that valid data is present on AD(31-0). During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY/ and TRDY/ are asserted together.
STOP/	27 W11	S/T/S	Stop indicates that the selected target is requesting the master to stop the current transaction.
DEVSEL/	25 Y10	S/T/S	Device Select indicates that the driving device has decoded its address as the target of the current access. As an input, it indicates to a master whether any device on the bus has been selected.
IDSEL	9 V6	I	Initialization Device Select is used as a chip select in place of the upper 24 address lines during configuration read and write transactions.

Table 4-8: Arbitration Pins

Symbol	Pin No. Ball No.	Type	Description
REQ/	198 U1	O	Request indicates to the arbiter that this agent desires use of the PCI bus. This is a point-to-point signal. Every master has its own REQ/.
GNT/	196 T2	I	Grant indicates to the agent that access to the PCI bus has been granted. This is a point-to-point signal. Every master has its own GNT/.

Table 4-9: Error Reporting Pins

Symbol	Pin No. Ball No.	Type	Description
PERR/	28 V11	S/T/S	Parity Error may be pulsed active by an agent that detects a data parity error. PERR/ can be used by any agent to signal data corruptions.
SERR/	29 U11	O	This open drain output pin reports address parity errors. On detection of a PERR/ pulse, the central resource may generate a non-maskable interrupt to the host CPU, which often implies the system will be unable to continue operation once error processing is complete.

Table 4-10: SCSI Pins, LVDlink Mode

Symbol	Pin No. Ball No.	Type	Description
SCLK	80 J20	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application's requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied low. For Ultra2 SCSI operation, this pin must be connected to an external 40 MHz oscillator, used with the internal clock quadrupler.
SD-(15-0), SDP-(1-0)	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132 F2, G2, H2, J3, G20, F20, E20, D20, A9, A8, A7, B6, B5, B4, B3, C1, E1, B10	I/O	Negative half of LVDlink signal pair for SCSI data lines. SCSI Data includes the following data lines and parity signals: SD(15-0)/(16-bit SCSI data bus), and SDP(1-0)/(SCSI data parity bits).
SD+(15-0), SDP+(1-0)	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133 F1, G1, H1, J2, G19, F19, E19, D19, B9, B8, B7, A5, A4, A3, B2, D1, F3, C10	I/O	Positive half of LVDlink signal pair for SCSI data lines.
SCTRL-	111, 97, 116, 99, 121, 123, 126, 118, 113 C17, C20, B16, D18, B14, B13, B12, B15, A18	I/O	Negative half of LVDlink signal pair for SCSI Control, which includes the following signals: SCD-SCSI phase line, command/data SIO-SCSI phase line, input/output SMSG-SCSI phase line, message SREQ-Data handshake signal from target device SACK-Data handshake signal from initiator device SBSY-SCSI bus arbitration signal, busy SATN-SCSI Attention, the initiator is requesting a message out phase SRST-SCSI bus reset SSEL-SCSI bus arbitration signal, select device

Table 4-10: SCSI Pins, LVDlink Mode (Continued)

Symbol	Pin No. Ball No.	Type	Description
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114 D16, E17, A16, C19, A14, A13, A12, A15, A17	I/O	Positive half of LVDlink signal pair for SCSI Control, which includes the following signals: SCD+SCSI phase line, command/data SIO+SCSI phase line, input/output SMSG+SCSI phase line, message SREQ+Data handshake signal from target device SACK+Data handshake signal from initiator device SBSY+SCSI bus arbitration signal, busy SATN+SCSI Attention, the initiator is requesting a message out phase SRST+SCSI bus reset SSEL+SCSI bus arbitration signal, select device
RBIAS+, RBIAS-	130, 129 A10, A11	I	Used to connect an external resistor to generate the bias current used by LVDlink pads.
DIFFSENS	84 H20	I	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a single-ended, LVD, or high-power differential device. The result is displayed in STEST4 bits 7-6. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs will be tri-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. Note: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4-11: SCSI Pins, Single-Ended Mode

Symbol	Pin No. Ball No.	Type	Description
SCLK	80 J20	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application's requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied low.
SD-(15-0), SDP-(1-0)	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132 F2, G2, H2, J3, G20, F20, E20, D20, A9, A8, A7, B6, B5, B4, B3, C1, E1, B10	I/O	SCSI Data includes the following data lines and parity signals: SD(15-0)/(16-bit SCSI data bus), and SDP(1-0)/(SCSI data parity bits).
SD+(15-0), SDP+(1-0)	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133 F1, G1, H1, J2, G19, F19, E19, D19, B9, B8, B7, A5, A4, A3, B2, D1, F3, C10	O	These signals will drive 0 Volts.
SCTRL-	111, 97, 116, 99, 121, 123, 126, 118, 113 C17, C20, B16, D18, B14, B13, B12, B15, A18	I/O	SCSI Control, includes the following signals: SCD-SCSI phase line, command/data SIO-SCSI phase line, input/output SMSG-SCSI phase line, message SREQ-Data handshake signal from target device SACK-Data handshake signal from initiator device SBSY-SCSI bus arbitration signal, busy SATN-SCSI Attention, the initiator is requesting a message out phase SRST-SCSI bus reset SSEL-SCSI bus arbitration signal, select device

Table 4-11: SCSI Pins, Single-Ended Mode (Continued)

Symbol	Pin No. Ball No.	Type	Description
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114 D16, E17, A16, C19, A14, A13, A12, A15, A17	O	These pins drive 0 Volts.
DIFFSENS	84 H20	I	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a single-ended, LVD, or high-power differential device. The result is displayed in STEST4 bits 7-6. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs will be tri-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. Note: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4-12: SCSI Pins, High Voltage Differential Mode

SCLK	80	I	SCLK derives all SCSI-related timings. The speed of this clock is determined by the application's requirements; in some applications SCLK may be sourced internally from the PCI bus clock (CLK). If SCLK is internally sourced, then the SCLK pin should be tied low.
SD-(15-0) SDP-(1-0)	167, 170, 172, 175, 87, 89, 92, 94, 135, 137, 140, 142, 145, 147, 149, 162, 165, 132	I/O	SCSI data lines. SCSI Data includes the following data lines and parity signals: SD(15-0)/(16-bit SCSI data bus), and SDP(1-0)/ (SCSI data parity bits).
SD+(15-0) SDP+(1-0)	168, 171, 173, 176, 88, 90, 93, 95, 136, 138, 141, 143, 146, 148, 150, 163, 166, 133	O	Driver direction control for SCSI data lines.

Table 4-12: SCSI Pins, High Voltage Differential Mode (Continued)

SCTRL-	111, 97, 116, 99, 121, 123, 126, 118, 113	I/O	SCSI Control includes the following signals: SCD- SCSI phase line, command/data SIO- SCSI phase line, input/output SMSG- SCSI phase line, message SREQ- Data handshake signal from target device SACK- Data handshake signal from initiator device SBSY- SCSI bus arbitration signal, busy SATN- SCSI Attention, the initiator is requesting a message out phase SRST- SCSI bus reset SSEL- SCSI bus arbitration signal, select device
SCTRL+	112, 98, 117, 100, 122, 124, 127, 119, 114	O	Driver direction control for the external transceivers, which includes the following signals: SREQ+ Data handshake signal from target device SACK+ Data handshake signal from initiator device SBSY+ SCSI bus arbitration signal, busy SRST+ SCSI bus reset SSEL+ SCSI bus arbitration signal, select device Note: For high voltage differential operation, SCD+, SIO+, SMSG+, and SATN+ are not used.
DIFFSENS	84	1	The Differential Sense pin detects the voltage level of an incoming SCSI signal to determine whether it is from a single-ended, LVD, or high-power differential device. The result is displayed in STEST4 bits 7-6. When external differential transceivers are used and a high level is detected on this pin, all chip SCSI outputs will be tri-stated to avoid damage to the transceivers. This pin should be connected to the DIFFSENS signal on the SCSI cable. Note: The maximum voltage allowed to this pin is 3.3 Volts.

Table 4-13: Additional Pins

TESTIN	178	I	Test In. When this pin is driven low, the SYM53C895 connects all inputs and outputs to an "AND tree." The SCSI control signals and data lines are not connected to the "AND tree." The output of the "AND tree" is connected to the TESTOUT pin. This allows manufacturers to verify chip connectivity and determine exactly which pins are not properly attached. When the TESTIN pin is driven low, internal pull-ups are enabled on all input, output, and bidirectional pins, all outputs and bidirectional signals will be tri-stated, and the MAC/_TESTOUT pin will be enabled. Connectivity can be tested by driving one of the SYM53C895 pins low. The MAC/_TESTOUT pin should respond by also driving low.
GPIO0_ FETCH/	61	I/O	General Purpose I/O pin. Optionally, when driven low, this pin indicates that the next bus request will be for an op code fetch. This pin powers up as a general purpose input. This pin has two specific purposes in the Symbios software. The software uses it to toggle SCSI device LEDs, turning on the LED whenever the SYM53C895 is on the SCSI bus. The software drives this pin low to turn on the LED, or drives it high to turn off the LED. This signal can also be used as data I/O for serial EEPROM access. In this case, it is used with the GPIO1 pin, which serves as a clock.
GPIO1_ MASTER/	63	I/O	General purpose I/O pin. Optionally, when driven low, this pin indicates that the SYM53C895 is bus master. This pin powers up as a general purpose input. Symbios software supports use of this signal in serial EEPROM applications, when enabled, in combination with the GPIO0 pin. When this signal is used as a clock for serial EEPROM access, the GPIO0 pin serves as data.
GPIO4-2	67-65	I/O	General purpose I/O pins. GPIO4 powers up as an output. Symbios software also supports use of this signal as the enable line for V_{PP}, the 12 Volt power supply to the external flash memory interface. GPIO3-2 power up as inputs.
MAC/_ TESTOUT	79	T/S	Memory Access Control. This pin can be programmed to indicate local or system memory accesses (non-PCI applications). It is also used to test the connectivity of the SYM53C895 signals using "AND tree" scheme. The MAC/_TESTOUT pin is only driven as the Test Out function when the TESTIN/ pin is driven low.
IRQ/	59	O	Interrupt. This signal, when asserted low, indicates that an interrupting condition has occurred and that service is required from the host CPU. The output drive of this pin is programmed as either open drain with an internal weak pull-up or, optionally, as a totem pole driver. Refer to the description of DCNTL Register, bit 3, for additional information.

Table 4-13: Additional Pins (Continued)

BIG_LIT/	192	I	Big_Little Endian Select. When this pin is driven low, the SYM53C895 will route the first byte of an aligned SCSI to PCI transfer to byte lane zero of the PCI bus and subsequent bytes received will be routed to ascending lanes. An aligned PCI to SCSI transfer will route PCI byte lane zero onto the SCSI bus first, and transfer ascending byte lanes in order. When this pin is driven high, the SYM53C895 will route the first byte of an aligned SCSI-to-PCI transfer to byte lane three of the PCI bus and subsequent bytes received will be routed to descending lanes. An aligned PCI-to-SCSI transfer will route PCI byte lane three onto the SCSI bus first and transfer descending byte lanes in order. This mode of operation also applies to the external memory interface. When this pin is driven in Little Endian mode and the chip is performing a read from external memory, the byte of data accessed at location 00000h will be routed to PCI byte lane zero and the data accessed at location 00003h will be routed to PCI byte lane three. When the chip is performing a write to flash memory, PCI byte lane zero will be routed to location 00000h and ascending byte lanes will be routed to subsequent memory locations. When this pin is driven in Big Endian mode and the chip is performing a read from external memory, the byte of data accessed at location 00000h will be routed to PCI byte lane three and the data accessed at location 00003h will be routed to byte lane zero. When the chip is performing a write to flash memory, PCI byte lane three will be routed to location 00000h and descending byte lanes will be routed to subsequent memory locations.
Test Pins	82, 177, 180, 181, 182, 183	I/O	Test Pins are used by Symbios for diagnostic testing. These pins should not be used in actual system design; they must be left floating or pulled high.

Table 4-14: External Memory Interface Pins

MAS0/	186	O	Memory Address Strobe 0. This pin latches in the least significant address byte of an external EPROM or flash memory. Since the SYM53C895 moves addresses eight bits at a time, this pin connects to the clock of an external bank of flip-flops which are used to assemble up to a 20-bit address for the external memory.
MAS/1	185	O	Memory Address Strobe 1. This pin latches in the address byte corresponding to address bits 15-8 of an external EPROM or flash memory. Since the SYM53C895 moves addresses eight bits at a time, this pin connects to the clock of an external bank of flip-flops which assemble up to a 20-bit address for the external memory.
MAD7-0	See individual pin descriptions		The MAD7-0 pins form the memory address/data bus. This bus is used in conjunction with the memory address strobe pins and external address latches to assemble up to a 20-bit address for an external EPROM or flash memory. This bus will put out the most significant byte first and finish with the least significant byte. It is also used to write data to a flash memory or read data into the chip from external EPROM or flash memory. The eight signals on the MAD bus have specific functions. Please refer to the individual pin description below.
MAD7-6	69-70	I/O	MAD7-6 enable different power-up options related to the external serial EEPROM interface. These options are programmed by connecting a 4.7 KΩ resistor between the appropriate MAD pin and V_{SS}. For more information, refer to the Serial EEPROM Interface section in Chapter 2 and the Subsystem ID/Subsystem Vendor ID register descriptions in Chapter 3.
MAD5	71	I/O	The MAD5 pin enables/disables the 4K internal RAM on the SYM53C895. Pull this pin high to enable the SCRIPTS RAM (default), and pull it low (with a 4 KΩ resistor) to disable the SCRIPTS RAM.

MAD(7-6)	Result
00	Vendor specific information is automatically downloaded from the serial EEPROM through BPIO0 (clock) and BPIO1 (data) and loaded into PCI configuration registers 2C-2Fh.
01	Reserved.
10	No download is performed, however, the PCI configuration registers 2C-2Fh are now writable.
11	Vendor-specific information is automatically downloaded from the EEPROM through GPIO0 (data) and GPIO1 (clock) and loaded into PCI configuration registers 2C-2Fh.

Table 4-14: External Memory Interface Pins (Continued)

<table>
<tr><td>MAD4</td><td>72</td><td>I/O</td><td>The MAD4 pin is reserved and should be pulled up. It may be used by Symbios in future devices.</td></tr>
<tr><td>MAD3-1</td><td>74-76</td><td>I/O</td><td>The MAD(3-1) pins set the size of the external parallel ROM device attached to the SYM53C895. Encoding for these pins is listed below (0 indicates a pull-down resistor is attached, 1 indicates a pull-up resistor is attached).

<table><tr><th>MAD(3-1)</th><th>Available Memory Space</th></tr><tr><td>000</td><td>16 KB</td></tr><tr><td>001</td><td>32 KB</td></tr><tr><td>010</td><td>64 KB</td></tr><tr><td>011</td><td>128 KB</td></tr><tr><td>100</td><td>256 KB</td></tr><tr><td>101</td><td>512 KB</td></tr><tr><td>110</td><td>1024 KB</td></tr><tr><td>111</td><td>no external memory present</td></tr></table></td></tr>
<tr><td>MAD0</td><td>77</td><td>I/O</td><td>MAD0 is the slow ROM pin. When pulled down, it enables two extra clock cycles of data access time. This accommodates a 200 ns memory device on the MAD bus. When the pin is high, a 150 ns or faster memory device must be used.</td></tr>
<tr><td>MWE/</td><td>188</td><td>O</td><td>Memory Write Enable. This pin is used as a write the enable signal to an external flash memory.</td></tr>
<tr><td>MOE/</td><td>189</td><td>O</td><td>Memory Output Enable. This pin is used as an output enable signal to an external EPROM or flash memory during read operations.</td></tr>
<tr><td>MCE/</td><td>191</td><td>O</td><td>Memory Chip Enable. This pin is used as a chip enable signal to an external EPROM or flash memory device.</td></tr>
</table>

Chapter 5
Operating Registers

This section contains descriptions of all SYM53C895 operating registers. Table 5-1 summarizes the SYM53C895 operating register set. Figure 5-1, the register map, lists registers by operating and configuration addresses. The terms “set” and “assert” refer to bits that are programmed to a binary one. Similarly, the terms “deassert,” “clear” and “reset” refer to bits that are programmed to a binary zero. Reserved bit functions may be changed at any time; these bits should never be set by the user. Unless otherwise indicated, all bits in registers are active high, that is, the feature is enabled by setting the bit. The bottom row of every register diagram shows the default register values, which are enabled after the chip is powered on or reset.

Note: The only register that the host CPU can access while the SYM53C895 is executing SCRIPTS is the ISTAT register; attempts to access other registers will interfere with the operation of the chip. However, all operating registers are accessible with SCRIPTS. All read data is synchronized and stable when presented to the PCI bus.

Note: The SYM53C895 cannot fetch SCRIPTS instructions from the operating register space. Instructions must be fetched from system memory or the internal SCRIPTS RAM.

Table 5-1: Operating Register Addresses and Descriptions

Memory or I/O Address Offset	PCI Configuration Address	Read/Write	Label	Description	Page No.
00	80	R/W	SCNTL0	SCSI Control 0	5-5
01	81	R/W	SCNTL1	SCSI Control 1	5-7
02	82	R/W	SCNTL2	SCSI Control 2	5-9
03	83	R/W	SCNTL3	SCSI Control 3	5-10
04	84	R/W	SCID	SCSI Chip ID	5-12
05	85	R/W	SXFER	SCSI Transfer	5-12
06	86	R/W	SDID	SCSI Destination ID	5-15
07	87	R/W	GPREG	General Purpose Bits	5-15
08	88	R/W	SFBR	SCSI First Byte Received	5-16
09	89	R/W	SOCL	SCSI Output Control Latch	5-16
0A	8A	R	SSID	SCSI Selector ID	5-17
0B	8B	R/W	SBCL	SCSI Bus Control Lines	5-17
0C	8C	R	DSTAT	DMA Status	5-18
0D	8D	R	SSTAT0	SCSI Status 0	5-19
0E	8E	R	SSTAT1	SCSI Status 1	5-20

Table 5-1: Operating Register Addresses and Descriptions (Continued)

Memory or I/O Address Offset	PCI Configuration Address	Read/Write	Label	Description	Page No.
0F	8F	R	SSTAT2	SCSI Status 2	5-21
10-13	90-93	R/W	DSA	Data Structure Address	5-22
14	94	R/W	ISTAT	Interrupt Status	5-23
18	98	R/W	CTEST0	Reserved	5-25
19	99	R/W	CTEST1	Chip Test 1	5-25
1A	9A	R	CTEST2	Chip Test 2	5-26
1B	9B	R	CTEST3	Chip Test 3	5-27
1C-1F	9C-9F	R/W	TEMP	Temporary Register	5-28
20	A0	R/W	DFIFO	DMA FIFO	5-28
21	A1	R/W	CTEST4	Chip Test 4	5-29
22	A2	R/W	CTEST5	Chip Test 5	5-30
23	A3	R/W	CTEST6	Chip Test 6	5-31
24-26	A4-A6	R/W	DBC	DMA Byte Counter	5-32
27	A7	R/W	DCMD	DMA Command	5-32
28-2B	A8-AB	R/W	DNAD	DMA Next Address for Data	5-33
2C-2F	AC-AF	R/W	DSP	DMA SCRIPTS Pointer	5-33
30-33	B0-B3	R/W	DSPS	DMA SCRIPTS Pointer Save	5-34
34-37	B4-B7	R/W	SCRATCHA	General Purpose Scratch Pad A	5-34
38	B8	R/W	DMODE	DMA Mode	5-35
39	B9	R/W	DIEN	DMA Interrupt Enable	5-36
3A	BA	R/W	SBR	Scratch Byte Register	5-37
3B	BB	R/W	DCNTL	DMA Control	5-37
3C-3F	BC-BF	R	ADDER	Sum output of internal adder	5-38
40	C0	R/W	SIEN0	SCSI Interrupt Enable 0	5-39
41	C1	R/W	SIEN1	SCSI Interrupt Enable 1	5-40
42	C2	R	SIST0	SCSI Interrupt Status 0	5-41
43	C3	R	SIST1	SCSI Interrupt Status 1	5-42
44	C4	R/W	SLPAR	SCSI Longitudinal Parity	5-43
45	C5	R	SWIDE	SCSI Wide Residue Data	5-44
46	C6	R/W	MACNTL	Memory Access Control	5-45
47	C7	R/W	GPCNTL	General Purpose Control	5-45
48	C8	R/W	STIME0	SCSI Timer 0	5-46
49	C9	R/W	STIME1	SCSI Timer 1	5-47
4A	CA	R/W	RESPID0	Response ID 0	5-48

Table 5-1: Operating Register Addresses and Descriptions (Continued)

Memory or I/O Address Offset	PCI Configuration Address	Read/Write	Label	Description	Page No.
4B	CB	R/W	RESPID1	Response ID 1	5-48
4C	CC	R	STEST0	SCSI Test 0	5-49
4D	CD	R	STEST1	SCSI Test 1	5-50
4E	CE	R/W	STEST2	SCSI Test 2	5-51
4F	CF	R/W	STEST3	SCSI Test 3	5-52
50-51	D0-D1	R	SIDL	SCSI Input Data Latch	5-54
52	D2	R	STEST4	SCSI Test 4	5-54
53	D3		Reserved		
54-55	D4-D5	R/W	SODL	SCSI Output Data Latch	5-55
56-57	D6-D7		Reserved		
58-59	D8-D9	R	SBDL	SCSI Bus Data Lines	5-55
5A-5B	DA-DB		Reserved		
5C-5F	DC-DF	R/W	SCRATCHB	General Purpose Scratch Pad B	5-56
60-7F	E0-FF	R/W	SCRATCHC-J	General Purpose Scratch Pad C-J	5-56

				Mem I/O	Config
SCNTL3	SCNTL2	SCNTL1	SCNTL0	00	80
GPREG	SDID	SXFER	SCID	04	84
SBCL	SSID	SOCL	SFBR	08	88
SSTAT2	SSTAT1	SSTAT0	DSTAT	0C	8C
DSA				10	90
RESERVED			ISTAT	14	94
CTEST3	CTEST2	CTEST1	RESERVED	18	98
TEMP				1C	9C
CTEST6	CTEST5	CTEST4	DFIFO	20	A0
DCMD	DBC			24	A4
DNAD				28	A8
DSP				2C	AC
DSPS				30	B0
SCRATCH A				34	B4
DCNTL	SBR	DIEN	DMODE	38	B8
ADDER				3C	BC
SIST1	SIST0	SIEN1	SIEN0	40	C0
GPCNTL	MACNTL	SWIDE	SLPAR	44	C4
RESPID1	RESPID0	STIME1	STIME0	48	C8
STEST3	STEST2	STEST1	STEST0	4C	CC
RESERVED	STEST4	SIDL		50	D0
RESERVED		SODL		54	D4
RESERVED		SBDL		58	D8
SCRATCH B				5C	DC
SCRATCHC				60	E0
SCRATCHD				64	E4
SCRATCHE				68	E8
SCRATCHF				6C	EC
SCRATCHG				70	F0
SCRATCHH				74	F4
SCRATCHI				78	F8
SCRATCHJ				7F	FF

Figure 5-1: SYM53C895 Register Address Map

Register 00 (80)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN	EPC	RES	AAP	TRG
7	6	5	4	3	2	1	0
Default>>>							
1	1	0	0	0	X	0	0

Bit 7 ARB1 (Arbitration Mode bit 1)

Bit 6 ARB0 (Arbitration Mode bit 0)

ARB1	ARB0	Arbitration Mode
0	0	Simple arbitration
0	1	Reserved
1	0	Reserved
1	1	Full arbitration, selection/reselection

Simple Arbitration

1. The SYM53C895 waits for a bus free condition to occur.
2. It asserts SBSY/ and its SCSI ID (contained in the SCID register) onto the SCSI bus. If the SSEL/ signal is asserted by another SCSI device, the SYM53C895 will deassert SBSY/, deassert its ID and set the Lost Arbitration bit (bit 3) in the SSTAT0 register.
3. After an arbitration delay, the CPU should read the SBDL register to check if a higher priority SCSI ID is present. If no higher priority ID bit is set, and the Lost Arbitration bit is not set, the SYM53C895 has won arbitration.
4. Once the SYM53C895 has won arbitration, SSEL/ must be asserted via the SOCL for a bus clear plus a bus settle delay (1.2 µs) before a low-level selection can be performed.

Full Arbitration, Selection/Reselection

1. The SYM53C895 waits for a bus free condition.
2. It asserts SBSY/ and its SCSI ID (the highest priority ID stored in the SCID register) onto the SCSI bus.
3. If the SSEL/ signal is asserted by another SCSI device or if the SYM53C895 detects a higher priority ID, the SYM53C895 will deassert BSY, deassert its ID, and wait until the next bus free state to try arbitration again.
4. The SYM53C895 repeats arbitration until it wins control of the SCSI bus. When it has won, the Won Arbitration bit is set in the SSTAT0 register, bit 2.
5. The SYM53C895 performs selection by asserting the following onto the SCSI bus: SSEL/, the target's ID (stored in the SDID register), and the SYM53C895's ID (stored in the SCID register).
6. After a selection is complete, the Function Complete bit is set in the SIST0 register, bit 6.
7. If a selection time-out occurs, the Selection Time-Out bit is set in the SIST1 register, bit 2.

Bit 5 START (Start Sequence)

When this bit is set, the SYM53C895 will start the arbitration sequence indicated by the Arbitration Mode bits. The Start Sequence bit is accessed directly in low-level mode; during SCSI SCRIPTS operations, this bit is controlled by the SCRIPTS processor. An arbitration sequence should not be started if the connected (CON) bit in the SCNTL1 register, bit 4, indicates that the SYM53C895 is already connected to the SCSI bus. This bit is automatically cleared when the arbitration sequence is complete. If a sequence is aborted, bit 4 in the SCNTL1 register should be checked to verify that the SYM53C895 did not connect to the SCSI bus.

Bit 4 WATN (Select with SATN/ on a Start Sequence)

When this bit is set and the SYM53C895 is in initiator mode, the SATN/ signal will be asserted during SYM53C895 selection of a SCSI target device. This is to inform the target that the SYM53C895 has a message to send. If a selection time-out occurs while attempting to select a target device, SATN/ will be deasserted at the same time SSEL/ is deasserted. When this bit is clear, the SATN/ signal will not be asserted during selection. When executing SCSI SCRIPTS, this bit is controlled by the SCRIPTS processor, but it may be set manually in low-level mode.

Bit 3 EPC (Enable Parity Checking)

When this bit is set, the SCSI data bus is checked for odd parity when data is received from the SCSI bus in either initiator or target mode. Parity is also checked as data goes from the SCSI FIFO to the DMA FIFO. If a parity error is detected, bit 0 of the SIST0 register is set and an interrupt may be generated.

If the SYM53C895 is operating in initiator mode and a parity error is detected, SATN/ can optionally be asserted, but the transfer continues until the target changes phase. When this bit is cleared, parity errors are not reported.

Bit 2 Reserved

Bit 1 AAP (Assert SATN/ on Parity Error)

When this bit is set, the SYM53C895 automatically asserts the SATN/ signal upon detection of a parity error. SATN/ is only asserted in initiator mode. The SATN/ signal is asserted before deasserting SACK/ during the byte transfer with the parity error. The Enable Parity Checking bit must also be set for the SYM53C895 to assert SATN/ in this manner. A parity error is detected on data received from the SCSI bus.

If the Assert SATN/ on Parity Error bit is cleared or the Enable Parity Checking bit is cleared, SATN/ will not be automatically asserted on the SCSI bus when a parity error is received.

Bit 0 TRG (Target Mode)

This bit determines the default operating mode of the SYM53C895. The user must manually set target or initiator mode. This can be done using the SCRIPTS language (SET TARGET or CLEAR TARGET). When this bit is set, the chip is a target device by default. When this bit is cleared, the SYM53C895 is an initiator device by default.

CAUTION:

Writing this bit while not connected may cause the loss of a selection or reselection due to the changing of target or initiator modes.

Register 01 (81)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 EXC (Extra Clock Cycle of Data Setup)

When this bit is set, an extra clock period of data setup is added to each SCSI send data transfer. The extra data setup time can provide additional system design margin, though it will affect the SCSI transfer rates. Clearing this bit disables the extra clock cycle of data setup time. Setting this bit only affects SCSI send operations.

Bit 6 ADB (Assert SCSI Data Bus)

When this bit is set, the SYM53C895 drives the contents of the SCSI Output Data Latch Register (SODL) onto the SCSI data bus. When the SYM53C895 is an initiator, the SCSI I/O signal must be inactive to assert the SODL contents onto the SCSI bus. When the SYM53C895 is a target, the SCSI I/O signal must be active for the SODL contents to be asserted onto the SCSI bus. The contents of the SODL register can be asserted at any time, even before the SYM53C895 is connected to the SCSI bus. This bit should be cleared when executing SCSI SCRIPTS. It is normally used only for diagnostics testing or operation in low-level mode.

Bit 5 DHP (Disable Halt on Parity Error or ATN) (Target Only)

The DHP bit is only defined for target mode. When this bit is cleared, the SYM53C895 halts the SCSI data transfer when a parity error is detected or when the SATN/ signal is asserted. If SATN/ or a parity error is received in the middle of a data transfer, the SYM53C895 may transfer up to three additional bytes before halting to synchronize between internal core cells. During synchronous operation, the SYM53C895 transfers data until there are no outstanding synchronous offsets. If the SYM53C895 is receiving data, any data residing in the DMA FIFO is sent to memory before halting.

When this bit is set, the SYM53C895 does not halt the SCSI transfer when SATN/ or a parity error is received.

Bit 4 CON (Connected)

This bit is automatically set any time the SYM53C895 is connected to the SCSI bus as an initiator or as a target. It is set after the SYM53C895 successfully completes arbitration or when it has responded to a bus initiated selection or reselection. This bit is also set after the chip wins simple arbitration when operating in low-level mode. When this bit is clear, the SYM53C895 is not connected to the SCSI bus.

The CPU can force a connected or disconnected condition by setting or clearing this bit. This feature would be used primarily during loopback mode.

Bit 3 RST (Assert SCSI RST/ Signal)

Setting this bit asserts the SRST/ signal. The SRST/ output remains asserted until this bit is cleared. The 25 µs minimum assertion time defined in the SCSI specification must be timed out by the controlling microprocessor or a SCRIPTS loop.

Bit 2 AESP (Assert Even SCSI Parity (force bad parity))

When this bit is set, the SYM53C895 asserts even parity. It forces a SCSI parity error on each byte sent to the SCSI bus from the SYM53C895. If parity checking is enabled, then the SYM53C895 checks data received for odd parity. This bit is used for diagnostic testing and should be clear for normal operation. It can be used to generate parity errors to test error handling functions.

Bit 1 IARB (Immediate Arbitration)

Setting this bit causes the SCSI core to immediately begin arbitration once a Bus Free phase is detected following an expected SCSI disconnect. This bit is useful for multi-threaded applications. The ARB1-0 bits in SCNTL0 should be set for full arbitration and selection before setting this bit.

Arbitration will be re-tried until won. At that point, the SYM53C895 will hold BSY and SEL asserted, and wait for a select or reselect sequence to be requested. The Immediate Arbitration bit will be reset automatically when the selection or reselection sequence is completed, or times out.

An unexpected disconnect condition will clear IARB without attempting arbitration. See the SCSI Disconnect Unexpected bit (SCNTL2, bit 7) for more information on expected versus unexpected disconnects.

An immediate arbitration sequence can be aborted. First, the Abort bit in the ISTAT register should be set. Then one of two things will eventually happen:

1. The Won Arbitration bit (SSTAT0 bit 2) will be set. In this case, the Immediate Arbitration bit needs to be reset. This will complete the abort sequence and disconnect the SYM53C895 from the SCSI bus. If it is not acceptable to go to Bus Free phase immediately following the arbitration phase, a low-level selection may be performed instead.
2. The abort will complete because the SYM53C895 loses arbitration. This can be detected by the Immediate Arbitration bit being cleared. The Lost Arbitration bit (SSTAT0 bit 3) should not be used to detect this condition. No further action needs to be taken in this case.

Bit 0 SST (Start SCSI Transfer)

This bit is automatically set during SCRIPTS execution, and should not be used. It causes the SCSI core to begin a SCSI transfer, including SREQ/SACK handshaking. The determination of whether the transfer is a send or receive is made according to the value written to the I/O bit in SOCL. This bit is self-resetting. It should not be set for low-level operation.

CAUTION:

Writing to this register while not connected may cause the loss of a selection/reselection by resetting the Connected bit.

Register 02 (82)
SCSI Control Two (SCNTL2)
Read/Write

SDU	CHM	SLPMD	SLPHBEN	WSS	VUE0	VUE1	WSR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 SDU (SCSI Disconnect Unexpected)

This bit is valid in initiator mode only. When this bit is set, the SCSI core is not expecting the SCSI bus to enter the Bus Free phase. If it does, an unexpected disconnect error will be generated (see the Unexpected Disconnect bit in the SIST0 register, bit 2). During normal SCRIPTS mode operation, this bit is set automatically whenever the SCSI core is reselected, or successfully selects another SCSI device. The SDU bit should be reset with a register write (MOVE 0X00 TO SCNTL2) before the SCSI core expects a disconnect to occur, normally prior to sending an Abort, Abort Tag, Bus Device Reset, Clear Queue or Release Recovery message, or before deasserting SACK/ after receiving a Disconnect command or Command Complete message.

Bit 6 CHM (Chained Mode)

This bit determines whether or not the SCSI core is programmed for chained SCSI mode. This bit is automatically set by the Chained Block Move (CHMOV) SCRIPTS instruction and is automatically cleared by the Block Move SCRIPTS instruction (MOVE).

Chained mode is primarily used to transfer consecutive wide data blocks. Using chained mode facilitates partial receive transfers and allows correct partial send behavior. When this bit is set and a data transfer ends on an odd byte boundary, the SYM53C895 will store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

For more information, see the "Chained Mode" section in Chapter 2, "Functional Description."

Bit 5 SLPMD (SLPAR Mode Bit)

If this bit is clear, the SLPAR register functions like the SYM53C825. If this bit is set, the SLPAR register reflects the high or low byte of the SLPAR word, depending on the state of SCNTL2 bit 4. It also allows a seed value to be written to the SLPAR register.

Bit 4 SLPHBEN (SLPAR High Byte Enable)

If this bit is clear, the low byte of the SLPAR word is present in the SLPAR register. If this bit is set, the high byte of the SLPAR word is present in the SLPAR register.

Bit 3 WSS (Wide SCSI Send)

When read, this bit returns the value of the Wide SCSI Send (WSS) flag. Asserting this bit will clear the WSS flag. This clearing function is self-resetting.

When the WSS flag is high following a wide SCSI send operation, the SCSI core is holding a byte of "chain" data in the SODL register. This data will become the first low-order byte sent when married with a high-order byte during a subsequent data send transfer.

Performing a SCSI receive operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

Bit 2 VUE0 (Vendor Unique Enhancements bit 0)

This bit is a read only value indicating whether the group code field in the SCSI instruction is standard or vendor unique. If reset, the bit indicates standard group codes; if set, the bit indicates vendor unique group codes. The value in this bit is reloaded at the beginning of all asynchronous target receives. The default for this bit is reset.

Bit 1 VUE1 (Vendor Unique Enhancements bit 1)

This bit is used to disable the automatic byte count reload during Block Move instructions in the command phase. If this bit is reset, the device will reload the Block Move byte count if the first byte received is one of the standard group codes. If this bit is set, the device will not reload the Block Move byte count, regardless of the group code.

Bit 0 WSR (Wide SCSI Receive)

When read, this bit returns the value of the Wide SCSI Receive (WSR) flag. Setting this bit clears the WSR flag. This clearing function is self-resetting.

The WSR flag indicates that the SCSI core received data from the SCSI bus, detected a possible partial transfer at the end of a chained or non-chained block move command, and temporarily stored the high-order byte in the SWIDE register rather than passing the byte out the DMA channel. The hardware uses the WSR status flag to determine what behavior must occur at the start of the next data receive transfer. When the flag is set, the stored data in SWIDE may be "residue" data, valid data for a subsequent data transfer, or overrun data. The byte may be read as normal data by starting a data receive transfer.

Performing a SCSI send operation will clear this bit. Also, performing any non-wide transfer will clear this bit.

Register 03 (83)
SCSI Control Three (SCNTL3)
Read/Write

ULTRA	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ULTRA (Ultra Enable)

Setting this bit enables Ultra SCSI or Ultra2 SCSI synchronous transfer rates. The default value of this bit is 0. This bit should remain cleared if the SYM53C895 is not operating in Ultra SCSI mode or faster.

Note: Set this bit to achieve Ultra SCSI transfer rates in legacy systems that use an 80 MHz clock.

When this bit is set, the signal filtering period for SREQ/ and SACK/ automatically changes to 8 ns for Ultra2 SCSI or 15 ns for Ultra SCSI, regardless of the value of the Extend REQ/ACK Filtering bit in the STEST2 register.

Bits 6-4 SCF2-0 (Synchronous Clock Conversion Factor)

These bits select the factor by which the frequency of SCLK is divided before being presented to the synchronous SCSI control logic. The bits are encoded as per Table 5-2. For synchronous receive, the output of this divider is always divided by 4 and that value determines the transfer rate. For example, if SCLK is 160 MHz, and the SCF value is set to divide by one, then the maximum synchronous receive rate is 40 MHz((160/1)/4 = 40).

For synchronous send, the output of this divider gets divided by the transfer period (XFERP) bits in the SCSI Transfer (SXFER)

register, and that value determines the transfer rate. For valid combinations of the SCF and XFERP, see Table 5-4 and Table 5-5.

Table 5-2: Synchronous Clock Conversion Factor

SCF2	SCF1	SCF0	Factor Frequency
0	0	0	SCLK/3
0	0	1	SCLK/1
0	1	0	SCLK/1.5
0	1	1	SCLK/2
1	0	0	SCLK/3
1	0	1	SCLK/4
1	1	0	SCLK/6
1	1	1	SCLK/8

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter 2.

Bit 3 EWS (Enable Wide SCSI)

When this bit is clear, all information transfer phases are assumed to be eight bits, transmitted on SD7-0/, SDP0/. When this bit is asserted, data transfers are done 16 bits at a time, with the least significant byte on SD7-0/, SDP/ and the most significant byte on SD15-8/, SDP1/. Command, Status, and Message phases are not affected by this bit.

Clearing this bit will also clear the Wide SCSI Receive bit in the SCNTL2 register, which indicates the presence of a valid data byte in the SWIDE register.

Bits 2-0 CCF2-0 (Clock Conversion Factor)

These bits select the frequency of the SCLK for asynchronous SCSI operations. The bits are encoded as per the following table.

Table 5-3: Asynchronous Clock Conversion Factor

CCF2	CCF1	CCF0	SCSI Clock (MHz)
0	0	0	50.01-75
0	0	1	16.67-25
0	1	0	25.01-37.5
0	1	1	37.51-50
1	0	0	50.01-75
1	0	1	75.01-80.00
1	1	0	120 (not normally used)
1	1	1	160 (with clock quadrupler and 40 MHz clock)

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter 2, “Functional Description.”

Register 04 (84)
SCSI Chip ID (SCID)
Read/Write

RES	RRE	SRE	RES	ENC3	ENC2	ENC1	ENC0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	X	0	0	0	0

Bit 7 Reserved

Bit 6 RRE (Enable Response to Reselection)

When this bit is set, the SYM53C895 is enabled to respond to bus-initiated reselection at the chip ID in the RESPID0 and RESPID1 registers. Note that the SYM53C895 will not automatically reconfigure itself to initiator mode as a result of being reselected.

Bit 5 SRE (Enable Response to Selection)

When this bit is set, the SYM53C895 is able to respond to bus-initiated selection at the chip ID in the RESPID0 and RESPID1 registers. Note that the SYM53C895 will not automatically reconfigure itself to target mode as a result of being selected.

Bit 4 Reserved

Bits 3-0 Encoded Chip SCSI ID, bits 3-0

These bits are used to store the SYM53C895 encoded SCSI ID. This is the ID which the chip will assert when arbitrating for the SCSI bus. The IDs that the SYM53C895 will respond to when being selected or reselected are configured in the RESPID0 and RESPID1 registers. The priority of the 16 possible IDs, in descending order is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8

Register 05 (85)
SCSI Transfer (SXFER)
Read/Write

TP2	TP1	TP0	MO4	MO3	MO2	MO1	MO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Note: When using Table Indirect I/O commands, bits 7-0 of this register will be loaded from the I/O data structure.

Note: For additional information on how the synchronous transfer rate is determined, refer to Chapter 2, “Functional Description.”

Bits 7-5 TP2-0 (SCSI Synchronous Transfer Period)

These bits determine the SCSI synchronous transfer period (XFERP) used by the SYM53C895 when sending synchronous SCSI data in either initiator or target mode. These bits control the programmable dividers in the chip.

Note: For Ultra SCSI transfers, the ideal transfer period is 4, and 5 is acceptable. Setting the transfer period to a value greater than 5 is not recommended.

TP2	TP1	TP0	XFERP
0	0	0	4
0	0	1	5
0	1	0	6
0	1	1	7
1	0	0	8
1	0	1	9
1	1	0	10
1	1	1	11

Use the following formula to calculate the synchronous send and receive rates. Table 5-4 and Table 5-5 show examples of possible bit combinations.

Synchronous Send Rate = (SCLK/SCF)/XFERP

Synchronous Receive Rate = (SCLK/SCF) / 4

Key:

SCLK = SCSI Clock

SCF = Synchronous Clock Conversion Factor, SCNTL3 bits 6-4

XFERP = Transfer period, SXFER register bits 7-5

Table 5-4: Examples of Synchronous Transfer Periods and Rates for SCSI-1

SCLK (MHz)	SCF (SCNTL3 bits 6-4)	XFERP (SXFER bits 7-5)	Sync Send Rate (MB/s)	Sync Send Period (ns)	Sync Receive Rate (MB/s)	Synch Receive Period (ns)
80	÷ 4	4	5	200	5	200
80	÷ 4	5	4	250	5	200
66.67	÷ 3	4	5.55	180	5.55	180
66.67	÷ 3	5	4.44	225	5.55	180
50	÷ 2	4	6.25	160	6.25	160
50	÷ 2	5	5	200	6.25	160
40	÷ 2	4	5	200	5	200
37.50	÷ 1.5	4	6.25	160	6.25	160
33.33	÷ 1.5	4	5.55	180	5.55	180
25	÷ 1	4	6.25	160	6.25	160
20	÷ 1	4	5	200	5	200
16.67	÷ 1	4	4.17	240	4.17	240

Table 5-5: Example Synchronous Transfer Periods and Rates for Fast SCSI, Ultra SCSI, and Ultra2 SCSI

SCLK (MHz)	SCF (SCNTL3 bits 6-4)	XFERP (SXFER bits 7-5)	Sync Send Rate (MB/s)	Sync Send Period (ns)	Sync Receive Rate (MB/s)	Synch Receive Period (ns)
160	÷ 1	4	40	25	40	25
80	÷ 1	4	20	50	20	50
80	÷ 2	4	10	100	10	100
66.67	÷ 1.5	4	11.11	90	11.11	90
66.67	÷ 1	5	8.88	112.5	11.11	90
50	÷ 1	4	12.5	80	12.5	80
50	÷ 1	5	10	100	12.5	80
40	÷ 1	4	10	100	10	100
37.50	÷ 1	4	9.375	106.67	9.375	106.67
33.33	÷ 1	4	8.33	120	8.33	120
25	÷ 1	4	6.25	160	6.25	160
20	÷ 1	4	5	200	5	200
16.67	÷ 1	4	4.17	240	4.17	240

Bits 4-0 MO4-MO0 (Max SCSI Synchronous Offset)

These bits describe the maximum SCSI synchronous offset used by the SYM53C895 when transferring synchronous SCSI data in either initiator or target mode. The following table describes the possible combinations and their relationship to the synchronous data offset used by the SYM53C895. These bits determine the SYM53C895's method of transfer for Data In and Data Out phases only; all other information transfers will occur asynchronously.

Table 5-6: SCSI Synchronous Offset Values

MO4	MO3	MO2	MO1	MO0	Synchronous Offset
0	0	0	0	0	0-Asynchronous
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Register 06 (86)
SCSI Destination ID (SDID)
Read/Write

RES	RES	RES	RES	ENC3	ENC2	ENC1	ENC0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 Reserved

Bits 3-0 Encoded Destination SCSI ID

Writing these bits sets the SCSI ID of the intended initiator or target during SCSI reselection or selection phases, respectively. When executing SCRIPTS, the SCRIPTS processor writes the destination SCSI ID to this register. The SCSI ID is defined by the user in a SCRIPTS SELECT or RESELECT instruction. The value written should be the binary-encoded ID value. The priority of the 16 possible IDs, in descending order, is:

Highest								Lowest							
7	6	5	4	3	2	1	0	15	14	13	12	11	0	9	8

Register 07 (87)
General Purpose (GPREG)
Read/Write

RES	RES	RES	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	X	X	X	X

Bits 7-5 Reserved

Bits 4-0 GPIO4-GPIO0 (General Purpose)

These bits can be programmed through the GPCNTL Register to become inputs, outputs or to perform special functions. As an output, these pins can enable or disable external terminators. These signals can also be programmed as live inputs and sensed through a SCRIPTS Register to Register Move Instruction. GPIO(3-0) default as inputs and GPIO4 defaults as an output pin.

GPIO4 can be used to enable or disable V_{PP}, the 12-volt power supply to the external flash memory. This bit powers up with the power to the external memory disabled.

Symbios Use of GPIO Pins

Symbios software uses the GPIO0 pin to toggle SCSI device LEDs, turning on the LED whenever the SYM53C895 is on the SCSI bus. Symbios software drives this pin low to turn on the LED, or drives it high to turn off the LED.

Symbios software uses the GPIO1-0 pins to support serial EEPROM access. When serial EEPROM access is enabled, GPIO1 is used as a clock and GPIO0 is used as data.

Register 08 (88)
SCSI First Byte Received (SFBR)
Read/Write

1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the first byte received in any asynchronous information transfer phase. For example, when the SYM53C895 is operating in initiator mode, this register contains the first byte received in the Message In, Status, and Data In phases.

When a Block Move instruction is executed for a particular phase, the first byte received is stored in this register— even if the present phase is the same as the last phase. The first byte received value for a particular input phase is not valid until after a MOVE instruction is executed.

This register is also the accumulator for register read-modify-writes with the SFBR as the destination. This allows bit testing after an operation.

The SFBR is not writable via the CPU, and therefore not by a Memory Move. The Load instruction may not be used to write to this register. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate SYM53C895 register (such as the SCRATCH register), and then to the SFBR.

This register will also contain the state of the lower eight bits of the SCSI data bus during the selection phase if the COM bit in the DCNTL register is clear.

Register 09 (89)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 REQ(Assert SCSI REQ/ Signal)

Bit 6 ACK(Assert SCSI ACK/ Signal)

Bit 5 BSY(Assert SCSI BSY/ Signal)

Bit 4 SEL(Assert SCSI SEL/ Signal)

Bit 3 ATN(Assert SCSI ATN/ Signal)

Bit 2 MSG(Assert SCSI MSG/ Signal)

Bit 1 C/D(Assert SCSI C_D/ Signal)

Bit 0 I/O(Assert SCSI I_O/ Signal)

This register is used primarily for diagnostic testing or programmed I/O operation. It is controlled by the SCRIPTS processor when executing SCSI SCRIPTS. SOCL should only be used when transferring data via programmed I/O. Some bits are set (1) or reset (0) when executing SCSI SCRIPTS. Do not write to the register once the SYM53C895 starts executing normal SCSI SCRIPTS.

Register 0A (8A)
SCSI Selector ID (SSID)
Read Only

VAL	RES	RES	RES	ENID3	ENID2	ENID1	ENID0
7	6	5	4	3	2	1	0
Default>>>							
0	X	X	X	0	0	0	0

Bit 7 VAL (SCSI Valid)

If VAL is asserted, the two SCSI IDs were detected on the bus during a bus-initiated selection or reselection, and the encoded destination SCSI ID bits below are valid. If VAL is deasserted, only one ID was present and the contents of the encoded destination ID are meaningless.

Bits 6-4 Reserved

Bits 3-0 Encoded Destination SCSI ID

Reading the SSID register immediately after the SYM53C895 has been selected or reselected returns the binary-encoded SCSI ID of the device that performed the operation. These bits are invalid for targets that are selected under the single initiator option of the SCSI-1 specification. This condition can be detected by examining the VAL bit above.

Register 0B (8B)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 REQ (SREQ/ Status)

Bit 6 ACK (SACK/ Status)

Bit 5 BSY (SBSY/ Status)

Bit 4 SEL (SSEL/ Status)

Bit 3 ATN (SATN/ Status)

Bit 2 MSG (SMSG/ Status)

Bit 1 C/D (SC_D/ Status)

Bit 0 I/O (SI_O/ Status)

When read, this register returns the SCSI control line status. A bit will be set when the corresponding SCSI control line is asserted. These bits are not latched; they are a true representation of what is on the SCSI bus at the time the register is read. The resulting read data is synchronized before being presented to the PCI bus to prevent parity errors from being passed to the system. This register can be used for diagnostics testing or operation in low-level mode.

Register 0C (8C)
DMA Status (DSTAT)
Read Only

DFE	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	0	0	0	X	0

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C895 stacks interrupts). The DIP bit in the ISTAT register will also be cleared. DMA interrupt conditions may be individually masked through the DIEN register.

When performing consecutive 8-bit reads of the DSTAT, SIST0 and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure that the interrupts clear properly. See Chapter 2, "Functional Description," for more information on interrupts.

Bit 7 DFE (DMA FIFO Empty)
This status bit is set when the DMA FIFO is empty. It may be used to determine if any data resides in the FIFO when an error occurs and an interrupt is generated. This bit is a pure status bit and will not cause an interrupt.

Bit 6 MDPE (Master Data Parity Error)
This bit is set when the SYM53C895 as a master detects a data parity error, or a target device signals a parity error during a data phase. This bit is completely disabled by the Master Parity Error Enable bit (bit 3 of CTEST4).

Bit 5 BF (Bus Fault)
This bit is set when a PCI bus fault condition is detected. A PCI bus fault can only occur when the SYM53C895 is bus master, and is defined as a cycle that ends with a Bad Address or Target Abort Condition.

Bit 4 ABRT (Aborted)
This bit is set when an abort condition occurs. An abort condition occurs when a software abort command is issued by setting bit 7 of the ISTAT register.

Bit 3 SSI (Single Step Interrupt)
If the Single-Step Mode bit in the DCNTL register is set, this bit will be set and an interrupt generated after successful execution of each SCRIPTS instruction.

Bit 2 SIR (SCRIPTS Interrupt Instruction Received)
This status bit is set whenever an Interrupt instruction is evaluated as true.

Bit 1 Reserved

Bit 0 IID (Illegal Instruction Detected)
This status bit will be set any time an illegal or reserved instruction op code is detected, whether the SYM53C895 is operating in single-step mode or automatically executing SCSI SCRIPTS. Any of the following conditions during instruction execution will also cause this bit to be set:

1. The SYM53C895 is executing a Wait Disconnect instruction and the SCSI REQ line is asserted without a disconnect occurring.
2. A Block Move instruction is executed with 000000h loaded into the DBC register, indicating that zero bytes are to be moved.
3. During a Transfer Control instruction, the Compare Data (bit 18) and Compare Phase (bit 17) bits are set in the DBC register while the SYM53C895 is in target mode.
4. During a Transfer Control instruction, the Carry Test bit (bit 21) is set and either the Compare Data (bit 18) or Compare Phase (bit 17) bit is set.

5. A Transfer Control instruction is executed with the reserved bit 22 set.
6. A Transfer Control instruction is executed with the Wait for Valid phase bit (bit 16) set while the chip is in target mode.
7. A Load/Store instruction is issued with the memory address mapped to the operating registers of the chip, not including ROM or RAM.
8. A Load/Store instruction is issued when the register address is not aligned with the memory address
9. A Load/Store instruction is issued with bit 5 in the DCMD register clear or bits 3 or 2 set.
10. A Load/Store instruction when the count value in the DBC register is not set at 1 to 4.
11. A Load/Store instruction attempts to cross a dword boundary.
12. A Memory Move instruction is executed with one of the reserved bits in the DCMD register set.
13. A Memory Move instruction is executed with the source and destination addresses not byte-aligned.

Register 0D (8D)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST	SDP0/
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 ILF (SIDL Least Significant Byte Full)

This bit is set when the least significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF (SODR Least Significant Byte Full)

This bit is set when the least significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It cannot be read or written by the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF (SODL Least Significant Byte Full)

This bit is set when the least significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asyn-

chronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4 AIP (Arbitration in Progress)
Arbitration in Progress (AIP = 1) indicates that the SYM53C895 has detected a Bus Free condition, asserted BSY, and asserted its SCSI ID onto the SCSI bus.

Bit 3 LOA (Lost Arbitration)
When set, LOA indicates that the SYM53C895 has detected a bus free condition, arbitrated for the SCSI bus, and lost arbitration due to another SCSI device asserting the SEL/ signal.

Bit 2 WOA (Won Arbitration)
When set, WOA indicates that the SYM53C895 has detected a Bus Free condition, arbitrated for the SCSI bus and won arbitration. The arbitration mode selected in the SCNTL0 register must be full arbitration and selection for this bit to be set.

Bit 1 RST/ (SCSI RST/ Signal)
This bit reports the current status of the SCSI RST/ signal, and the RST signal (bit 6) in the ISTAT register. This bit is not latched and may be changing when read.

Bit 0 SDP0/ (SCSI SDP0/ Parity Signal)
This bit represents the active high current status of the SCSI SDP0/ parity signal. This signal is not latched and may be changing as it is read.

Register 0E (8E)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDP0L	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	X	X

Bits 7-4 FF3-FF0 (FIFO Flags)
These four bits, along with SSTAT2 bit 4, define the number of bytes or words that currently reside in the SYM53C895's SCSI synchronous data FIFO. These bits are not latched and they will change as data moves through the FIFO.

Table 5-7: FIFO Flags Bit Values

FF4 (SSTAT2 bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16
1	0	0	0	1	17
1	0	0	1	0	18
1	0	0	1	1	19

Table 5-7: FIFO Flags Bit Values (Continued)

FF4 (SSTAT2 bit 4)	FF3	FF2	FF1	FF0	Bytes or Words in the SCSI FIFO
1	0	1	0	0	20
1	0	1	0	1	21
1	0	1	1	0	22
1	0	1	1	1	23
1	1	0	0	0	24
1	1	0	0	1	25
1	1	0	1	0	26
1	1	0	1	1	27
1	1	1	0	0	28
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31

Bit 3 SDP0L (Latched SCSI Parity)

This bit reflects the SCSI parity signal (SDP0/), corresponding to the data latched in the SCSI Input Data Latch register (SIDL). It changes when a new byte is latched into the least significant byte of the SIDL register. This bit is active high, in other words, it is set when the parity signal is active.

Bit 2 MSG (SCSI MSG/ Signal)

Bit 1 C/D (SCSI C_D/ Signal)

Bit 0 I/O (SCSI I_O/ Signal)

These SCSI phase status bits are latched on the asserting edge of SREQ/ when operating in either initiator or target mode. These bits are set when the corresponding signal is active. They are useful when operating in low-level mode.

Register 0F (8F)
SCSI Status Two (SSTAT2)
(Read Only)

ILF1 7	ORF1 6	OLF1 5	FF4 4	SPL1 3	DM 2	LDSC 1	SDP1 0
Default>>>							
0	0	0	0	X	X	1	X

Bit 7 ILF1 (SIDL Most Significant Byte Full)

This bit is set when the most significant byte in the SCSI Input Data Latch register (SIDL) contains data. Data is transferred from the SCSI bus to the SCSI Input Data Latch register before being sent to the DMA FIFO and then to the host bus. The SIDL register contains SCSI data received asynchronously. Synchronous data received does not flow through this register.

Bit 6 ORF1 (SODR Most Significant Byte Full)

This bit is set when the most significant byte in the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) contains data. The SODR register is used by the SCSI logic as a second storage register when sending data synchronously. It is not accessible to the user. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 5 OLF1 (SODL Most Significant Byte Full)

This bit is set when the most significant byte in the SCSI Output Data Latch (SODL) contains data. The SODL register is the interface between the DMA logic and the SCSI bus. In synchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI Output Data Register (SODR, a hidden buffer register which is not accessible) before being sent to the SCSI bus. In asynchronous mode, data is transferred from the host bus to the SODL register, and then to the SCSI bus. The SODR buffer register is not used for asyn-

chronous transfers. This bit can be used to determine how many bytes reside in the chip when an error occurs.

Bit 4 FF4 (FIFO Flags bit 4)
This is the most significant bit in the SCSI FIFO Flags field, with the rest of the bits in SSTAT1. For a complete description of this field, see the definition for SSTAT1 bits 7-4.

Bit 3 SPL1(Latched SCSI parity for SD15-8)
This active high bit reflects the SCSI odd parity signal corresponding to the data latched into the most significant byte in the SIDL register.

Bit 2 DM (DIFFSENS Mismatch)
This bit is set when the DIFFSENS pin detects a single-ended or LVD SCSI operating voltage level while the SYM53C895 is operating in high-power differential mode (by setting the DIF bit in the STEST2 register). If this bit is reset, the DIFFSENS value matches the DIF bit setting.

Bit 1 LDSC (Last Disconnect)
This status bit is used in conjunction with the Connected (CON) bit in SCNTL1 and allows the user to detect the case in which a target device disconnects, and then another SCSI device selects or reselects, the SYM53C895. If the Connected bit is asserted and the LDSC bit is asserted, a disconnect has occurred. This bit is set when the Connected bit in SCNTL1 is cleared. This bit is cleared when a Block Move instruction is executed while the Connected bit in SCNTL1 is set.

Bit 0 SDP1 (SCSI SDP1 Signal)
This bit represents the active-high current state of the SCSI SDP1 parity signal. It is unlatched and may be changing as it is read.

Registers 10-13 (90-93) Data Structure Address (DSA) Read/Write

This 32-bit register contains the base address used for all table indirect calculations. The DSA register is usually loaded prior to starting an I/O, but it is possible for a SCRIPTS Memory Move to load the DSA during the I/O.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register 14 (94)
Interrupt Status (ISTAT)
(Read/Write)

ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This is the only register that can be accessed by the host CPU while the SYM53C895 is executing SCRIPTS (without interfering in the operation of the SYM53C895). It may be used to poll for interrupts if hardware interrupts are disabled. There may be stacked interrupts pending; read this register after servicing an interrupt to check for stacked interrupts. For more information on interrupt handling refer to Chapter 2, “Functional Description.”

Bit 7 ABRT (Abort Operation)

Setting this bit aborts the current operation being executed by the SYM53C895. If this bit is set and an interrupt is received, reset this bit before reading the DSTAT register to prevent further aborted interrupts from being generated. The sequence to abort any operation is:

1. Set this bit.
2. Wait for an interrupt.
3. Read the ISTAT register.
4. If the SCSI Interrupt Pending bit is set, then read the SIST0 or SIST1 register to determine the cause of the SCSI Interrupt and go back to Step 2.
5. If the SCSI Interrupt Pending bit is clear, and the DMA Interrupt Pending bit is set, then write 00h value to this register.
6. Read the DSTAT register to verify the aborted interrupt and to see if any other interrupting conditions have occurred.

Bit 6 SRST (Software Reset)

Setting this bit resets the SYM53C895. All operating registers are cleared to their respective default values and all SCSI signals are deasserted. Setting this bit does not cause the SCSI RST/ signal to be asserted. This reset will not clear the 53C700 Compatibility bit or any of the PCI configuration registers. This bit is not self-clearing; it must be cleared to clear the reset condition (a hardware reset will also clear this bit).

Bit 5 SIGP (Signal Process)

The SIGP bit is a R/W bit that can be written at any time, and polled and reset via CTEST2. The SIGP bit can be used in various ways to pass a flag to or from a running SCRIPTS instruction.

The only SCRIPTS instruction directly affected by the SIGP bit is Wait For Selection/ Reselection. Setting this bit causes that instruction to jump to the alternate address immediately. The instructions at the alternate jump address should check the status of SIGP to determine the cause of the jump. The SIGP bit may be used at any time and is not restricted to the wait for selection/reselection condition.

Bit 4 SEM (Semaphore)

This bit can be set by the SCRIPTS processor using a SCRIPTS register write instruction. The bit may also be set by an external processor while the SYM53C895 is executing a SCRIPTS operation. This bit enables the SYM53C895 to notify an external processor of a predefined condition while SCRIPTS are running. The external processor may also notify the SYM53C895 of a predefined condition and the SCRIPTS processor may take action while SCRIPTS are executing.

Bit 3 CON (Connected)

This bit is automatically set any time the SYM53C895 is connected to the SCSI bus as an initiator or as a target. It will be set after successfully completing selection or when the SYM53C895 has responded to a bus-initiated selection or reselection. It will also be set after the SYM53C895 wins arbitration when operating in low-level mode. When this bit is clear, the SYM53C895 is not connected to the SCSI bus.

Bit 2 INTF (Interrupt on the Fly)

This bit is asserted by an INTFLY instruction during SCRIPTS execution. SCRIPTS programs will not halt when the interrupt occurs. This bit can be used to notify a service routine, running on the main processor while the SCRIPTS processor is still executing a SCRIPTS program. If this bit is set, when the ISTAT register is read it will not automatically be cleared. To clear this bit, it must be written to a one. The reset operation is self-clearing.

Note: If the INTF bit is set but SIP or DIP is not set, do not attempt to read the other chip status registers. An interrupt-on-the-fly interrupt must be cleared before servicing any other interrupts indicated by SIP or DIP.

Note: This bit must be written to one in order to clear it after it has been set.

Bit 1 SIP (SCSI Interrupt Pending)

This status bit is set when an interrupt condition is detected in the SCSI portion of the SYM53C895. The following conditions will cause a SCSI interrupt to occur:

- A phase mismatch (initiator mode) or SATN/ becomes active (target mode)
- An arbitration sequence completes
- A selection or reselection time-out occurs
- The SYM53C895 was selected
- The SYM53C895 was reselected
- A SCSI gross error occurs
- An unexpected disconnect occurs
- A SCSI reset occurs
- A parity error is detected
- The handshake-to-handshake timer is expired
- The general purpose timer is expired
- A SCSI bus mode change is detected

To determine exactly which condition(s) caused the interrupt, read the SIST0 and SIST1 registers.

Bit 0 DIP (DMA Interrupt Pending)

This status bit is set when an interrupt condition is detected in the DMA portion of the SYM53C895. The following conditions will cause a DMA interrupt to occur:

- A PCI parity error is detected
- A bus fault is detected
- An abort condition is detected
- A SCRIPTS instruction is executed in single-step mode
- A SCRIPTS interrupt instruction is executed
- An illegal instruction is detected.

To determine exactly which condition(s) caused the interrupt, read the DSTAT register.

Register 18 (98)
Chip Test Zero (CTEST0)
Read/Write

This was a general purpose read/write register in previous SYM53C8XX family chips. Although it is still a read/write register, Symbios reserves the right to use these bits for future SYM53C8XX family enhancements.

Register 19 (99)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
7	6	5	4	3	2	1	0
Default>>>							
1	1	1	1	0	0	0	0

Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)

These bits identify the bottom bytes in the DMA FIFO that are empty. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is empty, then FMT3 will be set. Since the FMT flags indicate the status of bytes at the bottom of the FIFO, if all FMT bits are set, the DMA FIFO is empty.

Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)

These status bits identify the top bytes in the DMA FIFO that are full. Each bit corresponds to a byte lane in the DMA FIFO. For example, if byte lane three is full then FFL3 will be set. Since the FFL flags indicate the status of bytes at the top of the FIFO, if all FFL bits are set, the DMA FIFO is full.

Register 1A (9A)
Chip Test Two (CTEST2)
Read/Write

DDIR	SIGP	CIO	CM	SRTCH	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	0	1

Bit 7 DDIR (Data Transfer Direction) (Read only)

This status bit indicates which direction data is being transferred. When this bit is set, the data will be transferred from the SCSI bus to the host bus. When this bit is clear, the data will be transferred from the host bus to the SCSI bus.

Bit 6 SIGP (Signal Process) (Read only)

This bit is a copy of the SIGP bit in the ISTAT register (bit 5). The SIGP bit is used to signal a running SCRIPTS instruction. When this register is read, the SIGP bit in the ISTAT register is cleared.

Bit 5 CIO (Configured as I/O) (Read only)

This bit is defined as the Configuration I/O Enable Status bit. This read-only bit indicates if the chip is currently enabled as I/O space.

Note: Both bits 4 and 5 may be set if the chip is dual-mapped.

Bit 4 CM (Configured as Memory) (Read only)

This bit is defined as the configuration memory enable status bit. This read-only bit indicates if the chip is currently enabled as memory space.

Note: Both bits 4 and 5 may be set if the chip is dual-mapped.

Bit 3 SRTCH (SCRATCHA/B Operation)

This bit controls the operation of the SCRATCHA and SCRATCHB registers. When it is set, SCRATCHB contains the RAM base address value from the PCI Configuration RAM Base Address Register. This is the base address for the 4 KB internal RAM. In addition, the SCRATCHA register displays the memory-mapped based address of the chip operating registers. When this bit is clear, the SCRATCHA and SCRATCHB registers return to normal operation.

Note: Bit 3 is the only writable bit in this register. All other bits are read only. When modifying this register, all other bits must be written to zero. Do not execute a Read-Modify-Write to this register.

Bit 2 TEOP (SCSI True End of Process) (Read only)

This bit indicates the status of the SYM53C895's internal TEOP signal. The TEOP signal acknowledges the completion of a transfer through the SCSI portion of the SYM53C895. When this bit is set, TEOP is active. When this bit is clear, TEOP is inactive.

Bit 1 DREQ (Data Request Status) (Read only)

This bit indicates the status of the SYM53C895's internal Data Request signal (DREQ). When this bit is set, DREQ is active. When this bit is clear, DREQ is inactive.

Bit 0 DACK (Data Acknowledge Status) (Read only)

This bit indicates the status of the SYM53C895's internal Data Acknowledge signal (DACK/). When this bit is set, DACK/ is inactive. When this bit is clear, DACK/ is active.

Register 1B (9B)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	WRIE
7	6	5	4	3	2	1	0
Default>>>							
x	x	x	x	0	0	0	0

Bits 7-4 V3-V0 (Chip revision level)
These bits identify the chip revision level for software purposes. The value should be the same as the lower nibble of the PCI Revision ID Register, at address 08h in configuration space.

Bit 3 FLF (Flush DMA FIFO)
When this bit is set, data residing in the DMA FIFO is transferred to memory, starting at the address in the DNAD register. The internal DMAWR signal, controlled by the CTEST5 register, determines the direction of the transfer. This bit is not self clearing; once the SYM53C895 has successfully transferred the data, this bit should be reset.

Note: Polling of FIFO flags is allowed during flush operations.

Bit 2 CLF (Clear DMA FIFO)
When this bit is set, all data pointers for the DMA FIFO are cleared. Any data in the FIFO is lost. This bit automatically resets after the SYM53C895 has successfully cleared the appropriate FIFO pointers and registers.

Note: This bit does not clear the data visible at the bottom of the FIFO.

Bit 1 FM (Fetch Pin Mode)
When set, this bit causes the FETCH/ pin to deassert during indirect and table indirect read operations. FETCH/ will only be active during the op code portion of an instruction fetch. This allows SCRIPTS to be stored in a PROM while data tables are stored in RAM.

If this bit is not set, FETCH/ will be asserted for all bus cycles during instruction fetches.

Bit 0 WRIE (Write and Invalidate Enable)
This bit, when set, causes Memory Write and Invalidate commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in detail in Chapter 3.

Registers 1C-1F (9C-9F) Temporary (TEMP) Read/Write

This 32-bit register stores the Return instruction address pointer from the Call instruction. The address pointer stored in this register is loaded into the DSP register when a Return instruction is executed. This address points to the next instruction to be executed. Do not write to this register while the SYM53C895 is executing SCRIPTS.

During any Memory-to-Memory Move operation, the contents of this register are preserved. The power-up value of this register is indeterminate.

Register 20 (A0) DMA FIFO (DFIFO) Read Only

BO7	BO6	BO5	BO4	BO3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bits 7-0 BO7-BO0 (Byte offset counter)

These bits, along with bits 1-0 in the CTEST5 register, indicate the amount of data transferred between the SCSI core and the DMA core. It may be used to determine the number of bytes in the DMA FIFO when an interrupt occurs. These bits are unstable while data is being transferred between the two cores; once the chip has stopped transferring data, these bits are stable.

Since the DFIFO register counts the number of bytes transferred between the DMA core and the SCSI core, and the DBC register counts the number of bytes transferred across the host bus, the difference between these two counters represents the number of bytes remaining in the DMA FIFO.

The following steps will determine how many bytes are left in the DMA FIFO when an error occurs, regardless of the direction of the transfer:

1. If the DMA FIFO size is set to 112 bytes, subtract the seven least significant bits of the DBC register from the 7-bit value of the DFIFO register.

   If the DMA FIFO size is set to 816 bytes (using bit 5 of the CTEST5 register), subtract the 10 least significant bits of the DBC register from the 10-bit value of the DMA FIFO Byte Offset Counter, which consists of bits 1-0 in the CTEST5 register and bits 7-0 of the DMA FIFO register.

2. If the DMA FIFO size is set to 112 bytes, AND the result with 7Fh for a byte count between zero and 64. If the DMA FIFO size is set to 816 bytes, AND the result with 3FFh for a byte count between 0 and 816.

Note: To calculate the total number of bytes in both the DMA FIFO and SCSI logic, see the section on Data Paths in Chapter Two, "Functional Description."

Register 21 (A1)
Chip Test Four (CTEST4)
Read/Write

BDIS	ZMOD	ZSD	SRTM	MPEE	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 BDIS (Burst Disable)
When set, this bit will cause the SYM53C895 to perform back to back cycles for all transfers. When reset, the SYM53C895 will perform back to back transfers for op code fetches and burst transfers for data moves.

Bit 6 ZMOD (High Impedance Mode)
Setting this bit causes the SYM53C895 to place all output and bidirectional pins into a high-impedance state. In order to read data out of the SYM53C895, this bit must be cleared. This bit is intended for board-level testing only. Do not set this bit during normal system operation.

Bit 5 ZSD (SCSI Data High Impedance)
Setting this bit causes the SYM53C895 to place the SCSI data bus SD(15-0) and the parity lines SDP(1-0) in a high-impedance state. In order to transfer data on the SCSI bus, this bit must be cleared.

Bit 4 SRTM (Shadow Register Test Mode)
Setting this bit allows access to the shadow registers used by Memory-to-Memory Move operations. When this bit is set, register accesses to the TEMP and DSA registers are directed to the shadow copies STEMP (Shadow TEMP) and SDSA (Shadow DSA). The registers are shadowed to prevent them from being overwritten during a Memory-to-Memory Move operation. The DSA and TEMP registers contain the base address used for table indirect calculations, and the address pointer for a call or return instruction, respectively. This bit is intended for manufacturing diagnostics only and should not be set during normal operations.

Bit 3 MPEE (Master Parity Error Enable)
Setting this bit enables parity checking during master data phases. A parity error during a bus master read is detected by the SYM53C895. A parity error during a bus master write is detected by the target, and the SYM53C895 is informed of the error by the PERR/ pin being asserted by the target. When this bit is reset, the SYM53C895 will not interrupt if a master parity error occurs. This bit is reset at power up.

Bits 2-0 FBL2-FBL0 (FIFO Byte Control)

FBL2	FBL1	FBL0	DMA FIFO Byte lane	Pins
0	X	X	Disabled	n/a
1	0	0	0	D(7-0)
1	0	1	1	D(15-8)
1	1	0	2	D(23-16)
1	1	1	3	D(31-24)

These bits steer the contents of the CTEST6 register to the appropriate byte lane of the 32-bit DMA FIFO. If the FBL2 bit is set, then FBL1 and FBL0 determine which of four byte lanes can be read or written. When cleared, the byte lane read or written is determined by the current contents of the DNAD and DBC registers. Each of the four bytes that make up the 32-bit DMA FIFO can be accessed by writing these bits to the proper value. For normal operation, FBL2 must equal zero.

Register 22 (A2)
Chip Test Five (CTEST5)
Read/Write

ADCK 7	BBCK 6	DFS 5	MASR 4	DDIR 3	BL2 2	BO9 1	BO8 0
Default>>>							
0	0	0	0	0	X	X	X

Bit 7 ADCK (Clock Address Incrementor)
Setting this bit increments the address pointer contained in the DNAD register. The DNAD register is incremented based on the DNAD contents and the current DBC value. This bit automatically clears itself after incrementing the DNAD register.

Bit 6 BBCK (Clock Byte Counter)
Setting this bit decrements the byte count contained in the 24-bit DBC register. It is decremented based on the DBC contents and the current DNAD value. This bit automatically clears itself after decrementing the DBC register.

Bit 5 DFS (DMA FIFO Size)
This bit controls the size of the DMA FIFO. When clear, the DMA FIFO will be 112 bytes deep. When set, the DMA FIFO size will increase to 816 bytes. Using a 112-byte FIFO allows software written for other SYM53C8XX family chips to properly calculate the number of bytes residing in the chip after a target disconnect. The default value of this bit is zero.

Bit 4 MASR (Master Control for Set or Reset Pulses)
This bit controls the operation of bit 3. When this bit is set, bit 3 asserts the corresponding signals. When this bit is reset, bit 3 deasserts the corresponding signals. Bits 4 and 3 should not be changed in the same write cycle.

Bit 3 DDIR (DMA Direction)

Setting this bit either asserts or deasserts the internal DMA Write (DMAWR) direction signal depending on the current status of the MASR bit in this register. Asserting the DMAWR signal indicates that data will be transferred from the SCSI bus to the host bus. Deasserting the DMAWR signal transfers data from the host bus to the SCSI bus.

Bit 2 BL2 (Burst Length bit 2)

This bit works with bits 6 and 7 in the DMODE register to determine the burst length. For complete definitions of this field, refer to the descriptions of DMODE bits 6 and 7. This bit is disabled if an 112-byte FIFO is selected by clearing the DMA FIFO Size bit.

Bits 1-0 BO9-8

These are the upper two bits of the DMA FIFO byte offset counter. The entire field is described under the DFIFO register, bits 7-0.

Register 23 (A3)
Chip Test Six (CTEST6)
Read/Write

DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-0 DF7-DF0 (DMA FIFO)

Writing to this register writes data to the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Reading this register unloads data from the appropriate byte lane of the DMA FIFO as determined by the FBL bits in the CTEST4 register. Data written to the FIFO is loaded into the top of the FIFO. Data read out of the FIFO is taken from the bottom. To prevent DMA data from being corrupted, this register should not be accessed during normal operation. This register should only be written when testing the DMA FIFO using the CTEST4 register. Reads or writes to this register while the test mode is not enabled will have unexpected results.

Registers 24-26 (A4-A6)
DMA Byte Counter (DBC)
Read/Write

This 24-bit register determines the number of bytes to be transferred in a Block Move instruction. While sending data to the SCSI bus, the counter is decremented as data is moved into the DMA FIFO from memory. While receiving data from the SCSI bus, the counter is decremented as data is written to memory from the SYM53C895. The DBC counter is decremented each time that data is transferred on the PCI bus. It is decremented by an amount equal to the number of bytes that were transferred.

The maximum number of bytes that can be transferred in any one Block Move command is 16,777,215 bytes. The maximum value that can be loaded into the DBC register is FFFFFFh. If the instruction is a Block Move and a value of 000000h is loaded into the DBC register, an illegal instruction interrupt will occur if the SYM53C895 is not in target mode, Command phase.

The DBC register is also used to hold the least significant 24 bits of the first dword of a SCRIPT fetch, and to hold the offset value during table indirect I/O SCRIPTS. For a complete description, see Chapter 6, “Instruction Set of the I/O Processor.” The power-up value of this register is indeterminate.

Register 27 (A7)
DMA Command (DCMD)
Read/Write

This 8-bit register determines the instruction for the SYM53C895 to execute. This register has a different format for each instruction. For complete descriptions, see Chapter 6, “Instruction Set of the I/O Processor.”

Registers 28-2B (A8-AB) DMA Next Address (DNAD) Read/Write

This 32-bit register contains the general purpose address pointer. At the start of some SCRIPTS operations, its value is copied from the DSPS register. Its value may not be valid except in certain abort conditions. The default value of this register is zero.

This register should not be used to determine data addresses during a Phase Mismatch interrupt, as its value is not always correct for this use. The DBC, DFIFO, and DSPS registers should be used to calculate residual byte counts and addresses as described in the Data Paths section in Chapter 2.

Registers 2C-2F (AC-AF) DMA SCRIPTS Pointer (DSP) Read/Write

To execute SCSI SCRIPTS, the address of the first SCRIPTS instruction must be written to this register. In normal SCRIPTS operation, once the starting address of the SCRIPT is written to this register, SCRIPTS are automatically fetched and executed until an interrupt condition occurs.

In single-step mode, there is a single step interrupt after each instruction is executed. The DSP register does not need to be written with the next address, but the Start DMA bit (bit 2, DCNTL register) must be set each time the step interrupt occurs to fetch and execute the next SCRIPTS command. When writing to this register eight bits at a time, writing the upper eight bits begins execution of SCSI SCRIPTS. The default value of this register is zero.

Registers 30-33 (B0-B3)
DMA SCRIPTS Pointer Save (DSPS)
Read/Write

This register contains the second dword of a SCRIPTS instruction. It is overwritten each time a SCRIPTS instruction is fetched. When a SCRIPTS interrupt instruction is executed, this register holds the interrupt vector. The power-up value of this register is indeterminate.

Registers 34-37 (B4-B7)
Scratch Register A (SCRATCH A)
Read/Write

This is a general purpose, user-definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves into the SCRATCH register will alter its contents. The SYM53C895 cannot fetch SCRIPTS instructions from this location. When bit 3 in the CTEST2 register is set, this register contains the memory-mapped base address of the operating registers. Setting CTEST2 bit 3 only causes the base address to appear in this register; any information that was previously in the register will remain intact. Any writes to this register while CTEST2 bit 3 is set will pass through to the actual SCRATCHA register. The power-up value of this register is indeterminate.

Register 38 (B8)
DMA Mode (DMODE)
Read/Write

BL1	BL0	SIOM	DIOM	ERL	ERMP	BOF	MAN
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7-6 BL1-BL0 (Burst Length)

These bits control the maximum number of transfers performed per bus ownership, regardless of whether the transfers are back-to-back, burst, or a combination of both. The SYM53C895 asserts the Bus Request (REQ/) output when the DMA FIFO can accommodate a transfer of at least one burst size of data. Bus Request (REQ/) is also asserted during start-of-transfer and end-of-transfer cleanup and alignment, even though less than a full burst of transfers may be performed. The SYM53C895 inserts a "fairness delay" of four CLKs between burst-length transfers (as set in BL1-0) during normal operation. The fairness delay is not inserted during PCI retry cycles. This gives the CPU and other bus master devices the opportunity to access the PCI bus between bursts.

Table 5-8: Burst Length Bit Decoding

BL2 (CTEST5 bit 2)	BL1	BL0	Burst Length
0	0	0	2-transfer burst
0	0	1	4-transfer burst
0	1	0	8-transfer burst
0	1	1	16-transfer burst
1	0	0	32-transfer burst*
1	0	1	64-transfer burst*
1	1	0	128-transfer burst*
1	1	1	Reserved

** Only valid if the FIFO size is set to 816 bytes*

Bit 5 SIOM (Source I/O-Memory Enable)

This bit is defined as an I/O Memory Enable bit for the source address of a Memory Move or Block Move Command. If this bit is set, then the source address is in I/O space; and if reset, then the source address is in memory space.

This function is useful for register-to-memory operations using the Memory Move instruction when the SYM53C895 is I/O mapped. Bits 4 and 5 of the CTEST2 register can be used to determine the configuration status of the SYM53C895.

Bit 4 DIOM (Destination I/O-Memory Enable)

This bit is defined as an I/O Memory Enable bit for the destination address of a Memory Move or Block Move Command. If this bit is set, then the destination address is in I/O space; and if reset, then the destination address is in memory space.

This function is useful for memory-to-register operations using the Memory Move instruction when the SYM53C895 is I/O mapped. Bits 4 and 5 of the CTEST2 register can be used to determine the configuration status of the SYM53C895.

Bit 3 ERL (Enable Read Line)

This bit enables a PCI Read Line command. If PCI cache mode is enabled by setting bits in the PCI Cache Line Size register, this chip issues a Read Line command on all read cycles if other conditions are met. For more information on these conditions, refer to Chapter 3, "PCI Functional Description."

Bit 2 ERMP (Enable Read Multiple)

Setting this bit will cause Read Multiple commands to be issued on the PCI bus after certain conditions have been met. These conditions are described in Chapter 3.

Bit 1 BOF (Burst Op Code Fetch Enable)
Setting this bit causes the SYM53C895 to fetch instructions in burst mode. Specifically, the chip will burst in the first two dwords of all instructions using a single bus ownership. If the instruction is a Memory-to-Memory Move type, the third dword will be accessed in a subsequent bus ownership. If the instruction is an indirect type, the additional dword will be accessed in a subsequent bus ownership. If the instruction is a table indirect block move type, the chip will access the remaining two dwords in a subsequent bus ownership, thereby fetching the four dwords required in two bursts of two dwords each. This bit has no effect if SCRIPTS instruction prefetching is enabled.

Bit 0 MAN (Manual Start Mode)
Setting this bit prevents the SYM53C895 from automatically fetching and executing SCSI SCRIPTS when the DSP register is written. When this bit is set, the Start DMA bit in the DCNTL register must be set to begin SCRIPTS execution. Clearing this bit causes the SYM53C895 to automatically begin fetching and executing SCSI SCRIPTS when the DSP register is written. This bit normally is not used for SCSI SCRIPTS operations.

Register 39 (B9)
DMA Interrupt Enable (DIEN)
Read/Write

RES	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	X	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the DSTAT register. An interrupt is masked by clearing the appropriate mask bit. Masking an interrupt prevents IRQ/ from being asserted for the corresponding interrupt, but the status bit will still be set in the DSTAT register. Masking an interrupt will not prevent the ISTAT DIP from being set. All DMA interrupts are considered fatal, therefore SCRIPTS will stop running when this condition occurs, whether or not the interrupt is masked. Setting a mask bit enables the assertion of IRQ/ for the corresponding interrupt. (A masked non-fatal interrupt will not prevent un-masked or fatal interrupts from getting through; interrupt stacking begins when either the ISTAT SIP or DIP bit is set.)

The SYM53C895 IRQ/ output is latched; once asserted, it will remain asserted until the interrupt is cleared by reading the appropriate status register. Masking an interrupt after the IRQ/ output is asserted will not cause IRQ/ to be deasserted.

For more information on interrupts, see Chapter 2, “Functional Description.”

Bit 7 Reserved

Bit 6 MDPE (Master Data Parity Error)

Bit 5 BF (Bus Fault)

Bit 4 ABRT (Aborted)

Bit 3 SSI (Single -step Interrupt)

Bit 2 SIR (SCRIPTS Interrupt Instruction Received

Bit 1 Reserved

Bit 0 IID (Illegal Instruction Detected)

Register 3A (BA)
Scratch Byte Register (SBR)
Read/Write

This is a general purpose register. Apart from CPU access, only Register Read/Write and Memory Moves into this register will alter its contents. The default value of this register is zero. This register was called the DMA Watchdog Timer on previous SYM53C8XX family products.

Register 3B (BB)
DMA Control (DCNTL)
Read/Write

CLSE	PFF	PFEN	SSM	IRQM	STD	IRQD	COM
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 CLSE (Cache Line Size Enable)
Setting this bit enables the SYM53C895 to sense and react to cache line boundaries set up by the DMODE or PCI Cache Line Size register, whichever contains the smaller value. Clearing this bit disables the cache line size logic and the SYM53C895 monitors the cache line size via the DMODE register.

Bit 6 PFF (Pre-fetch Flush)
Setting this bit will cause the pre-fetch unit to flush its contents. The bit will reset after the flush is complete.

Bit 5 PFEN (Pre-fetch Enable)
Setting this bit enables the pre-fetch unit if the burst size is equal to or greater than four. For more information on SCRIPTS instruction prefetching, see Chapter 2.

Bit 4 SSM (Single-step Mode)
Setting this bit causes the SYM53C895 to stop after executing each SCRIPTS instruction, and generate a single step interrupt. When this bit is clear the SYM53C895 will not stop after each instruction; instead it continues fetching and executing instructions until an interrupt condition occurs. For normal SCSI SCRIPTS operation, this bit should be clear. To restart the SYM53C895 after it generates a SCRIPTS Step interrupt, the ISTAT and DSTAT registers should be read to recognize and clear the interrupt and then the START DMA bit in this register should be set.

Bit 3 IRQM (IRQ Mode)
When set, this bit will enable a totem pole driver for the IRQ pin. When reset, this bit will enable an open drain driver for the IRQ pin with a internal weak pull-up. This bit is reset at power up. The bit should remain clear to retain full PCI compliance.

Bit 2 STD (Start DMA Operation)
The SYM53C895 fetches a SCSI SCRIPTS instruction from the address contained in the DSP register when this bit is set. This bit is required if the SYM53C895 is in one of the following modes:

1. Manual start mode – Bit 0 in the DMODE register is set.
2. Single-step mode – Bit 4 in the DCNTL register is set.

When the SYM53C895 is executing SCRIPTS in manual start mode, the Start DMA bit needs to be set to start instruction fetches, but does not need to be set again until an interrupt occurs. When the SYM53C895 is in single-step mode, the Start DMA bit needs to be set to restart execution of SCRIPTS after a single-step interrupt.

Bit 1 IRQD (IRQ Disable)
Setting this bit disables the IRQ pin; clearing this bit enables normal operation. As with any other register other than ISTAT, this register cannot be accessed except by a SCRIPTS instruction during SCRIPTS execution. For more information on the use of this bit in interrupt handling, see Chapter 2.

Bit 0 COM (SYM53C700 Compatibility)
When this bit is clear, the SYM53C895 will behave in a manner compatible with the SYM53C700; selection/reselection IDs will be stored in both the SSID and SFBR registers.

When this bit is set, the ID will be stored only in the SSID register, protecting the SFBR from being overwritten if a selection/reselection occurs during a DMA register-to-register operation. This bit is not affected by a software reset.

Register 3C-3F (BC-BF) Adder Sum Output (ADDER) Read Only

This register contains the output of the internal adder, and is used primarily for test purposes. The power-up value for this register is indeterminate.

Register 40 (C0)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST0 register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, see Chapter 2, “Functional Description.”

Bit 7 M/A (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)

Setting this bit allows the SYM53C895 to generate an interrupt when a Phase Mismatch or ATN condition occurs.

Bit 6 CMP (Function Complete)

Setting this bit allows the SYM53C895 to generate an interrupt when a full arbitration and selection sequence has completed.

Bit 5 SEL (Selected)

Setting this bit allows the SYM53C895 to generate an interrupt when the SYM53C895 has been selected by a SCSI target device.

Bit 4 RSL (Reselected)

Setting this bit allows the SYM53C895 to generate an interrupt when the SYM53C895 has been reselected by a SCSI initiator device.

Bit 3 SGE (SCSI Gross Error)

Setting this bit allows the SYM53C895 to generate an interrupt when a SCSI Gross Error occurs.The following conditions are considered SCSI Gross Errors:

1. Data underflow - the SCSI FIFO was read when no data was present.
2. Data overflow - the SCSI FIFO was written to while full.
3. Offset underflow - in target mode, a SACK/ pulse was received before the corresponding SREQ/ was sent.
4. Offset overflow - in initiator mode, an SREQ/ pulse was received which caused the maximum offset (Defined by the MO3-0 bits in the SXFER register) to be exceeded.
5. In initiator mode, a phase change occurred with an outstanding SREQ/SACK offset.
6. Residual data in SCSI FIFO - a transfer other than synchronous data receive was started with data left in the SCSI synchronous receive FIFO.

Bit 2 UDC (Unexpected Disconnect)

Setting this bit allows the SYM53C895 to generate an interrupt when an unexpected disconnect occurs.This condition only occurs in initiator mode. It happens when the target to which the SYM53C895 is connected disconnects from the SCSI bus unexpectedly. See the SCSI Disconnect Unexpected bit in the SCNTL2 register for more information on expected versus unexpected disconnects. Any disconnect in low-level mode causes this condition.

Bit 1 RST (SCSI Reset Condition)

Setting this bit allows the SYM53C895 to generate an interrupt when the SRST/ signal has been asserted by the SYM53C895 or any other SCSI device. This condition is edge-triggered, so multiple interrupts cannot occur because of a single SRST/ pulse.

Bit 0 PAR (SCSI Parity Error)

Setting this bit allows the SYM53C895 to generate an interrupt when the SYM53C895 detects a parity error while receiving or sending SCSI data. See the Disable Halt on Parity Error or SATN/ Condition bits in the SCNTL1 register for more information on when this condition will actually be raised.

Register 41 (C1)
SCSI Interrupt Enable One (SIEN1)
Read/Write

RES	RES	RES	SBMC	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	X	0	0	0

This register contains the interrupt mask bits corresponding to the interrupting conditions described in the SIST1 register. An interrupt is masked by clearing the appropriate mask bit. For more information on interrupts, refer to Chapter 2, “Functional Description.”

Bits 7-5 Reserved

Bit 4 SBMC (SCSI Bus Mode Change)

Setting this bit allows the SYM53C895 to generate an interrupt when the DIFFSENS pin detects a change in voltage level that indicates the SCSI bus has changed between single-ended, LVD, or high-power differential modes. For example, when this bit is clear and the SCSI bus changes modes, IRQ/ does not assert and the SIP bit in the ISTAT register is not set. However, bit 4 in the SIST1 register is set. Setting this bit allows the interrupt to occur.

Bit 3 Reserved

Bit 2 STO (Selection or Reselection Timeout)

Setting this bit allows the SYM53C895 to generate an interrupt when a selection or reselection timeout occurs.See the description of the STIME0 register bits 3-0 for more information on the time-out periods.

Bit 1 GEN (General Purpose Timer Expired)

Setting this bit allows the SYM53C895 to generate an interrupt when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake-to-Handshake Timer Expired)

Setting this bit allows the SYM53C895 to generate an interrupt when the handshake-to-handshake timer has expired. The time measured is the SCSI Request-to-Request (target) or Acknowledge-to-Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 42 (C2)
SCSI Interrupt Status Zero (SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Reading the SIST0 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN0 register or not. Each bit set indicates that the corresponding condition has occurred. Reading the SIST0 will clear the interrupt status.

Reading this register will clear any bits that are set at the time the register is read, but will not necessarily clear the register because additional interrupts may be pending (the SYM53C895 stacks interrupts). SCSI interrupt conditions may be individually masked through the SIEN0 register.

When performing consecutive 8-bit reads of the DSTAT, SIST0, and SIST1 registers (in any order), insert a delay equivalent to 12 CLK periods between the reads to ensure the interrupts clear properly. Also, if reading the registers when both the ISTAT SIP and DIP bits may not be set, the SIST0 and SIST1 registers should be read before the DSTAT register to avoid missing a SCSI interrupt. For more information on interrupts, refer to Chapter 2, “Functional Description.”

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: SATN/ Active)

In initiator mode, this bit is set if the SCSI phase asserted by the target does not match the instruction. The phase is sampled when SREQ/ is asserted by the target. In target mode, this bit is set when the SATN/ signal is asserted by the initiator.

Bit 6 CMP (Function Complete)

This bit is set when an arbitration only or full arbitration sequence has completed.

Bit 5 SEL (Selected)

This bit is set when the SYM53C895 is selected by another SCSI device. The Enable Response to Selection bit must have been set in the SCID register (and the RESPID register must hold the chip’s ID) for the SYM53C895 to respond to selection attempts.

Bit 4 RSL (Reselected)

This bit is set when the SYM53C895 is reselected by another SCSI device. The Enable Response to Reselection bit must have been set in the SCID register (and the RESPID register must hold the chip’s ID) for the SYM53C895 to respond to reselection attempts.

Bit 3 SGE (SCSI Gross Error)

This bit is set when the SYM53C895 encounters a SCSI Gross Error Condition. The following conditions can result in a SCSI Gross Error Condition:

1. Data Underflow - the SCSI FIFO register was read when no data was present.
2. Data Overflow - too many bytes were written to the SCSI FIFO or the synchronous offset caused the SCSI FIFO to be overwritten.
3. Offset Underflow - the SYM53C895 is operating in target mode and a SACK/ pulse is received when the outstanding offset is zero.
4. Offset Overflow - the other SCSI device sent a SREQ/ or SACK/ pulse with data which exceeded the maximum synchronous offset defined by the SXFER register.
5. A phase change occurred with an outstanding synchronous offset when the SYM53C895 was operating as an initiator.
6. Residual data in the Synchronous data FIFO - a transfer other than synchronous data receive was started with data left in the synchronous data FIFO.

Bit 2 UDC (Unexpected Disconnect)

This bit is set when the SYM53C895 is operating in initiator mode and the target device unexpectedly disconnects from the SCSI bus. This bit is only valid when the SYM53C895 operates in the initiator mode. When the SYM53C895 operates in low-level mode, any disconnect will cause an interrupt, even a valid SCSI disconnect. This bit will also be set if a selection time-out occurs (it may occur before, at the same time, or stacked after the STO interrupt, since this is not considered an expected disconnect).

Bit 1 RST (SCSI RST/ Received)

This bit is set when the SYM53C895 detects an active SRST/ signal, whether the reset was generated external to the chip or caused by the Assert SRST/ bit in the SCNTL1 register. This SYM53C895 SCSI reset detection logic is edge-sensitive, so that multiple interrupts will not be generated for a single assertion of the SRST/ signal.

Bit 0 PAR (Parity Error)

This bit is set when the SYM53C895 detects a parity error while receiving SCSI data. The Enable Parity Checking bit (bit 3 in the SCNTL0 register) must be set for this bit to become active. The SYM53C895 always generates parity when sending SCSI data.

Register 43 (C3)
SCSI Interrupt Status One (SIST1)
Read Only

RES 7	RES 6	RES 5	SBMC 4	RES 3	STO 2	GEN 1	HTH 0
Default>>>							
X	X	X	0	X	0	0	0

Reading the SIST1 register returns the status of the various interrupt conditions, whether they are enabled in the SIEN1 register or not. Each bit that is set indicates the corresponding condition has occurred.

Reading the SIST1 and SIST0 registers will clear the interrupt condition.

Bits 7-5 Reserved

Bit 4 SBMC (SCSI Bus Mode Change)

This bit is set when the DIFFSENS pin detects a change in voltage level that indicates the SCSI bus has switched between single-ended, LVD, or high-power differential modes.

Bit 3 Reserved

Bit 2 STO (Selection or Reselection Time-out)

The SCSI device which the SYM53C895 was attempting to select or reselect did not respond within the programmed time-out period. See the description of the STIME0 register, bits 3-0, for more information on the time-out timer.

Bit 1 GEN (General Purpose Timer Expired)

This bit is set when the general purpose timer has expired. The time measured is the time between enabling and disabling of the timer. See the description of the STIME1 register, bits 3-0, for more information on the general purpose timer.

Bit 0 HTH (Handshake-to-Handshake Timer Expired)

This bit is set when the handshake-to-handshake timer has expired. The time measured is the SCSI Request to Request (target) or Acknowledge to Acknowledge (initiator) period. See the description of the STIME0 register, bits 7-4, for more information on the handshake-to-handshake timer.

Register 44 (C4)
SCSI Longitudinal Parity (SLPAR)
Read/Write

The SLPAR register consists of two multiplexed bytes; other register bit settings determine what is displayed at this memory location at any given time. When bit 5 in the SCNTL2 (SLPMD) register is cleared, the chip XORs the high and low bytes of the SLPAR register together to give a single-byte value which is displayed in the SLPAR register. If the SLPMD bit is set, then the SLPAR register shows either the high byte or the low byte of the SLPAR word. The SLPAR High Byte Enable bit, SCNTL2 bit 4, determines which byte of the SLPAR register is visible on the SLPAR register at any given time. If this bit is cleared, the SLPAR register contains the low byte of the SLPAR word; if it is set, the SLPAR register contains the high byte of the SLPAR word.

This register performs a bytewise longitudinal parity check on all SCSI data received or sent through the SCSI core. If one of the bytes received or sent (usually the last) is the set of correct even parity bits, SLPAR should go to zero (assuming it started at zero). As an example, suppose that the following three data bytes and one check byte are received from the SCSI bus (all signals are shown active high):

Data Bytes	Running SLPAR
---	00000000
1. 11001100	11001100 (XOR of word 1)
2. 01010101	10011001 (XOR of word 1 and 2)
3. 00001111	10010110 (XOR of word 1, 2 and 3) Even Parity >>>10010110
4. 10010110	00000000

A one in any bit position of the final SLPAR value would indicate a transmission error.

The SLPAR register can also be used to generate the check bytes for SCSI send operations. If the SLPAR register contains all zeros prior to sending a block move, it will contain the appropriate check byte at the end of the block move. This byte must then be sent across the SCSI bus.

Note: Writing any value to this register resets it to zero.

The longitudinal parity checks are meant to provide an added measure of SCSI data integrity and are entirely optional. This register does not latch SCSI selection/reselection IDs under any circumstances. The default value of this register is zero.

Register 45 (C5)
SCSI Wide Residue (SWIDE)
Read Only

After a wide SCSI data receive operation, this register will contain a residual data byte if the last byte received was never sent across the DMA bus. It represents either the first data byte of a subsequent data transfer, or it is a residue byte which should be cleared when an Ignore Wide Residue message is received. It may also be an overrun data byte. The power-up value of this register is indeterminate.

Register 46 (C6)
Memory Access Control (MACNTL)
Read/Write

TYP3	TYP2	TYP1	TYP0	DWR	DRD	PSCPT	SCPTS
7	6	5	4	3	2	1	0
Default>>>							
1	1	0	1	0	0	0	0

Bits 7-4 TYP3-0 (Chip Type)
These bits identify the chip type for software purposes. This data manual applies to devices that have these bits set to D0h.

Bits 3 through 0 of this register are used to determine if an external bus master access is to local or far memory. When bits 3 through 0 are set, the corresponding access is considered local and the MAC/_TESTOUT pin is driven high. When these bits are clear, the corresponding access is to far memory and the MAC/_TESTOUT pin is driven low. This function is enabled after a Transfer Control SCRIPTS instruction is executed.

Bit 3 DWR (DataWR)
This bit defines if a data write is considered local memory access.

Bit 2 DRD (DataRD)
This bit defines if a data read is considered local memory access.

Bit 1 PSCPT (Pointer SCRIPTS)
This bit defines if a pointer to a SCRIPTS indirect or table indirect fetch is considered local memory access.

Bit 0 SCPTS (SCRIPTS)
This bit is used to define if a SCRIPTS fetch is considered local memory access.

Register 47 (C7)
General Purpose Pin Control (GPCNTL)
Read/Write

ME	FE	RES	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	1	1	1	1

This register determines if the pins controlled by the General Purpose register (GPREG) are inputs or outputs. Bits 4-0 in GPCNTL correspond to bits 4-0 in the GPREG register.

Bit 7 ME (Master Enable)
The internal bus master signal will be presented on GPIO1 if this bit is set, regardless of the state of Bit 1 (GPIO1_EN).

Bit 6 FE (Fetch Enable)
The internal op code fetch signal will be presented on GPIO0 if this bit is set, regardless of the state of Bit 0 (GPIO0_EN).

Bit 5 RES (Reserved)

Bits 4-2 GPIO4_EN–GPIO2_EN (GPIO Enable)
General purpose control, corresponding to bits 4-2 in the GPREG register and pins 67-65. GPIO4 powers up as a general purpose output, and GPIO3-2 power up as general purpose inputs.

Bits 1-0 GPIO1_EN– GPIO0_EN (GPIO Enable)
These bits power up set, causing the GPIO1 and GPIO0 pins to become inputs. Resetting these bits causes GPIO1-0 to become outputs.

Register 48 (C8)
SCSI Timer Zero (STIME0)
Read /Write

HTH 7	HTH 6	HTH 5	HTH 4	SEL 3	SEL 2	SEL 1	SEL 0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake-to-Handshake Timer Period)

These bits select the handshake-to-handshake time-out period, the maximum time between SCSI handshakes (SREQ/ to SREQ/ in target mode, or SACK/ to SACK/ in initiator mode). When this timing is exceeded, an interrupt is generated and the HTH bit in the SIST1 register is set. The following table contains time-out periods for the Handshake-to-Handshake Timer, the Selection/Reselection Timer (bits 3-0), and the General Purpose Timer (STIME1 bits 3-0). For a more detailed explanation of interrupts, refer to Chapter 2, "Functional Description."

Table 5-9: Handshake-to Handshake Timer Period

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out (40 or 160 MHz)
0000	Disabled
0001	125 µs
0010	250 µs
0011	500 µs
0100	1 ms
0101	2 ms
0110	4 ms
0111	8 ms
1000	16 ms
1001	32 ms
1010	64 ms
1011	128 ms
1100	256 ms
1101	512 ms
1110	1.024 sec
1111	2.048 sec

These values will be correct if the CCF bits in the SCNTL3 register are set according to the valid combinations in the bit description.

A quadrupled 40 MHz clock is required for Ultra2 SCSI operation.

Bits 3-0 SEL (Selection Time-Out)

These bits select the SCSI selection/reselection time-out period. When this timing (plus the 200 µs selection abort time) is exceeded, the STO bit in the SIST1 register is set. For a more detailed explanation of interrupts, refer to Chapter 2, "Functional Description."

Register 49 (C9)
SCSI Timer One (STIME1)
Read/Write

RES	HTHBA	GENSF	HTHSF	GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 Reserved

Bit 6 HTHBA (Handshake-to-Handshake Timer Bus Activity Enable)

Setting this bit causes this timer to begin testing for SCSI REQ/ACK activity as soon as SBSY/ is asserted, regardless of the agents participating in the transfer.

Bit 5 GENSF (General Purpose Timer Scale Factor)

Setting this bit causes this timer to shift by a factor of 16.

Table 5-10: Time-out Periods, 50 MHz Clock

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out (50 MHz Clock*)	
	GENSF= 0	GENSF=1
0000	Disabled	Disabled
0001	100 µs	1.6 ms
0010	200 µs	3.2 ms
0011	400 µs	6.4 ms
0100	800 µs	12.8 ms
0101	1.6 ms	25.6 ms
0110	3.2 ms	51.2 ms
0111	6.4 ms	102.4 ms
1000	12.8 ms	204.8 ms
1001	25.6 ms	409.6 ms
1010	51.2 ms	819.2 ms
1011	102.4 ms	1.6 sec
1100	204.8 ms	3.2 sec
1101	409.6 ms	6.4 sec
1110	819.2 ms	12.8 sec
1111	1.6 sec	25.6 sec

These values will be correct if the CCF bits in the SCNTL3 register are set according to the valid combinations in the bit description.
**50 MHz clock is not supported for Ultra2 SCSI operation.*

Table 5-11: Time-out Periods, 40/160 MHz Clock

HTH 7-4, SEL 3-0, GEN 3-0	Minimum Time-out (40 or 160 MHz Clock)	
	GENSF= 0	GENSF=1
0000	Disabled	Disabled
0001	125 µs	2 ms
0010	250 µs	4 ms
0011	500 µs	8 ms
0100	1 µs	16 ms
0101	2 ms	32 ms
0110	4 ms	64 ms
0111	8 ms	128 ms
1000	16 ms	256 ms
1001	32 ms	512 ms
1010	64 ms	1 sec
1011	128 ms	2 sec
1100	256 ms	4.1 sec
1101	512 ms	8.2 sec
1110	1.024 sec	16.4 sec
1111	2.048 sec	32.8 sec

These values will be correct if the CCF bits in the SCNTL3 register are set according to the valid combinations in the bit description.

Ultra2 SCSI operation requires a quadrupled 40 MHz clock.

Bit 4 HTHSF (Handshake to Handshake Timer Scale Factor)

Setting this bit causes this timer to shift by a factor of 16.

Bits 3-0 GEN3-0 (General Purpose Timer Period)

These bits select the period of the general purpose timer. The time measured is the time between enabling and disabling of the timer. When this timing is exceeded, the GEN bit in the SIST1 register is set. Refer to the table under STIME0, bits 3-0, for the available time-out periods.

Note: To reset a timer before it has expired and obtain repeatable delays, the time value must be written to zero first, and then written back to the desired value. This is also required when changing from one time value to another. See Chapter 2, "Functional Description," for an explanation of how interrupts will be generated when the timers expire.

Register 4A (CA)
Response ID Zero (RESPID0)
Read/Write

Register 4B (CB)
Response ID One(RESPID1)
Read/Write

RESPID0 and RESPID1 contain the selection or reselection IDs. In other words, these two 8-bit registers contain the ID that the chip responds to on the SCSI bus. Each bit represents one possible ID with the most significant bit of RESPID1 representing ID 15 and the least significant bit of RESPID0 representing ID 0. The SCID register still contains the chip ID used during arbitration. The chip can respond to more than one ID because more than one bit can be set in the RESPID1 and RESPID0 registers. However, the chip can arbitrate with only one ID value in the SCID register.

Register 4C (CC)
SCSI Test Zero (STEST0)
Read Only

SSAID3	SSAID2	SSAID1	SSAID0	SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	1	1

Bits 7-4 SSAID (SCSI Selected As ID)

These bits contain the encoded value of the SCSI ID that the SYM53C895 was selected or reselected as during a SCSI selection or reselection phase. These bits are read only and contain the encoded value of 0-15 possible IDs that could be used to select the SYM53C895. During a SCSI selection or reselection phase when a valid ID has been put on the bus, and the SYM53C895 responds to that ID, the "selected as" ID is written into these bits. These bits are used with the RESPID registers to allow response to multiple IDs on the bus.

Bit 3 SLT (Selection Response Logic Test)

This bit is set when the SYM53C895 is ready to be selected or reselected. This does not take into account the bus settle delay of 400 ns. This bit is used for functional test and fault purposes.

Bit 2 ART (Arbitration Priority Encoder Test)

This bit will always be set when the SYM53C895 exhibits the highest priority ID asserted on the SCSI bus during arbitration. It is primarily used for chip level testing, but it may be used during low-level mode operation to determine if the SYM53C895 has won arbitration.

Bit 1 SOZ (SCSI Synchronous Offset Zero)

This bit indicates that the current synchronous SREQ/SACK offset is zero. This bit is not latched and may change at any time. It is used in low-level synchronous SCSI operations. When this bit is set, the SYM53C895, as an initiator, is waiting for the target to request data transfers. If the SYM53C895 is a target, then the initiator has sent the offset number of acknowledges.

Bit 0 SOM (SCSI Synchronous Offset Maximum)

This bit indicates that the current synchronous SREQ/SACK offset is the maximum specified by bits 3-0 in the SCSI Transfer register. This bit is not latched and may change at any time. It is used in low-level synchronous SCSI operations. When this bit is set, the SYM53C895, as a target, is waiting for the initiator to acknowledge the data transfers. If the SYM53C895 is an initiator, then the target has sent the offset number of requests.

Register 4D (CD)
SCSI Test One (STEST1)
Read/Write

SCLK	SISO	RES	RES	QEN	QSEL	RES	RES
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	X	X

Bit 7 SCLK

Setting this bit will disable the external SCLK (SCSI Clock) pin and the internal SCSI Clock Quadrupler, and the chip will use the PCI clock as the internal SCSI clock. If a transfer rate of 10 MB/s (or 20 MB/s on a wide SCSI bus) is to be achieved on the SCSI bus, this bit must be reset and at least a 40 MHz external SCLK must be provided.

Bit 6 SISO (SCSI Isolation Mode)

This bit allows the SYM53C895 to put the SCSI bi-directional and input pins into a low power mode when the SCSI bus is not in use. When this bit is set, the SCSI bus inputs are logically isolated from the SCSI bus.

Bits 5-4 Reserved

Bit 3 QEN (SCLK Quadrupler Enable)

Set this bit to bring the SCSI clock quadrupler out of the powered-down state. The default value of this bit is clear (SCSI clock quadrupler powered down). Set bit 2 after setting this bit, to increase the SCLK frequency to 160 MHz.

Bit 2 QSEL (SCLK Quadrupler Select)

Set this bit after powering up the SCSI clock quadrupler to increase the SCLK frequency to 160 MHz. This bit has no effect unless bit 3 is set.

Bits 1-0 Reserved

Quadrupling the SCSI Clock Frequency

The SYM53C895 SCSI clock quadrupler increases the frequency of a 40 MHz SCSI clock to 160 MHz. Follow these steps to use the clock quadrupler:

1. Set the SCLK Quadrupler Enable bit (STEST1, bit 3).
2. Poll bit 5 of the STEST4 register. The SYM53C895 sets this bit as soon as it locks in the 160 MHz frequency. The frequency lockup takes approximately 100 microseconds.
3. Halt the SCSI clock by setting the Halt SCSI Clock bit (STEST3 bit 5).
4. Set the clock conversion factor using the SCF and CCF fields in the SCNTL3 register.
5. Set the SCLK Quadrupler Select bit (STEST1, bit2).
6. Clear the Halt SCSI Clock bit.

Register 4E (CE)
SCSI Test Two (STEST2)
Read/Write

SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 SCE (SCSI Control Enable)
Setting this bit allows all SCSI control and data lines to be asserted through the SOCL and SODL registers regardless of whether the SYM53C895 is configured as a target or initiator.

Note: This bit should not be set during normal operation, since it could cause contention on the SCSI bus. It is included for diagnostic purposes only.

Bit 6 ROF (Reset SCSI Offset)
Setting this bit clears any outstanding synchronous SREQ/SACK offset. This bit should be set if a SCSI gross error condition occurs, to clear the offset when a synchronous transfer does not complete successfully. The bit automatically clears itself after resetting the synchronous offset.

Bit 5 DIF (SCSI Differential Mode)
Setting this bit allows the SYM53C895 to interface properly to external differential transceivers. Its only real effect is to tri-state the SBSY/, SSEL/, and SRST/ pads so that they can be used as pure inputs. This bit must be cleared for single-ended or LVD operation. This bit should be set in the initialization routine if the high voltage differential interface is used.

Bit 4 SLB (SCSI Loopback Mode)
Setting this bit allows the SYM53C895 to perform SCSI loopback diagnostics. That is, it enables the SCSI core to simultaneously perform as both initiator and target.

Bit 3 SZM (SCSI High-Impedance Mode)
Setting this bit places all the open-drain 48 mA SCSI drivers into a high-impedance state. This is to allow internal loopback mode operation without affecting the SCSI bus.

Bit 2 AWS (Always Wide SCSI)
When this bit is set, all SCSI information transfers will be done in 16-bit wide mode. This includes data, message, command, status and reserved phases. This bit should normally be deasserted since 16-bit wide message, command, and status phases are not supported by the SCSI specifications.

Bit 1 EXT (Extend SREQ/SACK Filtering)
Symbios TolerANT SCSI receiver technology includes a special digital filter on the SREQ/ and SACK/ pins which will cause glitches on deasserting edges to be disregarded. Setting this bit will increase the filtering period from 30 ns to 60 ns on the deasserting edge of the SREQ/ and SACK/ signals.

Note: This bit must never be set during fast SCSI (greater than 5M transfers per second) operations, because a valid assertion could be treated as a glitch.

Note: This bit does not affect the filtering period when the Ultra Enable bit in the SCNTL3 register is set. When the SYM53C895 is executing Ultra2 SCSI transfers, the filtering period is automatically set at 8 ns. When the SYM53C895 is executing Ultra SCSI transfers, the filtering period is automatically set at 15 ns.

Bit 0 LOW (SCSI Low level Mode)
Setting this bit places the SYM53C895 in low-level mode. In this mode, no DMA operations occur, and no SCRIPTS execute. Arbitration and selection may be performed by setting the start sequence bit as described in the SCNTL0 register. SCSI bus transfers are performed by

manually asserting and polling SCSI signals. Clearing this bit allows instructions to be executed in SCSI SCRIPTS mode.

Note: It is not necessary to set this bit for access to the SCSI bit-level registers (SODL, SBCL, and input registers).

Register 4F (CF)
SCSI Test Three (STEST3)
Read/Write

TE	STR	HSC	DSI	S16	TTM	CSF	STW
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 TE (TolerANT Enable)

Setting this bit enables the active negation portion of Symbios TolerANT technology. Active negation causes the SCSI Request, Acknowledge, Data, and Parity signals to be actively deasserted, instead of relying on external pull-ups, when the SYM53C895 is driving these signals. Active deassertion of these signals will occur only when the SYM53C895 is in an information transfer phase. When operating in a differential environment or at fast SCSI timings, TolerANT Active negation should be enabled to improve setup and deassertion times. Active negation is disabled after reset or when this bit is cleared. For more information on Symbios TolerANT technology, refer to Chapter 1.

Note: This bit must be set if the Ultra Enable bit in SCNTL3 is set.

Note: This bit must be set to use the LVDlink transceivers.

Bit 6 STR (SCSI FIFO Test Read)

Setting this bit places the SCSI core into a test mode in which the SCSI FIFO can be easily read. Reading the least significant byte of the SODL register will cause the FIFO to unload. The functions are summarized in the table below.

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Read	15-0	Unload
SODL0	Read	7-0	Unload
SODL1	Read	15-8	None

Bit 5 HSC (Halt SCSI Clock)

Asserting this bit causes the internal divided SCSI clock to come to a stop in a glitchless manner. This bit may be used for test purposes or to lower I_{DD} during a power down mode.

This bit is used when enabling the SCSI clock quadrupler. For additional information on the clock quadrupler, please see "Using the SCSI Clock Quadrupler" in Chapter 2.

Bit 4 DSI (Disable Single Initiator Response)

If this bit is set, the SYM53C895 will ignore all bus-initiated selection attempts that employ the single-initiator option from SCSI-1. In order to select the SYM53C895 while this bit is set, the SYM53C895's SCSI ID and the initiator's SCSI ID must both be asserted. This bit should be asserted in SCSI-2 systems so that a single bit error on the SCSI bus will not be interpreted as a single initiator response.

Bit 3 S16 (16-bit System)

If this bit is set, all devices in the SCSI system implementation are assumed to be 16 bits. This causes the SYM53C895 to always check the parity bit for SCSI IDs 15-8 during bus-initiated selection or reselection, assuming parity checking has been enabled. If an 8-bit SCSI device attempts to select the SYM53C895 while this bit is set, the SYM53C895 will ignore the selection attempt, because the parity bit for IDs 15-8 will be undriven. See the description of the Enable Parity Checking bit in the SCNTL0 register for more information.

Bit 2 TTM (Timer Test Mode)

Asserting this bit facilitates testing of the selection time-out, general purpose, and handshake-to-handshake timers by greatly reducing all three time-out periods. Setting this bit starts all three timers and if the respective bits in the SIEN1 register are asserted, the SYM53C895 will generate interrupts at time-out. This bit is intended for internal manufacturing diagnosis and should not be used.

Bit 1 CSF (Clear SCSI FIFO)

Setting this bit will cause the "full flags" for the SCSI FIFO to be cleared. This empties the FIFO. This bit is self-resetting. In addition to the SCSI FIFO pointers, the SIDL, SODL, and SODR full bits in the SSTAT0 and SSTAT2 are cleared.

Bit 0 STW (SCSI FIFO Test Write)

Setting this bit places the SCSI core into a test mode in which the FIFO can easily be read or written. While this bit is set, writes to the least significant byte of the SODL register will cause the entire word contained in this register to be loaded into the FIFO. Writing the least significant byte of the SODL register will cause the FIFO to load. These functions are summarized in the table below:

Register Name	Register Operation	FIFO Bits	FIFO Function
SODL	Write	15-0	Load
SODL0	Write	7-0	Load
SODL1	Write	15-8	None

Register 50-51 (D0-D1)
SCSI Input Data Latch (SIDL)
Read Only

This register is used primarily for diagnostic testing, programmed I/O operation, or error recovery. Data received from the SCSI bus can be read from this register. Data can be written to the SODL register and then read back into the SYM53C895 by reading this register to allow loopback testing. When receiving SCSI data, the data will flow into this register and out to the host FIFO. This register differs from the SBDL register; SIDL contains latched data and the SBDL always contains exactly what is currently on the SCSI data bus. Reading this register causes the SCSI parity bit to be checked, and will cause a parity error interrupt if the data is not valid. The power-up values are indeterminate.

Register 52 (D2)
SCSI Test 4 (STEST4)
Read Only

SMODE		LOCK	RES	RES	RES	RES	RES
7	6	5	4	3	2	1	0
Default>>>							
X	X	0	X	X	X	X	X

Bit 7-6 SMODE (SCSI Mode)

These bits contain the encoded value of the SCSI operating mode that is indicated by the voltage level sensed at the DIFFSENS pin. The incoming SCSI signal goes to a pair of analog comparators that determine the voltage window of the DIFFSENS signal. These voltage windows indicate LVD, single-ended, or high-power differential operation. The bit values are defined in Table 5-12.

Table 5-12: DIFFSENS Voltage Levels and SCSI Operating Modes

Bit 7, Bit 6	Operating Mode
00	Not possible
01	High voltage differential or powered down (for high voltage differential mode, the DIF bit must also be set)
10	Single-ended
11	LVD SCSI

Bit 5 LOCK (Frequency Lock)

This bit is used when enabling the SCSI clock quadrupler, which allows the SYM53C895 to transfer data at Ultra2 SCSI rates. Poll this bit for a 1 to determine that the clock quadrupler has locked to 160 MHz. For more information on enabling the clock quadrupler, refer to the descriptions for STEST1, bits 2 and 3.

Bits 4-0 Reserved

Registers 54-55 (D4-D5)
SCSI Output Data Latch (SODL)
Read/Write

This register is used primarily for diagnostic testing or programmed I/O operation. Data written to this register is asserted onto the SCSI data bus by setting the Assert Data Bus bit in the SCNTL1 register. This register sends data via programmed I/O. Data flows through this register when sending data in any mode. It is also used to write to the synchronous data FIFO when testing the chip. The power-up value of this register is indeterminate.

Registers 58-59 (D8-D9)
SCSI Bus Data Lines (SBDL)
Read Only

This register contains the SCSI data bus status. Even though the SCSI data bus is active low, these bits are active high. The signal status is not latched and is a true representation of exactly what is on the data bus at the time the register is read. This register is used when receiving data via programmed I/O. This register can also be used for diagnostic testing or in low-level mode. The power-up value of this register is indeterminate.

Registers 5C-5F (DC-DF) Scratch Register B (SCRATCHB) (Read/Write)

This is a general purpose user definable scratch pad register. Apart from CPU access, only Register Read/Write and Memory Moves directed at the SCRATCH register will alter its contents. The SYM53C895 cannot fetch SCRIPTS instructions from this location.When bit 3 in the CTEST2 register is set, this register contains the base address for the 4 KB internal RAM. Setting CTEST2 bit 3 only causes the base address to appear in the SCRATCHB register; any information that was previously in the register will remain intact. Any writes to this register while the bit is set will pass through to the actual SCRATCHB register. The power-up values are indeterminate.

Registers 60h-7Fh (E0h-FFh) Scratch Registers C-J (SCRATCHC-SCRATCHJ) Read/Write

These registers are general-purpose scratch registers for user-defined functions. The SYM53C895 cannot fetch SCRIPTS instructions from this location.The power-up value of these registers is indeterminate.

Chapter 6
Instruction Set of the I/O Processor

After power up and initialization of the SYM53C895, the chip may be operated in the low level register interface mode, or using SCSI SCRIPTS.

With the low-level register interface, the user has access to the DMA control logic and the SCSI bus control logic. An external processor has access to the SCSI bus signals and the low-level DMA signals, which allows creation of complicated board level test algorithms. The low-level interface is useful for backward compatibility with SCSI devices that require certain unique timings or bus sequences to operate properly. Another feature allowed at the low level is loopback testing. In loopback mode, the SCSI core can be directed to talk to the DMA core to test internal data paths all the way out to the chip's pins.

SCSI SCRIPTS

To operate in the SCSI SCRIPTS mode, the SYM53C895 requires only a SCRIPTS start address. The start address must be at a dword (four byte) boundary. This will align all the following SCRIPTS at a dword boundary since all SCRIPTS are 8 or 12 bytes long. Instructions are fetched until an interrupt instruction is encountered, or until an unexpected event (such as a hardware error) causes an interrupt to the external processor.

Once an interrupt is generated, the SYM53C895 halts all operations until the interrupt is serviced. Then, the start address of the next SCRIPTS instruction may be written to the DMA SCRIPTS Pointer register to restart the automatic fetching and execution of instructions.

The SCSI SCRIPTS mode of execution allows the SYM53C895 to make decisions based on the status of the SCSI bus, which off-loads the microprocessor from servicing the numerous interrupts inherent in I/O operations.

Given the rich set of SCSI-oriented features included in the instruction set, and the ability to re-enter the SCSI algorithm at any point, this high level interface is all that is required for both normal and exception conditions. Switching to low level mode for error recovery should never be required.

The following types of SCRIPTS instructions are implemented in the SYM53C895:

- Block Move—used to move data between the SCSI bus and memory
- I/O or Read/Write—causes the SYM53C895 to trigger common SCSI hardware sequences, or to move registers
- Transfer Control—allows SCRIPTS instructions to make decisions based on real time SCSI bus conditions
- Memory Move—causes the SYM53C895 to execute block moves between different parts of main memory
- Load and Store—provides a more efficient way to move data to/from memory from/to an internal register in the chip without using the Memory Move instruction

Each instruction consists of two or three 32-bit words. The first 32-bit word is always loaded into the DCMD and DBC registers, the second into the DSPS register. The third word, used only by Memory Move instructions, is loaded into the TEMP shadow register. In an indirect I/O or Move instruction, the first two 32-bit op code fetches will be followed by one or two more 32-bit fetch cycles.

Sample Operation

The following example describes execution of a SCRIPTS instruction. This sample operation is for a Block Move instruction.

1. The host CPU, through programmed I/O, gives the DMA SCRIPTS Pointer (DSP) register (in the Operating Register file) the starting address in main memory that points to a SCSI SCRIPTS program for execution.
2. Loading the DSP register causes the SYM53C895 to fetch its first instruction at the address just loaded. This will be from main memory or the internal RAM, depending on the address.
3. The SYM53C895 typically fetches two dwords (64 bits) and decodes the high order byte of the first longword as a SCRIPTS instruction. If the instruction is a Block Move, the lower three bytes of the first longword are stored and interpreted as the number of bytes to be moved. The second longword is stored and interpreted as the 32-bit beginning address in main memory to which the move is directed.
4. For a SCSI send operation, the SYM53C895 waits until there is enough space in the DMA FIFO to transfer a programmable size block of data. For a SCSI receive operation, it waits until enough data is collected in the DMA FIFO for transfer to memory. At this point, the SYM53C895 requests use of the PCI bus again to transfer the data.
5. When the SYM53C895 is granted the PCI bus, it will execute (as a bus master) a burst transfer (programmable size) of data, decrement the internally stored remaining byte count, increment the address pointer, and then release the PCI bus. The SYM53C895 stays off the PCI bus until the FIFO can again hold (for a write) or has collected (for a read) enough data to repeat the process.

The process repeats until the internally stored byte count has reached zero. The SYM53C895 releases the PCI bus and then performs another SCRIPTS instruction fetch cycle, using the incremented stored address maintained in the DMA SCRIPTS Pointer register. Execution of SCRIPTS instructions continues until an error condition occurs or an interrupt SCRIPTS instruction is received. At this point, the SYM53C895 interrupts the host CPU and waits for further servicing by the host system. It can execute independent Block Move instructions specifying new byte counts and starting locations in main memory. In this manner, the SYM53C895 performs scatter/gather operations on data without requiring help from the host program, generating a host interrupt, or requiring an external DMA controller to be programmed.

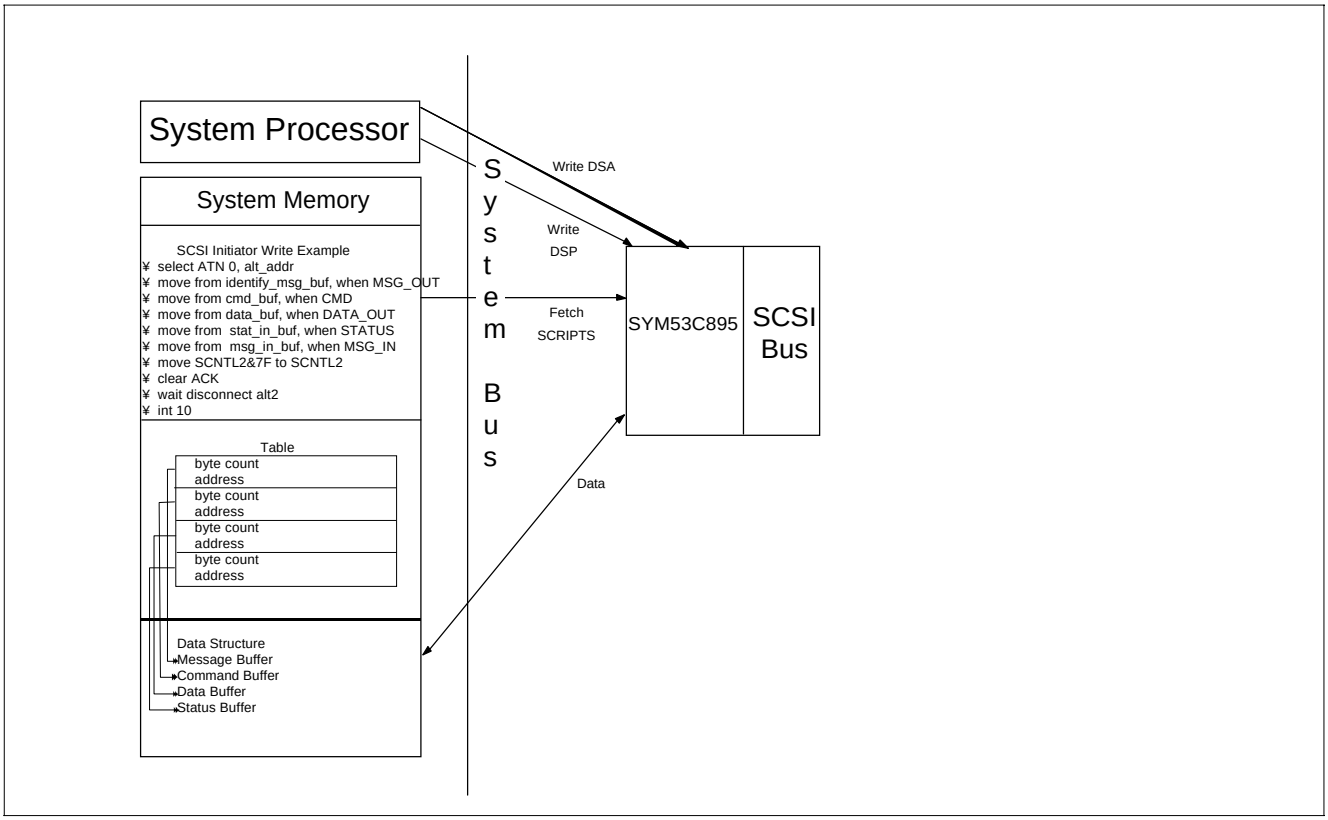


Figure 6-1: SCRIPTS Overview

Block Move Instructions

For Block Move instructions, bits 5 and 4 (SIOM and DIOM) in the DMODE register determine whether the source/destination address resides in memory or I/O space. When data is being moved onto the SCSI bus, SIOM controls whether that data comes from I/O or memory space. When data is being moved off of the SCSI bus, DIOM controls whether that data goes to I/O or memory space.

First Dword

Bits 31-30 Instruction Type-Block Move

Bit 29 Indirect Addressing

When this bit is cleared, user data is moved to or from the 32-bit data start address for the Block Move instruction. The value is loaded into the chip's address register and incremented as data is transferred. The address of the data to be moved is in the second dword of this instruction.

When set, the 32-bit user data start address for the Block Move is the address of a pointer to the actual data buffer address. The value at the 32-bit start address is loaded into the chip's DNAD register via a third longword fetch (4-byte transfer across the host computer bus).

Direct

The byte count and absolute address are as follows.

Command	Byte Count
Address of Data	

Indirect

Use the fetched byte count, but fetch the data address from the address in the instruction.

Command	Byte Count
Address of Pointer to Data	

Once the data pointer address is loaded, it is executed as when the chip operates in the direct mode. This indirect feature allows a table of data buffer addresses to be specified. Using the Symbios SCSI SCRIPTS assembler, the table offset is placed in the script at compile time. Then at the actual data transfer time, the offsets are added to the base address of the data address table by the external processor. The logical I/O driver builds a structure of addresses for an I/O rather than treating each address individually. This feature makes it possible to locate SCSI SCRIPTS in a PROM.

Note: Indirect and table indirect addressing cannot be used simultaneously; only one addressing method may be used at a time.

Bit 28 Table Indirect

When this bit is set, the 24-bit signed value in the start address of the move is treated as a relative displacement from the value in the DSA register. Both the transfer count and the source/destination address are fetched from this address.

Use the signed integer offset in bits 23-0 of the second four bytes of the instruction, added to the value in the DSA register, to fetch first the byte count and then the data address. The signed value is combined with the data structure base address to generate the physical address used to fetch values from the data structure. Sign-extended values of all ones for negative values are allowed, but bits 31-24 are ignored.

Command	Not Used
Don't Care	Table Offset

Note: Indirect and table indirect addressing cannot be used simultaneously; only one addressing method may be used at a time.

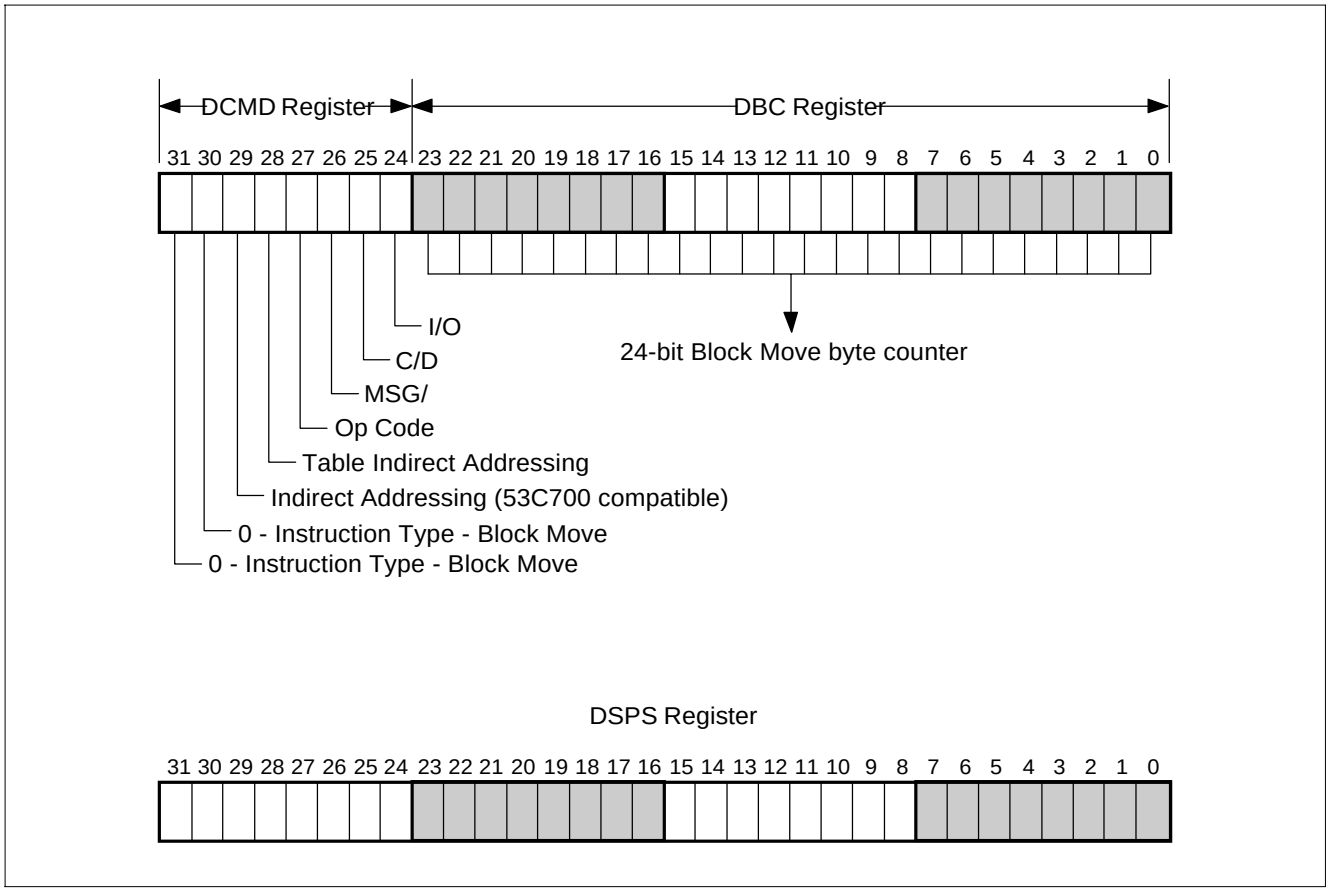


Figure 6-2: Block Move Instruction Register

Prior to the start of an I/O, the Data Structure Base Address register (DSA) should be loaded with the base address of the I/O data structure. The address may be any address on a long word boundary.

After a Table Indirect op code is fetched, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

For a MOVE instruction, the 24-bit byte count is fetched from system memory. Then the 32-bit physical address is brought into the SYM53C895. Execution of the move begins at this point.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries.

There are two restrictions on the placement of pointer data in system memory: the eight bytes of data in the MOVE instruction must be contiguous, as shown below; and indirect data fetches are not available during execution of a Memory-to-Memory DMA operation.

00	Byte Count
Physical Data Address	

Bit 27 Op Code

This 1-bit field defines the instruction to be executed as a block move (MOVE).

Target Mode

OPC	Instruction Defined
0	MOVE
1	CHMOV

1. The SYM53C895 verifies that it is connected to the SCSI bus as a target before executing this instruction.
2. The SYM53C895 asserts the SCSI phase signals (SMSG/, SC_D/, and SI_O/) as defined by the Phase Field bits in the instruction.
3. If the instruction is for the command phase, the SYM53C895 receives the first command byte and decodes its SCSI Group Code.
   a) If the SCSI Group Code is either Group 0, Group 1, Group 2, or Group 5, and if the Vendor Unique Enhancement 1 (VUE1) bit (SCNTL2 bit 1) is clear, then the SYM53C895 overwrites the DBC register with the length of the Command Descriptor Block: 6, 10, or 12 bytes.
   b) If the Vendor Unique Enhancement 1 (VUE1) bit (SCNTL2 bit 1) is set, the SYM53C895 receives the number of bytes in the byte count regardless of the group code.
   c) If the Vendor Unique Enhancement 1 bit is clear and group code is vendor unique, the SYM53C895 receives the number of bytes in the count.
   d) If any other Group Code is received, the DBC register is not modified and the SYM53C895 will request the number of bytes specified in the DBC register. If the DBC register contains 000000h, an illegal instruction interrupt is generated.
4. The SYM53C895 transfers the number of bytes specified in the DBC register starting at the address specified in the DNAD register. If the Op Code bit is set and a data transfer ends on an odd byte boundary, the SYM53C895 will store the last byte in the SCSI Wide Residue Data Register during a receive operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.
5. If the SATN/ signal is asserted by the initiator or a parity error occurred during the transfer, the transfer can optionally be halted and an interrupt generated. The Disable Halt on Parity Error or ATN bit in the SCNTL1 register controls whether the SYM53C895 will halt on these conditions immediately, or wait until completion of the current Move.

Initiator Mode

OPC	Instruction Defined
0	CHMOV
1	MOVE

1. The SYM53C895 verifies that it is connected to the SCSI bus as an initiator before executing this instruction.
2. The SYM53C895 waits for an unserviced phase to occur. An unserviced phase is defined as any phase (with SREQ/ asserted) for which the SYM53C895 has not yet transferred data by responding with a SACK/.
3. The SYM53C895 compares the SCSI phase bits in the DCMD register with the latched SCSI phase lines stored in the SSTAT1 register. These phase lines are latched when SREQ/ is asserted.
4. If the SCSI phase bits match the value stored in the SSTAT1 register, the SYM53C895 will transfer the number of bytes specified in the DBC register starting at the address pointed to by the DNAD register. If the op code bit is cleared and a data transfer ends on an odd byte

boundary, the SYM53C895 will store the last byte in the SCSI Wide Residue Data Register during a receive operation, or in the SCSI Output Data Latch Register during a send operation. This byte will be combined with the first byte from the subsequent transfer so that a wide transfer can be completed.

5. If the SCSI phase bits do not match the value stored in the SSTAT1 register, the SYM53C895 generates a phase mismatch interrupt and the instruction is not executed.
6. During a Message Out phase, after the SYM53C895 has performed a select with Attention (or SATN/ has been manually asserted with a Set ATN instruction), the SYM53C895 will deassert SATN/ during the final SREQ/SACK handshake.
7. When the SYM53C895 is performing a block move for Message In phase, it will not deassert the SACK/ signal for the last SREQ/SACK handshake. The SACK signal must be cleared using the Clear SACK I/O instruction.

Bits 26-24 SCSI Phase

This 3-bit field defines the desired SCSI information transfer phase. When the SYM53C895 operates in initiator mode, these bits are compared with the latched SCSI phase bits in the SSTAT1 register. When the SYM53C895 operates in target mode, the SYM53C895 asserts the phase defined in this field. The following table describes the possible combinations and the corresponding SCSI phase.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bits 23-0 Transfer Counter

This 24-bit field specifies the number of data bytes to be moved between the SYM53C895 and system memory. The field is stored in the DBC register. When the SYM53C895 transfers data to/from memory, the DBC register is decremented by the number of bytes transferred. In addition, the DNAD register is incremented by the number of bytes transferred. This process is repeated until the DBC register has been decremented to zero. At that time, the SYM53C895 fetches the next instruction.

If bit 28 is set, indicating table indirect addressing, this field is not used. The byte count is instead fetched from a table pointed to by the DSA register.

Second Dword

Bits 31-0 Start Address

This 32-bit field specifies the starting address of the data to be moved to/from memory. This field is copied to the DNAD register. When the SYM53C895 transfers data to or from memory, the DNAD register is incremented by the number of bytes transferred.

When bit 29 is set, indicating indirect addressing, this address is a pointer to an address in memory that points to the data location. When bit 28 is set, indicating table indirect addressing, the value in this field is an offset into a table pointed to by the DSA. The table entry contains byte count and address information.

I/O Instructions

First Dword

Bits 31-30 Instruction Type - I/O Instruction

Bits 29-27 Op Code

The following Op Code bits have different meanings, depending on whether the SYM53C895 is operating in initiator or target mode. Note: Op Code selections 101-111 are considered Read/Write instructions, and are described in that section.

Target Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Reselect
0	0	1	Disconnect
0	1	0	Wait Select
0	1	1	Set
1	0	0	Clear

Reselect Instruction

1. The SYM53C895 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the SYM53C895 loses arbitration, then it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the SYM53C895 wins arbitration, it attempts to reselect the SCSI device whose ID is defined in the destination ID field of the instruction. Once the SYM53C895 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register. Therefore, the SCRIPTS can move on to the next instructions before the reselection has completed. It will continue executing SCRIPTS until a SCRIPT that requires a response from the initiator is encountered.
3. If the SYM53C895 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C895 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.

Disconnect Instruction

The SYM53C895 disconnects from the SCSI bus by deasserting all SCSI signal outputs.

Wait Select Instruction

1. If the SYM53C895 is selected, it fetches the next instruction from the address pointed to by the DSP register.
2. If reselected, the SYM53C895 fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C895 should manually be set to initiator mode when reselected.
3. If the CPU sets the SIGP bit in the ISTAT register, the SYM53C895 will abort the Wait Select instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SOCL register are set. SACK/ or SATN/ should not be set except for testing pur-

poses. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the Arithmetic Logic Unit (ALU) is set.

Note: None of the signals are set on the SCSI bus in target mode.

Clear Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits are cleared in the SOCL register. SACK/ or SATN/ should not be set except for testing purposes. When the target bit is set, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is set, the corresponding bit in the ALU is cleared.

Note: The Clear instruction does not cause any of the SCSI bus signals to be reset when the SYM53C895 is in target mode.

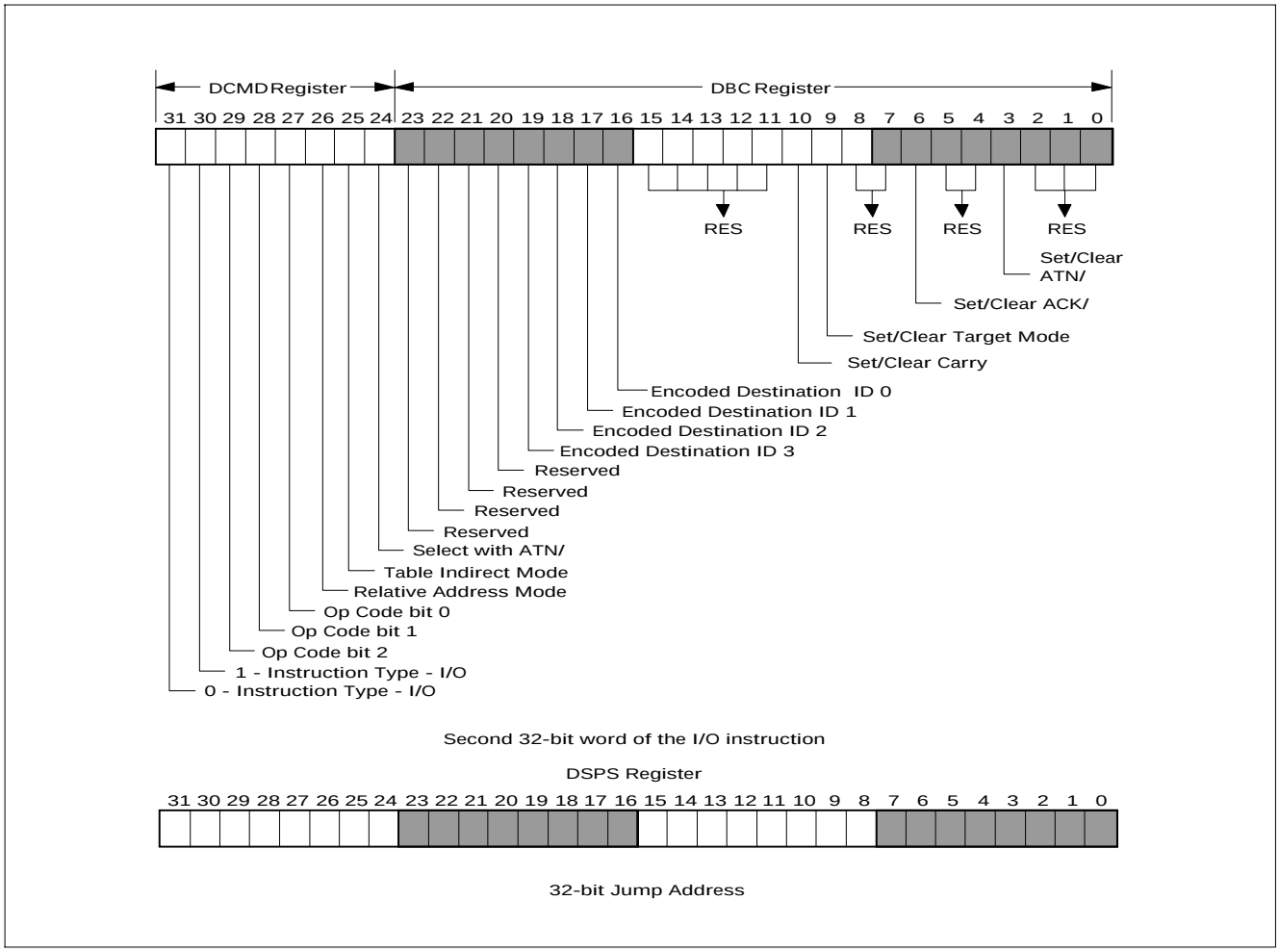


Figure 6-3: I/O Instruction Register

Initiator Mode

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Select
0	0	1	Wait Disconnect
0	1	0	Wait Reselect
0	1	1	Set
1	0	0	Clear

Select Instruction

1. The SYM53C895 arbitrates for the SCSI bus by asserting the SCSI ID stored in the SCID register. If the SYM53C895 loses arbitration, it tries again during the next available arbitration cycle without reporting any lost arbitration status.
2. If the SYM53C895 wins arbitration, it attempts to select the SCSI device whose ID is defined in the destination ID field of the instruction. Once the SYM53C895 has won arbitration, it fetches the next instruction from the address pointed to by the DSP register. Therefore, the scripts can move to the next instruction before the selection has completed. It will continue executing SCRIPTS until a SCRIPT that requires a response from the target is encountered.
3. If the SYM53C895 is selected or reselected before winning arbitration, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C895 should manually be set to initiator mode if it is reselected, or to target mode if it is selected.
4. If the Select with SATN/ field is set, the SATN/ signal is asserted during the selection phase.

Wait Disconnect Instruction

The SYM53C895 waits for the target to perform a "legal" disconnect from the SCSI bus. A "legal" disconnect occurs when SBSY/ and SSEL/ are inactive for a minimum of one Bus Free delay (400 ns), after the SYM53C895 has received a Disconnect Message or a Command Complete Message.

Wait Reselect Instruction

1. If the SYM53C895 is selected before being reselected, it fetches the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register. The SYM53C895 should be manually set to target mode when selected.
2. If the SYM53C895 is reselected, it fetches the next instruction from the address pointed to by the DSP register.
3. If the CPU sets the SIGP bit in the ISTAT register, the SYM53C895 will abort the Wait Reselect instruction and fetch the next instruction from the address pointed to by the 32-bit jump address field stored in the DNAD register.

Set Instruction

When the SACK/ or SATN/ bits are set, the corresponding bits in the SOCL register are set. When the target bit is set, the corresponding bit in the SCNTL0 register is also set. When the carry bit is set, the corresponding bit in the ALU is set.

Clear Instruction

When the SACK/or SATN/ bits are set, the corresponding bits are cleared in the SOCL register. When the target bit is set, the corresponding bit in the SCNTL0 register is cleared. When the carry bit is set, the corresponding bit in the ALU is cleared.

Bit 26 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DNAD register is used as a relative displacement from the current DSP address. This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. The Select and Reselect instructions can contain an absolute alternate jump address or a relative transfer address.

Bit 25 Table Indirect Mode

When this bit is set, the 24-bit signed value in the DBC register is added to the value in the DSA register, used as an offset relative to the value in the Data Structure Base Address (DSA) register. The SCNTL3 value, SCSI ID,

synchronous offset and synchronous period are loaded from this address. Prior to the start of an I/O, the DSA should be loaded with the base address of the I/O data structure. The address may be any address on a longword boundary. After a Table Indirect op code is fetched, the DSA is added to the 24-bit signed offset value from the op code to generate the address of the required data; both positive and negative offsets are allowed. A subsequent fetch from that address brings the data values into the chip.

SCRIPTS can directly execute operating system I/O data structures, saving time at the beginning of an I/O operation. The I/O data structure can begin on any longword boundary and may cross system segment boundaries. There are two restrictions on the placement of data in system memory:

1. The I/O data structure must lie within the 8 MB above or below the base address.
2. An I/O command structure must have all four bytes contiguous in system memory, as shown below. The offset/period bits are ordered as in the SXFER register. The configuration bits are ordered as in the SCNTL3 register.

Config	ID	Offset/ period	(00)

This bit should only be used in conjunction with the Select, Reselect, Wait Select, and Wait Reselect instructions. Bits 25 and 26 may be set individually or in combination:

	Bit 25	Bit 26
Direct	0	0
Table Indirect	0	1
Relative	1	0
Table Relative	1	1

Direct
Uses the device ID and physical address in the instruction.

Command	ID	Not Used	Not Used
Absolute Alternate Address			

Table Indirect
Uses the physical jump address, but fetches data using the table indirect method.

Command	Table Offset
Absolute Alternate Address	

Relative
Uses the device ID in the instruction, but treats the alternate address as a relative jump

Command	ID	Not Used	Not Used
Alternate Jump Offset			

Table Relative
Treats the alternate jump address as a relative jump and fetches the device ID, synchronous offset, and synchronous period indirectly. Adds the value in bits 23-0 of the first four bytes of the SCRIPTS instruction to the data structure base address to form the fetch address.

Command	Table Offset
Alternate Jump Offset	

Bit 24 Select with ATN/

This bit specifies whether SATN/ will be asserted during the selection phase when the SYM53C895 is executing a Select instruction.

When operating in initiator mode, set this bit for the Select instruction. If this bit is set on any other I/O instruction, an illegal instruction interrupt is generated.

Bits 23-20 Reserved

Bits 19-16 Encoded SCSI Destination ID

This 4-bit field specifies the destination SCSI ID for an I/O instruction.

Bits 15-11Reserved

Bit 10 Set/Clear Carry

This bit is used in conjunction with a Set or Clear instruction to set or clear the Carry bit. Setting this bit with a Set instruction asserts the Carry bit in the ALU. Setting this bit with a Clear instruction deasserts the Carry bit in the ALU.

Bits 8-7 Reserved

Bit 9 Set/Clear Target Mode

This bit is used in conjunction with a Set or Clear instruction to set or clear target mode. Setting this bit with a Set instruction configures the SYM53C895 as a target device (this sets bit 0 of the SCNTL0 register). Setting this bit with a Clear instruction configures the SYM53C895 as an initiator device (this clears bit 0 of the SCNTL0 register).

Bit 6 Set/Clear SACK/

Bit 3 Set/Clear SATN/

These two bits are used in conjunction with a Set or Clear instruction to assert or deassert the corresponding SCSI control signal. Bit 6 controls the SCSI SACK/ signal; bit 3 controls the SCSI SATN/ signal.

Setting either of these bits will set or reset the corresponding bit in the SOCL register, depending on the instruction used. The Set instruction is used to assert SACK/ and/or SATN/ on the SCSI bus. The Clear instruction is used to deassert SACK/ and/or SATN/ on the SCSI bus.

Since SACK/ and SATN/ are initiator signals, they will not be asserted on the SCSI bus unless the SYM53C895 is operating as an initiator or the SCSI Loopback Enable bit is set in the STEST2 register.

The Set/Clear SCSI ACK/ATN instruction would be used after message phase Block Move operations to give the initiator the opportunity to assert attention before acknowledging the last message byte. For example, if the initiator wishes to reject a message, an Assert SCSI ATN instruction would be issued before a Clear SCSI ACK instruction.

Bits 2-0 Reserved

Second Dword

Bits 31-0 Start Address

This 32-bit field contains the memory address to fetch the next instruction if the selection or reselection fails.

If relative or table relative addressing is used, this value is a 24-bit signed offset relative to the current DSP register value.

Read/Write Instructions

The Read/Write instruction supports addition, subtraction, and comparison of two separate values within the chip. It performs the desired operation on the specified register and the SFBR register, then stores the result back to the specified register or the SFBR.

First Dword

Bits 31-30 Instruction Type - Read/Write Instruction

The Read/Write instruction uses operator bits 26 through 24 in conjunction with the op code bits to determine which instruction is currently selected.

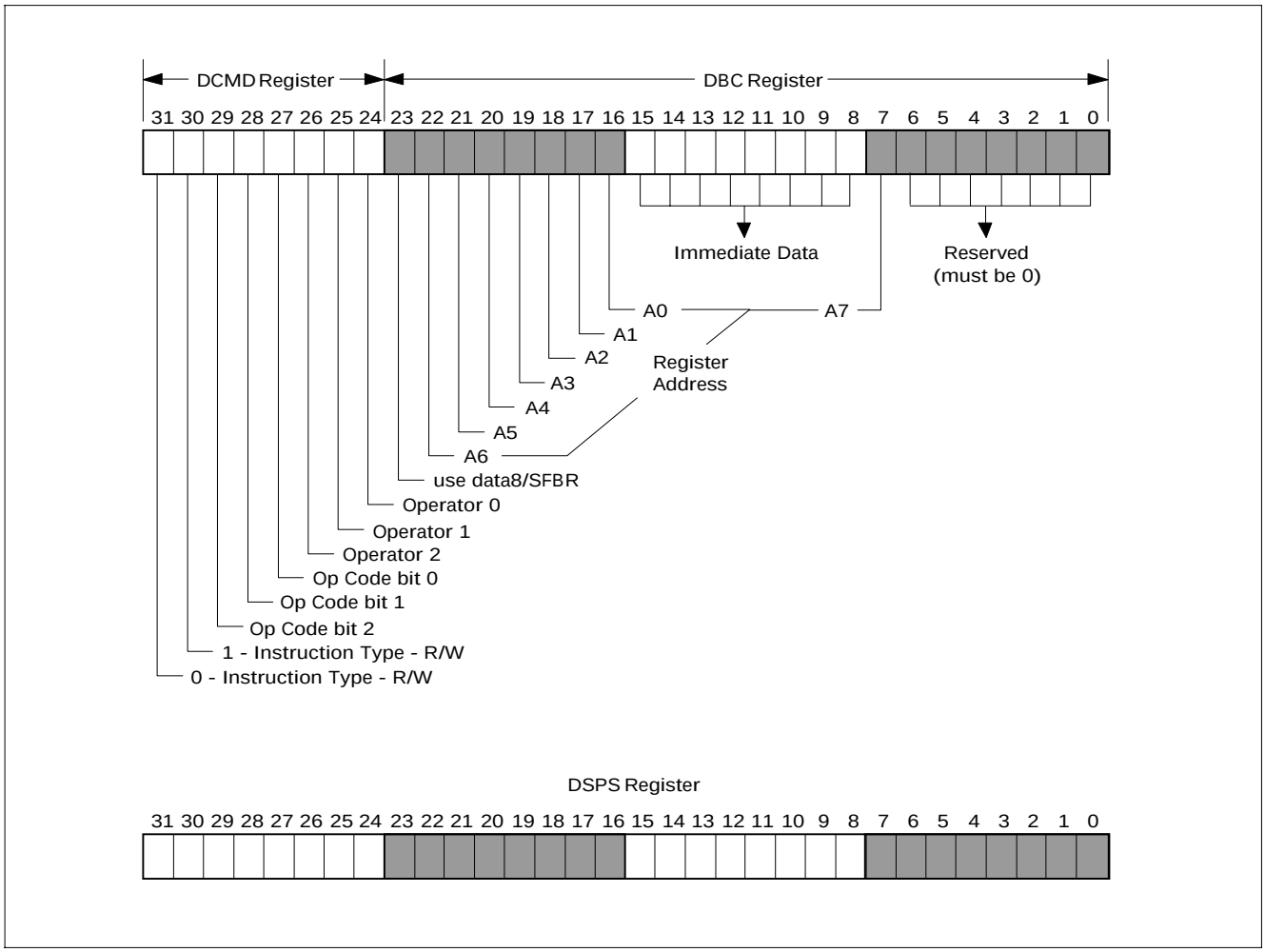


Figure 6-4: Read/Write Instruction Register

Bits 29-27 Op Code

The combinations of these bits determine if the instruction is a Read/Write or an I/O instruction. Op codes 000 through 100 are considered I/O instructions.

Bits 26-24 Operator

These bits are used in conjunction with the op code bits to determine which instruction is currently selected. Refer to table 6-1 for field definitions.

Bit 23 Use data8/SFBR

When this bit is set, SFBR will be used instead of the data8 value during a Read-Modify-Write instruction (see Table 6-1). This allows the user to add two register values.

Bits 22-16 Register Address - A(6-0)

Register values may be changed from SCRIPTS in read-modify-write cycles or move to/from SFBR cycles. A(6-0) select an 8-bit source/destination register within the SYM53C895.

Bits 15-8 Immediate Data

This 8-bit value is used as a second operand in logical and arithmetic functions.

Bits 7-0 Reserved

Second Dword

Bits 31-0 Destination Address

This field contains the 32-bit destination address where the data is to be moved.

Read-Modify-Write Cycles

During these cycles the register is read, the selected operation is performed, and the result is written back to the source register.

The Add operation can be used to increment or decrement register values (or memory values if used in conjunction with a Memory-to-Register Move operation) for use as loop counters.

Subtraction is not available when SFBR is used instead of data8 in the instruction syntax. To subtract one value from another when using SFBR, first XOR the value to subtract (subtrahend) with 0xFF, and add 1 to the resulting value. This creates the 2's compliment of the subtrahend. The two values can then be added to obtain the difference.

Move to/from SFBR Cycles

All operations are read-modify-writes. However, two registers are involved, one of which is always the SFBR. The possible functions of this instruction are:

- Write one byte (value contained within the SCRIPTS instruction) into any chip register.
- Move to/from the SFBR from/to any other register.
- Alter the value of a register with AND/OR/ ADD/XOR/SHIFT LEFT/SHIFT RIGHT operators.
- After moving values to the SFBR, the compare and jump, call, or similar instructions may be used to check the value.
- A Move-to-SFBR followed by a Move-from-SFBR can be used to perform a register to register move.

Table 6-1: Read/Write Instructions

Operator	Op Code 111 Read Modify Write	Op Code 110 Move to SFBR	Op Code 101 Move from SFBR
000	Move data into register. Syntax: “Move data8 to RegA”	Move data into SFBR register. Syntax: “Move data8 to SFBR”	Move data into register. Syntax: “Move data8 to RegA”
001*	Shift register one bit to the left and place the result in the same register. Syntax: “Move RegA SHL RegA”	Shift register one bit to the left and place the result in the SFBR register. Syntax: “Move RegA SHL SFBR”	Shift the SFBR register one bit to the left and place the result in the register. Syntax: “Move SFBR SHL RegA”
010	OR data with register and place the result in the same register. Syntax: “Move RegA | data8 to RegA”	OR data with register and place the result in the SFBR register. Syntax: “Move RegA | data8 to SFBR”	OR data with SFBR and place the result in the register. Syntax: “Move SFBR | data8 to RegA”
011	XOR data with register and place the result in the same register. Syntax: “Move RegA XOR data8 to RegA”	XOR data with register and place the result in the SFBR register. Syntax: “Move RegA XOR data8 to SFBR”	XOR data with SFBR and place the result in the register. Syntax: “Move SFBR XOR data8 to RegA”
100	AND data with register and place the result in the same register. Syntax: “Move RegA & data8 to RegA”	AND data with register and place the result in the SFBR register. Syntax: “Move RegA & data8 to SFBR”	AND data with SFBR and place the result in the register. Syntax: “Move SFBR & data8 to RegA”
101*	Shift register one bit to the right and place the result in the same register. Syntax: “Move RegA SHR RegA”	Shift register one bit to the right and place the result in the SFBR register. Syntax: “Move RegA SHR SFBR”	Shift the SFBR register one bit to the right and place the result in the register. Syntax: “Move SFBR SHR RegA”
110	Add data to register without carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA”	Add data to register without carry and place the result in the SFBR register. Syntax: “Move RegA + data8 to SFBR”	Add data to SFBR without carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA”
111	Add data to register with carry and place the result in the same register. Syntax: “Move RegA + data8 to RegA with carry”	Add data to register with carry and place the result in the SFBR register. Syntax: “Move RegA + data8 to SFBR with carry”	Add data to SFBR with carry and place the result in the register. Syntax: “Move SFBR + data8 to RegA with carry”

Notes:

1. Substitute the desired register name or address for “RegA” in the syntax examples

2. data8 indicates eight bits of data

3. Use SFBR instead of data8 to operate on two register values.

** Data is shifted through the Carry bit and the Carry bit is shifted into the data byte*

Transfer Control Instructions

First Dword

Bits 31-30 Instruction Type - Transfer Control Instruction

Bits 29-27 Op Code

This 3-bit field specifies the type of transfer control instruction to be executed. All transfer control instructions can be conditional. They can be dependent on a true/false comparison of the ALU Carry bit or a comparison of the SCSI information transfer phase with the Phase field, and/or a comparison of the First Byte Received with the Data Compare field. Each instruction can operate in initiator or target mode.

OPC2	OPC1	OPC0	Instruction Defined
0	0	0	Jump
0	0	1	Call
0	1	0	Return
0	1	1	Interrupt
1	X	X	Reserved

Jump Instruction

1. The SYM53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare and True/False bit fields. If the comparisons are true, the SYM53C895 loads the DSP register with the contents of the DSPS register. The DSP register now contains the address of the next instruction.
2. If the comparisons are false, the SYM53C895 fetches the next instruction from the address pointed to by the DSP register, leaving the instruction pointer unchanged.

Call Instruction

1. The SYM53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, the SYM53C895 loads the DSP register with the contents of the DSPS register and that address value becomes the address of the next instruction.

   When the SYM53C895 executes a Call instruction, the instruction pointer contained in the DSP register is stored in the TEMP register. Since the TEMP register is not a stack and can only hold one dword, nested call instructions are not allowed.
2. If the comparisons are false, the SYM53C895 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer is not modified.

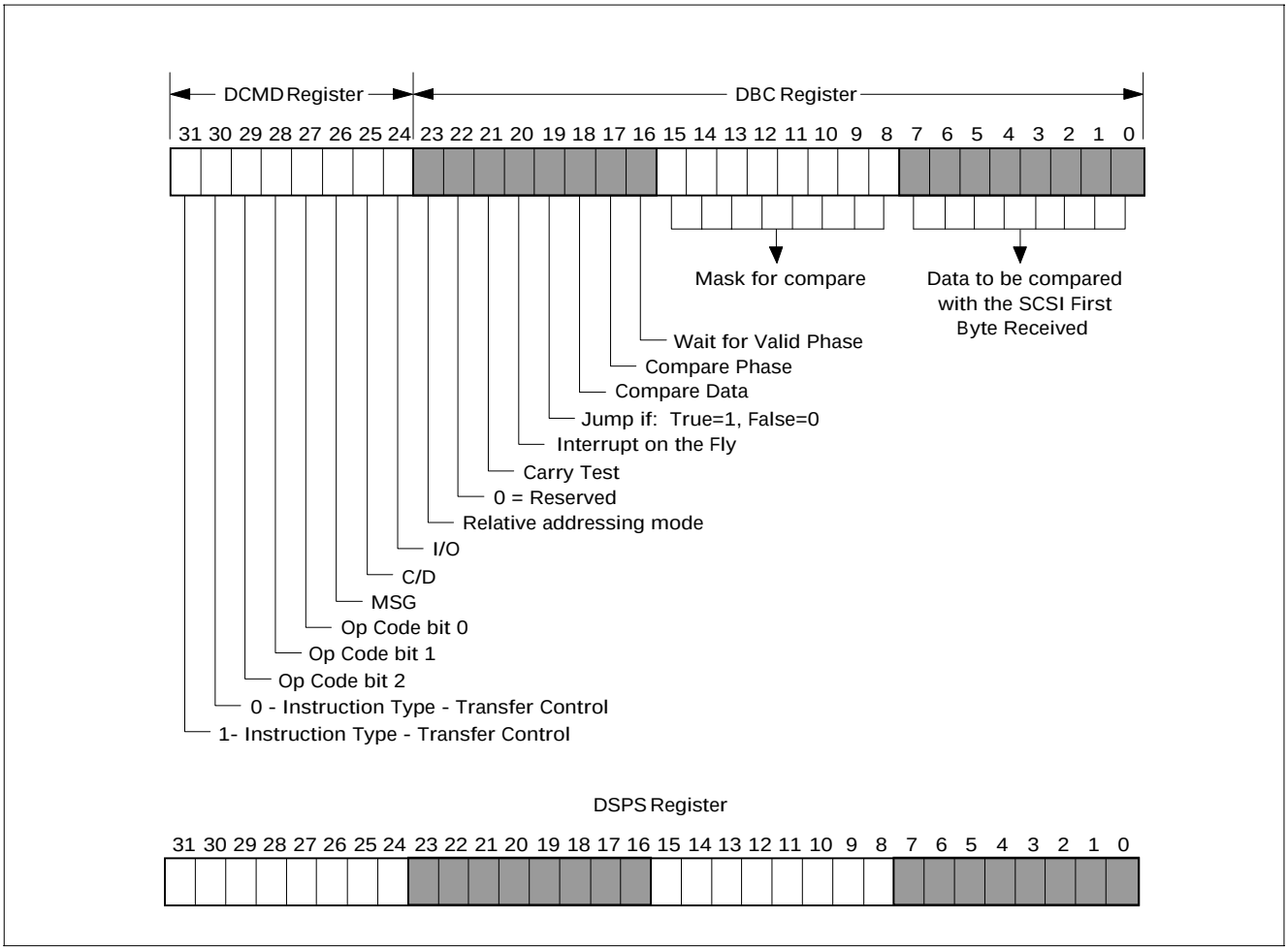


Figure 6-5: Transfer Control Instruction

Return Instruction

1. The SYM53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, then the SYM53C895 loads the DSP register with the contents of the DSPS register. That address value becomes the address of the next instruction.

   When a Return instruction is executed, the value stored in the TEMP register is returned to the DSP register. The SYM53C895 does not check to see whether the Call instruction has already been executed. It will not generate an interrupt if a Return instruction is executed without previously executing a Call instruction.

2. If the comparisons are false, then the SYM53C895 fetches the next instruction from the address pointed to by the DSP register and the instruction pointer will not be modified.

Interrupt Instructions

Interrupt

a) The SYM53C895 can do a true/false comparison of the ALU carry bit, or compare the phase and/or data as defined by the Phase Compare, Data Compare,

and True/False bit fields. If the comparisons are true, then the SYM53C895 generates an interrupt by asserting the IRQ/ signal.

b) The 32-bit address field stored in the DSPS register (not DNAD as in SYM53C700) can contain a unique interrupt service vector. When servicing the interrupt, this unique status code allows the ISR to quickly identify the point at which the interrupt occurred.

c) The SYM53C895 halts and the DSP register must be written to start any further operation.

Interrupt on-the-Fly

a) The SYM53C895 can do a true/false comparison of the ALU carry bit or compare the phase and/or data as defined by the Phase Compare, Data Compare, and True/False bit fields. If the comparisons are true, and the Interrupt on the Fly bit is set (bit 20), the SYM53C895 will assert the Interrupt on the Fly bit (ISTAT bit 2).

Bits 26-24 SCSI Phase

This 3-bit field corresponds to the three SCSI bus phase signals which are compared with the phase lines latched when SREQ/ is asserted. Comparisons can be performed to determine the SCSI phase actually being driven on the SCSI bus. The following table describes the possible combinations and their corresponding SCSI phase. These bits are only valid when the SYM53C895 is operating in initiator mode; when the SYM53C895 is operating in the target mode, these bits should be cleared.

MSG	C/D	I/O	SCSI Phase
0	0	0	Data out
0	0	1	Data in
0	1	0	Command
0	1	1	Status
1	0	0	Reserved out
1	0	1	Reserved in
1	1	0	Message out
1	1	1	Message in

Bit 23 Relative Addressing Mode

When this bit is set, the 24-bit signed value in the DSPS register is used as a relative offset from the current DSP address (which is pointing to the next instruction, not the one currently executing). Relative mode does not apply to Return and Interrupt SCRIPTS.

Jump/Call an Absolute Address
Start execution at the new absolute address.

Command	Condition Codes
Absolute Alternate Address	

Jump/Call a Relative Address
Start execution at the current address plus (or minus) the relative offset.

Command	Condition Codes
Don't Care	Alternate Jump Offset

The SCRIPTS program counter is a 32-bit value pointing to the SCRIPT currently being executed by the SYM53C895. The next address is formed by adding the 32-bit program counter to the 24-bit signed value of the last 24 bits of the Jump or Call instruction. Because it is signed (2's compliment), the jump can be forward or backward.

A relative transfer can be to any address within a 16-MB segment. The program counter is combined with the 24-bit signed offset (using addition or subtraction) to form the new execution address.

SCRIPTS programs may contain a mixture of direct jumps and relative jumps to provide maximum versatility when writing SCRIPTS. For example, major sections of code can be accessed with far calls using the 32-bit physical address, then local labels can be called using relative transfers. If a SCRIPT is written using only relative transfers it would not require any run time alteration of physical addresses, and could be stored in and executed from a PROM.

Bit 21 Carry Test

When this bit is set, decisions based on the ALU carry bit can be made. True/False comparisons are legal, but Data Compare and Phase Compare are illegal.

Bit 20 Interrupt on the Fly

When this bit is set, the interrupt instruction will not halt the SCRIPTS processor. Once the interrupt occurs, the Interrupt on the Fly bit (ISTAT bit 2) will be asserted.

Bit 19 Jump If True/False

This bit determines whether the SYM53C895 should branch when a comparison is true or when a comparison is false. This bit applies to phase compares, data compares, and carry tests. If both the Phase Compare and Data Compare bits are set, then both compares must be true to branch on a true condition. Both compares must be false to branch on a false condition.

Bit 19	Result of Compare	Action
0	False	Jump Taken
0	True	No Jump
1	False	No Jump
1	True	Jump Taken

Bit 18 Compare Data

When this bit is set, the first byte received from the SCSI data bus (contained in SFBR register) is compared with the Data to be Compared Field in the Transfer Control instruction. The Wait for Valid Phase bit controls when this compare will occur. The Jump if True/False bit determines the condition (true or false) to branch on.

Bit 17 Compare Phase

When the SYM53C895 is in initiator mode, this bit controls phase compare operations. When this bit is set, the SCSI phase signals (latched by SREQ/) are compared to the Phase Field in the Transfer Control instruction; if they match, the comparison is true. The Wait for Valid Phase bit controls when the compare will occur. When the SYM53C895 is operating in target mode, setting this bit tests for an active SCSI SATN/ signal.

Bit 16 Wait For Valid Phase

If the Wait for Valid Phase bit is set, the SYM53C895 waits for a previously unserviced phase before comparing the SCSI phase and data.

If the Wait for Valid Phase bit is clear, the SYM53C895 compares the SCSI phase and data immediately.

Bits 15-8 Data Compare Mask

The Data Compare Mask allows a SCRIPT to test certain bits within a data byte. During the data compare, any mask bits that are set cause the corresponding bit in the SFBR data byte to be ignored. For instance, a mask of 01111111b and data compare value of 1XXXXXXXb allows the SCRIPTS processor to determine whether or not the high order bit is set while ignoring the remaining bits.

Bits 7-0 Data Compare Value

This 8-bit field is the data to be compared against the SCSI First Byte Received (SFBR) register. These bits are used in conjunction with the Data Compare Mask Field to test for a particular data value.

Second Dword

Bits 31-0 Jump Address

This 32-bit field contains the address of the next instruction to fetch when a jump is taken. Once the SYM53C895 has fetched the instruction from the address pointed to by these 32 bits, this address is incremented by 4, loaded into the DSP register and becomes the current instruction pointer.

Memory Move Instructions

For Memory Move instructions, bits 5 and 4 (SIOM and DIOM) in the DMODE register determine whether the source or destination addresses reside in memory or I/O space. By setting these bits appropriately, data may be moved within memory space, within I/O space, or between the two address spaces.

The Memory Move instruction copies the specified number of bytes from the source address to the destination address.

Allowing the SYM53C895 to perform memory moves frees the system processor for other tasks and moves data at higher speeds than available from current DMA controllers. Up to 16 MB may be transferred with one instruction. There are two restrictions:

1. Both the source and destination addresses must start with the same address alignment (A(1-0) must be the same). If source and destination are not aligned, then an illegal instruction interrupt will occur. For the PCI Cache Line Size register setting to take effect, the source and destination must be the same distance from a cache line boundary.
2. Indirect addresses are not allowed. A burst of data is fetched from the source address, put into the DMA FIFO and then written out to the destination address. The move continues until the byte count decrements to zero, then another SCRIPT is fetched from system memory.

The DSPS and DSA registers are additional holding registers used during the Memory Move; however, the contents of the DSA register are preserved.

Bits 31-39 Instruction Type—Memory Move

Bits 28-25 Reserved

These bits are reserved and must be zero. If any of these bits is set, an illegal instruction interrupt will occur.

Bit 24 No Flush

Note: This bit has no effect unless the Pre-fetch Enable bit in the DCNTL register is set. For information on SCRIPTS instruction prefetching, see Chapter 2, “Functional Description.”

When this bit is set, the SYM53C895 performs a Memory Move without flushing the prefetch unit. When this bit is clear, the Memory Move instruction automatically flushes the prefetch unit. The No Flush option should be used if the source and destination are not within four instructions of the current Memory Move instruction.

Bits 23-0 Transfer Count

The number of bytes to be transferred is stored in the lower 24 bits of the first instruction word.

Read/Write System Memory from a Script

By using the Memory Move instruction, single or multiple register values may be transferred to or from system memory.

Because the SYM53C895 will respond to addresses as defined in the Base I/O or Base Memory registers, it could be accessed during a Memory Move operation if the source or destination address decodes to within the chip’s register space. If this occurs, the register indicated by the lower seven bits of the address is taken to be the data source or destination. In this way, register values can be saved to system memory and later restored, and SCRIPTS can make decisions based on data values in system memory.

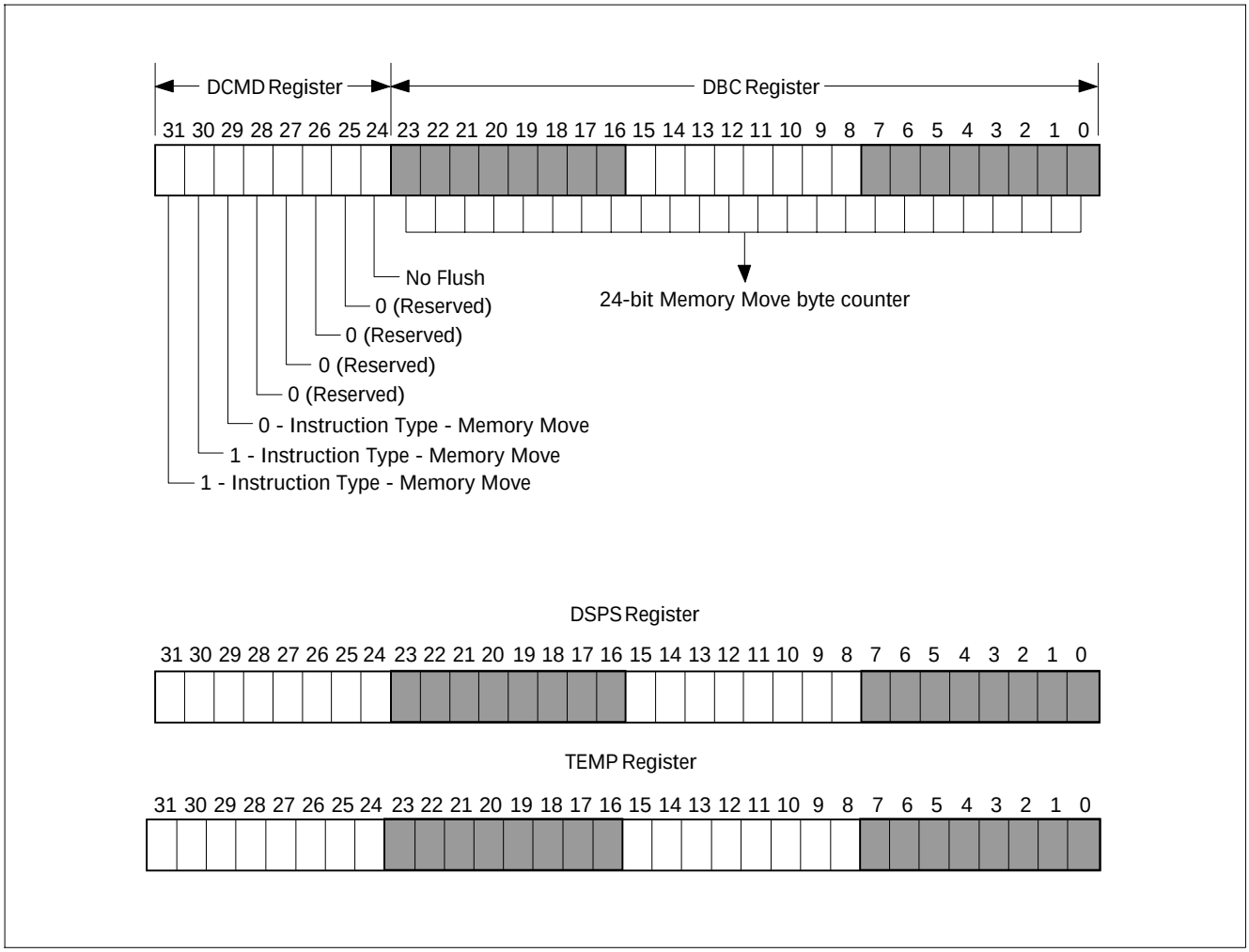


Figure 6-6: Memory Move Instructions

The SFBR is not writable via the CPU, and therefore not by a Memory Move. However, it can be loaded via SCRIPTS Read/Write operations. To load the SFBR with a byte stored in system memory, the byte must first be moved to an intermediate SYM53C895 register (for example, a SCRATCH register), and then to the SFBR.

The same address alignment restrictions apply to register access operations as to normal memory-to-memory transfers.

Second Dword

Bits 31-0, DSPS Register

These bits contain the source address of the Memory Move.

Third Dword

Bits 31-0, TEMP Register

These bits contain the destination address for the Memory Move.

Load and Store Instructions

The Load and Store instruction provides a more efficient way to move data from/to memory to/from an internal register in the chip without using the normal memory move instruction.

The load and store instructions are represented by two-dword op codes. The first dword contains the DCMD and DBC register values. The second dword contains the DSPS value. This is either the actual memory location of where to load or store, or the offset from the DSA, depending on the value of Bit 28 (DSA Relative).

A maximum of 4 bytes may be moved with these instructions. The register address and memory address must have the same byte alignment, and the count set such that it does not cross dword boundaries. The destination memory address in the Store instruction and the source memory address of the Load instruction may not map back to the operating register set of the chip. This excludes the SCRIPTS RAM and ROM memory spaces. If it does, a PCI read/write cycle will occur (the data does not actually transfer to/from the chip), and the chip will issue an interrupt (Illegal Instruction Detected) immediately following.

Bits A1, A0	Number of bytes allowed to load/ store
00	One, two, three or four
01	One, two, or three
10	One or two
11	One

The SIOM and DIOM bits in the DMODE register determine whether the destination or source address of the instruction is in Memory space or I/O space, as illustrated in the following table. The Load/Store utilizes the PCI commands for I/O READ and I/O WRITE to access the I/O space.

Bit	Source	Destination
SIOM (Load)	memory	register
DIOM (Store)	register	memory

First Dword

Bit 31-29, Instruction Type

These bits should be 111, indicating the Load and Store instruction.

Bit 28, DSA Relative

When this bit is clear, the value in the DSPS is the actual 32-bit memory address to perform the load/store to/from. When this bit is set, the chip determines the memory address to perform the load/store to/from by adding the 24-bit signed offset value in the DSPS to the DSA.

Bits 27-26, Reserved

Bit 25, No Flush (Store instruction only)

Note: This bit has no effect unless the Pre-fetch Enable bit in the DCNTL register is set. For information on SCRIPTS instruction prefetching, see Chapter 2, “Functional Description.”

When this bit is set, the SYM53C895 performs a Store without flushing the prefetch unit. When this bit is clear, the Store instruction automatically flushes the prefetch unit. No Flush should be used if the source and destination are not within four instructions of the current Store instruction. This bit is has no effect on the Load instruction.

Bit 24, Load/Store

When this bit is set, the instruction is a Load. When cleared, it is a Store.

Bit 23, Reserved

Bits 22-16, Register Address

A6-A0 select the register to load/store to/from within the SYM53C895.

Note: It is not possible to Load the SFBR register, although it is possible to Store the SFBR contents to another location.

Bits 15-3, Reserved

Bits 2-0, Byte Count

This value is the number of bytes to load/store.

Second Dword

Bits 31-0, Memory/IO Address / DSA Offset

This is the actual memory location of where to load or store, or the offset from the DSA register value.

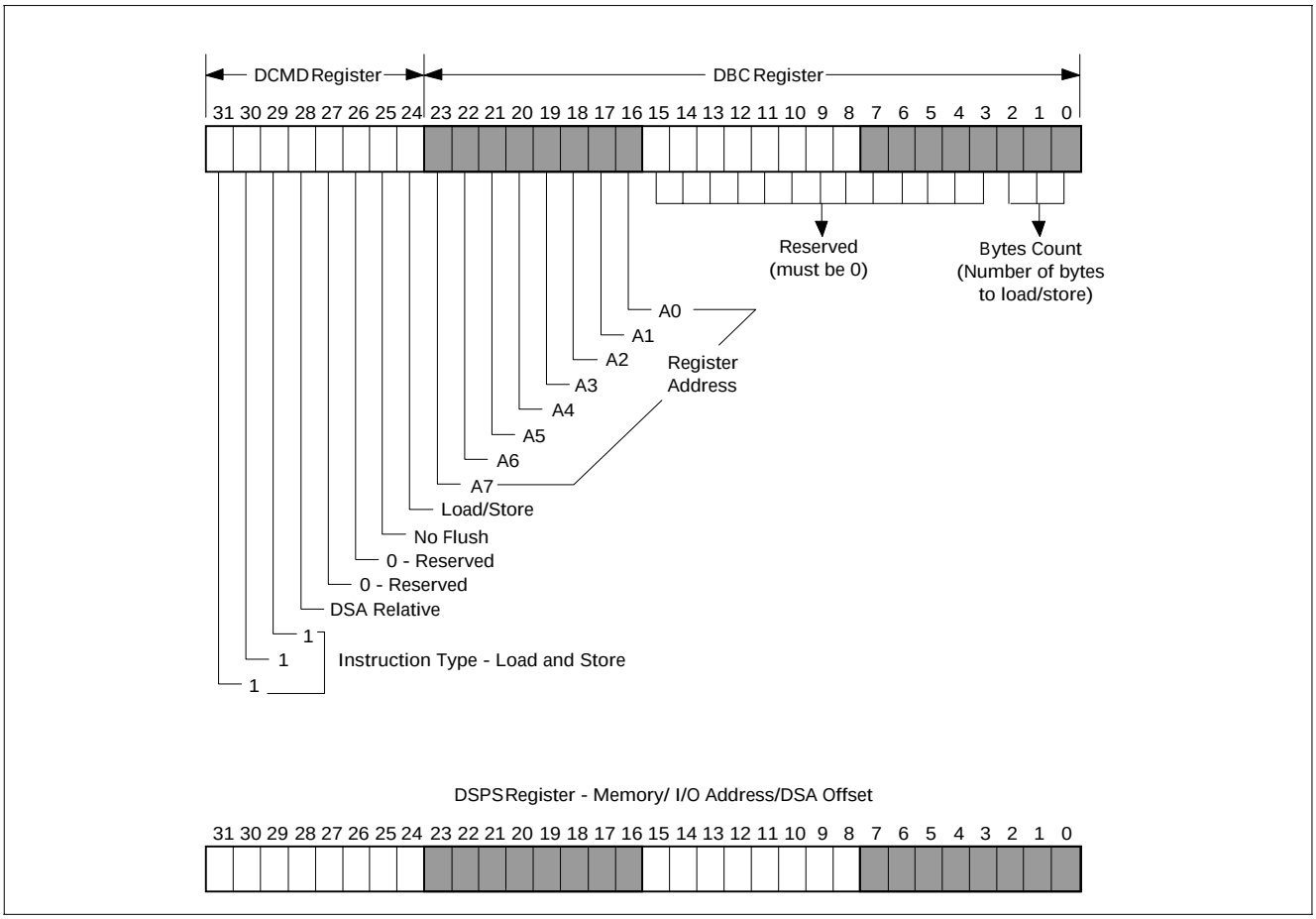


Figure 6-7: Load and Store Instruction Format

Chapter 7
Electrical Characteristics

DC Characteristics

Table 7-1: Absolute Maximum Stress Ratings

Symbol	Parameter	Min	Max	Unit	Test Conditions
T_{STG}	Storage temperature	-55	150	°C	-
V_{DD}	Supply voltage	-0.5	5.0	V	-
V_{IN}	Input Voltage	V_{SS} - 0.3	V_{DD} + 0.3	V	-
I_{LP}*	Latch-up current	± 150	-	mA	-
ESD**	Electrostatic discharge	-	2K	V	MIL-STD 883C, Method 3015.7

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the Operating Conditions section of the manual is not implied.
** $-2V < V_{PIN} < 8V$*
*** SCSI pins only*

Table 7-2: Operating Conditions

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{DD}	Supply voltage	3.135	3.465	V	-
I_{DD}	Supply current (dynamic)	-	130	mA	-
	Supply current (static)	-	1	mA	-
$I_{DD\text{-}SCSI}$	LVD pad supply current	-	600	mA	RBIAS = 2.2 K Ω, V_{DD} = 3.3 V
T_A	Operating free air	0	70	°C	-
θ_{JA}	Thermal resistance (junction to ambient air)	-	67	°C/W	-

Conditions that exceed the operating limits may cause the device to function incorrectly

Table 7-3: SCSI Signals, Low Voltage Differential Drivers—SD (15-0)+/, SDP (1-0)+/-, SREQ+/-, SACK+/-, SMSG+/-, SIO+/-, SCD+/-, SATN+/-, SBSY+/-, SSEL+/-, SRST+/-*

Symbol	Parameter	Min	Max	Units	Test Conditions
I_O+	Source (+) current	-7	-11	mA	Asserted state
I_O-	Sink (-) current	7	11	mA	Asserted state
I_O+	Sink (-) current	3.5	5.5	mA	Negated state
I_O-	Source (+) current	-3.5	-5.5	mA	Negated state
I_{OZ}	Tristate leakage	-20	20	µA	
I_{OZ} (SRST-only)	Tristate leakage	-500	-50	µA	

V_{CM} = 0.7 - 1.8 V
R_L = 0-110Ω
R_{bias} = 2.2 KΩ
Note: Positive current is into SIOP chip

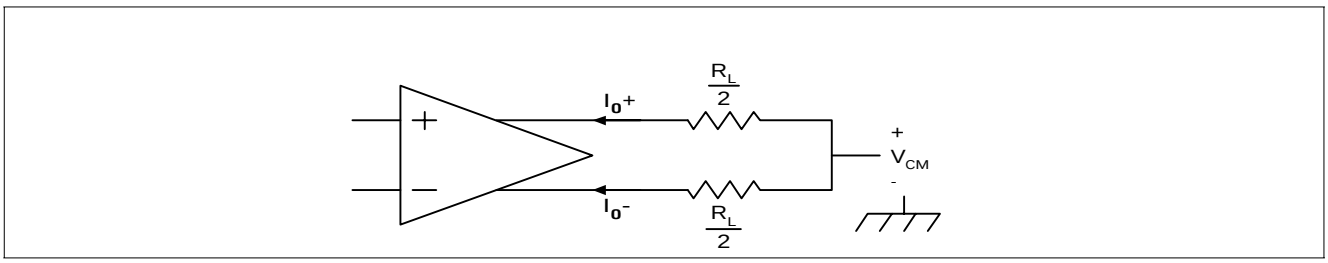


Figure 7-1: LVD Transmitter

Table 7-4: SCSI Signals, Low Voltage Differential Receivers—SD (15-0)+/-, SDP (1-0)+/-, SREQ+/-, SACK+/-, SMSG+/-, SIO+/-, SCD+/-, SATN+/-, SBSY+/-, SSEL+/-, SRST+/-*

Symbol	Parameter	Min	Max	Units
V_I	LVD receiver voltage asserting	60	-	mV
V_I	LVD receiver voltage negating	-	-60	mV

V_{CM} = 0.7 - 1.8 V

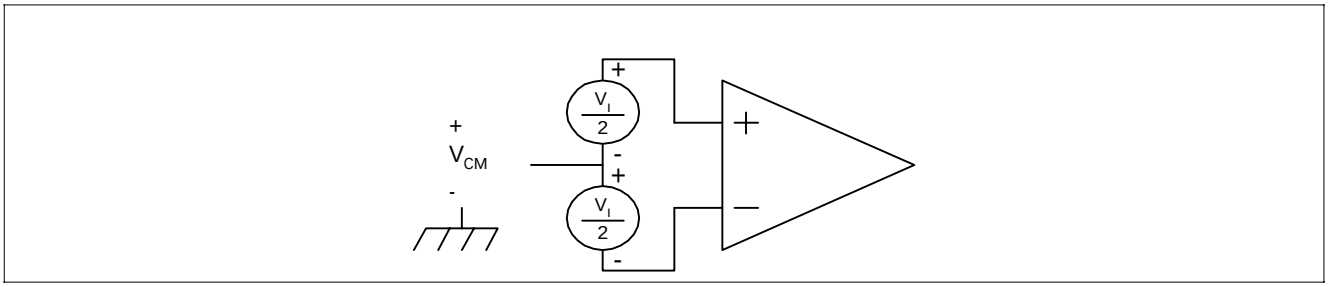


Figure 7-2: LVD Receiver

Table 7-5: SCSI Signal —DIFFSENS

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	High voltage differential sense voltage	2.4	V_{DD} + 0.3	V	-
V_S	LVD sense voltage	.7	1.9	V	-
V_{IL}	Single-ended sense voltage	V_{SS} - 0.3	0.5	V	-
I_{OZ}	Tristate leakage	-10	10	µA	-

Table 7-6: SCSI Signals—RBIAS+/-

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IN}	Input voltage	V_{DD} - 0.2	-	V	- 125 µA

Table 7-7: Capacitance

Symbol	Parameter	Min	Max	Unit	Test Conditions
C_I	Input capacitance of input pads	-	7	pF	-
C_{IO}	Input capacitance of I/O pads	-	15	pF	-

Table 7-8: Output Signal— MAC/_TESTOUT

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{OH}	Output high voltage	2.4	V_{DD}	V	-16 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	16 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Table 7-9: Input Signals—CLK*, RST/*, IDSEL, GNT/, SCLK/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V5BIAS(+)	V	-
V_{IL}	Input low voltage	V_{SS} - 0.3	0.3 V_{DD}	V	-
I_{IN}	Input current	-10	10	µA	-
I_{PULL}	Pull-up current	25	-	µA	

I_{PULL} not possible

Table 7-10: Bidirectional Signals— AD(31-0), C_BE/(3-0), FRAME/, IRDY/, TRDY/, DEVSEL/, STOP/, PERR/, PAR, REQ/ IRQ/, SERR/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	0.5 V_{DD}	V5BIAS(+)	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.3 V_{DD}	V	-
V_{OH}	Output high voltage	0.9 V_{DD}	V_{DD}	V	-0.5 µA
V_{OL}	Output low voltage	V_{SS}	0.1 V_{DD}	V	1.5 µA
I_{OZ}	Tristate leakage	-10	10	µA	-
I_{PULL}	Pull-up current	25		µA	

Table 7-11: Bidirectional Signals—GPIO0_FETCH/, GPIO1_MASTER/, GPIO2, GPIO3, GPIO4, MAD(7-0)

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS(-)	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	-8 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	8 mA
I_{OZ}	Tristate leakage	-10	10	µA	-

Table 7-12: Bidirectional Signals—MAS/(1-0), MCE/, MOE/, MWE/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS(+ or -?)	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
V_{OH}	Output high voltage	2.4	V_{DD}	V	-4 mA
V_{OL}	Output low voltage	V_{SS}	0.4	V	4 mA
I_{OZ}	Tristate leakage	-10	10	µA	-
I_{PULL}	Pull-up current	25		µA	

Table 7-13: Input Signal— BIG_LIT/

Symbol	Parameter	Min	Max	Unit	Test Conditions
V_{IH}	Input high voltage	2.0	V5BIAS(+)	V	-
V_{IL}	Input low voltage	V_{SS} - 0.5	0.8	V	-
I_{IN}	Input current	-10	10	µA	-
I_{PULL}	Pull-up current	25	-	µA	

TolerANT Technology Electrical Characteristics

Table 7-14: TolerANT Technology Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{OH}[1]	Output high voltage	2.0	V_{DD} + 0.3	V	I_{OH} = 7 mA
V_{OL}	Output low voltage	V_{SS}	0.5	V	I_{OL} = 48 mA
V_{IH}	Input high voltage	2.0	V_{DD} + 0.3	V	-
V_{IL}	Input low voltage	V_{SS} - 0.3	0.8	V	Referenced to V_{SS}
V_{IK}	Input clamp voltage	-0.66	-0.77	V	V_{DD} = 4.75; I_I = -20 mA
V_{TH}	Threshold, high to low	1.0	1.2	V	-
V_{TL}	Threshold, low to high	1.4	1.6	V	-
V_{TH}- V_{TL}	Hysteresis	300	500	mV	-
I_{OH}[1]	Output high current	2.5	24	mA	V_{OH} = 2.5 V
I_{OL}	Output low current	100	200	mA	V_{OL} = 0.5 V
I_{OSH}[1]	Short-circuit output high current	-	625	mA	Output driving low, pin shorted to V_{DD} supply[2]
I_{OSL}	Short-circuit output low current	-	95	mA	Output driving high, pin shorted to V_{SS} supply
I_{LH}	Input high leakage	-	20	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 2.7 V
I_{LL}	Input low leakage	-	-20	µA	-0.5 < V_{DD} < 5.25 V_{PIN} = 0.5 V
R_I	Input resistance	20	-	MΩ	SCSI pins[3]
C_P	Capacitance per pin	-	15	pF	PQFP
t_R[1]	Rise time, 10% to 90%	4.0	18.5	ns	Figure 7-1
t_F	Fall time, 90% to 10%	4.0	18.5	ns	Figure 7-1
dV_H/dt	Slew rate, low to high	0.15	0.50	V/ns	Figure 7-1

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.
[1] Active negation outputs only: Data, Parity, SREQ/, SACK/
[2] Single pin only; irreversible damage may occur if sustained for one second
[3] SCSI RESET pin has 10 KΩ pull-up resistor

Table 7-14: TolerANT Technology Electrical Characteristics (Continued)

Symbol	Parameter	Min	Max	Units	Test Conditions
dV_L/dt	Slew rate, high to low	0.15	0.50	V/ns	Figure 7-1
ESD	Electrostatic discharge	2	-	KV	MIL-STD-883C; 3015-7
	Latch-up	100	-	mA	-
	Filter delay	20	30	ns	Figure 7-2
	Ultra filter delay	10	15	ns	Figure 7-2
	Ultra2 filter delay	5	8	ns	Figure 7-2
	Extended filter delay	40	60	ns	Figure 7-2

Note: These values are guaranteed by periodic characterization; they are not 100% tested on every device.
[1] Active negation outputs only: Data, Parity, SREQ/, SACK/
[2] Single pin only; irreversible damage may occur if sustained for one second
[3] SCSI RESET pin has 10 KΩ pull-up resistor

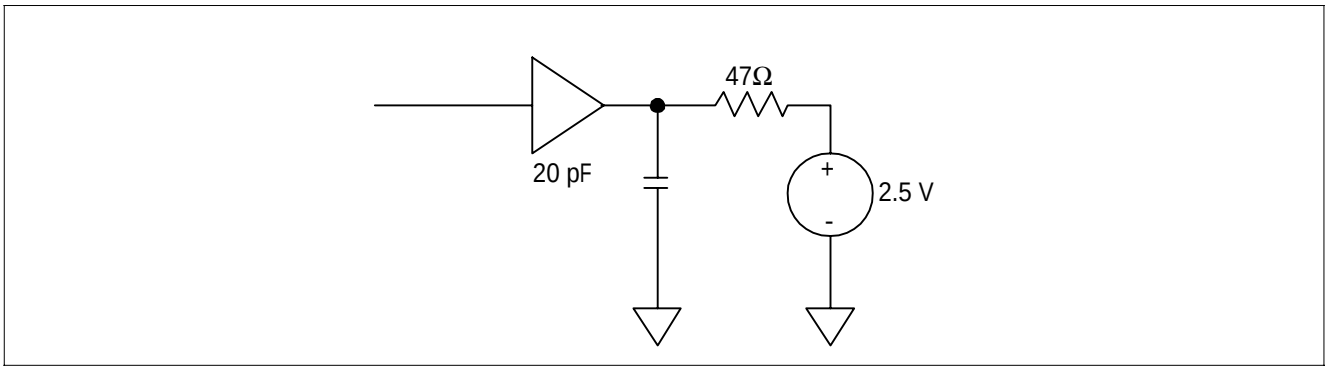


Figure 7-3: Rise and Fall Time Test Conditions

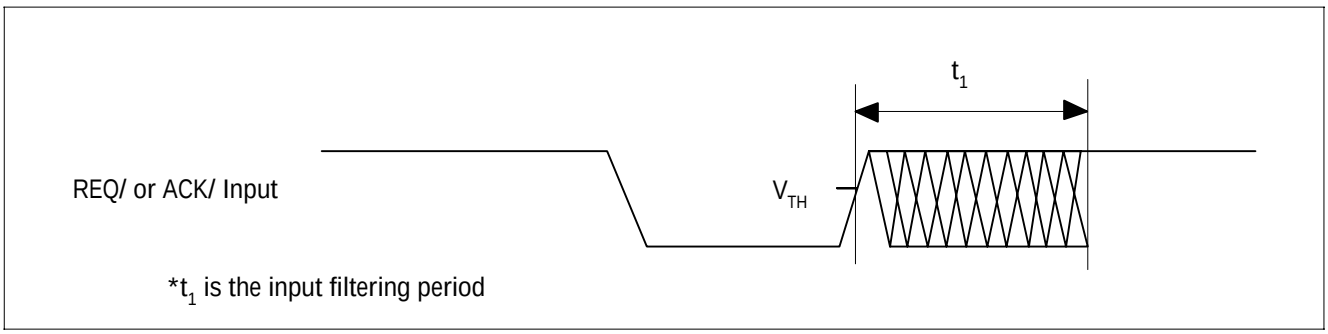


Figure 7-4: SCSI Input Filtering

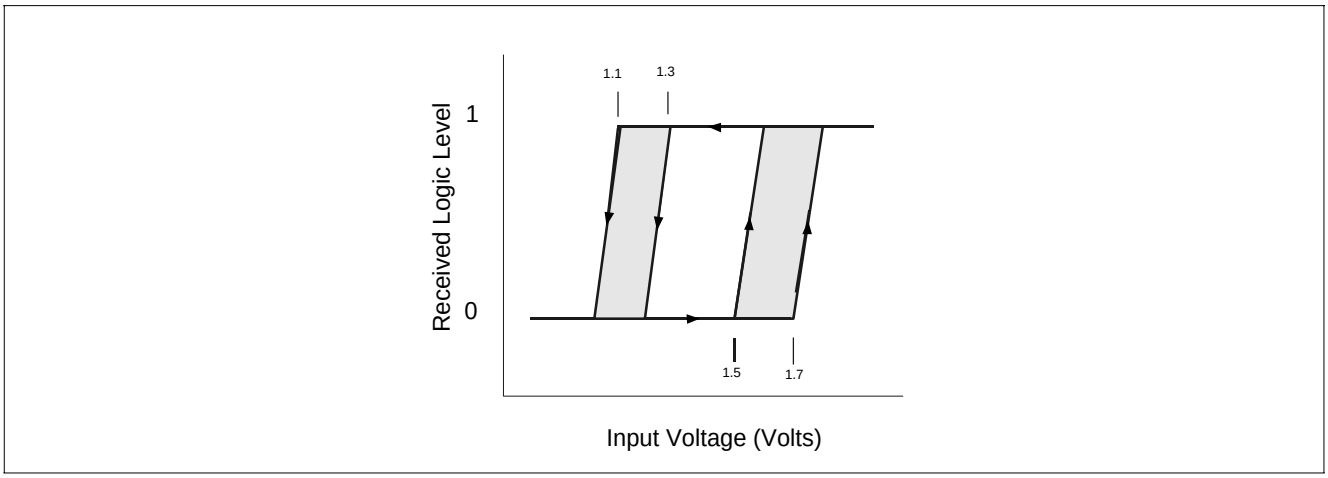


Figure 7-5: Hysteresis of SCSI Receiver

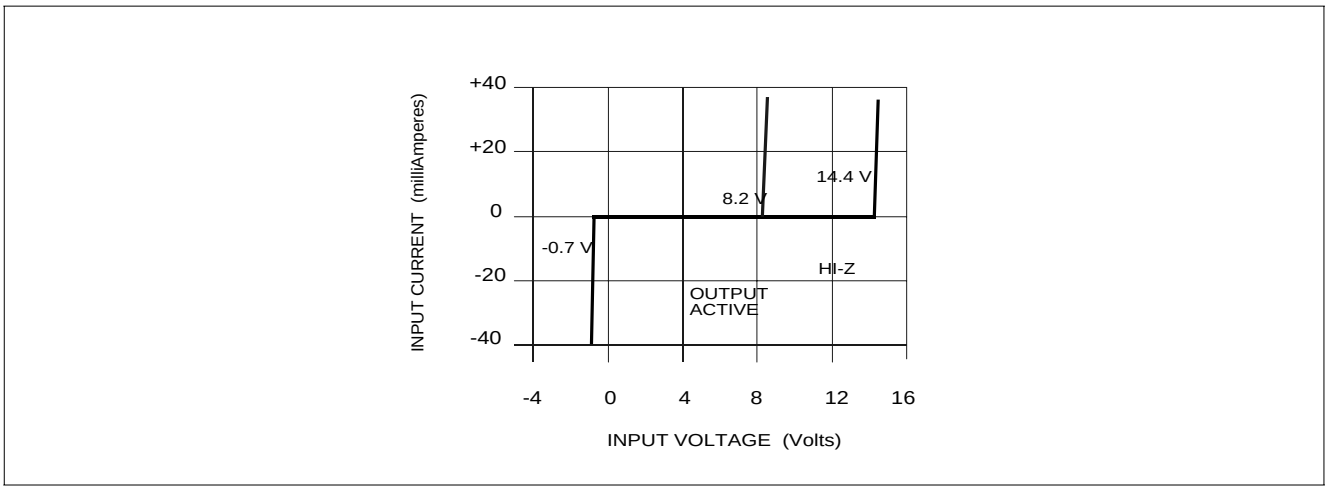


Figure 7-6: Input Current as a Function of Input Voltage

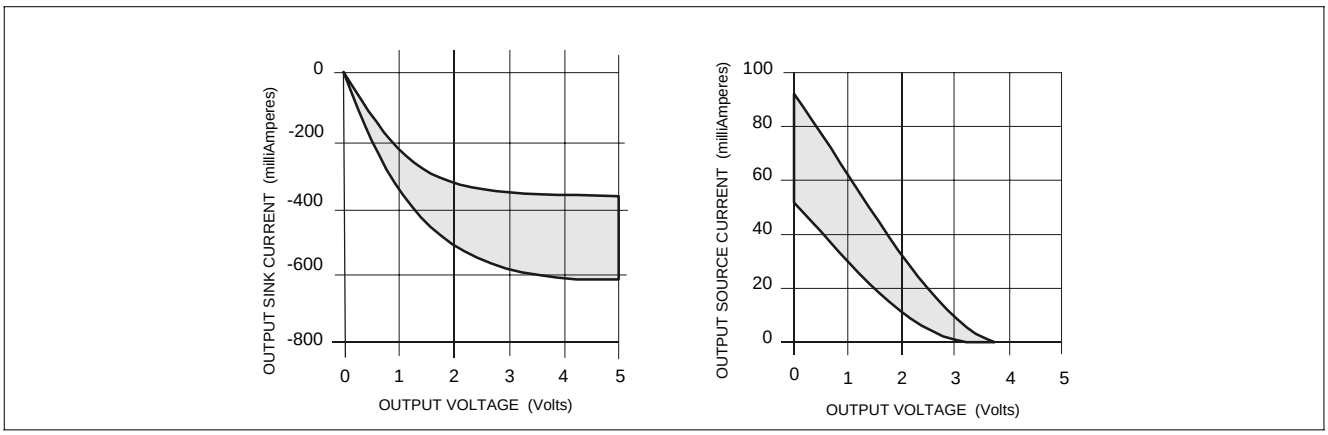


Figure 7-7: Output Current as a Function of Output Voltage

AC Characteristics

The AC characteristics described in this section apply over the entire range of operating conditions (refer to the DC Characteristics section). Chip timings are based on simulation at worst case voltage, temperature, and processing. Timings were developed with a load capacitance of 50 pF.

Figure 7-8: External Clock Timing

Symbol	Parameter	Min	Max	Units
t_1	Bus clock cycle time	30	DC	ns
	SCSI clock cycle time (SCLK)*	25	60	ns
t_2	CLK low time**	10	-	ns
	SCLK low time**	6	33	ns
t_3	CLK high time**	12	-	ns
	SCLK high time**	10	33	ns
t_4	CLK slew rate	1	-	V/ns
	SCLK slew rate	1	-	V/ns

Timings are for an external 40 MHz clock. A quadrupled 40 MHz clock is required for Ultra2 SCSI operation.

** This parameter must be met to insure SCSI timings are within specification*

***Duty cycle not to exceed 60/40*

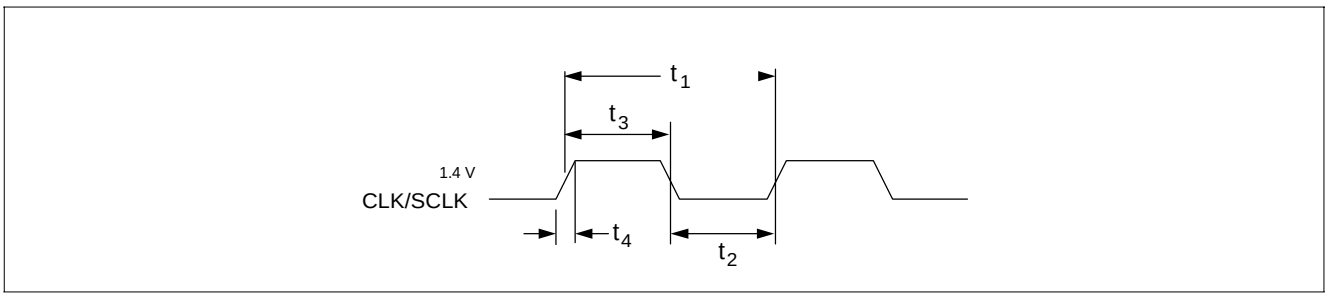


Figure 7-9: Reset Input

Symbol	Parameter	Min	Max	Units
t_1	Reset pulse width	10	-	t_{CLK}
t_2	Reset deasserted setup to CLK high	0	-	ns
t_3	MAD setup time to CLK high (for configuring the MAD bus only)	20	-	ns
t_4	MAD hold time from CLK high (for configuring the MAD bus only)	20	-	ns

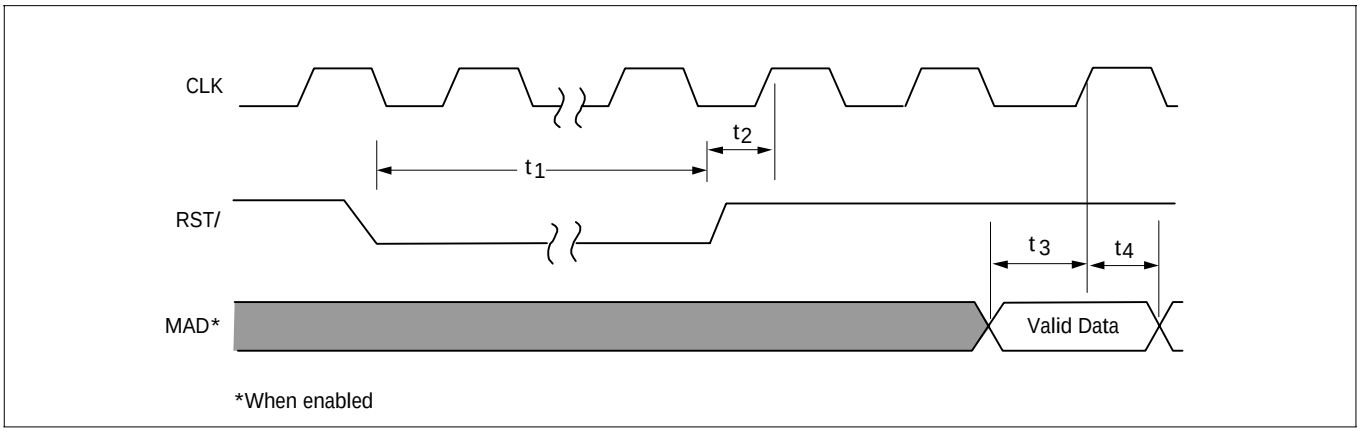
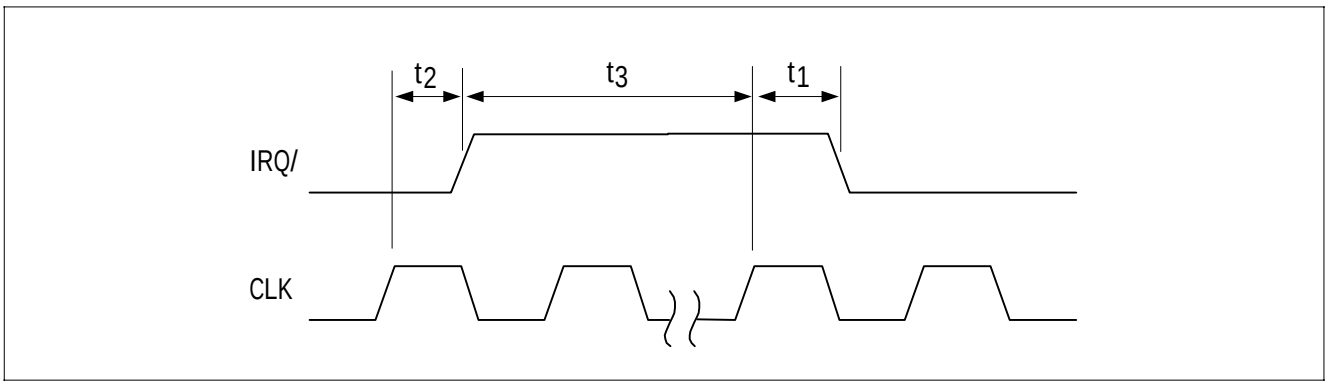


Figure 7-10: Interrupt Output

Symbol	Parameter	Min	Max	Units
t_1	CLK high to IRQ/ low	2	11	ns
t_2	CLK high to IRQ/ high	2	11	ns
t_3	IRQ/ deassertion time	3	-	CLKs



PCI and External Memory Interface Timing Diagrams

Figure 7-11 through Figure 7 represent signal activity when the SYM53C895 accesses the PCI bus. This section includes timing diagrams for access to three groups of external memory configurations. The first group applies to systems with memory size of 64 KB and above; one byte read or write cycle, and fast or normal ROMs. The second group applies to systems with memory size of 64 KB and above, one-byte read or write cycles, and slow ROMs. The third group applies to systems with memory size of 64 KB or less, one-byte read or write cycles, and normal or fast ROM.

Note: Multiple byte accesses to the external memory bus increase the read or write cycle by 11 clocks for each additional byte.

Timing diagrams included in this section

Target Cycles

- PCI configuration register read
- PCI configuration register write
- Operating Register/SCRIPTS RAM read
- Operating Register/SCRIPTS RAM write
- External Memory Read
- External Memory Write

Initiator Cycles

- Op code fetch, non-burst
- Burst op code fetch
- Back-to-back read
- Back-to-back write
- Burst read
- Burst write

External Memory Cycles

- Read cycle, normal/fast memory (≥128 KB), single-byte access
- Write cycle, normal/fast memory (≥ 128 KB), single-byte access
- Read cycle, normal/fast memory (≥ 128 KB), multiple-byte access
- Write cycle, normal/fast memory (≥ 128 KB), multiple-byte access
- Read cycle, slow memory (≥ 128 KB)
- Write cycle, slow memory ≥ 128 KB)
- Read cycle, 64 KB ROM
- Write cycle, 64 KB ROM

Table 7-15: Configuration Register Read Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns

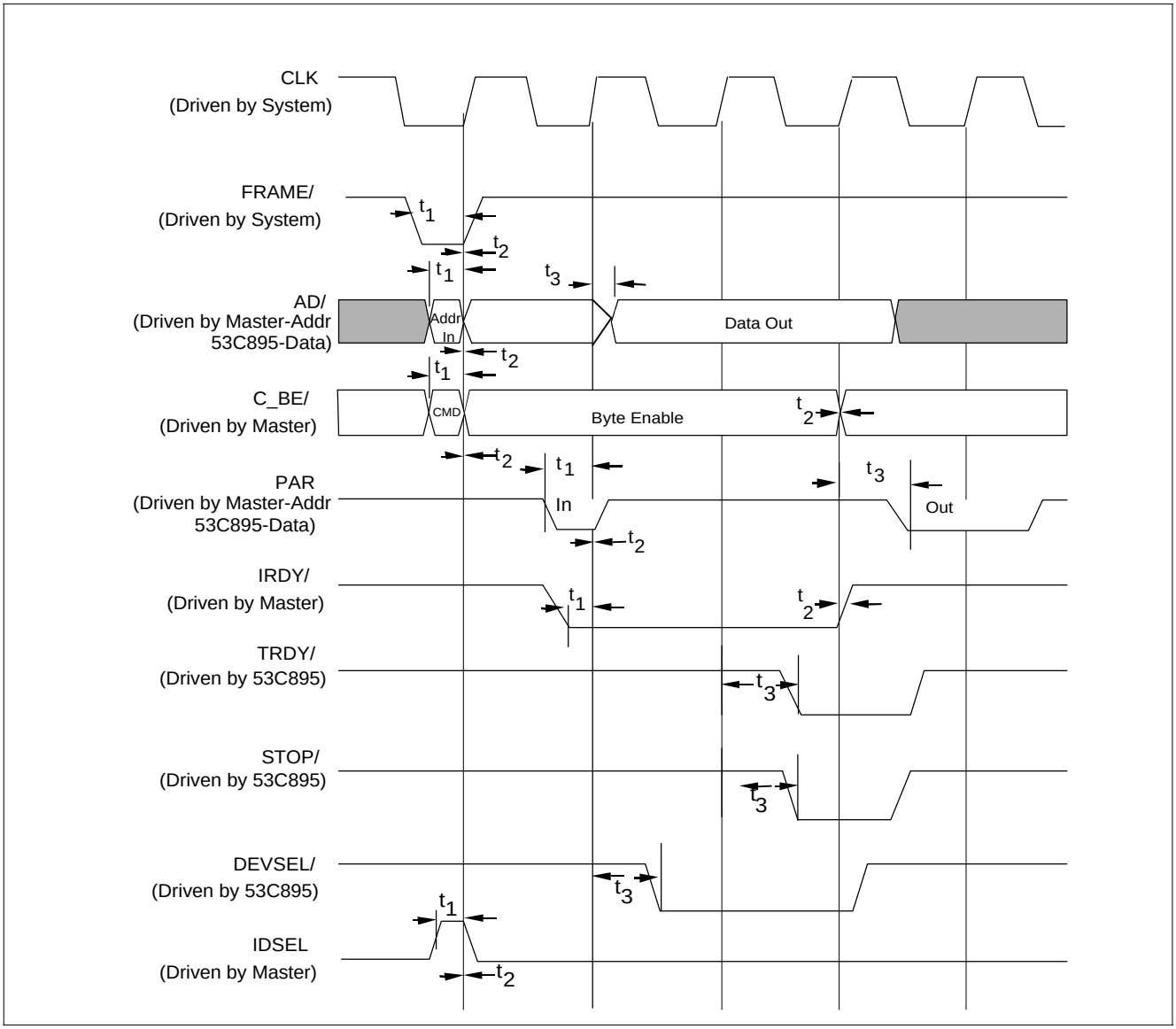


Figure 7-11: PCI Configuration Register Read

Table 7-16: Configuration Register Write Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns

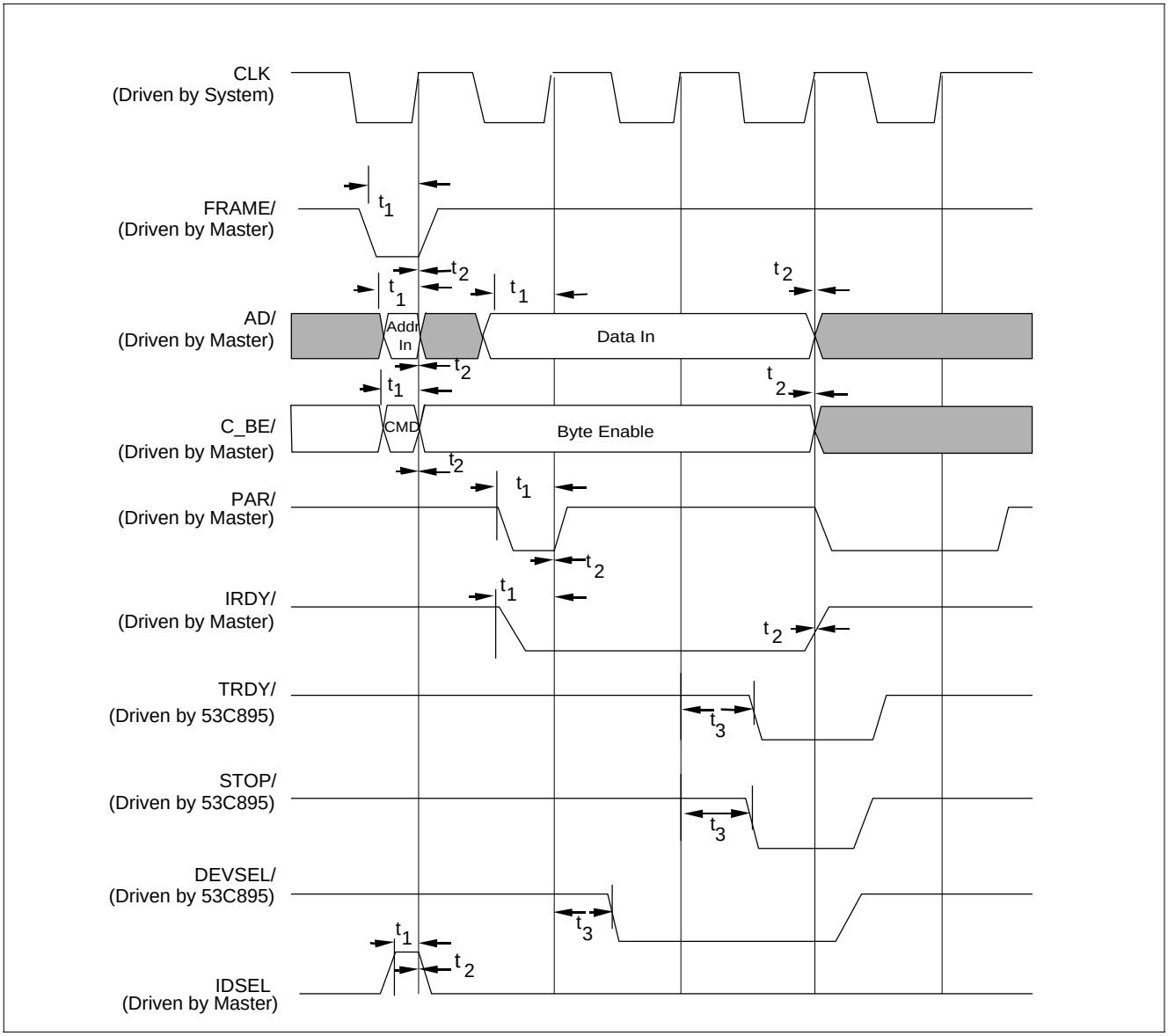


Figure 7-12: PCI Configuration Register Write

Table 7-17: Operating Register/SCRIPTS RAM Read Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns

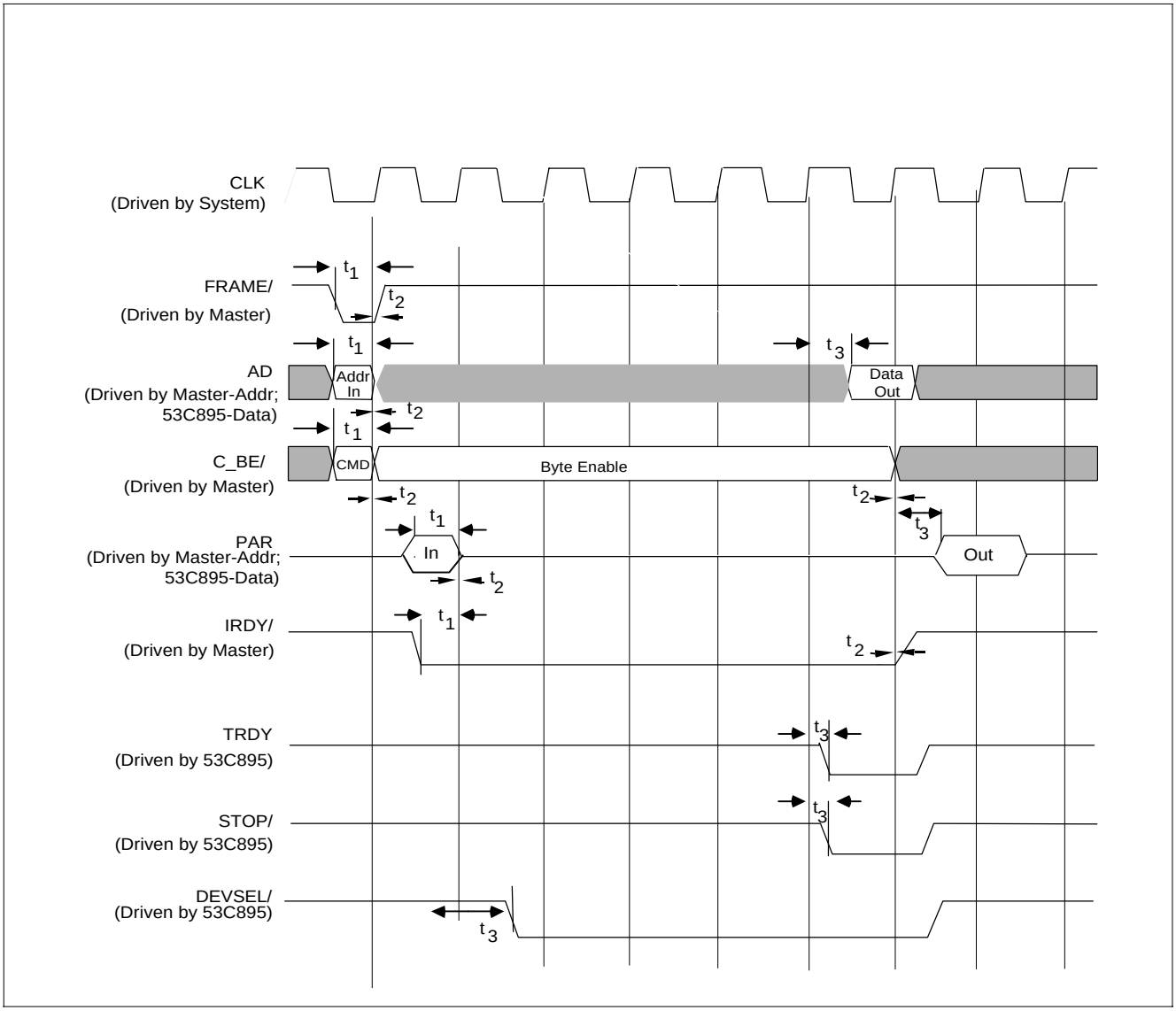


Figure 7-13: Operating Register/SCRIPTS RAM Read

Table 7-18: Operating Register/SCRIPTS RAM Write Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns

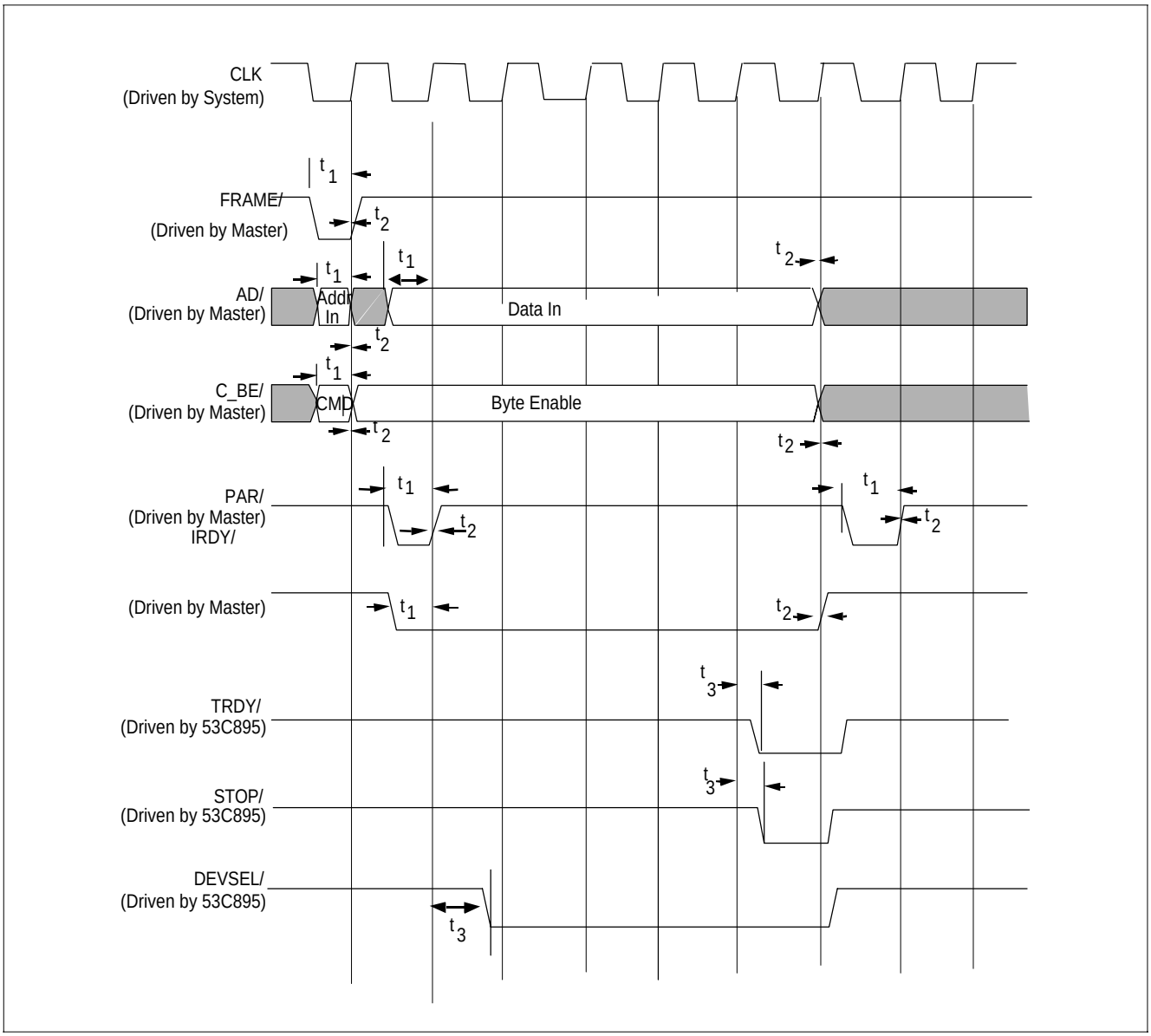


Figure 7-14: Operating Register/SCRIPTS RAM Write

Table 7-19: External Memory Read Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns
t_4	Side signal input setup time	10	-	ns
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{14}	MCE/ low to data clocked in	160	-	ns
t_{15}	Address valid to data clocked in	205	-	ns
t_{16}	MOE/ low to data clocked in	100	-	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	-	ns
t_{18}	Address out from MOE/, MCE/ high	50	-	ns
t_{19}	Data setup to CLK high	5	-	ns

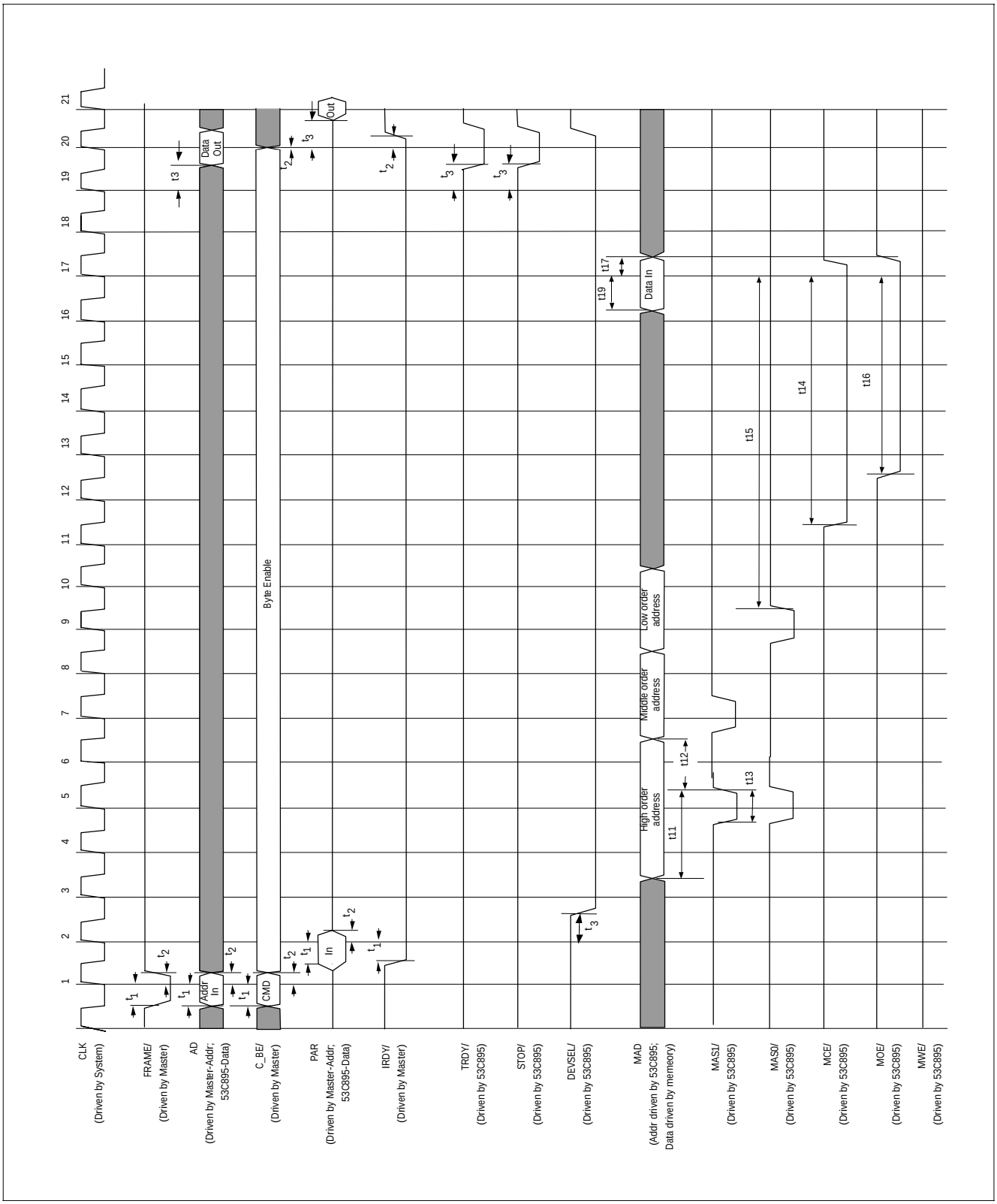


Figure 7-15: External Memory Read

Table 7-20: External Memory Write Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	-	11	ns
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{20}	Data setup to MWE/ low	30	-	ns
t_{21}	Data hold from MWE/ high	20	-	ns
t_{22}	MWE/ pulse width	100	-	ns
t_{23}	Address setup to MWE/ low	75	-	ns
t_{24}	MCE/ low to MWE/ high	120	-	ns
t_{25}	MCE/ low to MWE/ low	25	-	ns
t_{26}	MWE/ high to MCE/ high	25	-	ns

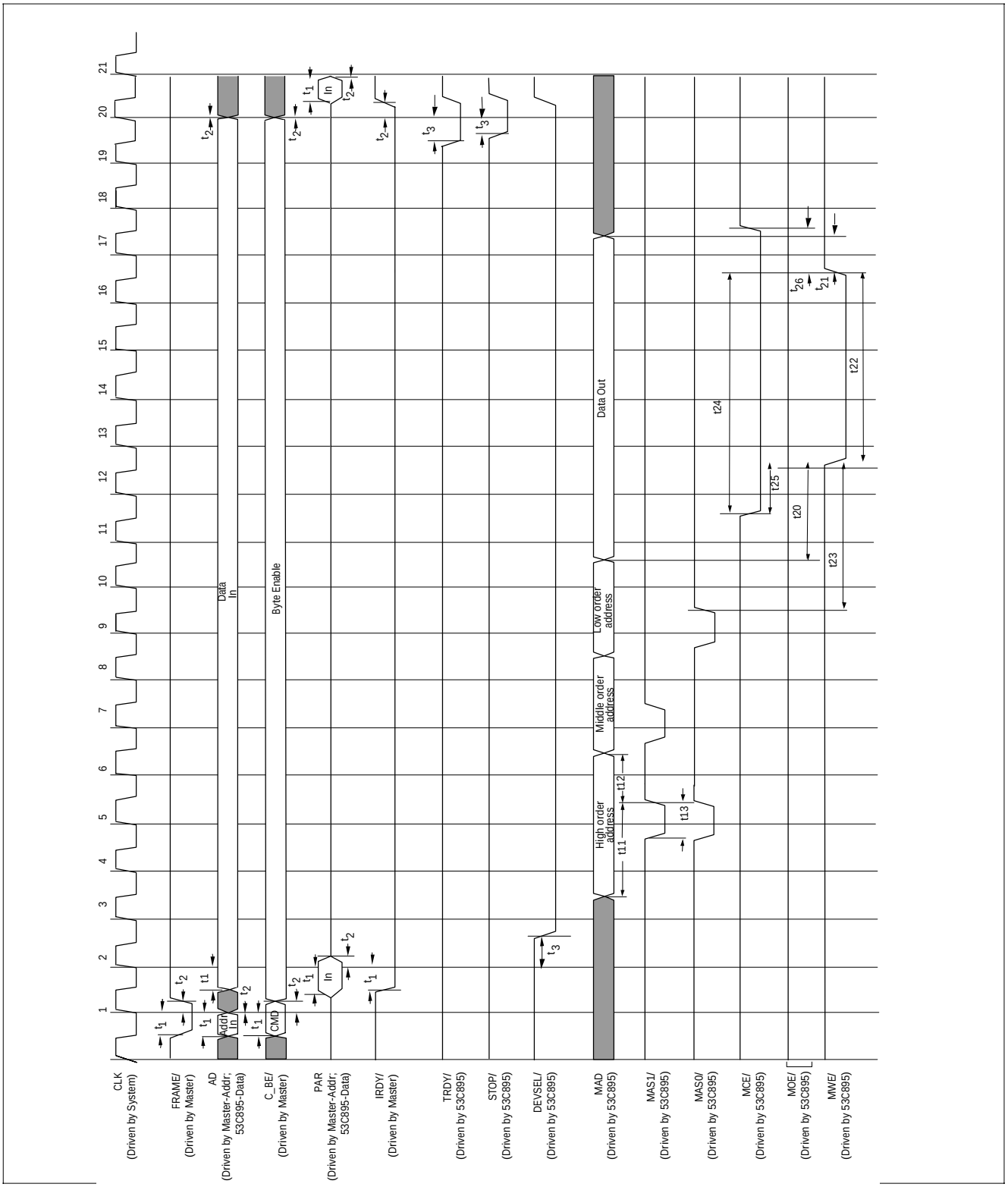


Figure 7-16: External Memory Write

Table 7-21: Op Code Fetch, non burst Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_7	CLK high to FETCH/ low	-	20	ns
t_8	CLK high to FETCH/ high	-	20	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

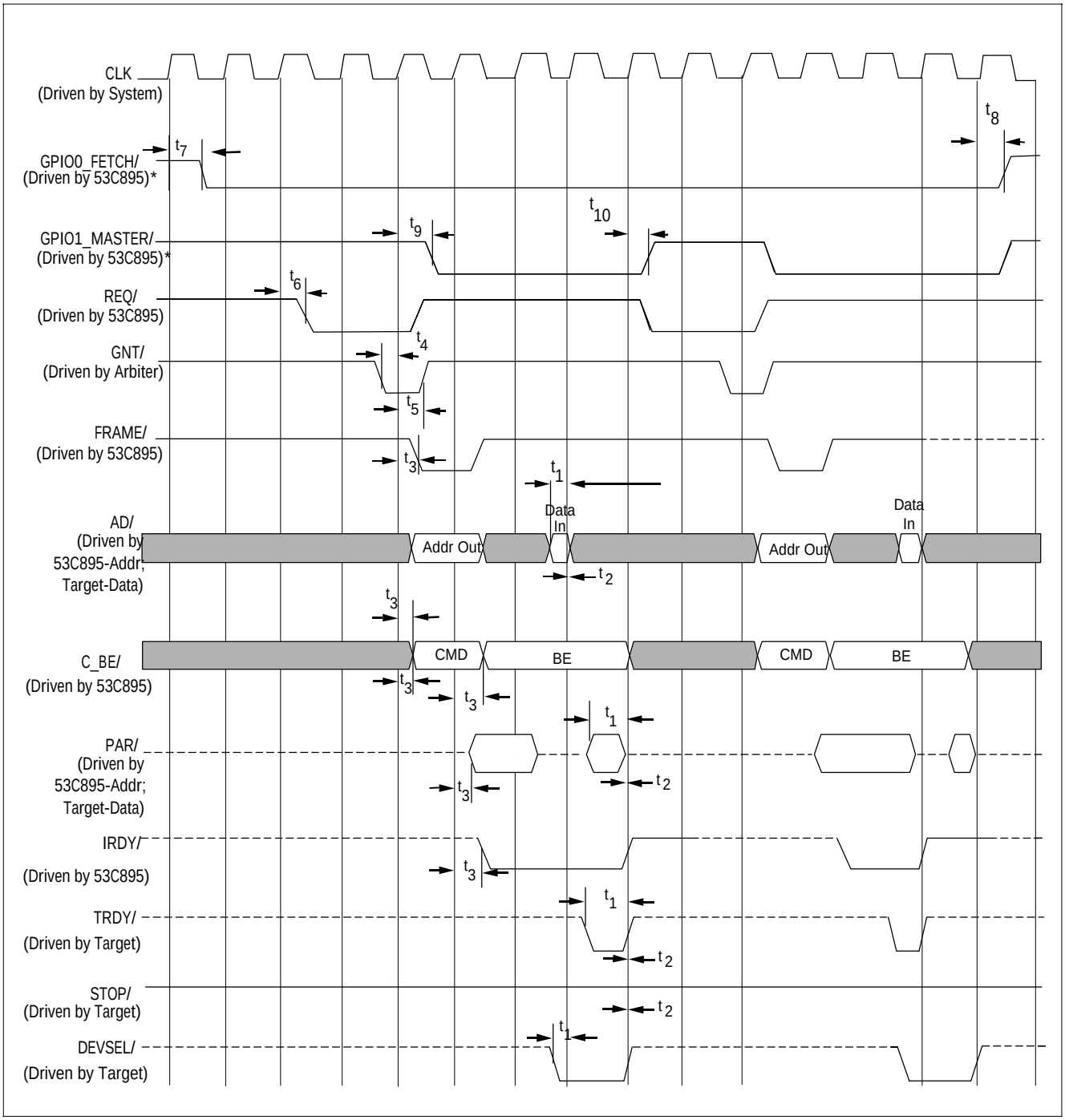


Figure 7-17: Op Code Fetch, non-burst

Table 7-22: Burst Op Code Fetch Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_7	CLK high to FETCH/low	-	20	ns
t_8	CLK high to FETCH/high	-	20	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

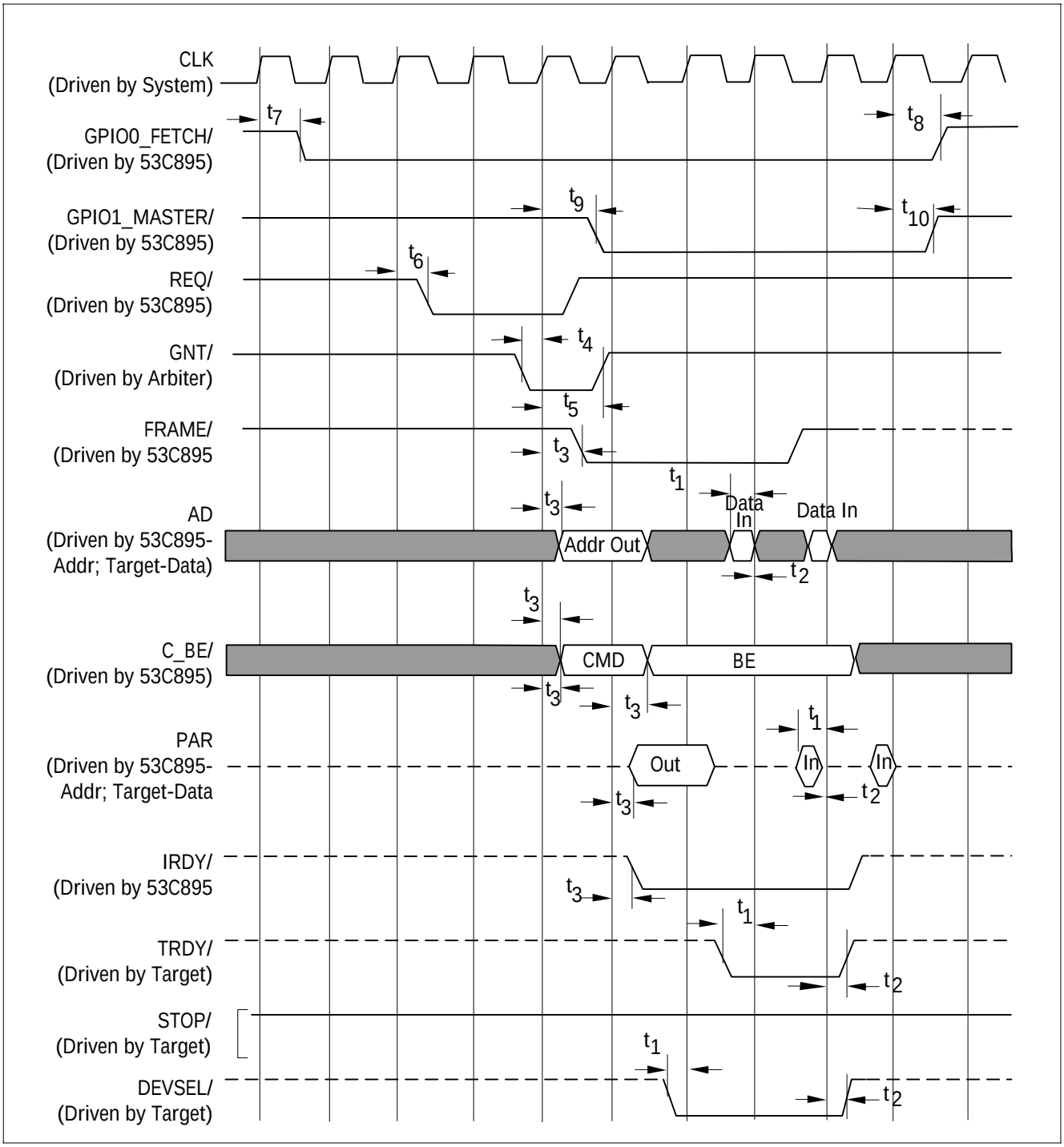


Figure 7-18: Burst Op Code Fetch

Table 7-23: Back to Back Read Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

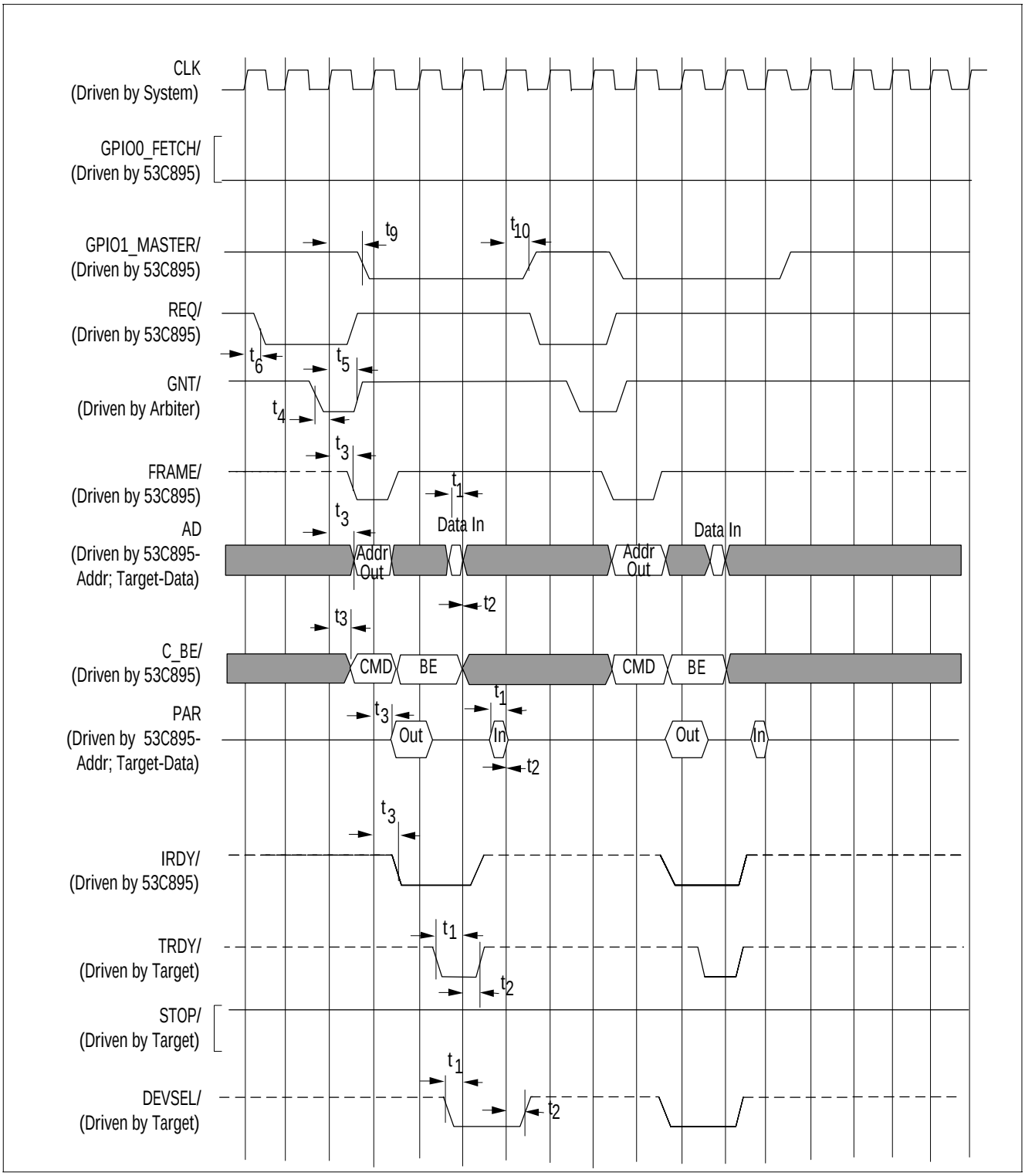


Figure 7-19: Back-to-Back Read

Table 7-24: Back to Back Write Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

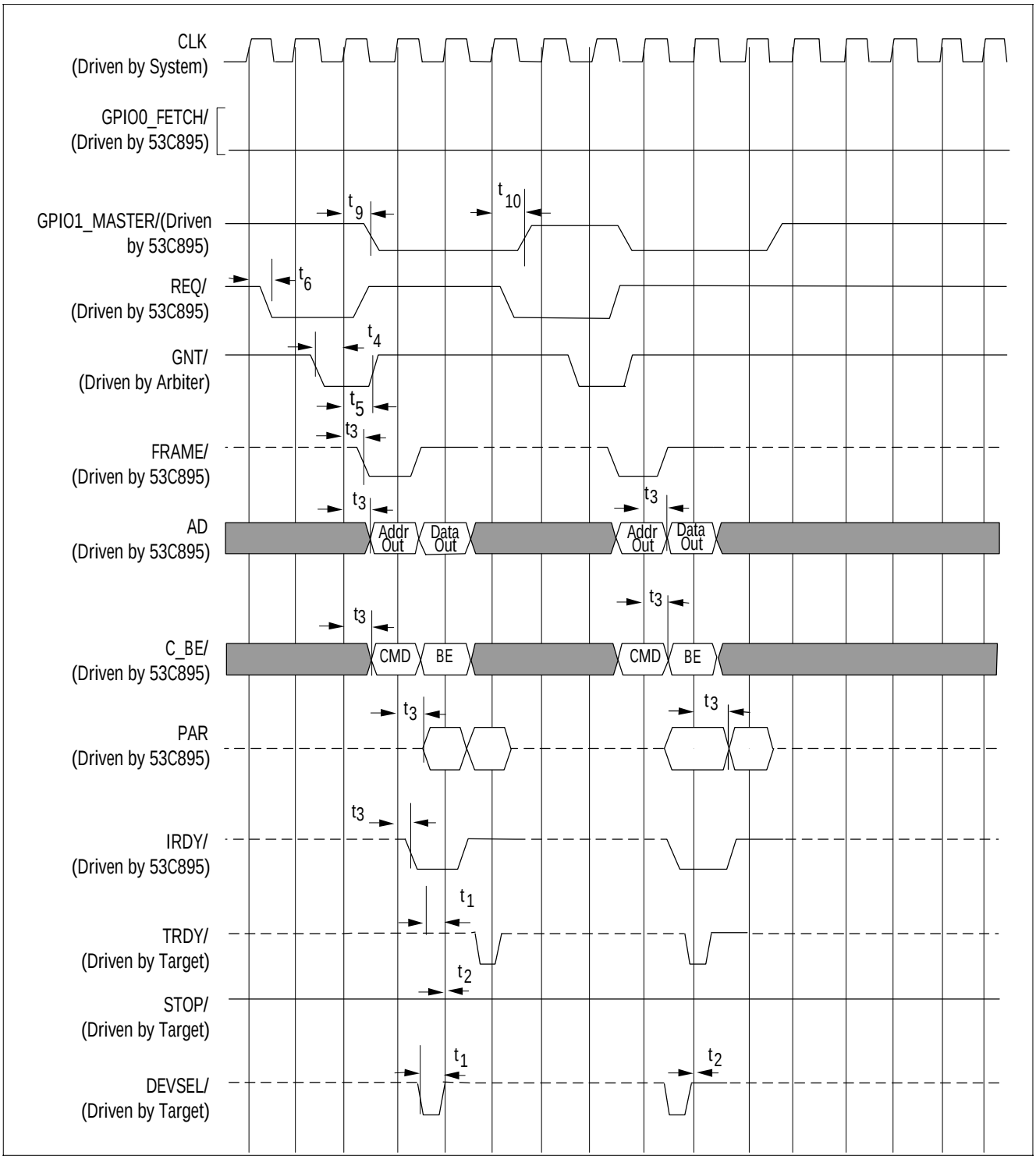


Figure 7-20: Back-to-Back Write

Table 7-25: Burst Read Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

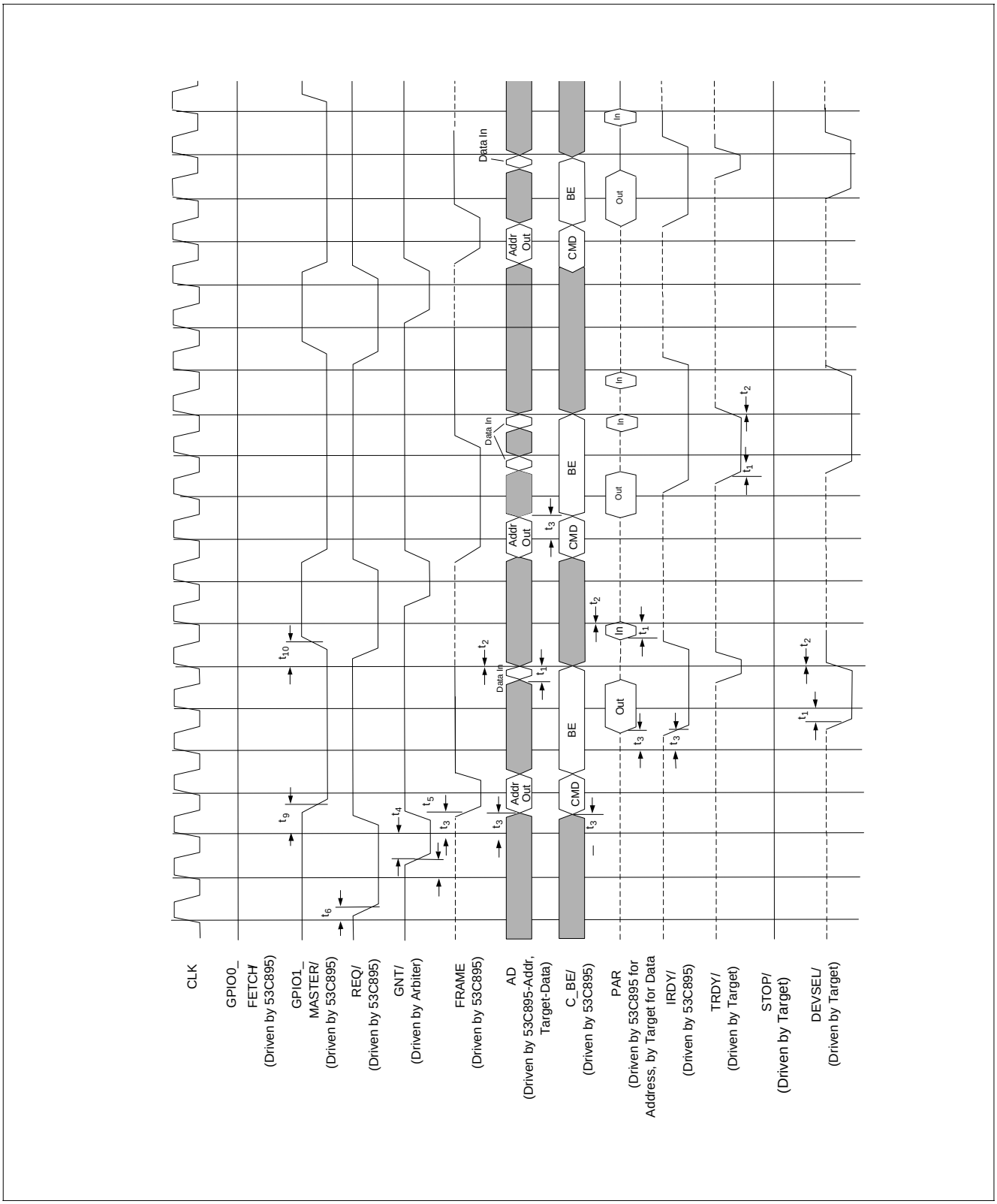


Figure 7-21: Burst Read

Table 7-26: Burst Write Timings

Symbol	Parameter	Min	Max	Unit
t_1	Shared signal input setup time	7	-	ns
t_2	Shared signal input hold time	0	-	ns
t_3	CLK to shared signal output valid	2	11	ns
t_4	Side signal input setup time	10	-	ns
t_5	Side signal input hold time	0	-	ns
t_6	CLK to side signal output valid	-	12	ns
t_9	CLK high to MASTER/ low	-	20	ns
t_{10}	CLK high to MASTER/ high	-	20	ns

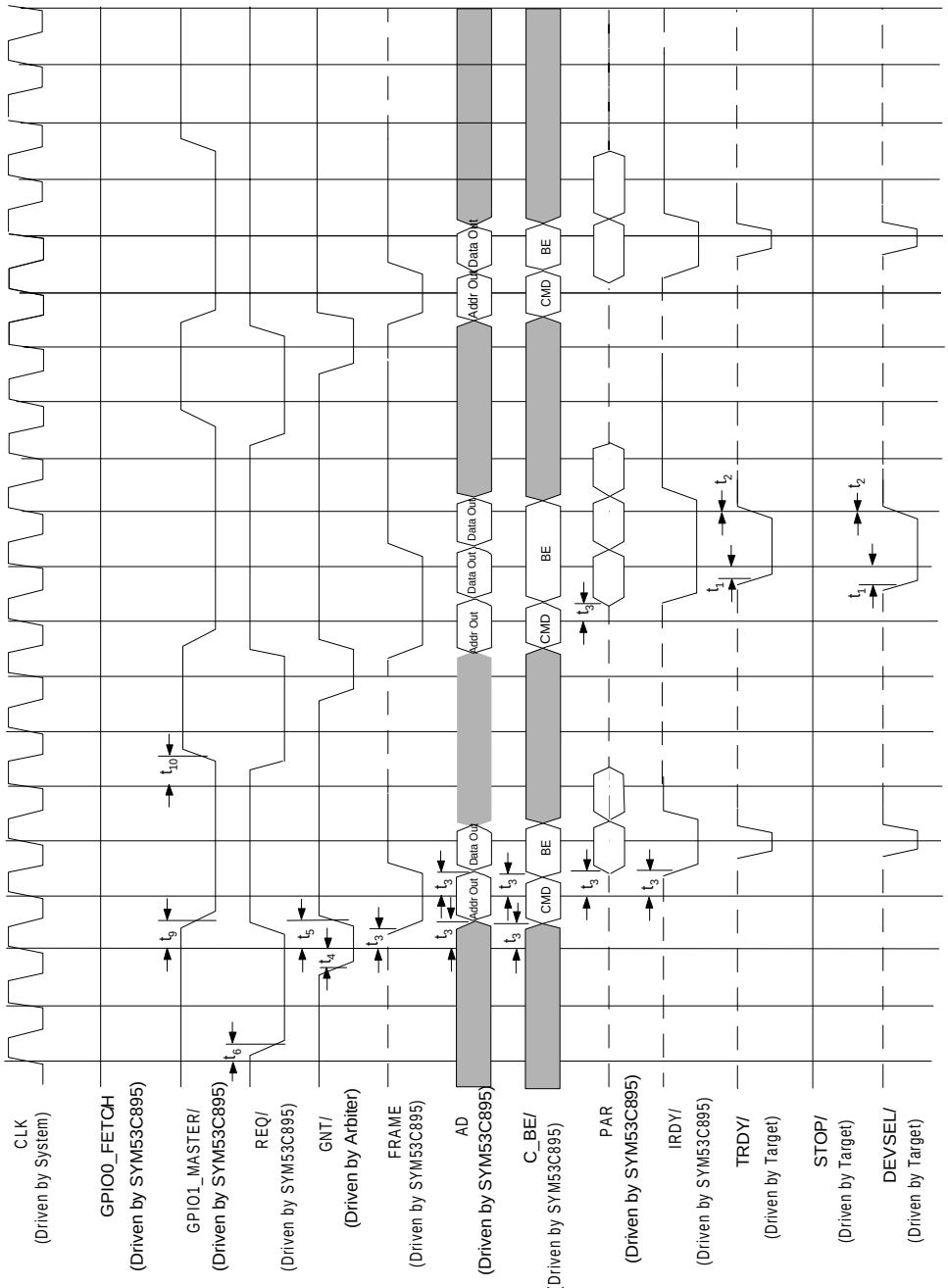


Figure 7-22: Burst Write

Table 7-27: Read Cycle TImings, Normal/Fast Memory (≥128 KB), single byte access

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{14}	MCE/ low to data clocked in	160	-	ns
t_{15}	Address valid to data clocked in	205	-	ns
t_{16}	MOE/ low to data clocked in	100	-	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	-	ns
t_{18}	Address out from MOE/, MCE/ high	50	-	ns
t_{19}	Data setup to CLK high	5	-	ns

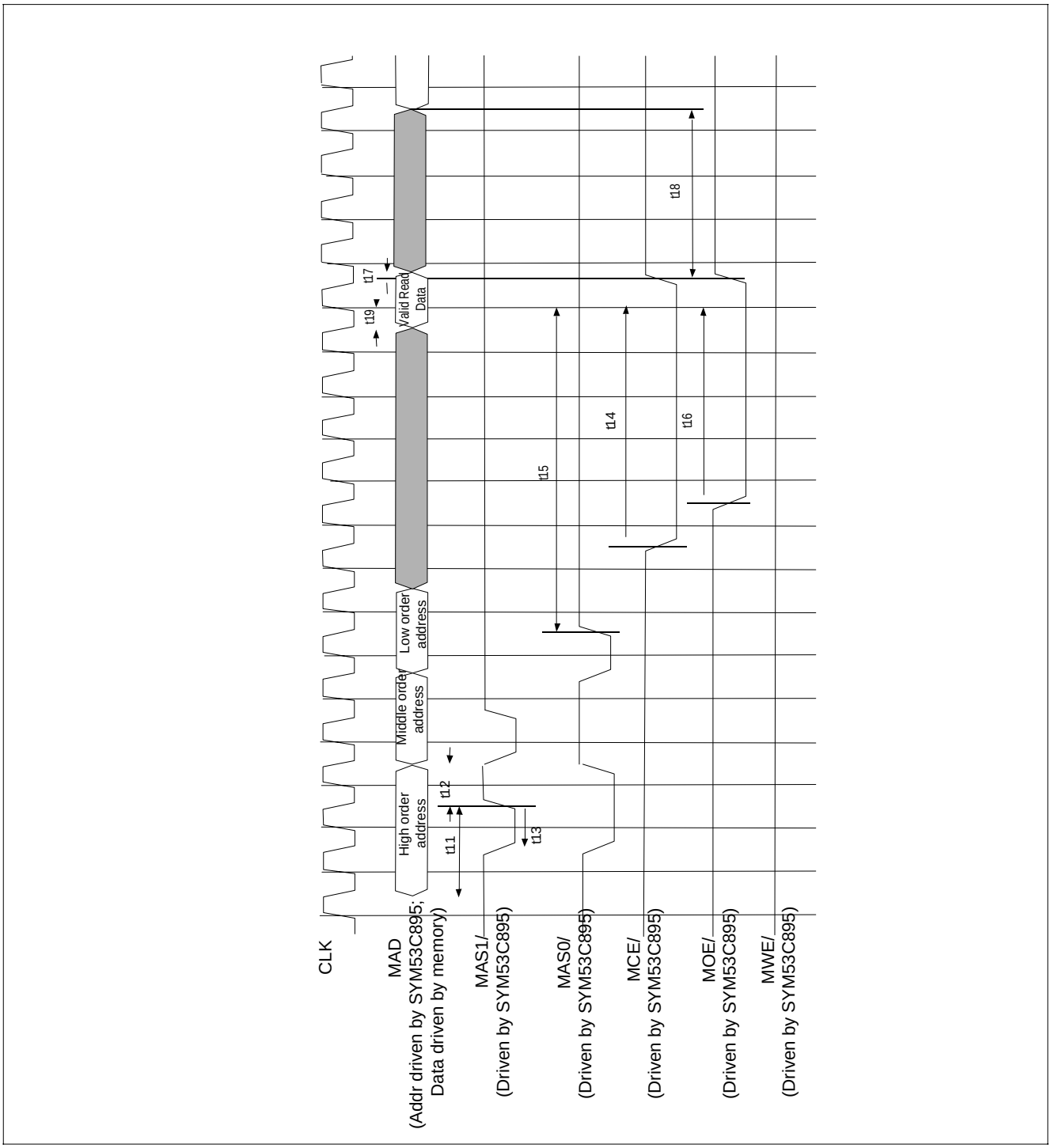


Figure 7-23: Read Cycle, Normal/Fast Memory (≥ 128 KB), single byte access

Table 7-28: Write Cycle Timings, Normal/Fast Memory (≥128 KB), single byte access

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{20}	Data setup to MWE/ low	30	-	ns
t_{21}	Data hold from MWE/ high	20	-	ns
t_{22}	MWE/ pulse width	100	-	ns
t_{23}	Address setup to MWE/ low	75	-	ns
t_{24}	MCE/ low to MWE/ high	120	-	ns
t_{25}	MCE/ low to MWE/ low	25	-	ns
t_{26}	MWE/ high to MCE/ high	25	-	ns

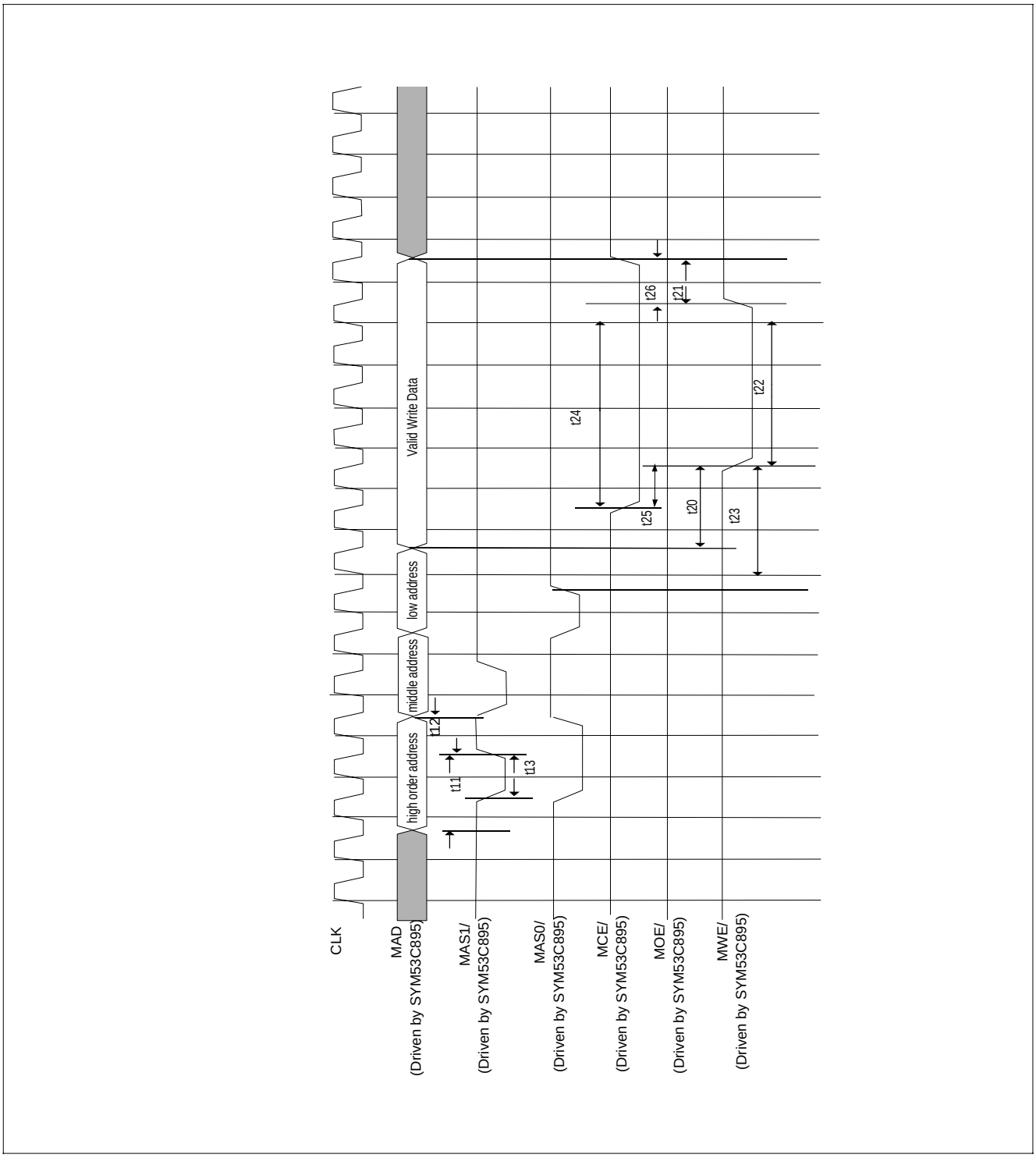


Figure 7-24: Write Cycle, Normal/Fast Memory (≥ 128 KB), single byte access

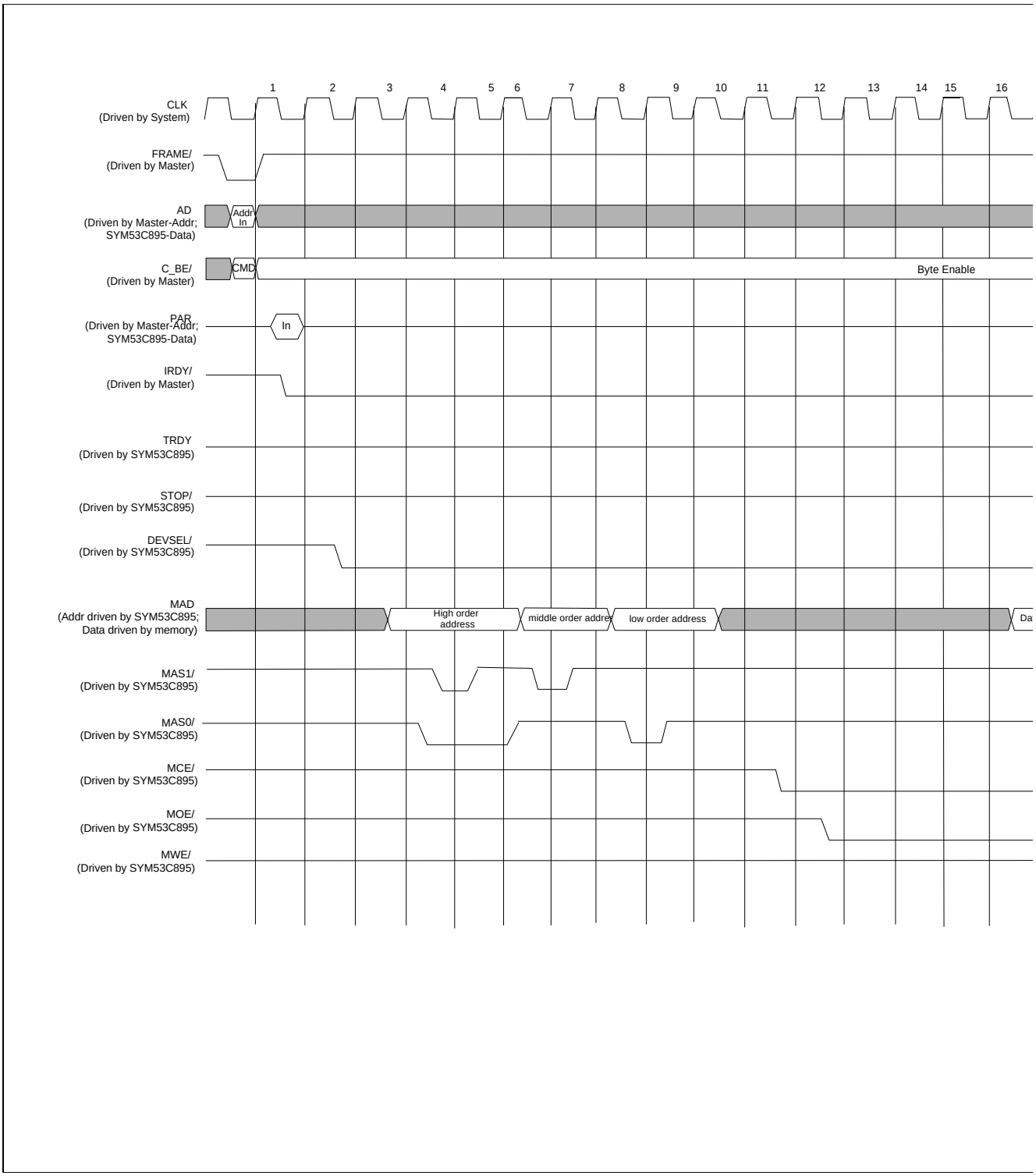


Figure 7-25: Read Cycle, Normal/Fast Memory (≥ 128 KB) multiple byte access

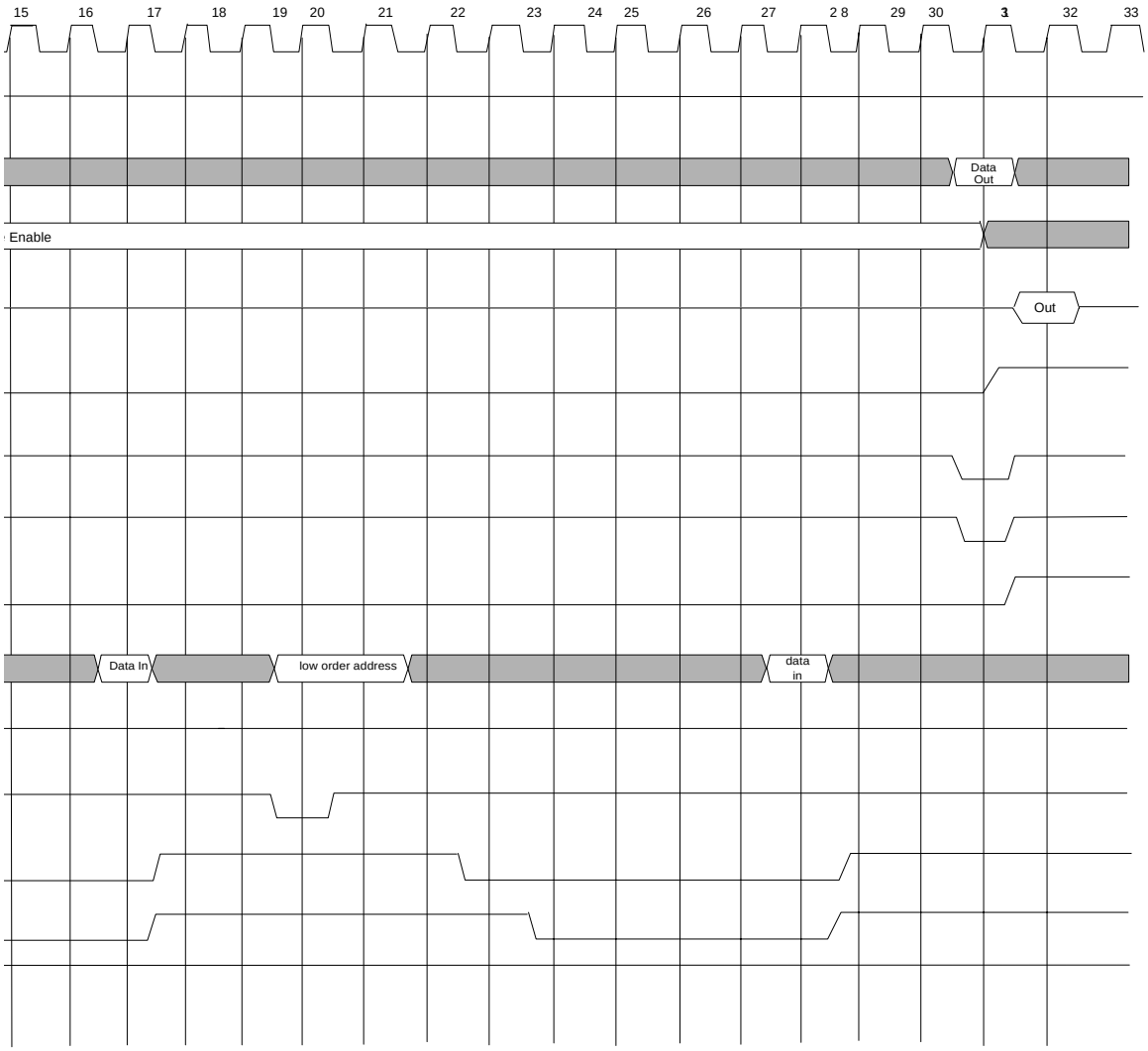


Figure 7-25: Read Cycle, Normal/Fast Memory (≥ 128 KB), multiple byte access (Continued)

Table 7-29: Read Cycle Timings, Slow Memory (≥128 KB)

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{14}	MCE/ low to data clocked in	160	-	ns
t_{15}	Address valid to data clocked in	205	-	ns
t_{16}	MOE/ low to data clocked in	100	-	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	-	ns
t_{18}	Address out from MOE/, MCE/ high	50	-	ns
t_{19}	Data setup to CLK high	5	-	ns

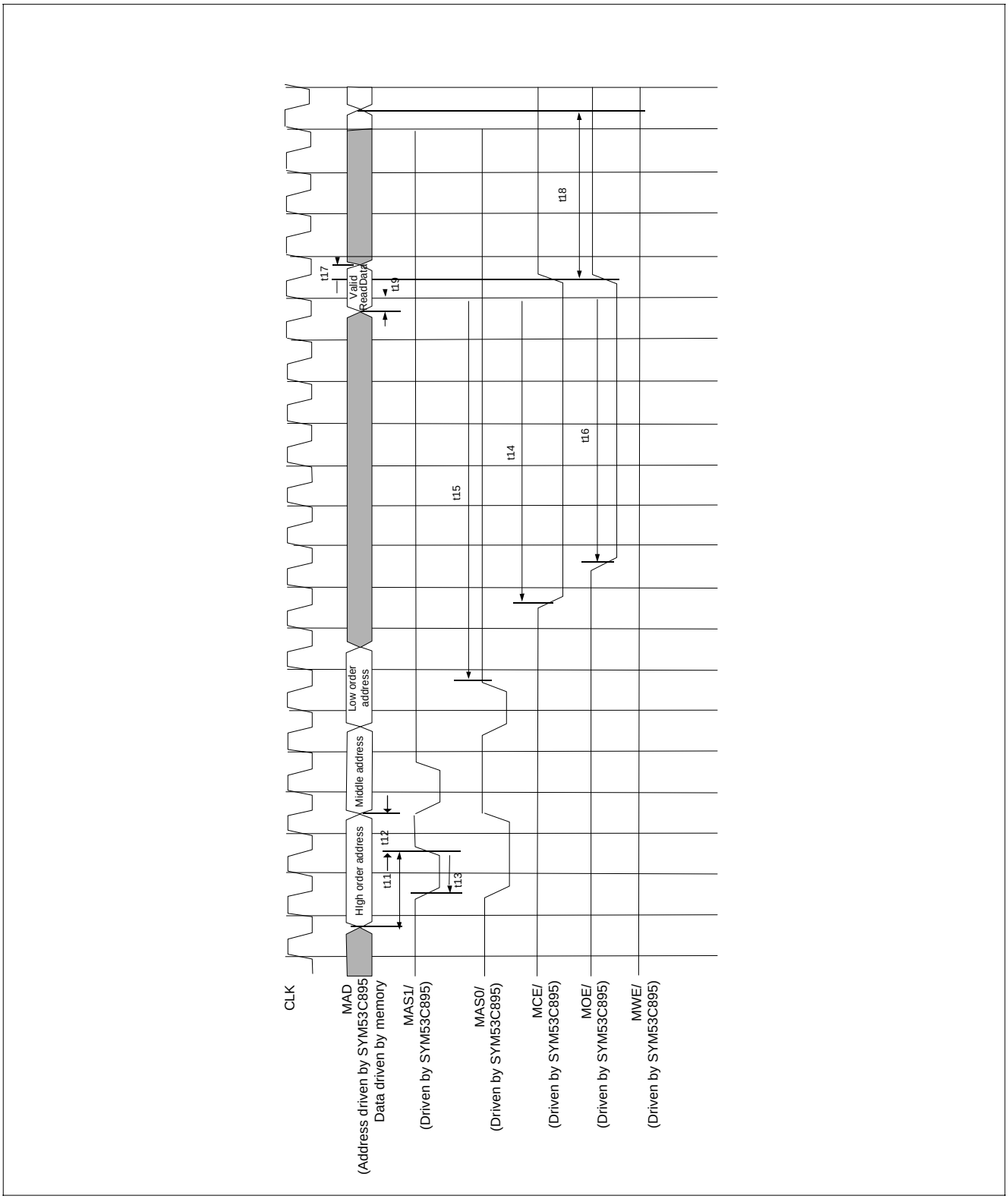


Figure 7-26: Read Cycle, Slow Memory (≥ 128 KB)

Table 7-30: Write Cycle Timings, Slow Memory (≥128 KB)

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{20}	Data setup to MWE/ low	30	-	ns
t_{21}	Data hold from MWE/ high	20	-	ns
t_{22}	MWE/ pulse width	100	-	ns
t_{23}	Address setup to MWE/ low	75	-	ns
t_{24}	MCE/ low to MWE/ high	120	-	ns
t_{25}	MCE/ low to MWE/ low	25	-	ns
t_{26}	MWE/ high to MCE/ high	25	-	ns

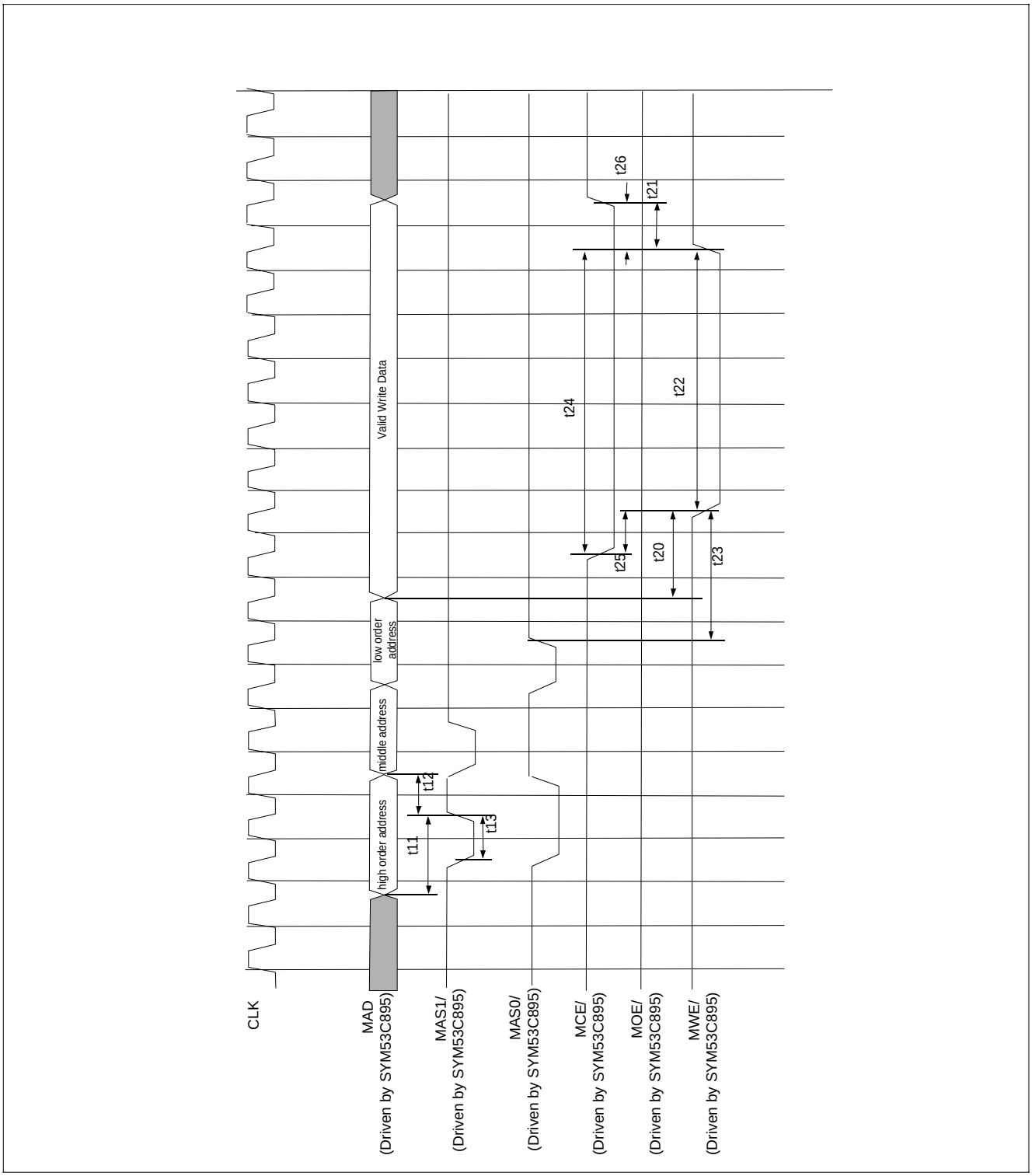


Figure 7-27: Write Cycle, Slow Memory (≥ 128 KB)

Table 7-31: Read Cycle Timings, ≤ 64 KB ROM

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{14}	MCE/ low to data clocked in	160	-	ns
t_{15}	Address valid to data clocked in	205	-	ns
t_{16}	MOE/ low to data clocked in	100	-	ns
t_{17}	Data hold from address, MOE/, MCE/ change	0	-	ns
t_{18}	Address out from MOE/, MCE/ high	50	-	ns
t_{19}	Data setup to CLK high	5	-	ns

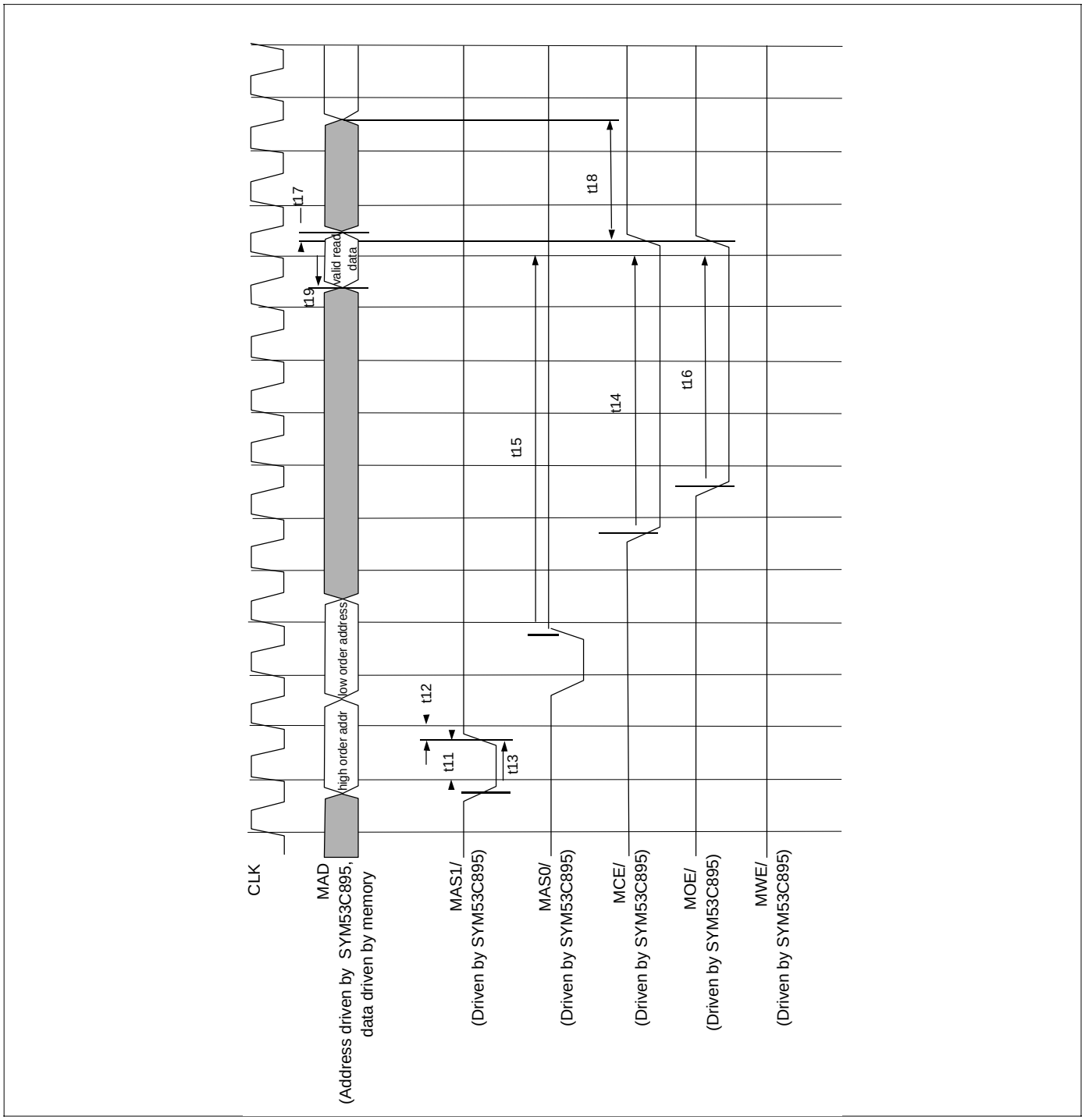


Figure 7-28: Read Cycle, ≤ 64 KB ROM

Table 7-32: Write Cycle Timings, ≤ 64 KB ROM

Symbol	Parameter	Min	Max	Unit
t_{11}	Address setup to MAS/ high	25	-	ns
t_{12}	Address hold from MAS/ high	15	-	ns
t_{13}	MAS/ pulse width	25	-	ns
t_{20}	Data setup to MWE/ low	30	-	ns
t_{21}	Data hold from MWE/ high	20	-	ns
t_{22}	MWE/ pulse width	100	-	ns
t_{23}	Address setup to MWE/ low	75	-	ns
t_{24}	MCE/ low to MWE/ high	120	-	ns
t_{25}	MCE/ low to MWE/ low	25	-	ns
t_{26}	MWE/ high to MCE/ high	25	-	ns

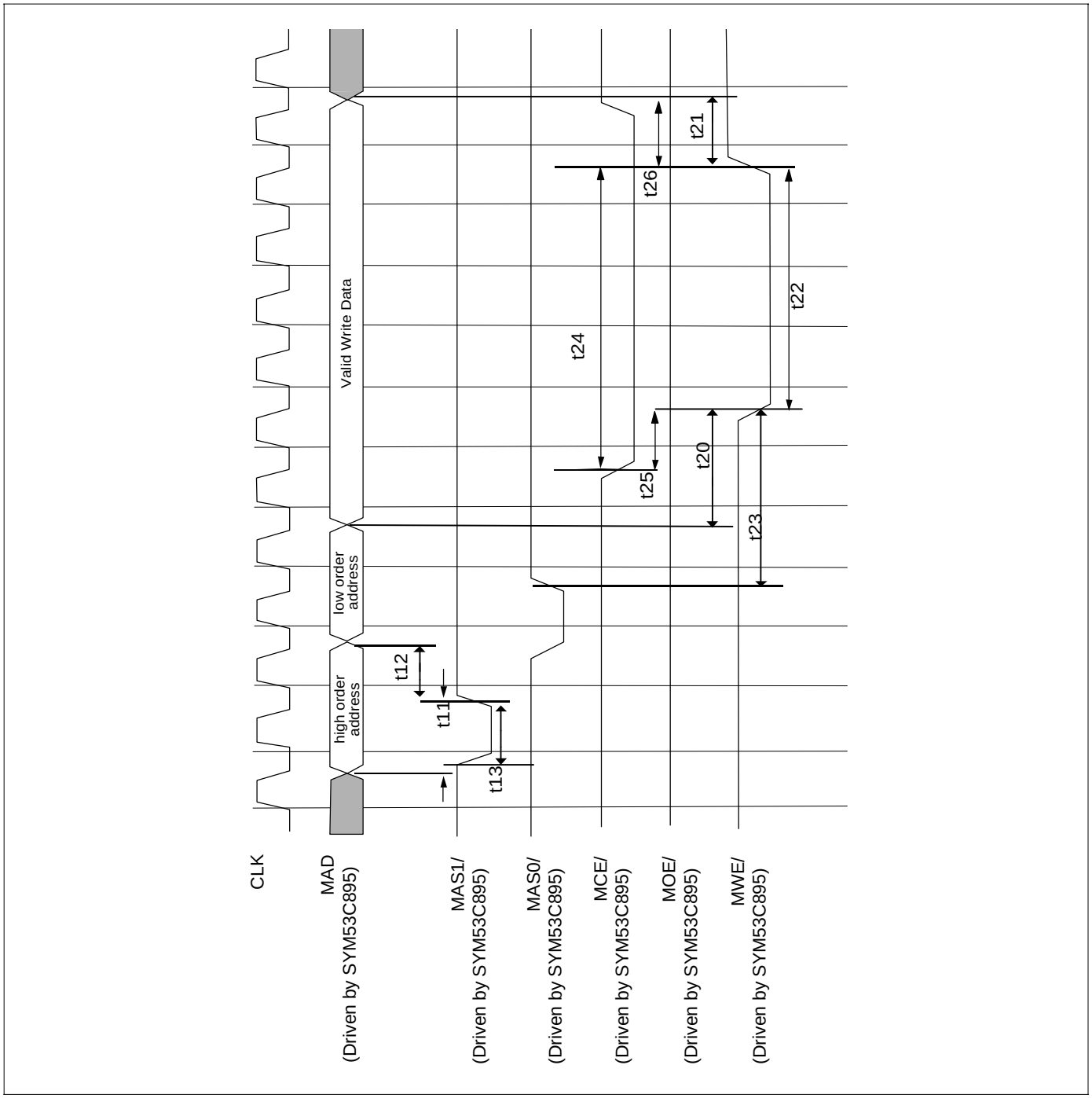


Figure 7-29: Write Cycle, ≤ 64 KB ROM

SCSI Timings

Figure 7-30: Initiator Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	-	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	-	ns
t_3	Data setup to SACK/ asserted	55	-	ns
t_4	Data hold from SREQ/ deasserted	20	-	ns

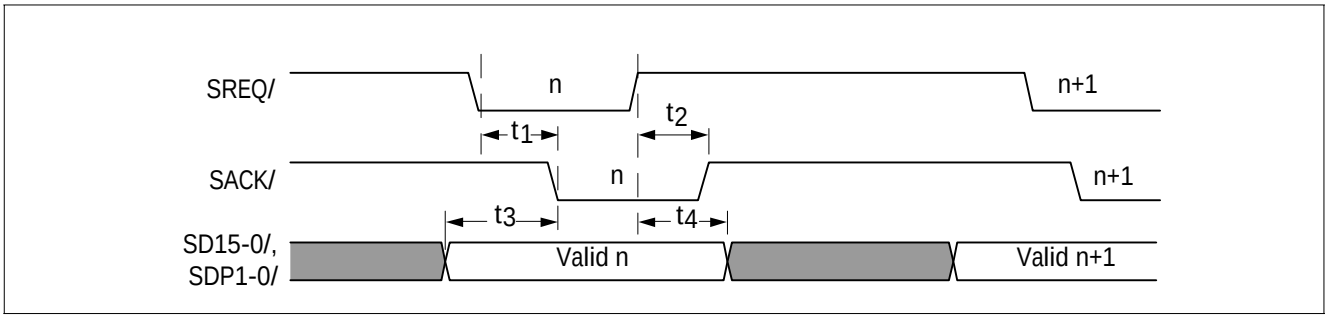


Figure 7-31: Initiator Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SACK/ asserted from SREQ/ asserted	5	-	ns
t_2	SACK/ deasserted from SREQ/ deasserted	5	-	ns
t_3	Data setup to SREQ/ asserted	0	-	ns
t_4	Data hold from SACK/ asserted	0	-	ns

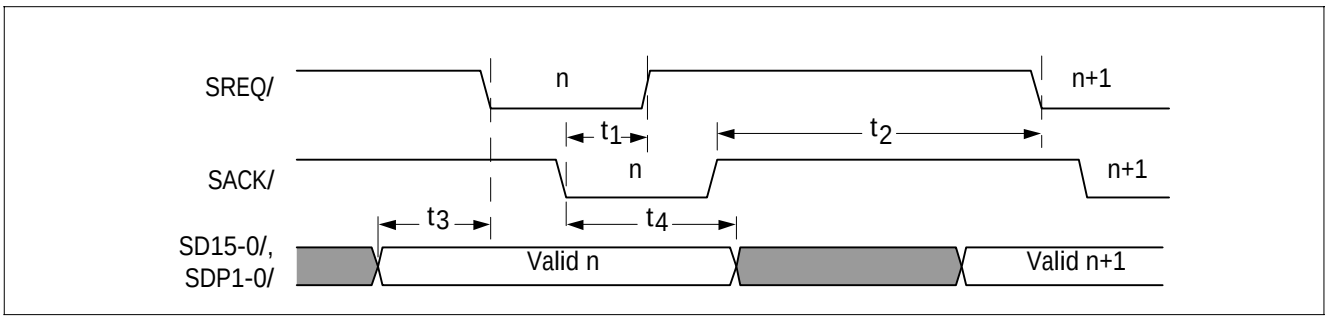


Figure 7-32: Target Asynchronous Send

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	-	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	-	ns
t_3	Data setup to SREQ/ asserted	55	-	ns
t_4	Data hold from SACK/ asserted	20	-	ns

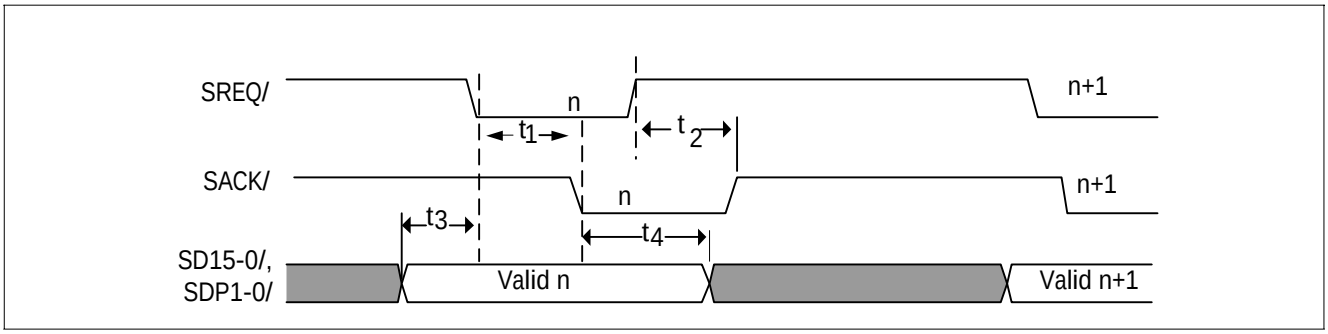
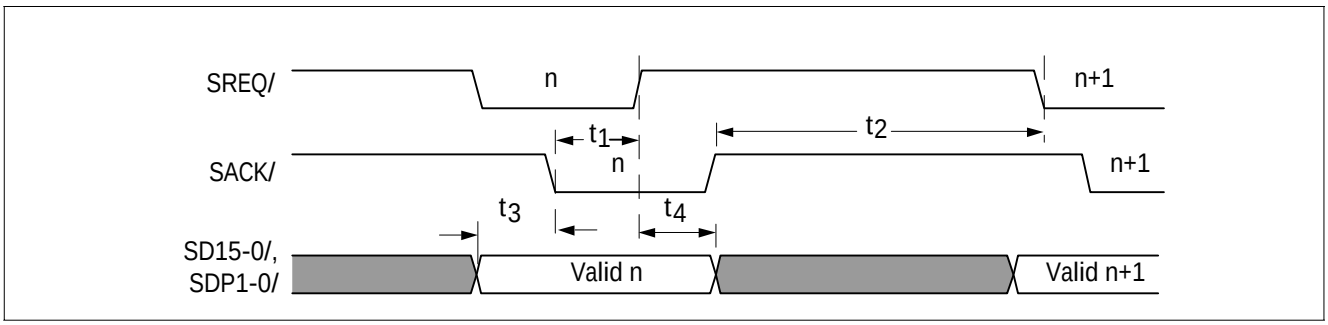


Figure 7-33: Target Asynchronous Receive

Symbol	Parameter	Min	Max	Units
t_1	SREQ/ deasserted from SACK/ asserted	5	-	ns
t_2	SREQ/ asserted from SACK/ deasserted	5	-	ns
t_3	Data setup to SACK/ asserted	0	-	ns
t_4	Data hold from SREQ/ deasserted	0	-	ns



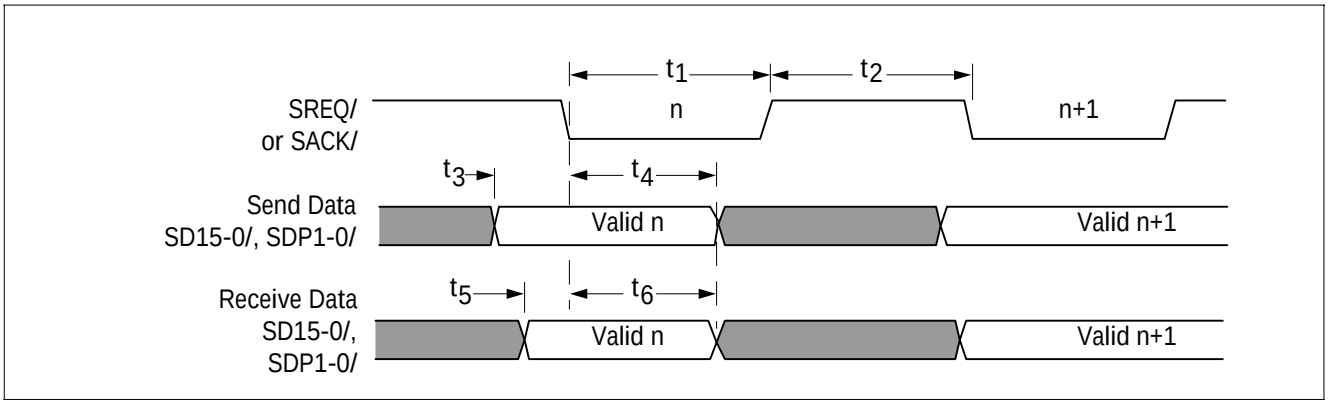


Figure 7-34: Initiator and Target Synchronous Transfers

Table 7-33: SCSI-1 Transfers (Single-Ended, 5.0 MB/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	90	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	90	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	90	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	90	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	55	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	100	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	-	ns

Table 7-34: SCSI-1 Transfers (Differential, 4.17 MB/s)

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	96	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	96	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	84	-	ns
t_2	Receive SREQ/ or SACK/deassertion pulse width	84	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	65	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	110	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	45	-	ns

Table 7-35: SCSI-2 Fast Transfers 10.0 MB/s (8-bit transfers) or 20.0 MB/s (16-bit transfers), 40 MHz clock

Symbol	Parameter	Min	Max	Units
t_1	Send SREQ/ or SACK/ assertion pulse width	35	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	45	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	-	ns

Table 7-36: SCSI-2 Fast Transfers 10.0 MB/s (8-bit transfers) or 20.0 MB/s (16-bit transfers), 50 MHz clock

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	35	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	35	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	20	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	20	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	33	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	40**	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	10	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

***Analysis of system configuration is recommended due to reduced driver skew margin in differential systems*

Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3).

Table 7-37: Ultra SCSI Single-Ended Transfers 20.0 MB/s (8-bit transfers) or 40.0 MB/s (16-bit transfers), quadrupled 40 MHz clock

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	12	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	17	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	7	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

Note: for fast SCSI, set the TolerANT Enable bit (bit 7 in STEST3). During Ultra SCSI transfers, the value of the Extend REQ/ ACK Filtering bit (STEST2, bit 1) has no effect.

Table 7-38: Ultra SCSI High Voltage Differential Transfers 20.0 MB/s (8-bit transfers) or 40.0 MB/s (16-bit transfers), 80 MHz clock

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	16	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	16	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	10	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	10	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	16	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	21	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	0	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	6	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

Note: During Ultra SCSI transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

Table 7-39: Ultra2 SCSI Transfers 40.0 MB/s (8-bit transfers) or 80.0 MB/s (16-bit transfers), quadrupled 40 MHz clock

Symbol	Parameter	Min	Max	Unit
t_1	Send SREQ/ or SACK/ assertion pulse width	8	-	ns
t_2	Send SREQ/ or SACK/ deassertion pulse width	8	-	ns
t_1	Receive SREQ/ or SACK/ assertion pulse width	6	-	ns
t_2	Receive SREQ/ or SACK/ deassertion pulse width	6	-	ns
t_3	Send data setup to SREQ/ or SACK/ asserted	10	-	ns
t_4	Send data hold from SREQ/ or SACK/ asserted	10	-	ns
t_5	Receive data setup to SREQ/ or SACK/ asserted	4.5	-	ns
t_6	Receive data hold from SREQ/ or SACK/ asserted	4.5	-	ns

**Transfer period bits (bits 6-4 in the SXFER register) are set to zero and the Extra Clock Cycle of Data Setup bit (bit 7 in SCNTL1) is set.*

Note: During Ultra2 SCSI transfers, the value of the Extend REQ/ACK Filtering bit (STEST2, bit 1) has no effect.

Appendix A
Register Summary

Register 00 (80)
SCSI Control Zero (SCNTL0)
Read/Write

ARB1	ARB0	START	WATN	EPC	RES	AAP	TRG
7	6	5	4	3	2	1	0
Default>>>							
1	1	0	0	0	X	0	0

Bit 7 **ARB1 (Arbitration Mode bit 1)**
Bit 6 **ARB0 (Arbitration Mode bit 0)**
Bit 5 **START (Start Sequence)**
Bit 4 **WATN (Select with SATN/ on a Start Sequence)**
Bit 3 **EPC (Enable Parity Checking)**
Bit 2 **Reserved**
Bit 1 **AAP (Assert SATN/ on Parity Error)**
Bit 0 **TRG (Target Mode)**

Register 01 (81)
SCSI Control One (SCNTL1)
Read/Write

EXC	ADB	DHP	CON	RST	AESP	IARB	SST
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **EXC (Extra Clock Cycle of Data Setup)**
Bit 6 **ADB (Assert SCSI Data Bus)**
Bit 5 **DHP (Disable Halt on Parity Error or ATN) (Target Only)**
Bit 4 **CON (Connected)**
Bit 3 **RST (Assert SCSI RST/ Signal)**
Bit 2 **AESP (Assert Even SCSI Parity (force bad parity))**
Bit 1 **IARB (Immediate Arbitration)**
Bit 0 **SST (Start SCSI Transfer)**

Register 02 (82)
SCSI Control Two (SCNTL2)
Read/Write

SDU	CHM	SLPMD	SLPHBEN	WSS	VUE0	VUE1	WSR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **SDU (SCSI Disconnect Unexpected)**
Bit 6 **CHM (Chained Mode)**
Bit 5 **SLPMD (SLPAR Mode Bit)**
Bit 4 **SLPHBEN (SLPAR High Byte Enable)**
Bit 3 **WSS (Wide SCSI Send)**
Bit 2 **VUE0 (Vendor Unique Enhancements bit 0)**
Bit 1 **VUE1 (Vendor Unique Enhancements bit 1)**
Bit 0 **WSR (Wide SCSI Receive)**

Register 03 (83)
SCSI Control Three (SCNTL3)
Read/Write

ULTRA	SCF2	SCF1	SCF0	EWS	CCF2	CCF1	CCF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **ULTRA (Ultra Enable)**
Bits 6-4 **SCF2-0 (Synchronous Clock Conversion Factor)**
Bit 3 **EWS (Enable Wide SCSI)**
Bits 2-0 **CCF2-0 (Clock Conversion Factor)**

Register 04 (84)
SCSI Chip ID (SCID)
Read/Write

RES	RRE	SRE	RES	ENC3	ENC2	ENC1	ENC0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	X	0	0	0	0

Bit 7 **Reserved**
Bit 6 **RRE (Enable Response to Reselection)**
Bit 5 **SRE (Enable Response to Selection)**
Bit 4 **Reserved**
Bits 3-0 **Encoded Chip SCSI ID, bits 3-0**

Register 05 (85)
SCSI Transfer (SXFER)
Read/Write

TP2	TP1	TP0	MO4	MO3	MO2	MO1	MO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-5 TP2-0 (SCSI Synchronous Transfer Period)
Bits 4-0 MO4-MO0 (Max SCSI Synchronous Offset)

Register 06 (86)
SCSI Destination ID (SDID)
Read/Write

RES	RES	RES	RES	ENC3	ENC2	ENC1	ENC0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	0	0	0	0

Bits 7-4 Reserved
Bits 3-0 Encoded Destination SCSI ID

Register 07 (87)
General Purpose (GPREG)
Read/Write

RES	RES	RES	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	X	X	X	X

Bits 7-5 Reserved
Bits 4-0 GPIO4-GPIO0 (General Purpose)

Register 08 (88)
SCSI First Byte Received (SFBR)
Read/Write

1B7	1B6	1B5	1B4	1B3	1B2	1B1	1B0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Register 09 (89)
SCSI Output Control Latch (SOCL)
Read /Write

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 REQ(Assert SCSI REQ/ Signal)
Bit 6 ACK(Assert SCSI ACK/ Signal)
Bit 5 BSY(Assert SCSI BSY/ Signal)
Bit 4 SEL(Assert SCSI SEL/ Signal)
Bit 3 ATN(Assert SCSI ATN/ Signal)
Bit 2 MSG(Assert SCSI MSG/ Signal)
Bit 1 C/D(Assert SCSI C_D/ Signal)
Bit 0 I/O(Assert SCSI I_O/ Signal)

Register 0A (8A)
SCSI Selector ID (SSID)
Read Only

VAL	RES	RES	RES	ENID3	ENID2	ENID1	ENID0
7	6	5	4	3	2	1	0
Default>>>							
0	X	X	X	0	0	0	0

Bit 7 VAL (SCSI Valid)
Bits 6-4 Reserved
Bits 3-0 Encoded Destination SCSI ID

Register 0B (8B)
SCSI Bus Control Lines (SBCL)
Read Only

REQ	ACK	BSY	SEL	ATN	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	X	X	X	X	X

Bit 7 REQ (SREQ/ Status)
Bit 6 ACK (SACK/ Status)
Bit 5 BSY (SBSY/ Status)
Bit 4 SEL (SSEL/ Status)
Bit 3 ATN (SATN/ Status)
Bit 2 MSG (SMSG/ Status)
Bit 1 C/D (SC_D/ Status)
Bit 0 I/O (SI_O/ Status)

Register 0C (8C)
DMA Status (DSTAT)
Read Only

DFE	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
1	0	0	0	0	0	X	0

Bit 7 **DFE (DMA FIFO Empty)**
Bit 6 **MDPE (Master Data Parity Error)**
Bit 5 **BF (Bus Fault)**
Bit 4 **ABRT (Aborted)**
Bit 3 **SSI (Single Step Interrupt)**
Bit 2 **SIR (SCRIPTS Interrupt Instruction Received)**
Bit 1 **Reserved**
Bit 0 **IID (Illegal Instruction Detected)**

Register 0D (8D)
SCSI Status Zero (SSTAT0)
Read Only

ILF	ORF	OLF	AIP	LOA	WOA	RST	SDP0/
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **ILF (SIDL Least Significant Byte Full)**
Bit 6 **ORF (SODR Least Significant Byte Full)**
Bit 5 **OLF (SODL Least Significant Byte Full)**
Bit 4 **AIP (Arbitration in Progress)**
Bit 3 **LOA (Lost Arbitration)**
Bit 2 **WOA (Won Arbitration)**
Bit 1 **RST/ (SCSI RST/ Signal)**
Bit 0 **SDP0/ (SCSI SDP0/ Parity Signal)**

Register 0E (8E)
SCSI Status One (SSTAT1)
Read Only

FF3	FF2	FF1	FF0	SDP0L	MSG	C/D	I/O
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	X	X

Bits 7-4 **FF3-FF0 (FIFO Flags)**
Bit 3 **SDP0L (Latched SCSI Parity)**
Bit 2 **MSG (SCSI MSG/ Signal)**
Bit 1 **C/D (SCSI C_D/ Signal)**
Bit 0 **I/O (SCSI I_O/ Signal)**

Register 0F (8F)
SCSI Status Two (SSTAT2)
(Read Only)

ILF1	ORF1	OLF1	FF4	SPL1	DM	LDSC	SDP1
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	X	X	1	X

Bit 7 **ILF1 (SIDL Most Significant Byte Full)**
Bit 6 **ORF1 (SODR Most Significant Byte Full)**
Bit 5 **OLF1 (SODL Most Significant Byte Full)**
Bit 4 **FF4 (FIFO Flags bit 4)**
Bit 3 **SPL1(Latched SCSI parity for SD15-8)**
Bit 2 **DM (DIFFSENS Mismatch)**
Bit 1 **LDSC (Last Disconnect)**
Bit 0 **SDP1 (SCSI SDP1 Signal)**

Registers 10-13 (90-93)
Data Structure Address (DSA)
Read/Write

Register 14 (94)
Interrupt Status (ISTAT)
(Read/Write)

ABRT	SRST	SIGP	SEM	CON	INTF	SIP	DIP
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **ABRT (Abort Operation)**
Bit 6 **SRST (Software Reset)**
Bit 5 **SIGP (Signal Process)**
Bit 4 **SEM (Semaphore)**
Bit 3 **CON (Connected)**
Bit 2 **INTF (Interrupt on the Fly)**
Bit 1 **SIP (SCSI Interrupt Pending)**
Bit 0 **DIP (DMA Interrupt Pending)**

Register 18 (98)
Chip Test Zero (CTEST0)
Read/Write

Register 19 (99)
Chip Test One (CTEST1)
Read Only

FMT3	FMT2	FMT1	FMT0	FFL3	FFL2	FFL1	FFL0
7	6	5	4	3	2	1	0
Default>>>							
1	1	1	1	0	0	0	0

Bits 7-4 FMT3-0 (Byte Empty in DMA FIFO)
Bits 3-0 FFL3-0 (Byte Full in DMA FIFO)

Register 1A (9A)
Chip Test Two (CTEST2)
Read/Write

DDIR	SIGP	CIO	CM	SRTCH	TEOP	DREQ	DACK
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	0	1

Bit 7 DDIR (Data Transfer Direction)
Bit 6 SIGP (Signal Process)
Bit 5 CIO (Configured as I/O)
Bit 4 CM (Configured as Memory)
Bit 3 SRTCH (SCRATCHA/B Operation)
Bit 2 TEOP (SCSI True End of Process)
Bit 1 DREQ (Data Request Status)
Bit 0 DACK (Data Acknowledge Status)

Register 1B (9B)
Chip Test Three (CTEST3)
Read/Write

V3	V2	V1	V0	FLF	CLF	FM	WRIE
7	6	5	4	3	2	1	0
Default>>>							
x	x	x	x	0	0	0	0

Bits 7-4 V3-V0 (Chip revision level)
Bit 3 FLF (Flush DMA FIFO)
Bit 2 CLF (Clear DMA FIFO)
Bit 1 FM (Fetch Pin Mode)
Bit 0 WRIE (Write and Invalidate Enable)

Registers 1C-1F (9C-9F)
Temporary (TEMP)
Read/Write

Register 20 (A0)
DMA FIFO (DFIFO)
Read/Write

BO7	BO6	BO5	BO4	Bo3	BO2	BO1	BO0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bits 7-0 BO7-BO0 (Byte offset counter)

Register 21 (A1)
Chip Test Four (CTEST4)
Read/Write

BDIS	ZMOD	ZSD	SRTM	MPEE	FBL2	FBL1	FBL0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 BDIS (Burst Disable)
Bit 6 ZMOD (High Impedance Mode)
Bit 5 ZSD (SCSI Data High Impedance)
Bit 4 SRTM (Shadow Register Test Mode)
Bit 3 MPEE (Master Parity Error Enable)
Bits 2-0 FBL2-FBL0 (FIFO Byte Control

Register 22 (A2)
Chip Test Five (CTEST5)
Read/Write

ADCK	BBCK	DFS	MASR	DDIR	BL2	BO9	BO8
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	X	X

Bit 7 ADCK (Clock Address Incrementor)
Bit 6 BBCK (Clock Byte Counter)
Bit 5 DFS (DMA FIFO Size)
Bit 4 MASR (Master Control for Set or Reset Pulses)
Bit 3 DDIR (DMA Direction)
Bit 2 BL2 (Burst Length bit 2)
Bits 1-0 BO9-8

Register 23 (A3)
Chip Test Six (CTEST6)
Read/Write

DF7	DF6	DF5	DF4	DF3	DF2	DF1	DF0
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-0 DF7-DF0 (DMA FIFO)

Registers 24-26 (A4-A6)
DMA Byte Counter (DBC)
Read/Write

Register 27 (A7)
DMA Command (DCMD)
Read/Write

Registers 28-2B (A8-AB)
DMA Next Address (DNAD)
Read/Write

Registers 2C-2F (AC-AF)
DMA SCRIPTS Pointer (DSP)
Read/Write

Registers 30-33 (B0-B3)
DMA SCRIPTS Pointer Save (DSPS)
Read/Write

Registers 34-37 (B4-B7)
Scratch Register A (SCRATCH A)
Read/Write

Register 38 (B8)
DMA Mode (DMODE)
Read/Write

BL1	BL0	SIOM	DIOM	ER	ERMP	BOF	MAN
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7-6 **BL1-BL0 (Burst Length)**
Bit 5 **SIOM (Source I/O-Memory Enable)**
Bit 4 **DIOM (Destination I/O-Memory Enable)**
Bit 3 **ERL (Enable Read Line)**
Bit 2 **ERMP (Enable Read Multiple)**
Bit 1 **BOF (Burst Op Code Fetch Enable)**
Bit 0 **MAN (Manual Start Mode)**

Register 39 (B9)
DMA Interrupt Enable (DIEN)
Read/Write

RES	MDPE	BF	ABRT	SSI	SIR	RES	IID
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	X	0

Bit 7 **Reserved**
Bit 6 **MDPE (Master Data Parity Error)**
Bit 5 **BF (Bus Fault)**
Bit 4 **ABRT (Aborted)**
Bit 3 **SSI (Single -step Interrupt)**
Bit 2 **SIR (SCRIPTS Interrupt Instruction Received**
Bit 1 **Reserved**
Bit 0 **IID (Illegal Instruction Detected)**

Register 3A (BA)
Scratch Byte Register (SBR)
Read/Write

Register 3B (BB)
DMA Control (DCNTL)
Read/Write

CLSE	PFF	PFEN	SSM	IRQM	STD	IRQD	COM
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 **CLSE (Cache Line Size Enable)**
Bit 6 **PFF (Pre-fetch Flush)**
Bit 5 **PFEN (Pre-fetch Enable)**
Bit 4 **SSM (Single-step Mode)**
Bit 3 **IRQM (IRQ Mode)**
Bit 2 **STD (Start DMA Operation)**
Bit 1 **IRQD (IRQ Disable)**
Bit 0 **COM (53C700 Compatibility)**

Register 3C-3F (BC-BF)
Adder Sum Output (ADDER)
Read Only

Register 40 (C0)
SCSI Interrupt Enable Zero (SIEN0)
Read/Write

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 M/A (SCSI Phase Mismatch - Initiator Mode; SCSI ATN Condition - Target Mode)
Bit 6 CMP (Function Complete)
Bit 5 SEL (Selected)
Bit 4 RSL (Reselected)
Bit 3 SGE (SCSI Gross Error)
Bit 2 UDC (Unexpected Disconnect)
Bit 1 RST (SCSI Reset Condition)
Bit 0 PAR (SCSI Parity Error)

Register 41 (C1)
SCSI Interrupt Enable One (SIEN1)
Read/Write

RES	RES	RES	SBMC	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	X	0	0	0

Bits 7-5 Reserved
Bit 4 SBMC (SCSI Bus Mode Change)
Bit 3 Reserved
Bit 2 STO (Selection or Reselection Time-out)
Bit 1 GEN (General Purpose Timer Expired)
Bit 0 HTH (Handshake-to-Handshake Timer Expired)

Register 42 (C2)
SCSI Interrupt Status Zero (SIST0)
Read Only

M/A	CMP	SEL	RSL	SGE	UDC	RST	PAR
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 M/A (Initiator Mode: Phase Mismatch; Target Mode: SATN/ Active)
Bit 6 CMP (Function Complete)
Bit 5 SEL (Selected)
Bit 4 RSL (Reselected)
Bit 3 SGE (SCSI Gross Error)
Bit 2 UDC (Unexpected Disconnect)
Bit 1 RST (SCSI RST/ Received)
Bit 0 PAR (Parity Error)

Register 43 (C3)
SCSI Interrupt Status One (SIST1)
Read Only

RES	RES	RES	SBMC	RES	STO	GEN	HTH
7	6	5	4	3	2	1	0
Default>>>							
X	X	X	0	X	0	0	0

Bits 7-5 Reserved
Bit 4 SBMC (SCSI Bus Mode Change)
Bit 3 Reserved
Bit 2 STO (Selection or Reselection Time-out)
Bit 1 GEN (General Purpose Timer Expired)
Bit 0 HTH (Handshake-to-Handshake Timer Expired)

Register 44 (C4)
SCSI Longitudinal Parity (SLPAR)
Read/Write

Register 45 (C5)
SCSI Wide Residue (SWIDE)
Read/Write

Register 46 (C6)
Memory Access Control (MACNTL)
Read/Write

TYP3	TYP2	TYP1	TYP0	DWR	DRD	PSCPT	SCPTS
7	6	5	4	3	2	1	0
Default>>>							
1	1	0	1	0	0	0	0

Bits 7-4 TYP3-0 (Chip Type)
Bit 3 DWR (DataWR)
Bit 2 DRD (DataRD)
Bit 1 PSCPT (Pointer SCRIPTS)
Bit 0 SCPTS (SCRIPTS)

Register 47 (C7)
General Purpose Pin Control (GPCNTL)
Read/Write

ME	FE	RES	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	0	1	1	1	1

Bit 7 Master Enable
Bit 6 Fetch Enable
Bit 5 Reserved
Bits 4-2 GPIO4_EN–GPIO2_EN (GPIO Enable)
Bits 1-0 GPIO1_EN– GPIO0_EN (GPIO Enable)

Register 48 (C8)
SCSI Timer Zero (STIME0)
Read /Write

HTH	HTH	HTH	HRH	SEL	SEL	SEL	SEL
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bits 7-4 HTH (Handshake-to-Handshake Timer Period)
Bits 3-0 SEL (Selection Time-Out)

Register 49 (C9)
SCSI Timer One (STIME1)
Read/Write

RES	HTHBA	GENSF	HTHSF	GEN3	GEN2	GEN1	GEN0
7	6	5	4	3	2	1	0
Default>>>							
X	0	0	0	0	0	0	0

Bit 7 Reserved
Bit 6 HTHBA (Handshake-to-Handshake Timer Bus Activity Enable)
Bit 5 GENSF (General Purpose Timer Scale Factor)
Bit 4 HTHSF (Handshake to Handshake Timer Scale Factor)
Bits 3-0 GEN3-0 (General Purpose Timer Period)

Register 4A (CA)
Response ID Zero (RESPID0)
Read/Write

Register 4B (CB)
Response ID One(RESPID1)
Read/Write

.

Register 4C (CC)
SCSI Test Zero (STEST0)
Read Only

SSAID3	SSAID2	SSAID1	SSAID0	SLT	ART	SOZ	SOM
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	X	1	1

Bits 7-4 SSAID (SCSI Selected As ID)
Bit 3 SLT (Selection Response Logic Test)
Bit 2 ART (Arbitration Priority Encoder Test)
Bit 1 SOZ (SCSI Synchronous Offset Zero)
Bit 0 SOM (SCSI Synchronous Offset Maximum)

Register 4D (CD)
SCSI Test One (STEST1)
Read/Write

SCLK	SISO	RES	RES	QEN	QSEL	RES	RES
7	6	5	4	3	2	1	0
Default>>>							
0	0	X	X	0	0	X	X

Bit 7 SCLK
Bit 6 SISO (SCSI Isolation Mode)
Bits 5-4 Reserved
Bit 3 QEN (SCLK Quadrupler Enable)
Bit 2 QSEL (SCLK Quadrupler Select)
Bits1-0 Reserved

Register 4E (CE)
SCSI Test Two (STEST2)
Read/Write

SCE	ROF	DIF	SLB	SZM	AWS	EXT	LOW
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 SCE (SCSI Control Enable)
Bit 6 ROF (Reset SCSI Offset)
Bit 5 DIF (SCSI Differential Mode)
Bit 4 SLB (SCSI Loopback Mode)
Bit 3 SZM (SCSI High-Impedance Mode)
Bit 2 AWS (Always Wide SCSI)
Bit 1 EXT (Extend SREQ/SACK Filtering)
Bit 0 LOW (SCSI Low level Mode)

Register 4F (CF)
SCSI Test Three (STEST3)
Read/Write

TE	STR	HSC	DSI	S16	TTM	CSF	STW
7	6	5	4	3	2	1	0
Default>>>							
0	0	0	0	0	0	0	0

Bit 7 TE (TolerANT Enable)
Bit 6 STR (SCSI FIFO Test Read)
Bit 5 HSC (Halt SCSI Clock)
Bit 4 DSI (Disable Single Initiator Response)
Bit 3 S16 (16-bit System)
Bit 2 TTM (Timer Test Mode)
Bit 1 CSF (Clear SCSI FIFO)
Bit 0 STW (SCSI FIFO Test Write)

Register 50-51 (D0-D1)
SCSI Input Data Latch (SIDL)
Read Only

Register 52 (D2)
SCSI Test 4 (STEST4)
Read Only

SMODE		LOCK	RES	RES	RES	RES	RES
7	6	5	4	3	2	1	0
Default>>>							
X	X	0	X	X	X	X	X

Bit 7-6 SMODE (SCSI Mode)
Bit 5 LOCK (Frequency Lock)
Bits 4-0 Reserved

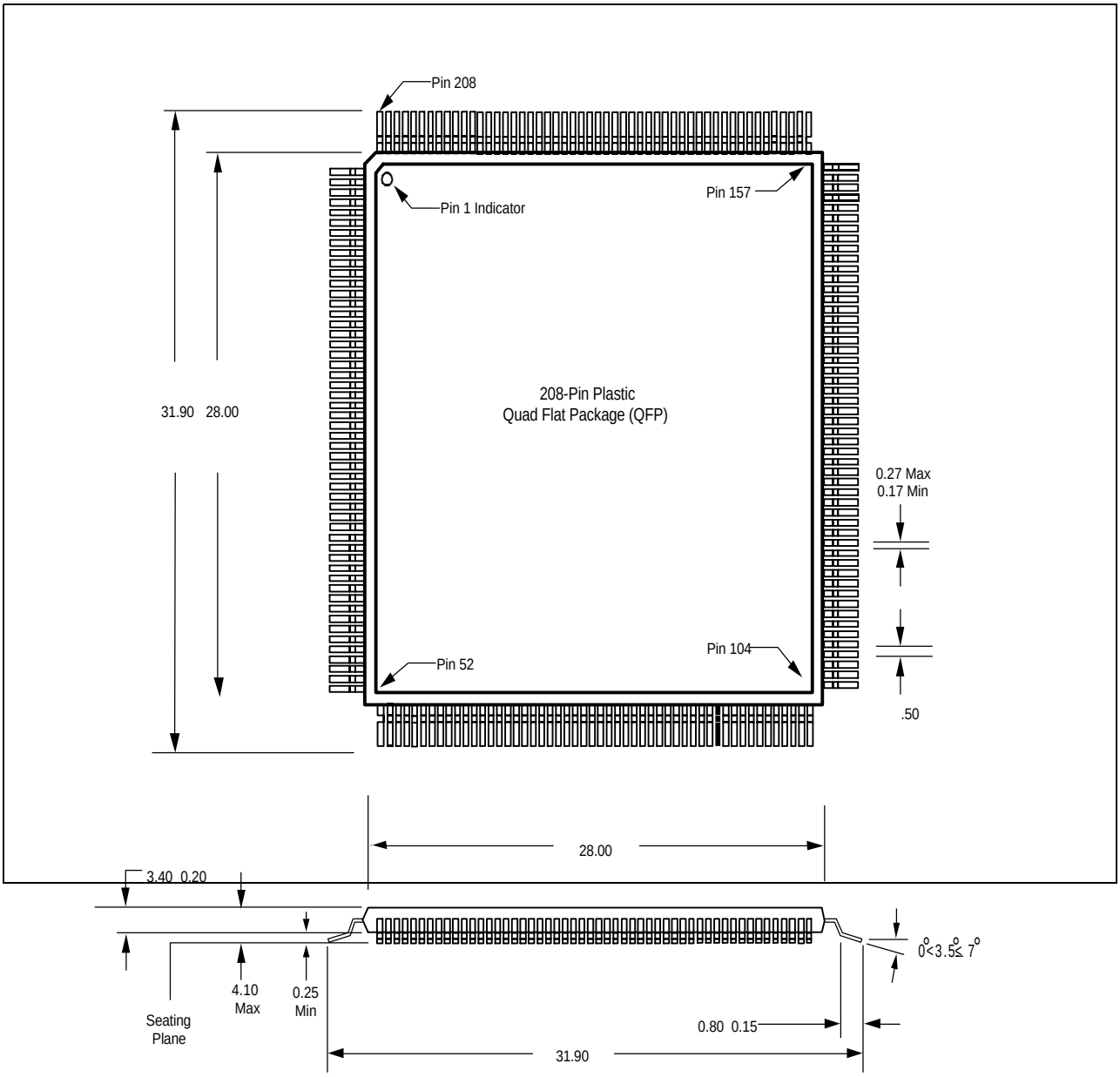
Registers 54-55 (D4-D5)
SCSI Output Data Latch (SODL)
Read/Write

Registers 58-59 (D8-D9)
SCSI Bus Data Lines (SBDL)
Read Only

Registers 5C-5F (DC-DF)
Scratch Register B (SCRATCHB)
(Read/Write)

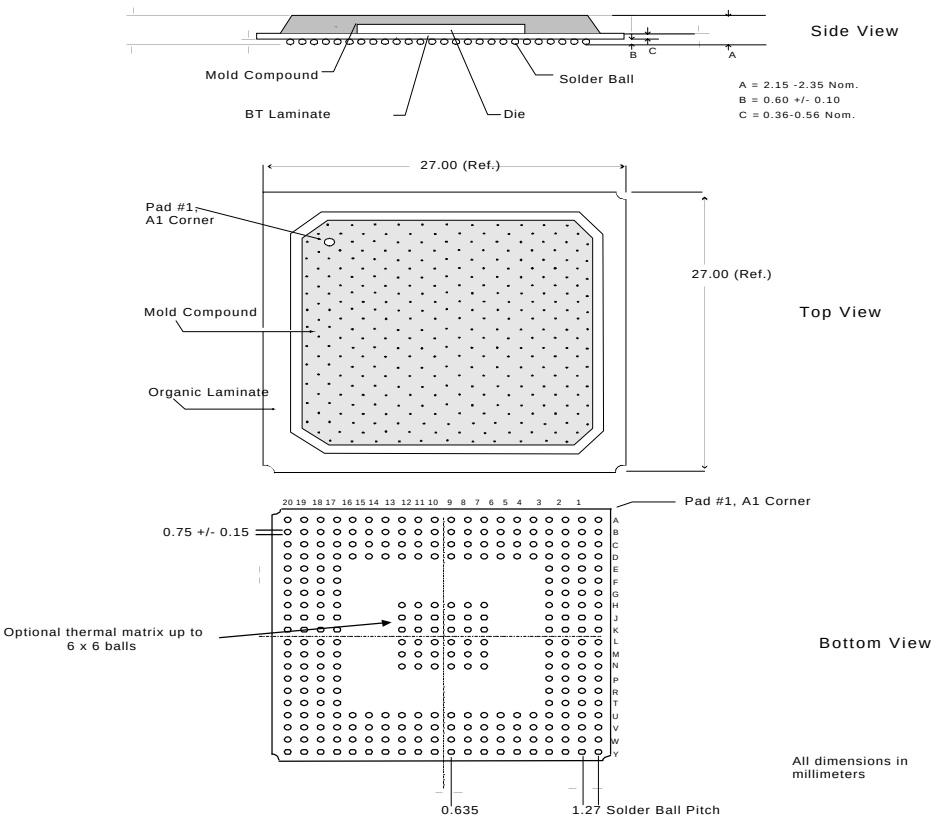
Registers 60h-7Fh (E0h-FFh)
Scratch Registers C-J
(SCRATCHC-SCRATCHJ)
Read/Write

Appendix B
Mechanical Drawing



All dimensions in millimeters

Figure B-1: SYM53C895 Mechanical Drawing, 208-pin QFP



All dimensions in millimeters

Figure B-2:SYM53C895 Mechanical Drawing, 292-ball BGA

Appendix C
External Memory Interface Diagram Examples

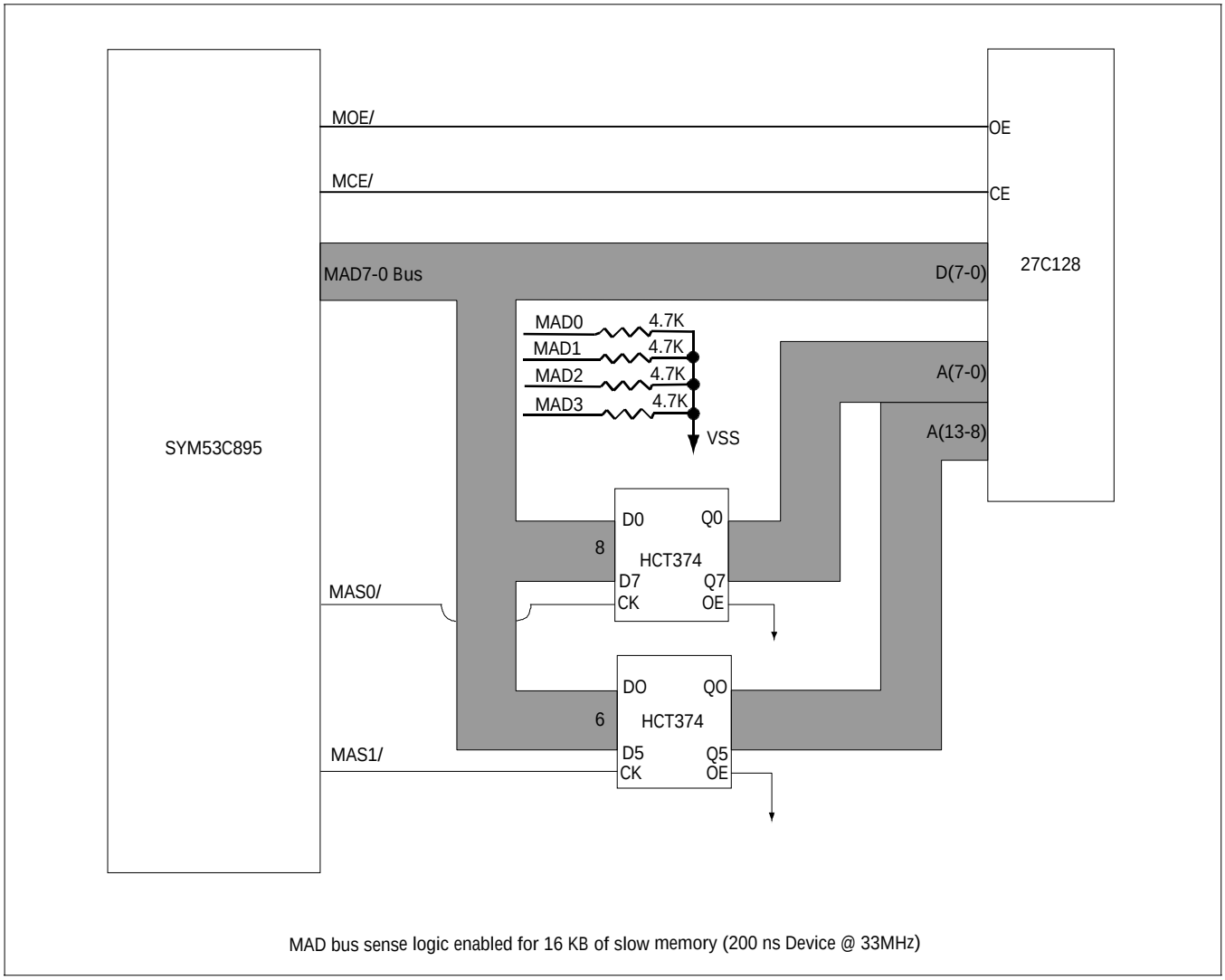


Figure C-1:16 K Interface With 200 ns Memory

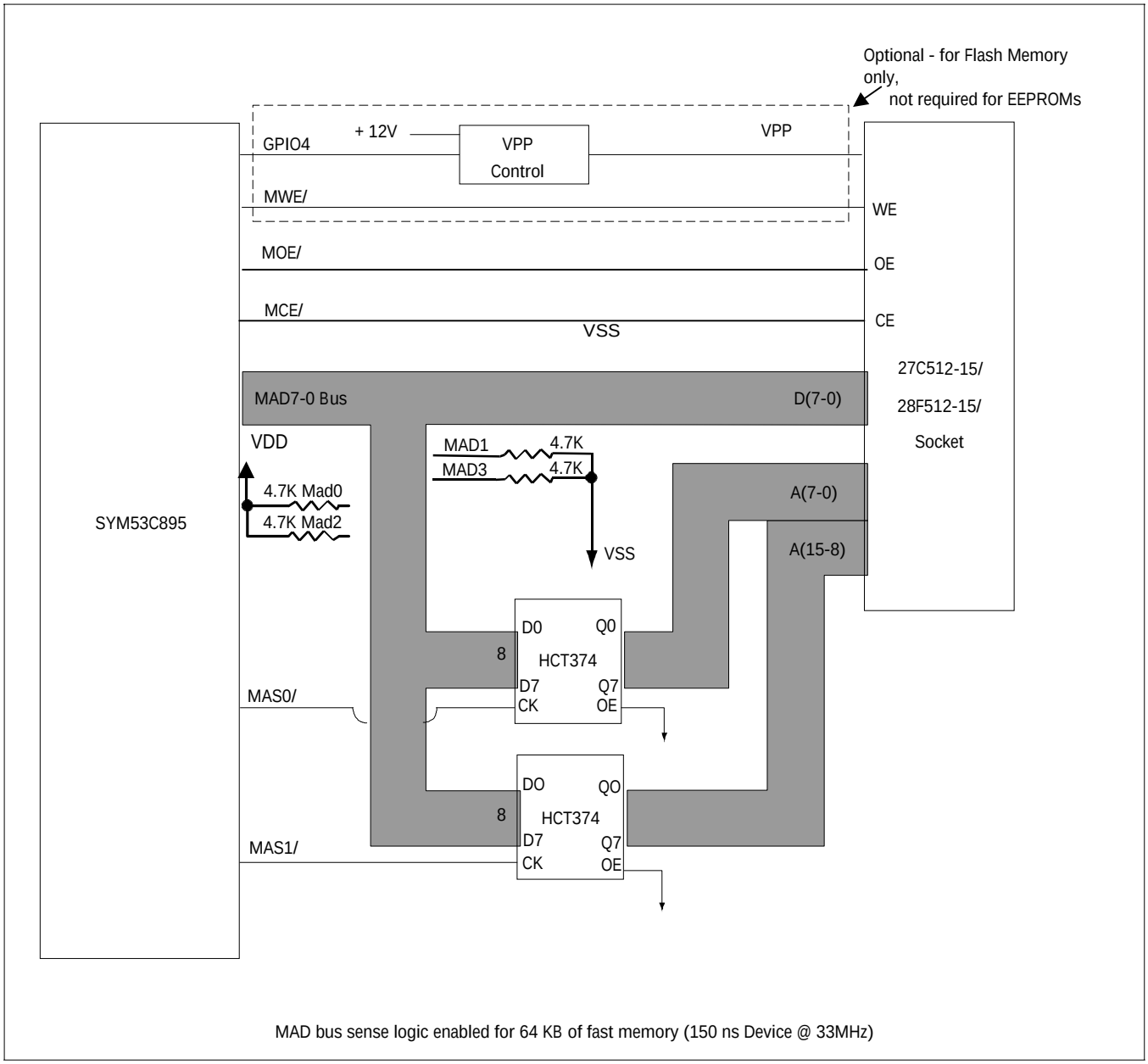


Figure C-2:64 K Interface with 150 ns Memory

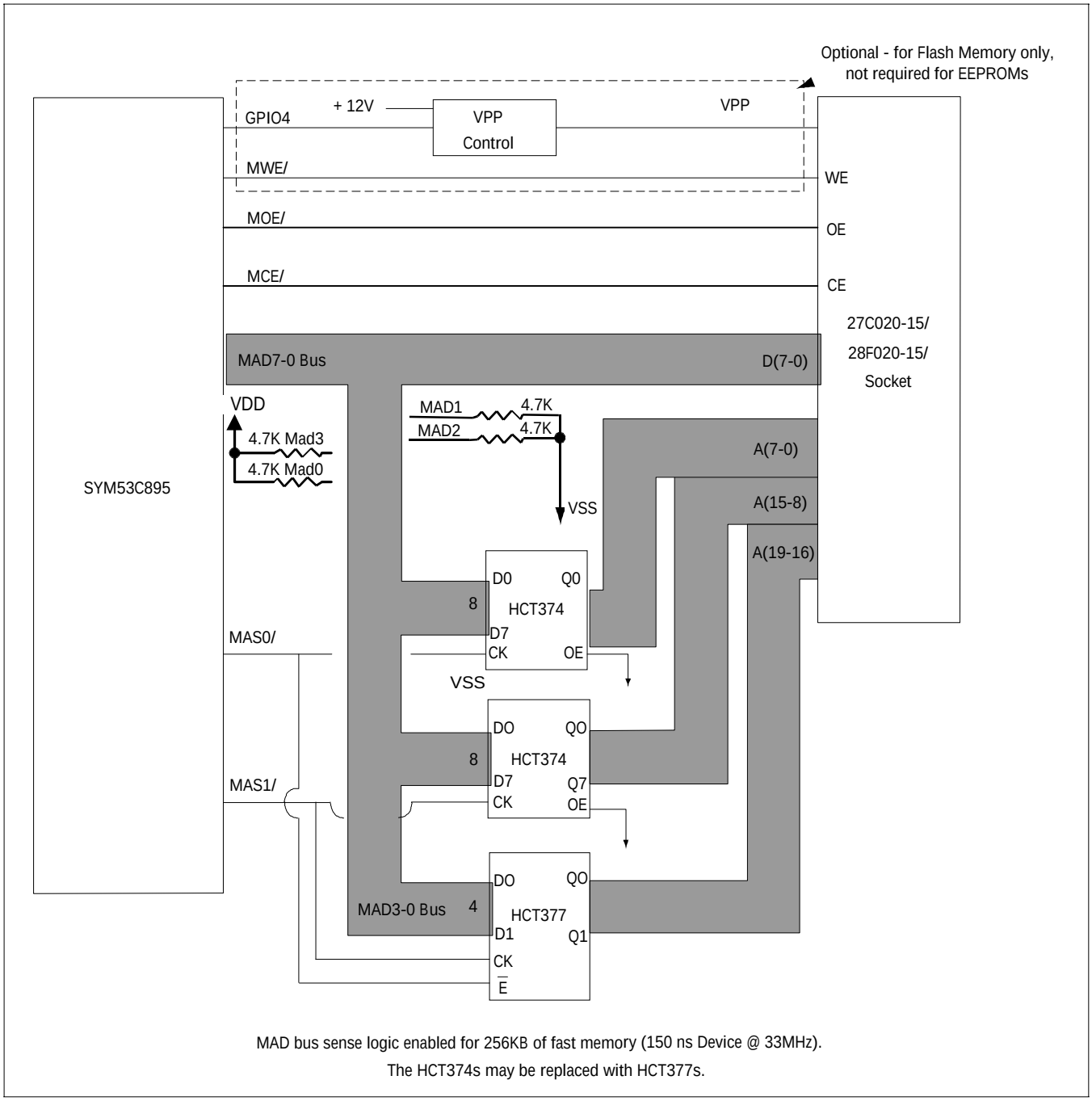


Figure C-3:256 K Interface With 150 ns Memory

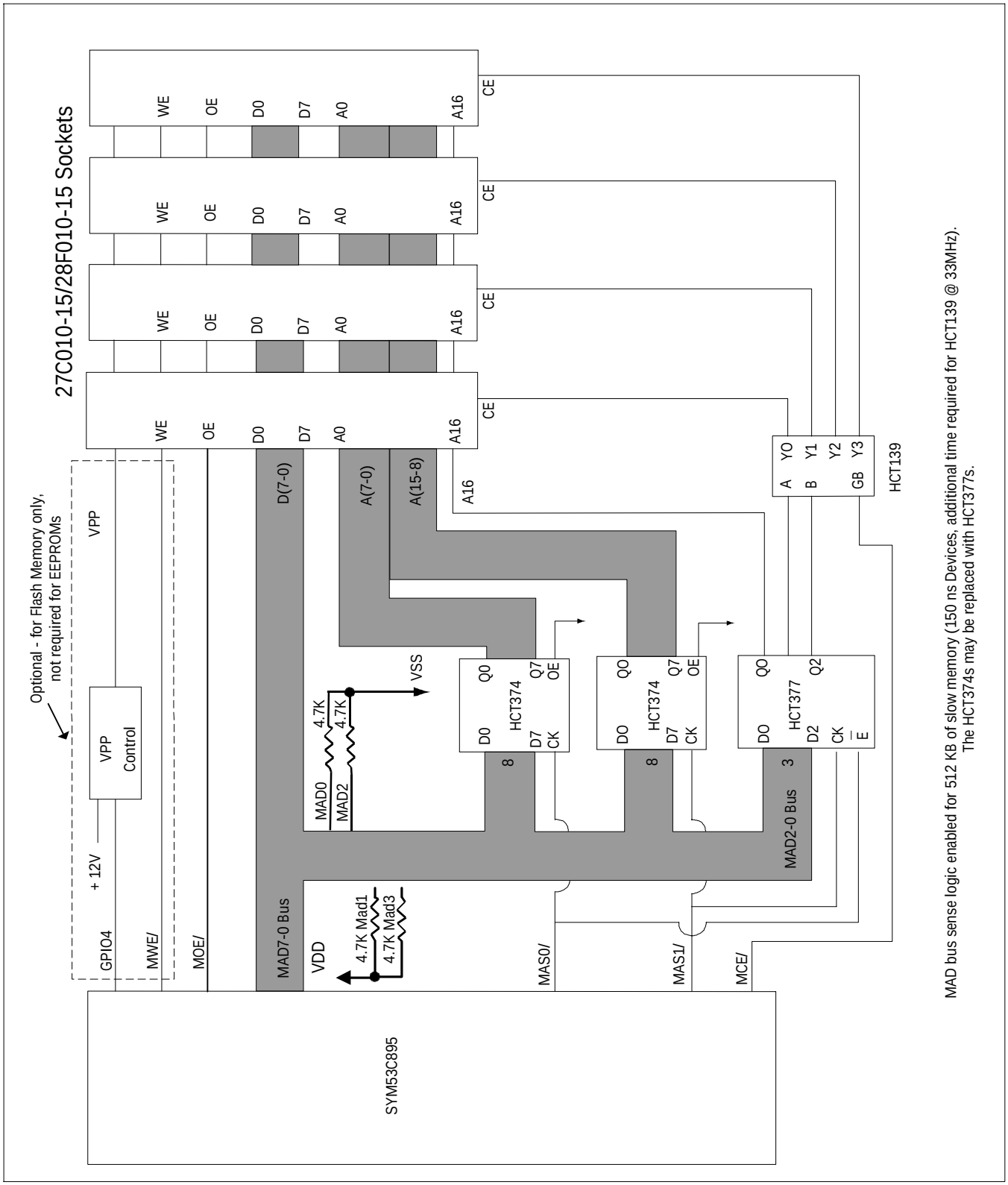


Figure C-4:512 K Interface With 150 ns Memory

Appendix D

Circuit Board Layout Issues

Higher data transfer rates, such as Ultra2 SCSI, make good printed circuit board (PCB) layout practices more critical than ever. Some of the layout design criteria that need to be considered are separation of LVD and TTL/CMOS signals, routing of the differential pairs, trace impedance, stub lengths, decoupling power supplies and the dielectric constant of the board material. When certain PCB layout guidelines are not followed, various signal degradation effects can result. Reflections are caused by impedance mismatches. Cross-talk, dielectric loss, skin effects, dispersion loss and reduction of noise margin are some other unwanted by-products of poor PCB layout practices.

Note: This information was originally published in Symbios System Engineering Notes 893 (PCB Layout for SYM53C895) and 898 (Analog Power Filtering for SYM53C895).

Signal Separation

Avoid crosstalk problems by providing a good separation between LVD and TTL/CMOS signals. Crosstalk is proportional to dv/dt. TTL/CMOS signals have larger voltage swings than LVD and can effect them if lines are running in close proximity. The best means of separation is to provide a ground trace between the two types of signals. Another means of keeping the two kinds of signals apart is to place them on separate layers. If LVD and TTL/CMOS signals need to be on the same layer, they should be separated by as much distance as possible.

Routing Signal Lines

Routing of differential lines is an important factor in maintaining signal integrity. Differentially paired traces must be kept equidistant. Each line should be kept as parallel as possible to its counterpart. To avoid skew issues, the two lines should be exactly the same in length. Abiding by these rules ensures that the rejection of common mode noise, inherent to differentially paired signals, remains intact. Another consideration in laying out these traces is to avoid sharp orthogonal turns. his type of turn needs to be angled to avoid sharp changes in impedance.

Impedance Matching

Trace impedance should match the impedance of the media as close as possible to avoid signal reflections. A typical differential impedance for the cable is about 120 Ohms. The impedance of a trace on the PCB is controlled by its height and width, as well as the thickness of the dielectric. The impedance of a trace pair is controlled by the distance between the two traces.

Termination and Stub Length

The impedance of the terminator should match that of the cable. Terminators need to be placed at the far ends of the cable and as close to the receiver inputs as possible. Stub lengths of any device placed along the bus need to be kept short to avoid impedance mismatches that result in reflections. The Ultra2 SCSI standard stipulates that stub lengths for LVD busses should not exceed 0.1m.

Additionally differences in stub lengths between REQ, ACK, DATA and PARITY signals shall not exceed 1.27cm.

Decoupling

Decoupling caps need to be as close to the chip Vdd pins as possible. The main power supply line should also be decoupled. SMT parts are preferred. The long lead lengths of axial leaded parts add inductance to the line.

Dielectric

Another design criteria that should be considered is that the dielectric constant of the board material should be as low as possible. Teflon has a dielectric constant rating twice as low as FR-4 which is a common material used in PCBs and so has lower losses. The disadvantage of Teflon is that it is more expensive.

Considerations Specific to the SYM53C895

RBIAS +/- Pins

The RBIAS +/- pins, 130 and 129, need to have a 2.2 KOhm resistor between them to provide the correct bias current to the LVD pads. Additionally +3.3V needs to be connected to RBIAS-, pin 129.

- SCSI lines should be short, with no Ts and all of them are about the same length.
- All PCI lines need to be less than 1.5 inches long.
- All GND's and PWR traces need to be short, wide and doubled.

Physical Dimensions

The SYM53C895 is packaged in a 28 X 28 mm plastic quad flat package (PQFP). The total space required is 31.9 X 31.9 mm including pins. Refer to the mechanical drawing in the data manual for other specific dimensions.

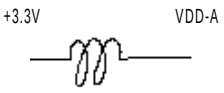
Power Requirements

A 3.3V regulator (LT1086) is used to derive the V_{DD} supply voltage.

V_{DD-A} Pin

The V_{DD-A} pin (pin 85 or H19) on the SYM53C895 SCSI I/O processor (SIOP) provides power to the phase locked loop (PLL) and is sensitive to noise. Board configurations that expose V_{DD-A} to noise above 90 mV at frequencies above 120 MHz are susceptible. External AC filtering is required to prevent high frequency noise from reaching the PLL. Neglecting to incorporate this filter may result in unpredictable SCSI bus behavior. This is particularly problematic during SCSI DATA OUT and DATA IN phases at Ultra2 speeds.

Analog power noise will affect the ability of the SIOP to accurately clock REQ/ and ACK/ signals. As a result, the SIOP may double clock an incoming REQ/ signal or generate an extra ACK/ signal. This miscounting will manifest itself as a data underrun or a data overrun. A ferrite bead is required to perform this filtering. The bead should be placed in series between V_{DD-A} and the 3.3V power supply as follows:



The bead should provide between 50W and 90W impedance above 120 MHz and should be rated to handle currents up to 25 mA. No de-coupling capacitor is needed in this configuration.

Terminators

Unitrode terminators (UCC5630) are recommended. They provide both LVD and single-ended termination, depending on what mode of operation is detected by the DIFFSENS pin. All GND's to the terminators should be short, wide and doubled. REG is tied to ground through five 1uF caps.

Capacitive Load

The total capacitance budget dictated by the SCSI Parallel Interconnect - 2 (SPI-2) standard is presently 25pF. The SYM53C895 is about 13pF. A high density (68 pin) connector is about 3pF. That leaves a budget of about 10pF for traces. Calculations show that the trace lengths should be held to about 4 inches maximum under these conditions. Further calculations to determine allowable deltas in trace length between different signals show that +/- 1.46 inches is the maximum. This will accommodate less than 200ps of skew between signals.

SPI-2 Document

Refer to the SCSI Parallel Interconnect 2 (SPI-2) standard on Ultra2 SCSI for specific definitions of LVD technology as it pertains to SCSI. It also talks about requirements for Ultra2 SCSI data rates, VHDCI connectors, SCA-2 connectors, DIFFSENS and TERMPWR signals. The spec, which is up to revision 11, can be found on the World Wide Web at:

ftp.symbios.com/pub/standards/io/x3t10/drafts/spi2

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