M58BW032BT, M58BW032BB
M58BW032DT, M58BW032DB

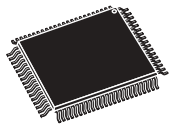
32 Mbit (1Mb x32, Boot Block, Burst) 3.3V Supply Flash Memory

PRELIMINARY DATA

FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{DD} = 3.0V to 3.6V for Program, Erase and Read
  - V_{DDQ} = V_{DDQIN} = 1.6V to 3.6V for I/O Buffers
- HIGH PERFORMANCE
  - Access Time: 45, 55 and 60ns
  - 75MHz Effective Zero Wait-State Burst Read
  - Synchronous Burst Reads
  - Asynchronous Page Reads
- MEMORY ORGANIZATION
  - Eight 64 Kbit small parameter Blocks
  - Four 128Kbit large parameter Blocks (of which one is OTP)
  - Sixty-two 512Kbit main Blocks
- HARDWARE BLOCK PROTECTION
  - $\overline{WP}$ pin Lock Program and Erase
  - V_{PEN} signal for Program/Erase Enable
- SOFTWARE BLOCK PROTECTION
  - Tuning Protection to Lock Program and Erase with 64-bit User Programmable Password (M58BW032B version only)
- SECURITY
  - 64-bit Unique Device Identifier (UID)
- FAST PROGRAMMING
  - Write to Buffer and Program capability
- OPTIMIZED FOR FDI DRIVERS
  - Common Flash Interface (CFI)
  - Fast Program/Erase Suspend feature in each block
- LOW POWER CONSUMPTION
  - 100µA Typical Standby

Figure 1. Packages



PQFP80 (T)

LBGA80 (ZA)
10 x 8 ball array

- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code M58BW032xT: 8838h
  - Bottom Device Code M58BW032xB: 8837h
- OPERATING TEMPERATURE RANGE
  - Automotive (Grade 3): –40 to 125°C
  - Industrial (Grade 6): –40 to 90°C

SUMMARY DESCRIPTION

The M58BW032B/D is a 32Mbit non-volatile Flash memory that can be erased electrically at the block level and programmed in-system on a Double-Word basis using a 3.0V to 3.6V V_{DD} supply for the circuit and a V_{DDQ} supply down to 1.6V for the Input and Output buffers.

The devices support Asynchronous (Latch Controlled and Page Read) and Synchronous Bus operations. The Synchronous Burst Read Interface allows a high data transfer rate controlled by the Burst Clock, K, signal. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length are configurable and can be easily adapted to a large variety of system clock frequencies and microprocessors. All Writes are Asynchronous. On power-up the memory defaults to Read mode with an Asynchronous Bus.

The device features an asymmetrical block architecture. The M58BW032B/D has an array of 62 main blocks of 512 Kbits each, plus 4 large parameter blocks of 128Kbits each and 8 small parameter blocks of 64 Kbits each. The large and small parameter blocks are located either at the top (M58BW032BT, M58BW032DT) or at the bottom (M58BW032BB, M58BW032DB) of the address space. The first large parameter block is referred to as Boot Block and can be used either to store a boot code or parameters.

Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up. The M58BW032B features four different levels of hardware and software block protection to avoid unwanted program/erase operations:

- Write/Protect Enable input, $\overline{WP}$, provides a hardware protection of a combination of blocks from program or erase operations. The Block Protection configuration can be defined individually by issuing a Set Block Protection Configuration Register or Clear Block Protection Configuration Register commands.
- All Program or Erase operations are blocked when Reset, $\overline{RP}$, is held low.
- A Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.
- The Program and Erase commands can be password protected by the Tuning Protection command.

The M58BW032D offers the same protection features with the exception of the Tuning Block Protection which is disabled in the factory.

A Reset/Power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is reduced to the standby level, the device is write protected and both the Status and Burst Configuration Registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

A manufacturer and device code are available. They can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory.

Finally, the M58BW032B/D features a Unique Device Identifier (UID) which is programmed by ST. It is unique for each die and can be used to implement cryptographic algorithms to improve security.

The memory is offered in PQFP80 (14 x 20mm) and LBGA80 (1.0mm pitch) packages and it is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

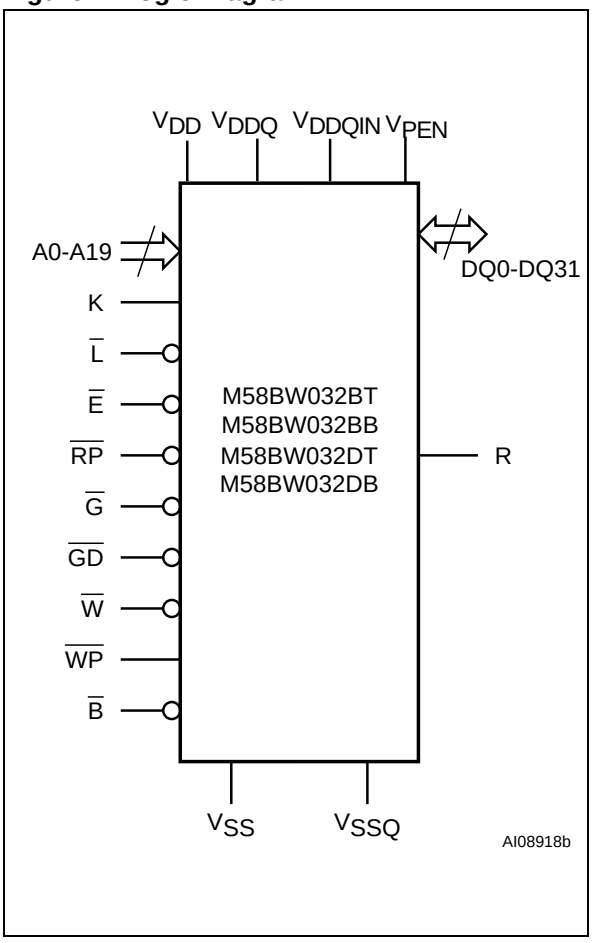


Table 1. Signal Names

A0-A19	Address inputs
DQ0-DQ7	Data Input/Output, Command Input
DQ8-DQ15	Data Input/Output, Burst Configuration Register
DQ16-DQ31	Data Input/Output
$\overline{B}$	Burst Address Advance
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
K	Burst Clock
$\overline{L}$	Latch Enable
R	Valid Data Ready
$\overline{RP}$	Reset /Power-Down
$\overline{W}$	Write Enable
$\overline{GD}$	Output Disable
$\overline{WP}$	Write Protect
V_{DD}	Supply Voltage
V_{DDQ}	Power Supply for Output Buffers
V_{DDQIN}	Power Supply for Input Buffers only
V_{PEN}	Program/Erase Enable
V_{SS}	Ground
V_{SSQ}	Input/Output Ground
NC	Not Connected Internally
DU	Don’t Use as Internally Connected

Figure 3. LBGA Connections (Top view through package)

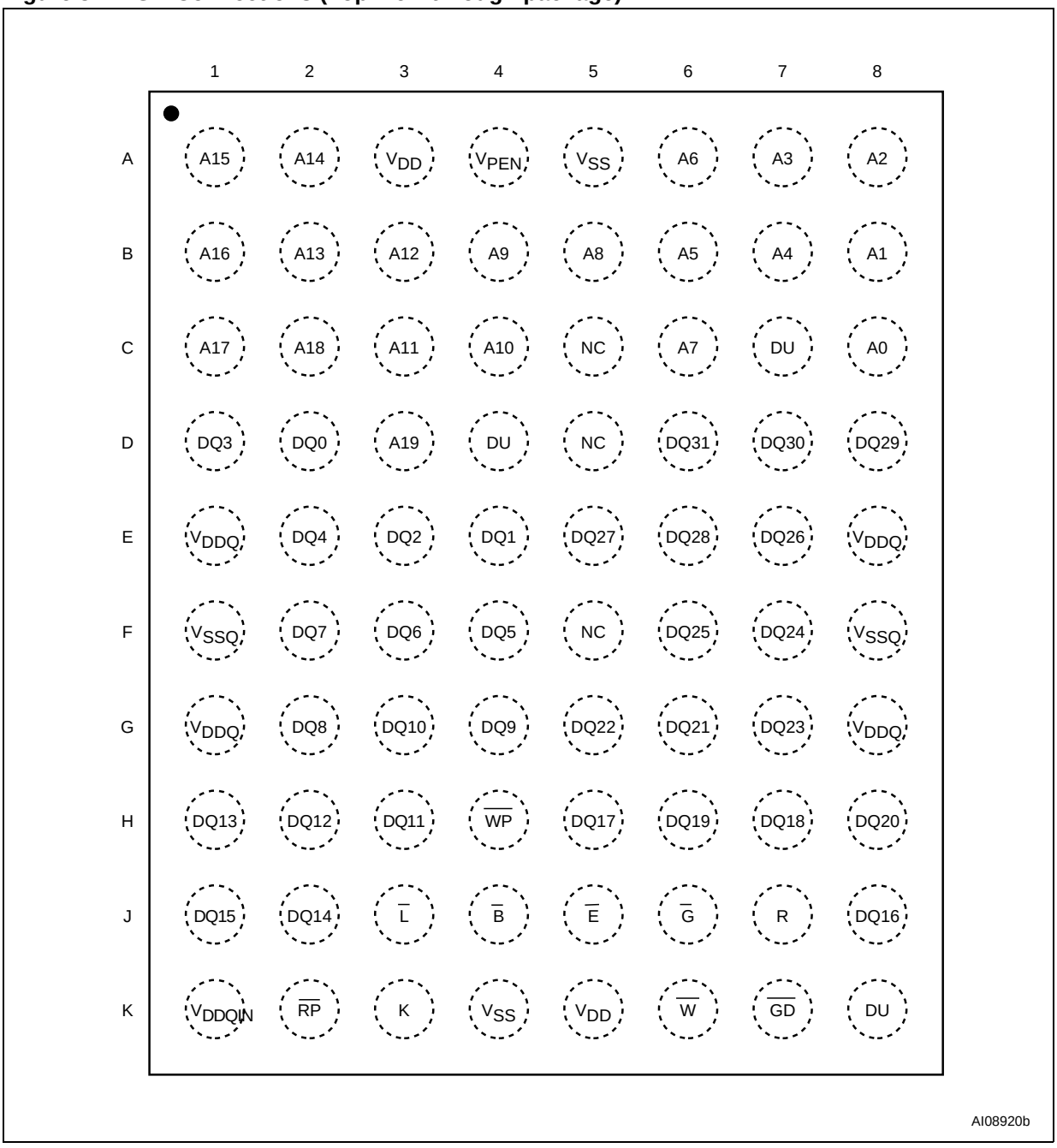
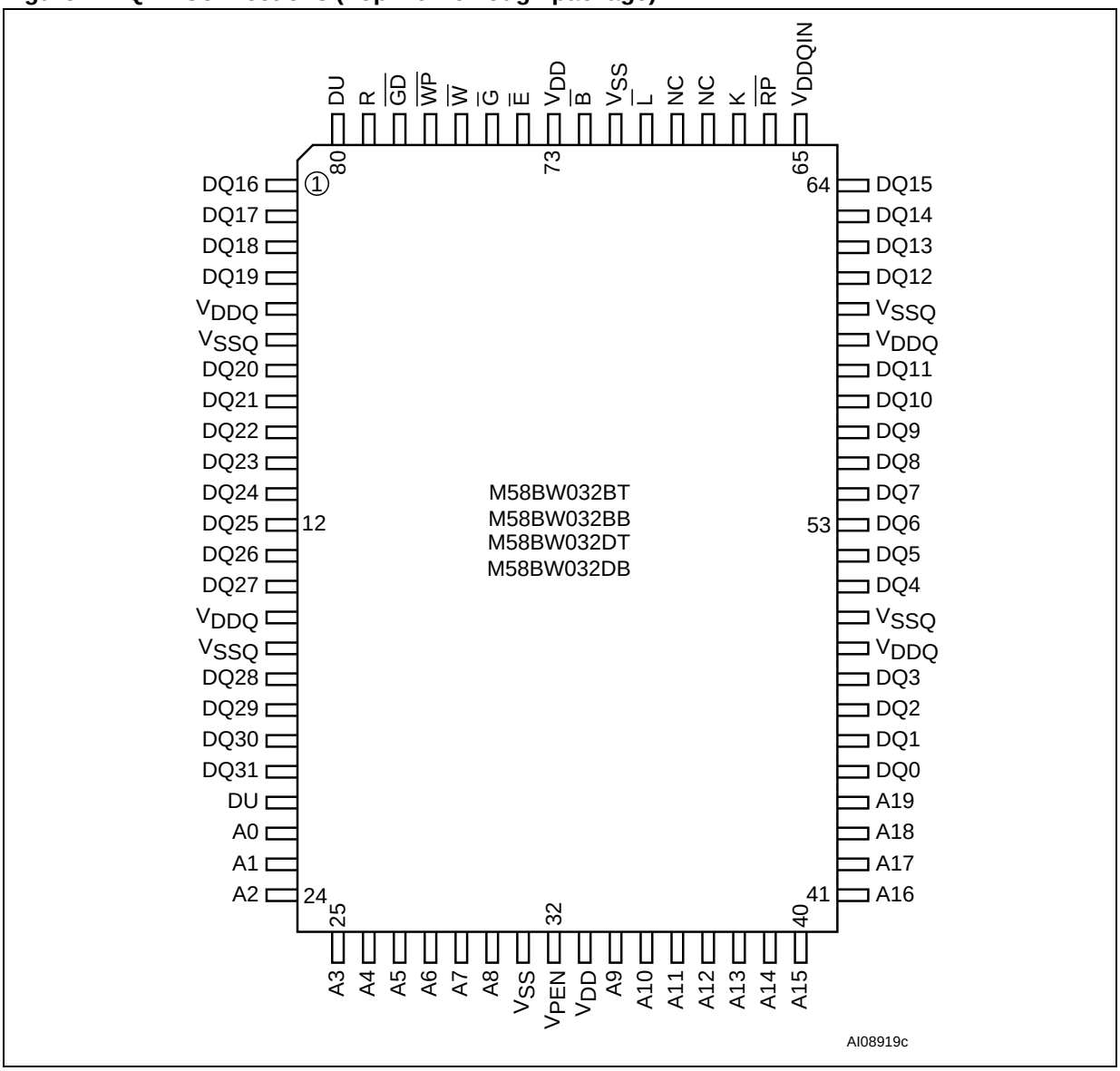


Figure 4. PQFP Connections (Top view through package)



Block Protection

The M58BW032B features four different levels of block protection. The M58BW032D has the same block protection with the exception of the Tuning Block Protection, which is disabled in the factory.

- **Write Protect Pin, WP, -** When WP is Low, V_{IL}, the protection status that has been configured in the Block Protection Configuration Register is activated. The Block Protection Configuration Register is volatile. Any combination of blocks is possible. Any attempt to program or erase a protected block will be ignored and will return an error in the Status Register.
- **Reset/Power-Down Pin, RP, -** If the device is held in reset mode (RP at V_{IL}), no program or erase operations can be performed on any block.
- **Program/Erase Enable, V_{PEN}, -** V_{PEN} protects all blocks preventing Program and Erase operations from affecting their data. Program/Erase Enable must be kept High (V_{IH}) during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.
- **Tuning Block Protection** - M58BW032B features a 64 bit password protection for program and erase operations for a fixed number of blocks After power-up or reset the device is tuning protected. An Unlock command is provided to allow program or erase operations in all the blocks.

After a device reset the first two kinds of block protection (WP, RP) can be combined to give a flexible block protection. They do not affect the Tuning Block Protection. When the two protections are disabled, WP and RP at V_{IH}, the blocks locked by the Tuning Block Protection cannot be modified. All blocks are protected at power-up.

Tuning Block Protection

The Tuning Block Protection is a software feature to protect blocks from program or erase operations. It allows the user to lock program and erase operations with a user definable 64 bit code. It is only available on the M58BW032B version.

The code is written once in the Tuning Protection Register and cannot be erased. When shipped the flash memory will have the Tuning Protection Code bits set to ‘1'. The user can program a ‘0’ in any of the 64 positions. Once programmed it is not possible to reset a bit to ‘1’ as the cells cannot be erased. The Tuning Protection Register can be programmed at any moment (after providing the correct code), however once all bits are set to ‘0’ the Tuning Protection Code can no longer be altered.

The Tuning Protection Code locks the program and erase operations of all the blocks except for blocks 12 and 13 for the bottom configuration, and blocks 60 and 61 for the top configuration.

The tuning blocks are "locked" if the tuning protection code has not been provided, and “unlocked" once the correct code has been provided. The tuning blocks are locked after reset or power-up. The tuning protection status can be monitored in the Status Register. Refer to the Status Register section.

Refer to the Command Interface section for the Tuning Protection Block Unlock and Tuning Protection Program commands.

PART NUMBERING

Table 2. Ordering Information Scheme

Example: M58BW032B T 45 T 3 T

Device Type
M58

Architecture
B = Burst Mode

Operating Voltage
W = V_{DD} = 3.0V to 3.6V; V_{DDQ} = V_{DDQIN} =1.6 to V_{DD}

Device Function
032B = 32 Mbit (x32), Boot Block, Burst Tuning Protection
032D = 32 Mbit (x32), Boot Block, Burst no Tuning Protection

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
45 = 45ns
55 = 55ns
60 = 60ns

Package
T = PQFP80
ZA = LBGA80: 1.0mm pitch

Temperature Range
3 = –40 to 125 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Note: Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 3. Document Revision History

Date	Version	Revision Details
05-Nov-2004	1.0	First Issue.