M4003 & M4004 Series
9x14 mm, 5.0 or 3.3 Volt, PECL, VCSO

- Integrated phase jitter of less than 0.5 ps from 12 kHz to 20 MHz
- Ideal for SONET and 10 and 40 Gigabit Ethernet applications

Ordering Information

M4003/M4004 1 0 B 1 P J 00.0000 MHz

Product Series
M4003= 3.3 V
M4004 = 5.0 V

Temperature Range
1: 0°C to +70°C **2:** -40°C to +85°C *

Stability
0: Nominal per APR selection

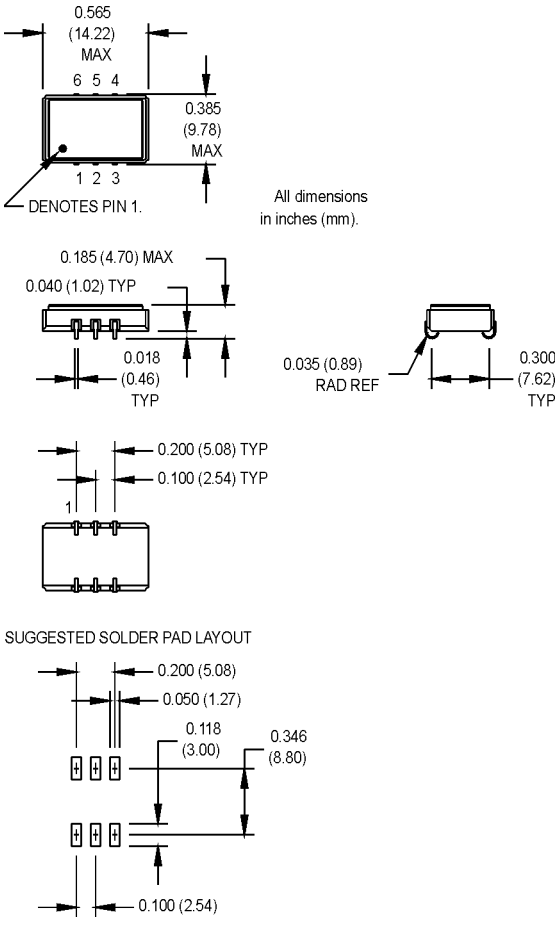
Output Type
B: Complementary, Enable (Enable High)
S: Complementary, Enable (Enable Low)

Absolute Pull Range
1: ±50 ppm (±100 ppm typical stability)

Symmetry/Output Logic Type
P: 45/55% PECL

Package/Lead Configurations
J: J-lead

Frequency (customer specified)



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	Output Enable or N/C
3	Ground/Case
4	Output Q
5	Output Q or N/C
6	+Vcc

M-tron Industries, Inc., PO Box 630, Yankton, SD 57078-0630, USA Phone: 605-665-9321 or 1-800-762-8800 Fax: 605-665-1709 Website: www.mtron.com
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	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition
Electrical Specifications	Frequency Range	F	500		1300	MHz	
			(Consult factory for exact frequency availability)				
	Frequency Stability	ΔF/F	(See Ordering Information)				With respect to 25°C
	Operating Temperature	TA	(See Ordering Information)				
	Storage Temperature	Ts	-55		+125	°C	
	Input Voltage	Vcc	3.135	3.3	3.465	V	3.3 Volt
			4.5	5.0	5.5	V	5.0 Volt
	Input Current	Iee/Icc		65	75	mA	3.3 Volt
				73	85	mA	5.0 Volt
	Output Current	Iout			20	mA	
	Symmetry (Duty Cycle)		45	50	55	%	Vcc -1.3
	Load		50 Ω to Vcc -2 V or Thevenin Equivalent				
	Rise/Fall Time	Tr/Tf			0.4	ns	20% to 80%
	Logic "1" Level	Voh	Vcc -0.98			V	
	Logic "0" Level	Vol			Vcc -1.63	V	
	Phase Jitter @ 622.08 MHz	ϕ J		0.15	0.30	ps RMS	12 kHz to 20 MHz
				0.25	0.40	ps RMS	50 kHz to 80 MHz
	Phase Noise @ 622.08 MHz	ϕ N		-70	-67	dBc/Hz	100 Hz Offset
				-100	-97	dBc/Hz	1 kHz Offset
				-120	-117	dBc/Hz	10 kHz Offset
				-137	-134	dBc/Hz	100 kHz Offset
	Spurious Suppression		-50			dB	
	Modulation Bandwidth	fm	500		kHz	-3 dB	
	Input Imepdance (Pin 1)	Zin	500			KΩ	
	Control Voltage	Vc	0		3.3	V	3.3 Volt
			0		5.0	V	5.0 Volt
	Pullability	APR	±50			ppm	See Note 1
	Deviation Slope (Positive)			125		ppm/V	@ 622.08 MHz
	Linearity			±3	±10	%	
	Enable/Disable Logic		CMOS high or Vcc - enables output CMOS low or GND - disables output				Output Option B
			PECL low, GND, or N/C - enables output PECL high - disables output				Output Option S
Environmental	Mechanical Shock	Per MIL-STD-202, Method 213, Condition E					
	Vibration	Per MIL-STD-202, Method 201 & 204					
	Reflow Solder Conditions	See "Figure 2" on page 147					
	Hermeticity	Per MIL-STD-202, Method 112 (1 x 10^{-8} atm.cc/s of helium)					
	Solderability	Per EIAJ-STD-002					

1. APR specification inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage and aging.

VCSO

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