# DDR2 Unbuffered SDRAM MODULE

**240pin Unbuffered Module based on 512Mb B-die**

**64/72-bit Non-ECC/ECC**

Revision 0.6

October 2003

# Revision History

## Revision 0.3 (Sep. 2003)

- Initial Release

## Revision 0.4 (Sep. 2003)

- Removed x16 base ECC UDIMM product

## Revision 0.5 (Oct. 2003)

- Removed D4 speed bin(400 4-4-4)

## Revision 0.6 (Oct. 2003)

- Added operation temperature condition
- Changed setup/hold time values(tIS/tDS, tIH/tDH)
- Added notes for setup/hold time(tIS/tDS, tIH/tDH)
- Added tREFI values by $T_{CASE}$ (85°C/95°C)

## DDR2 Unbuffered DIMM Ordering Information

| Part Number | Density | Organization | Component Composition | Number of Rank | Height |
|---|---|---|---|---|---|
| **x64 Non ECC** | | | | | |
| M378T3354BG0-CE6/D5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30.00mm |
| M378T3354BG0-LE6/D5/CC | 256MB | 32Mx64 | 32Mx16(K4T51163QB)*4 | 1 | 30.00mm |
| M378T6553BG0-CE6/D5/CC | 512MB | 64Mx64 | 64Mx8(K4T51083QB)*8 | 1 | 30.00mm |
| M378T6553BG0-LE6/D5/CC | 512MB | 64Mx64 | 64Mx8(K4T51083QB)*8 | 1 | 30.00mm |
| M378T2953BG0-CE6/D5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30.00mm |
| M378T2953BG0-LE6/D5/CC | 1GB | 128Mx64 | 64Mx8(K4T51083QB)*16 | 2 | 30.00mm |
| **x72 ECC** | | | | | |
| M391T6553BG0-CE6/D5/CC | 512MB | 64Mx72 | 64Mx8(K4T51083QB)*9 | 1 | 30.00mm |
| M391T6553BG0-LE6/D5/CC | 512MB | 64Mx72 | 64Mx8(K4T51083QB)*9 | 1 | 30.00mm |
| M391T2953BG0-CE6/D5/CC | 1GB | 128Mx72 | 64Mx8(K4T51083QB)*18 | 2 | 30.00mm |
| M391T2953BG0-LE6/D5/CC | 1GB | 128Mx72 | 64Mx8(K4T51083QB)*18 | 2 | 30.00mm |

Note:
1. Speed bin is in order of CL-tRCD-tRP

## Features

- Performance range

| | E6(DDR2-667) | D5(DDR2-533) | CC(DDR2-400) | Unit |
|---|---|---|---|---|
| Speed@CL3 | 400 | 400 | 400 | Mbps |
| Speed@CL4 | 533 | 533 | 400 | Mbps |
| Speed@CL5 | 533 | - | - | Mbps |
| Speed@CL6 | 667 | - | - | Mbps |
| CL-tRCD-tRP | 4-4-4 | 4-4-4 | 3-3-3 | CK |

- JEDEC standard 1.8V ± 0.1V Power Supply
- VDDQ = 1.8V ± 0.1V
- 200 MHz $f_{CK}$ for 400Mb/sec/pin, 267MHz $f_{CK}$ for 533Mb/sec/pin, 333MHz $f_{CK}$ for 667Mb/sec/pin
- 4 Bank
- Posted $\overline{CAS}$
- Programmable $\overline{CAS}$ Latency: 3, 4, 5
- Programmable Additive Latency: 0, 1 , 2 , 3 and 4
- Write Latency(WL) = Read Latency(RL) -1
- Burst Length: 4 , 8(Interleave/nibble sequential)
- Programmable Sequential / Interleave Burst Mode
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- Off-Chip Driver(OCD) Impedance Adjustment
- On Die Termination
- Average Refesh Period 7.8us at lower then $T_{CASE}$ 85×C, 3.9us at 85×C < $T_{CASE}$ ≤ 95 ×C
- Serial presence detect with EEPROM
- DDR2 SDRAM Package: 60ball FBGA - 64Mx8, 84ball FBGA - 32Mx16

## Address Configuration

| Organization | Row Address | Column Address | Bank Address | Auto Precharge |
|---|---|---|---|---|
| 64Mx8(512Mb) based Module | A0-A13 | A0-A9 | BA0-BA1 | A10 |
| 32Mx16(512Mb) based Module | A0-A12 | A0-A9 | BA0-BA1 | A10 |

## x64 DIMM Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 121 | $V_{SS}$ | 31 | DQ19 | 151 | $V_{SS}$ | 61 | A4 | 181 | $V_{DDQ}$ | 91 | $V_{SS}$ | 211 | DM5 |
| 2 | $V_{SS}$ | 122 | DQ4 | 32 | $V_{SS}$ | 152 | DQ28 | 62 | $V_{DDQ}$ | 182 | A3 | 92 | $\overline{DQS}5$ | 212 | NC |
| 3 | DQ0 | 123 | DQ5 | 33 | DQ24 | 153 | DQ29 | 63 | A2 | 183 | A1 | 93 | DQS5 | 213 | $V_{SS}$ |
| 4 | DQ1 | 124 | $V_{SS}$ | 34 | DQ25 | 154 | $V_{SS}$ | 64 | $V_{DD}$ | 184 | $V_{DD}$ | 94 | $V_{SS}$ | 214 | DQ46 |
| 5 | $V_{SS}$ | 125 | DM0 | 35 | $V_{SS}$ | 155 | DM3 | KEY | | | | 95 | DQ42 | 215 | DQ47 |
| 6 | $\overline{DQS}0$ | 126 | NC | 36 | $\overline{DQS}3$ | 156 | NC | 65 | $V_{SS}$ | 185 | CK0 | 96 | DQ43 | 216 | $V_{SS}$ |
| 7 | DQS0 | 127 | $V_{SS}$ | 37 | DQS3 | 157 | $V_{SS}$ | 66 | $V_{SS}$ | 186 | $\overline{CK}0$ | 97 | $V_{SS}$ | 217 | DQ52 |
| 8 | $V_{SS}$ | 128 | DQ6 | 38 | $V_{SS}$ | 158 | DQ30 | 67 | $V_{DD}$ | 187 | $V_{DD}$ | 98 | DQ48 | 218 | DQ53 |
| 9 | DQ2 | 129 | DQ7 | 39 | DQ26 | 159 | DQ31 | 68 | NC | 188 | A0 | 99 | DQ49 | 219 | $V_{SS}$ |
| 10 | DQ3 | 130 | $V_{SS}$ | 40 | DQ27 | 160 | $V_{SS}$ | 69 | $V_{DD}$ | 189 | $V_{DD}$ | 100 | $V_{SS}$ | 220 | CK2 |
| 11 | $V_{SS}$ | 131 | DQ12 | 41 | $V_{SS}$ | 161 | NC | 70 | A10/AP | 190 | BA1 | 101 | SA2 | 221 | $\overline{CK}2$ |
| 12 | DQ8 | 132 | DQ13 | 42 | NC | 162 | NC | 71 | BA0 | 191 | $V_{DDQ}$ | 102 | NC, TEST[2] | 222 | $V_{SS}$ |
| 13 | DQ9 | 133 | $V_{SS}$ | 43 | NC | 163 | $V_{SS}$ | 72 | $V_{DDQ}$ | 192 | $\overline{RAS}$ | 103 | $V_{SS}$ | 223 | DM6 |
| 14 | $V_{SS}$ | 134 | DM1 | 44 | $V_{SS}$ | 164 | NC | 73 | $\overline{WE}$ | 193 | $\overline{S}0$ | 104 | $\overline{DQS}6$ | 224 | NC |
| 15 | $\overline{DQS}1$ | 135 | NC | 45 | NC | 165 | NC | 74 | $\overline{CAS}$ | 194 | $V_{DDQ}$ | 105 | DQS6 | 225 | $V_{SS}$ |
| 16 | DQS1 | 136 | $V_{SS}$ | 46 | NC | 166 | $V_{SS}$ | 75 | $V_{DDQ}$ | 195 | ODT0 | 106 | $V_{SS}$ | 226 | DQ54 |
| 17 | $V_{SS}$ | 137 | CK1 | 47 | $V_{SS}$ | 167 | NC | 76 | $\overline{S}1$ | 196 | A13[1] | 107 | DQ50 | 227 | DQ55 |
| 18 | NC | 138 | $\overline{CK}1$ | 48 | NC | 168 | NC | 77 | ODT1 | 197 | $V_{DD}$ | 108 | DQ51 | 228 | $V_{SS}$ |
| 19 | NC | 139 | $V_{SS}$ | 49 | NC | 169 | $V_{SS}$ | 78 | $V_{DDQ}$ | 198 | $V_{SS}$ | 109 | $V_{SS}$ | 229 | DQ60 |
| 20 | $V_{SS}$ | 140 | DQ14 | 50 | $V_{SS}$ | 170 | $V_{DDQ}$ | 79 | $V_{SS}$ | 199 | DQ36 | 110 | DQ56 | 230 | DQ61 |
| 21 | DQ10 | 141 | DQ15 | 51 | $V_{DDQ}$ | 171 | CKE1 | 80 | DQ32 | 200 | DQ37 | 111 | DQ57 | 231 | $V_{SS}$ |
| 22 | DQ11 | 142 | $V_{SS}$ | 52 | CKE0 | 172 | $V_{DD}$ | 81 | DQ33 | 201 | $V_{SS}$ | 112 | $V_{SS}$ | 232 | DM7 |
| 23 | $V_{SS}$ | 143 | DQ20 | 53 | $V_{DD}$ | 173 | NC | 82 | $V_{SS}$ | 202 | DM4 | 113 | $\overline{DQS}7$ | 233 | NC |
| 24 | DQ16 | 144 | DQ21 | 54 | NC | 174 | NC | 83 | $\overline{DQS}4$ | 203 | NC | 114 | DQS7 | 234 | $V_{SS}$ |
| 25 | DQ17 | 145 | $V_{SS}$ | 55 | NC | 175 | $V_{DDQ}$ | 84 | DQS4 | 204 | $V_{SS}$ | 115 | $V_{SS}$ | 235 | DQ62 |
| 26 | $V_{SS}$ | 146 | DM2 | 56 | $V_{DDQ}$ | 176 | A12 | 85 | $V_{SS}$ | 205 | DQ38 | 116 | DQ58 | 236 | DQ63 |
| 27 | $\overline{DQS}2$ | 147 | NC | 57 | A11 | 177 | A9 | 86 | DQ34 | 206 | DQ39 | 117 | DQ59 | 237 | $V_{SS}$ |
| 28 | DQS2 | 148 | $V_{SS}$ | 58 | A7 | 178 | $V_{DD}$ | 87 | DQ35 | 207 | $V_{SS}$ | 118 | $V_{SS}$ | 238 | VDDSPD |
| 29 | $V_{SS}$ | 149 | DQ22 | 59 | $V_{DD}$ | 179 | A8 | 88 | $V_{SS}$ | 208 | DQ44 | 119 | SDA | 239 | SA0 |
| 30 | DQ18 | 150 | DQ23 | 60 | A5 | 180 | A6 | 89 | DQ40 | 209 | DQ45 | 120 | SCL | 240 | SA1 |
| | | | | | | | | 90 | DQ41 | 210 | $V_{SS}$ | | | | |

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)

## x72 DIMM Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REF}$ | 121 | $V_{SS}$ | 31 | DQ19 | 151 | $V_{SS}$ | 61 | A4 | 181 | $V_{DDQ}$ | 91 | $V_{SS}$ | 211 | DM5 |
| 2 | $V_{SS}$ | 122 | DQ4 | 32 | $V_{SS}$ | 152 | DQ28 | 62 | $V_{DDQ}$ | 182 | A3 | 92 | $\overline{DQS}5$ | 212 | NC |
| 3 | DQ0 | 123 | DQ5 | 33 | DQ24 | 153 | DQ29 | 63 | A2 | 183 | A1 | 93 | DQS5 | 213 | $V_{SS}$ |
| 4 | DQ1 | 124 | $V_{SS}$ | 34 | DQ25 | 154 | $V_{SS}$ | 64 | $V_{DD}$ | 184 | $V_{DD}$ | 94 | $V_{SS}$ | 214 | DQ46 |
| 5 | $V_{SS}$ | 125 | DM0 | 35 | $V_{SS}$ | 155 | DM3 | KEY | | | | 95 | DQ42 | 215 | DQ47 |
| 6 | $\overline{DQS}0$ | 126 | NC | 36 | $\overline{DQS}3$ | 156 | NC | 65 | $V_{SS}$ | 185 | CK0 | 96 | DQ43 | 216 | $V_{SS}$ |
| 7 | DQS0 | 127 | $V_{SS}$ | 37 | DQS3 | 157 | $V_{SS}$ | 66 | $V_{SS}$ | 186 | $\overline{CK}0$ | 97 | $V_{SS}$ | 217 | DQ52 |
| 8 | $V_{SS}$ | 128 | DQ6 | 38 | $V_{SS}$ | 158 | DQ30 | 67 | $V_{DD}$ | 187 | $V_{DD}$ | 98 | DQ48 | 218 | DQ53 |
| 9 | DQ2 | 129 | DQ7 | 39 | DQ26 | 159 | DQ31 | 68 | NC | 188 | A0 | 99 | DQ49 | 219 | $V_{SS}$ |
| 10 | DQ3 | 130 | $V_{SS}$ | 40 | DQ27 | 160 | $V_{SS}$ | 69 | $V_{DD}$ | 189 | $V_{DD}$ | 100 | $V_{SS}$ | 220 | CK2 |
| 11 | $V_{SS}$ | 131 | DQ12 | 41 | $V_{SS}$ | 161 | CB4 | 70 | A10/AP | 190 | BA1 | 101 | SA2 | 221 | $\overline{CK}2$ |
| 12 | DQ8 | 132 | DQ13 | 42 | CB0 | 162 | CB5 | 71 | BA0 | 191 | $V_{DDQ}$ | 102 | NC, TEST[2] | 222 | $V_{SS}$ |
| 13 | DQ9 | 133 | $V_{SS}$ | 43 | CB1 | 163 | $V_{SS}$ | 72 | $V_{DDQ}$ | 192 | $\overline{RAS}$ | 103 | $V_{SS}$ | 223 | DM6 |
| 14 | $V_{SS}$ | 134 | DM1 | 44 | $V_{SS}$ | 164 | DM8 | 73 | $\overline{WE}$ | 193 | $\overline{S}0$ | 104 | $\overline{DQS}6$ | 224 | NC |
| 15 | $\overline{DQS}1$ | 135 | NC | 45 | $\overline{DQS}8$ | 165 | NC | 74 | $\overline{CAS}$ | 194 | $V_{DDQ}$ | 105 | DQS6 | 225 | $V_{SS}$ |
| 16 | DQS1 | 136 | $V_{SS}$ | 46 | DQS8 | 166 | $V_{SS}$ | 75 | $V_{DDQ}$ | 195 | ODT0 | 106 | $V_{SS}$ | 226 | DQ54 |
| 17 | $V_{SS}$ | 137 | CK1 | 47 | $V_{SS}$ | 167 | CB6 | 76 | $\overline{S}1$ | 196 | A13 | 107 | DQ50 | 227 | DQ55 |
| 18 | NC | 138 | $\overline{CK}1$ | 48 | CB2 | 168 | CB7 | 77 | ODT1 | 197 | $V_{DD}$ | 108 | DQ51 | 228 | $V_{SS}$ |
| 19 | NC | 139 | $V_{SS}$ | 49 | CB3 | 169 | $V_{SS}$ | 78 | $V_{DDQ}$ | 198 | $V_{SS}$ | 109 | $V_{SS}$ | 229 | DQ60 |
| 20 | $V_{SS}$ | 140 | DQ14 | 50 | $V_{SS}$ | 170 | $V_{DDQ}$ | 79 | $V_{SS}$ | 199 | DQ36 | 110 | DQ56 | 230 | DQ61 |
| 21 | DQ10 | 141 | DQ15 | 51 | $V_{DDQ}$ | 171 | CKE1 | 80 | DQ32 | 200 | DQ37 | 111 | DQ57 | 231 | $V_{SS}$ |
| 22 | DQ11 | 142 | $V_{SS}$ | 52 | CKE0 | 172 | $V_{DD}$ | 81 | DQ33 | 201 | $V_{SS}$ | 112 | $V_{SS}$ | 232 | DM7 |
| 23 | $V_{SS}$ | 143 | DQ20 | 53 | $V_{DD}$ | 173 | NC | 82 | $V_{SS}$ | 202 | DM4 | 113 | $\overline{DQS}7$ | 233 | NC |
| 24 | DQ16 | 144 | DQ21 | 54 | NC | 174 | NC | 83 | $\overline{DQS}4$ | 203 | NC | 114 | DQS7 | 234 | $V_{SS}$ |
| 25 | DQ17 | 145 | $V_{SS}$ | 55 | NC | 175 | $V_{DDQ}$ | 84 | DQS4 | 204 | $V_{SS}$ | 115 | $V_{SS}$ | 235 | DQ62 |
| 26 | $V_{SS}$ | 146 | DM2 | 56 | $V_{DDQ}$ | 176 | A12 | 85 | $V_{SS}$ | 205 | DQ38 | 116 | DQ58 | 236 | DQ63 |
| 27 | $\overline{DQS}2$ | 147 | NC | 57 | A11 | 177 | A9 | 86 | DQ34 | 206 | DQ39 | 117 | DQ59 | 237 | $V_{SS}$ |
| 28 | DQS2 | 148 | $V_{SS}$ | 58 | A7 | 178 | $V_{DD}$ | 87 | DQ35 | 207 | $V_{SS}$ | 118 | $V_{SS}$ | 238 | VDDSPD |
| 29 | $V_{SS}$ | 149 | DQ22 | 59 | $V_{DD}$ | 179 | A8 | 88 | $V_{SS}$ | 208 | DQ44 | 119 | SDA | 239 | SA0 |
| 30 | DQ18 | 150 | DQ23 | 60 | A5 | 180 | A6 | 89 | DQ40 | 209 | DQ45 | 120 | SCL | 240 | SA1 |
| | | | | | | | | 90 | DQ41 | 210 | $V_{SS}$ | | | | |

NC = No Connect, RFU = Reserved for Future Use
1. Pin196(A13) is used for x4/x8 base Unbuffered DIMM.
2. The TEST pin is reserved for bus analysis tools and is not connected on standard memory module products (DIMMs.)



## Pin Description

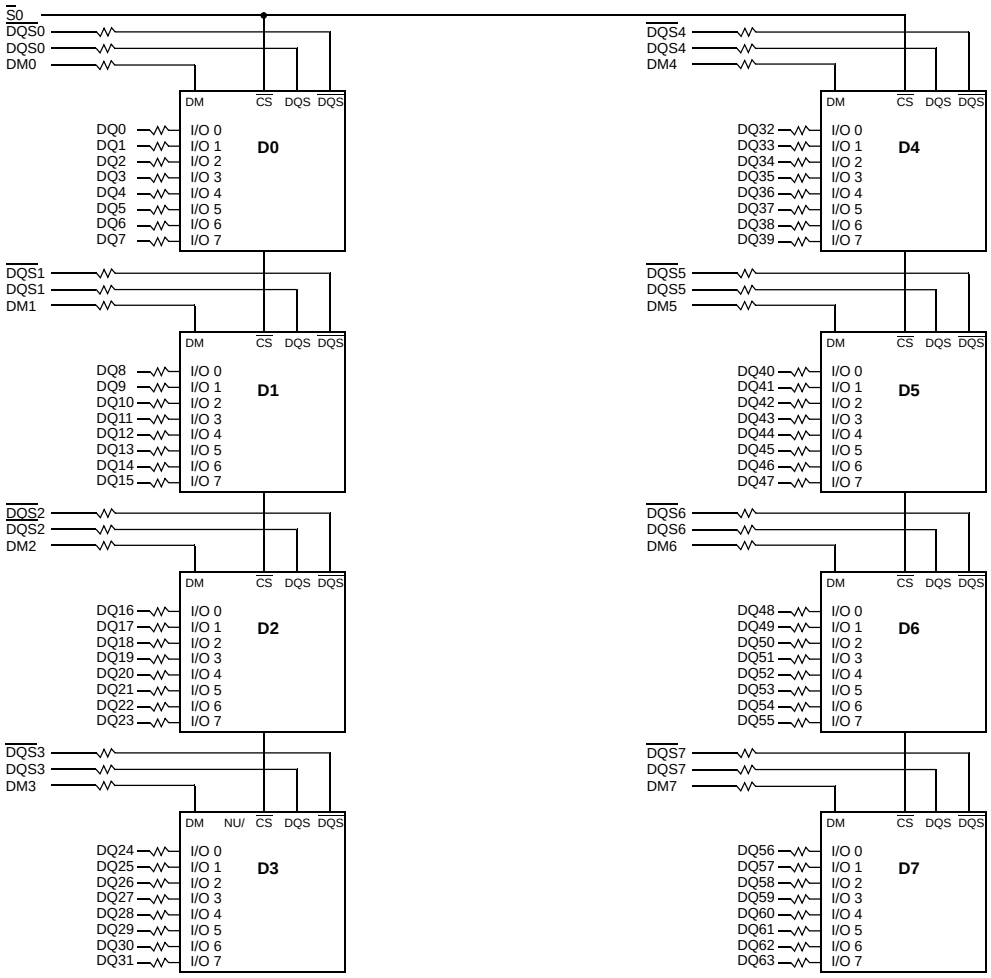
| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0-A13 | DDR2 SDRAM address bus | CK0, CK1, CK2 | DDR2 SDRAM clocks (positive line of differential pair) |
| BA0, BA1 | DDR2 SDRAM bank select | $\overline{CK}0$, $\overline{CK}1$, $\overline{CK}2$ | DDR2 SDRAM clocks (negative line of differential pair) |
| $\overline{RAS}$ | DDR2 SDRAM row address strobe | SCL | $I^2C$ serial bus clock for EEPROM |
| $\overline{CAS}$ | DDR2 SDRAM column address strobe | SDA | $I^2C$ serial bus data line for EEPROM |
| $\overline{WE}$ | DDR2 SDRAM wirte enable | SA0-SA2 | $I^2C$ serial address select for EEPROM |
| $\overline{S}0$, $\overline{S}1$ | DIMM Rank Select Lines | $V_{DD}$* | DDR2 SDRAM core power supply |
| CKE0,CKE1 | DDR2 SDRAM clock enable lines | $V_{DDQ}$* | DDR2 SDRAM I/O Driver power supply |
| ODT0, ODT1 | On-die termination control lines | $V_{REF}$ | DDR2 SDRAM I/O reference supply |
| DQ0 - DQ63 | DIMM memory data bus | $V_{SS}$ | Power supply return (ground) |
| CB0 - CB7 | DIMM ECC check bits | $V_{DD}$SPD | Serial EEPROM positive power supply |
| DQS0 - DQS8 | DDR2 SDRAM data strobes | NC | Spare Pins(no connect) |
| DM(0-8) | DDR2 SDRAM data masks | RESET | Not used on UDIMM |
| $\overline{DQS}0$-$\overline{DQS}8$ | DDR2 SDRAM differential data strobes | TEST | Used by memory bus analysis tools (unused on memory DIMMs) |

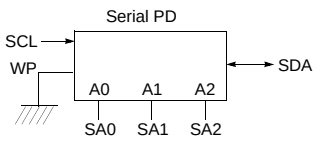
*The VDD and VDDQ pins are tied to the single power-plane on PCB.

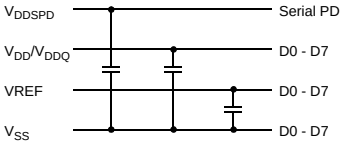
## Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0-CK2<br>CK0-CK2 | SSTL_1.8 | Differential crossing | CK and CK are differential clock inputs. All the SDRAM addr/cntl inputs are sampled on the crossing of positive edge of CK and negative edge of CK. Output (read) data is reference to the crossing of CK and CK (Both directions of crossing) |
| CKE0-CKE1 | SSTL_1.8 | Active High | Activates the SDRAM CK signal when high and deactivates the CK Signal When low. By deactivating the clocks, CKE low initiates the Powe Down mode, or the Self-Refresh mode |
| S0-S1 | SSTL_1.8 | Active Low | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disbled, new command are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks |
| RAS, CAS, WE | SSTL_1.8 | - | RAS, CAS, and WE (ALONG WITH CS) define the command being entered. |
| ODT0-ODT1 | SSTL_1.8 | TBD | When high, termination resistance is enabled for all DQ, DQ and DM pins, assuming the function is enabled in the Extended Mode Register Set (EMRS). |
| $V_{REF}$ | Supply | - | Reference voltage for SSTL 18 inputs. |
| $V_{DDQ}$ | Supply | - | Power supply for the DDR II SDRAM output buffers to provide improved noise immunity. For all current DDR2 unbuffered DIMM designs, VDDQ shares the same power plane as VDD pins. |
| BA0-BA1 | SSTL_1.8 | - | Selects which SDRAM BANK of four is activated. |
| A0-A13 | SSTL_1.8 | - | During a Bank Activate command cycle, Address input defines the row address (RA0-RA13)<br><br>During a Read or Write command cycle, Address input defines the colum address, In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disbled. During a precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1. If AP is low, BA0, BA1are used to define which bank to precharge. |
| DQ0-DQ63<br>CB0-CB7 | SSTL_1.8 | - | Data and Check Bit Input/Output pins. |
| DM0-DM8 | SSTL_1.8 | Active High | DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. |
| $V_{DD}$,$V_{SS}$ | Supply | - | Power and ground for DDR2 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to $V_{DD}$/$V_{DDQ}$ planes on these modules. |
| DQS0-DQS8<br>DQS0-DQS8 | SSTL_1.8 | Differential crossing | Data strobe for input and output data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM |
| SA0-SA2 | - | - | These signals and tied at the system planar to either $V_{SS}$ or $V_{DD}$ to configure the serial SPD EERPOM address range. |
| SDA | - | - | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to VDD to act as a pullup on the system board. |
| SCL | - | - | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to VDD to act as a pullup onthe system board. |
| $V_{DD}$ SPD | Supply | - | Power supply for SPD EEPROM. This supply is separate from the $V_{DD}$/$V_{DDQ}$ power plane. EEPROM supply is operable from 1.7V to 3.6V. |

## Functional Block Diagram: 512MB, 64Mx64 Module(Populated as 1 rank of x8 DDR2 SDRAMs)
## (M378T6553BG0)



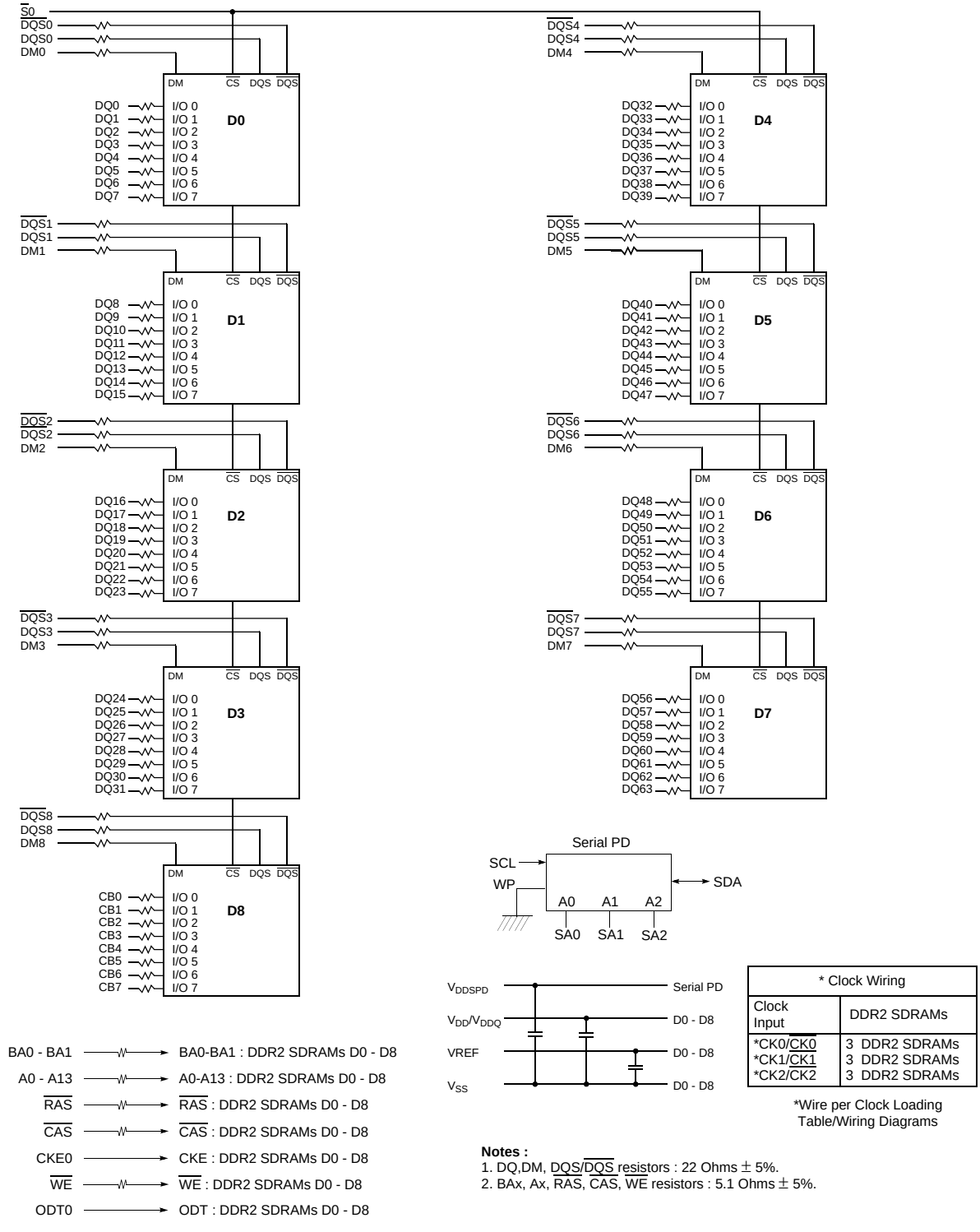

| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 2 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 3 DDR2 SDRAMs |
| *CK2/CK2 | 3 DDR2 SDRAMs |

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D7
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D7
$\overline{RAS}$ → $\overline{RAS}$ : DDR2 SDRAMs D0 - D7
$\overline{CAS}$ → $\overline{CAS}$ : DDR2 SDRAMs D0 - D7
CKE0 → CKE : DDR2 SDRAMs D0 - D7
$\overline{WE}$ → $\overline{WE}$ : DDR2 SDRAMs D0 - D7
ODT0 → ODT : DDR2 SDRAMs D0 - D7

**Notes :**
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, $\overline{WE}$ resistors : 5.1 Ohms ± 5%.

## Functional Block Diagram: 512MB, 64Mx72 ECC Module(Populated as 1 rank of x8 DDR2 SDRAMs)
## (M391T6553BG0)



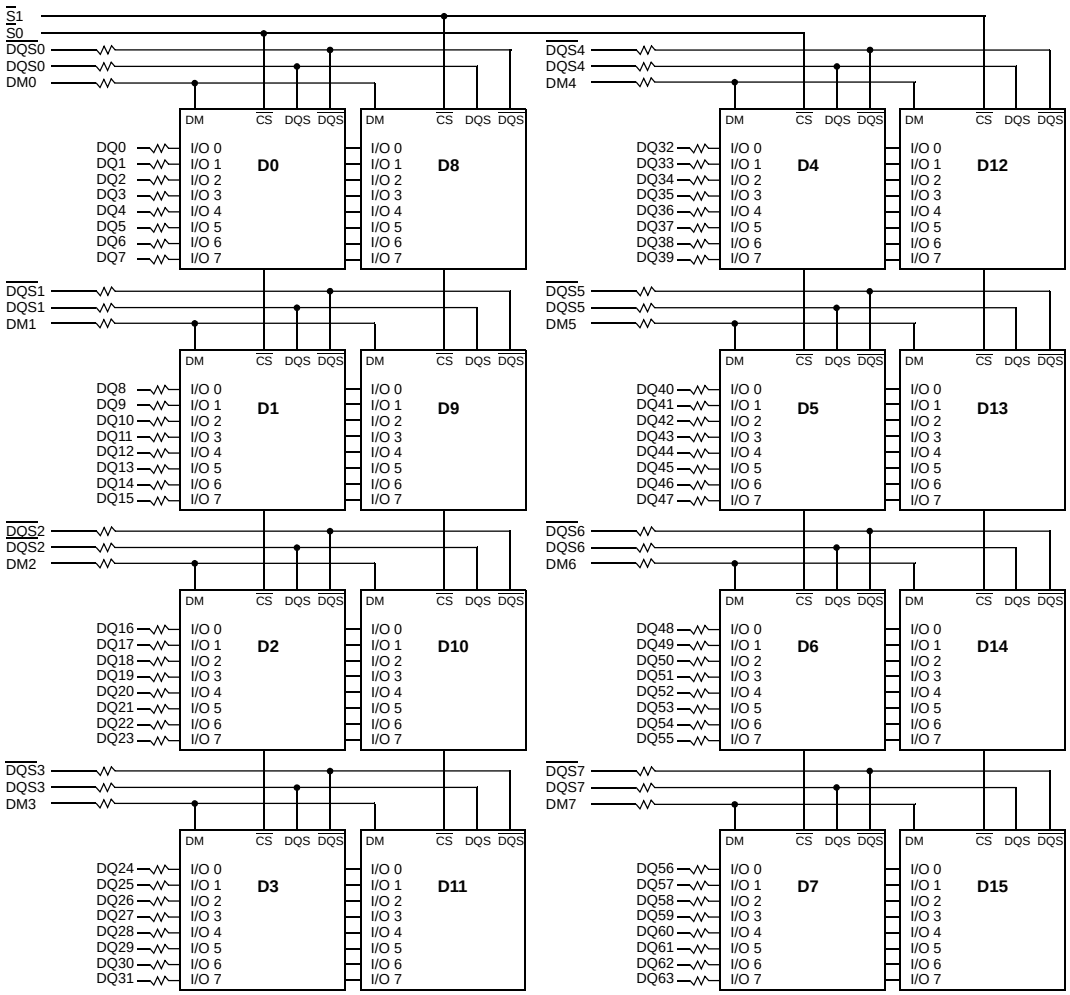

| | | |
|---|---|---|
| BA0 - BA1 | → | BA0-BA1 : DDR2 SDRAMs D0 - D8 |
| A0 - A13 | → | A0-A13 : DDR2 SDRAMs D0 - D8 |
| $\overline{RAS}$ | → | $\overline{RAS}$ : DDR2 SDRAMs D0 - D8 |
| $\overline{CAS}$ | → | $\overline{CAS}$ : DDR2 SDRAMs D0 - D8 |
| CKE0 | → | CKE : DDR2 SDRAMs D0 - D8 |
| $\overline{WE}$ | → | $\overline{WE}$ : DDR2 SDRAMs D0 - D8 |
| ODT0 | → | ODT : DDR2 SDRAMs D0 - D8 |

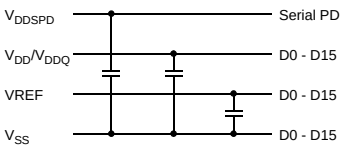
| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 3 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 3 DDR2 SDRAMs |
| *CK2/CK2 | 3 DDR2 SDRAMs |

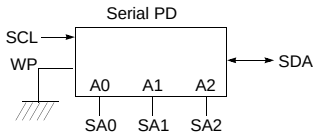
*Wire per Clock Loading Table/Wiring Diagrams

**Notes :**
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 5.1 Ohms ± 5%.

## Functional Block Diagram: 1GB, 128Mx64 Module(Populated as 2 ranks of x8 DDR2 SDRAMs)
## (M378T2953BG0)



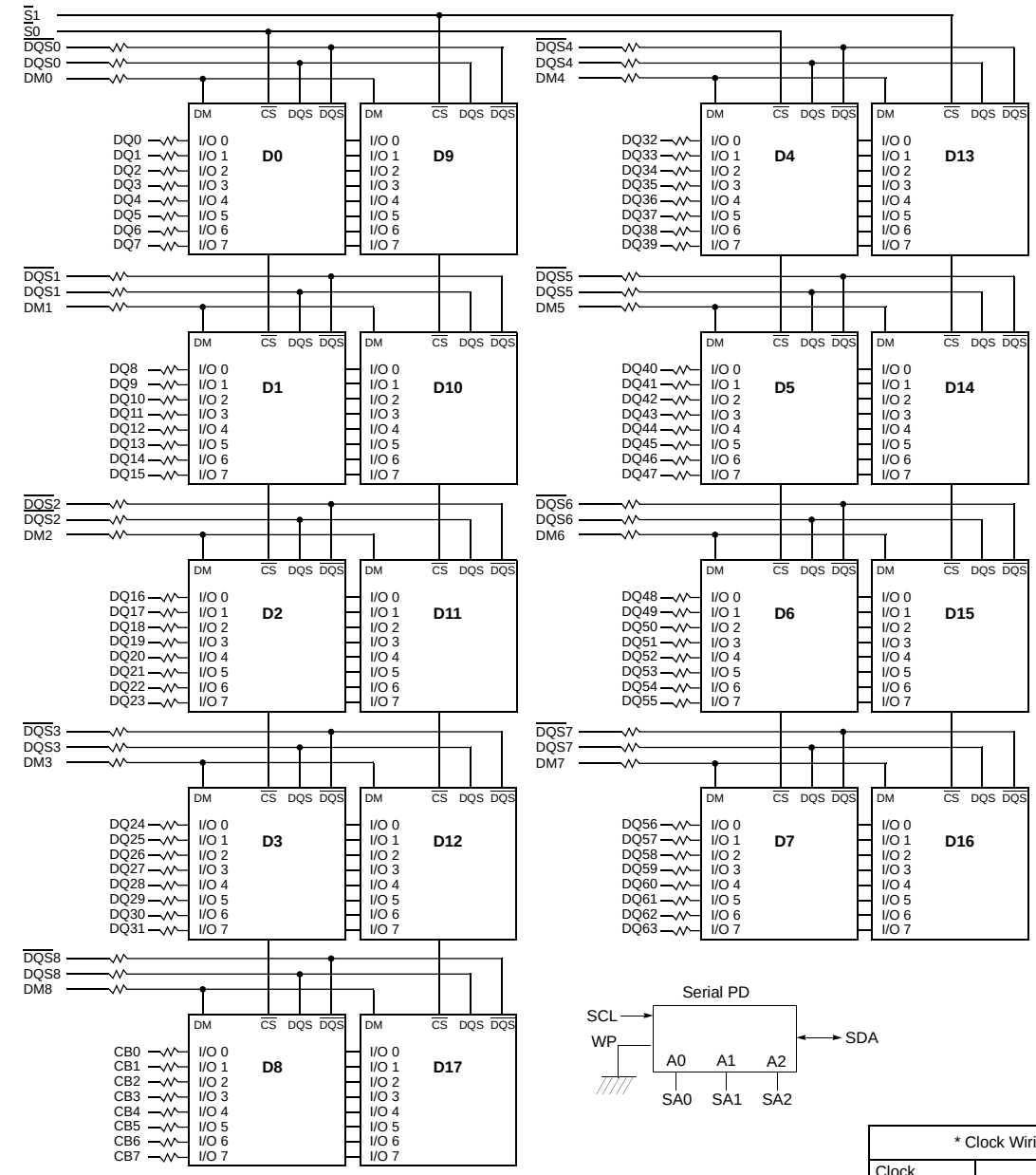

| | |
|---|---|
| BA0 - BA1 | BA0-BA1 : DDR2 SDRAMs D0 - D15 |
| A0 - A13 | A0-A13 : DDR2 SDRAMs D0 - D15 |
| CKE0 | CKE : DDR2 SDRAMs D0 - D7 |
| CKE1 | CKE : DDR2 SDRAMs D8 - D15 |
| $\overline{RAS}$ | $\overline{RAS}$ : DDR2 SDRAMs D0 - D15 |
| $\overline{CAS}$ | $\overline{CAS}$ : DDR2 SDRAMs D0 - D15 |
| $\overline{WE}$ | $\overline{WE}$ : DDR2 SDRAMs D0 - D15 |
| ODT0 | ODT : DDR2 SDRAMs D0 - D7 |
| ODT1 | ODT : DDR2 SDRAMs D8 - D15 |

| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 4 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 6 DDR2 SDRAMs |
| *CK2/CK2 | 6 DDR2 SDRAMs |

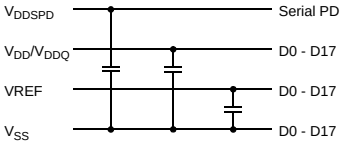
*Wire per Clock Loading Table/Wiring Diagrams

**Notes :**
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ resistors : 3 Ohms ± 5%.

## Functional Block Diagram: 1GB, 128Mx72 ECC Module (Populated as 2 ranks of x8 DDR2 SDRAMs)
## (M391T2953BG0)




BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D17
A0 - A13 → A0-A13 : DDR2 SDRAMs D0 - D17
CKE0 → CKE : DDR2 SDRAMs D0 - D8
CKE1 → CKE : DDR2 SDRAMs D9 - D17
$\overline{RAS}$ → $\overline{RAS}$ : DDR2 SDRAMs D0 - D17
$\overline{CAS}$ → $\overline{CAS}$ : DDR2 SDRAMs D0 - D17
$\overline{WE}$ → $\overline{WE}$ : DDR2 SDRAMs D0 - D17
ODT0 → ODT : DDR2 SDRAMs D0 - D8
ODT1 → ODT : DDR2 SDRAMs D9 - D17

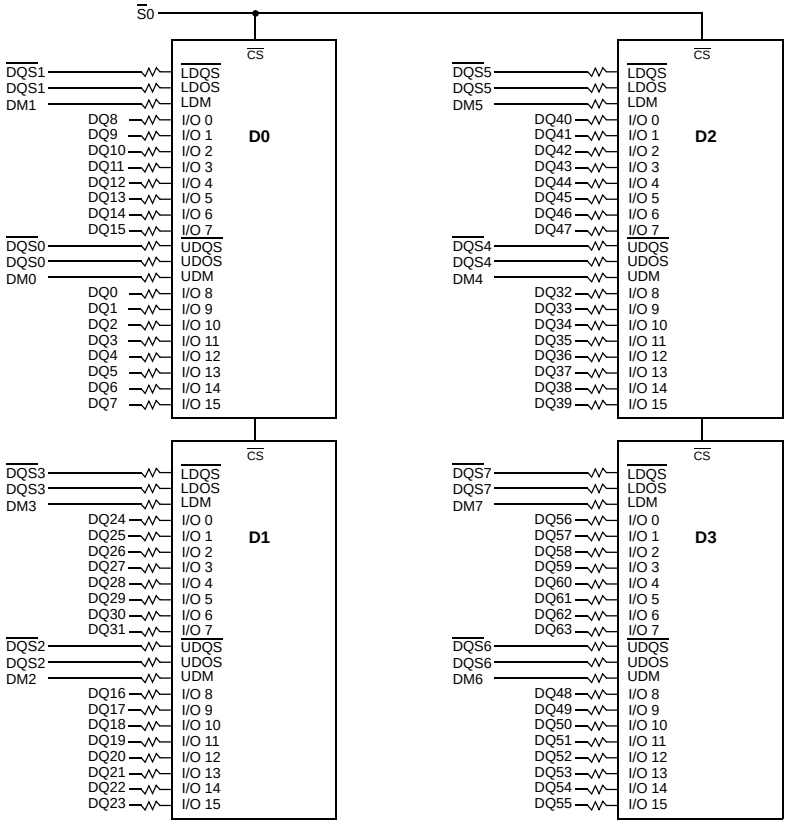


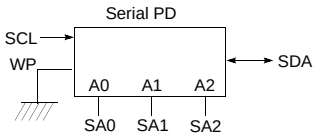

| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/$\overline{CK0}$ | 6 DDR2 SDRAMs |
| *CK1/$\overline{CK1}$ | 6 DDR2 SDRAMs |
| *CK2/$\overline{CK2}$ | 6 DDR2 SDRAMs |

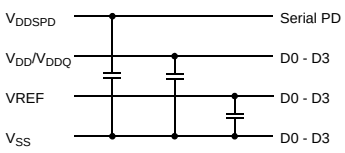
*Wire per Clock Loading Table/Wiring Diagrams

**Notes :**
1. DQ,DM, DQS/$\overline{DQS}$ resistors : 22 Ohms ± 5%.
2. BAx, Ax, RAS, CAS, WE resistors : 3 Ohms ± 5%.

## Functional Block Diagram: 256MB, 32Mx64 Module (Populated as 1 rank of x16 DDR2 SDRAMs)
## (M378T3354BG0)




| * Clock Wiring | |
|---|---|
| Clock Input | DDR2 SDRAMs |
| *CK0/CK0 | NC |
| *CK1/CK1 | 2 DDR2 SDRAMs |
| *CK2/CK2 | 2 DDR2 SDRAMs |

*Wire per Clock Loading Table/Wiring Diagrams

BA0 - BA1 → BA0-BA1 : DDR2 SDRAMs D0 - D3
A0 - A12 → A0-A12 : DDR2 SDRAMs D0 - D3
CKE0 → CKE : DDR2 SDRAMs D0 - D3
RAS → RAS : DDR2 SDRAMs D0 - D3
CAS → CAS : DDR2 SDRAMs D0 - D3
WE → WE : DDR2 SDRAMs D0 - D3
ODT0 → ODT : DDR2 SDRAMs D0 - D3

**Notes :**
1. DQ,DM, DQS/DQS resistors : 22 Ohms ± 5%.
4. BAx, Ax, RAS, CAS, WE resistors : 10 Ohms ± 5%.

## Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| VDD | Voltage on VDD pin relative to Vss | - 1.0 V ~ 2.3 V | V | 1 |
| VDDQ | Voltage on VDDQ pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| VDDL | Voltage on VDDL pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to Vss | - 0.5 V ~ 2.3 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1 |

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.

## AC & DC Operating Conditions

## Recommended DC Operating Conditions (SSTL - 1.8)

| Symbol | Parameter | Rating | | | Units | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| VDD | Supply Voltage | 1.7 | 1.8 | 1.9 | V | |
| VDDL | Supply Voltage for DLL | 1.7 | 1.8 | 1.9 | V | 4 |
| VDDQ | Supply Voltage for Output | 1.7 | 1.8 | 1.9 | V | 4 |
| VREF | Input Reference Voltage | 0.49*VDDQ | 0.50*VDDQ | 0.51*VDDQ | mV | 1.2 |
| VTT | Termination Voltage | VREF-0.04 | VREF | VREF+0.04 | V | 3 |

There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
2. Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together.

## Operating Temperature Condition

| SYMBOL | PARAMETER | RATING | UNITS | NOTES |
|---|---|---|---|---|
| TOPER | Operating Temperature | 0 to 95 | °C | 1, 2 |

Note :
1. Operating Temperature is the case surface temperature on the center/top side of the DRAM.
2. The operation temperature range are the temperature where all DRAM specification will be supported.

## Input DC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $V_{IH}$(dc) | dc input logic high | VREF + 0.125 | VDDQ + 0.3 | V | |
| $V_{IL}$(dc) | dc input logic low | - 0.3 | VREF - 0.125 | V | |

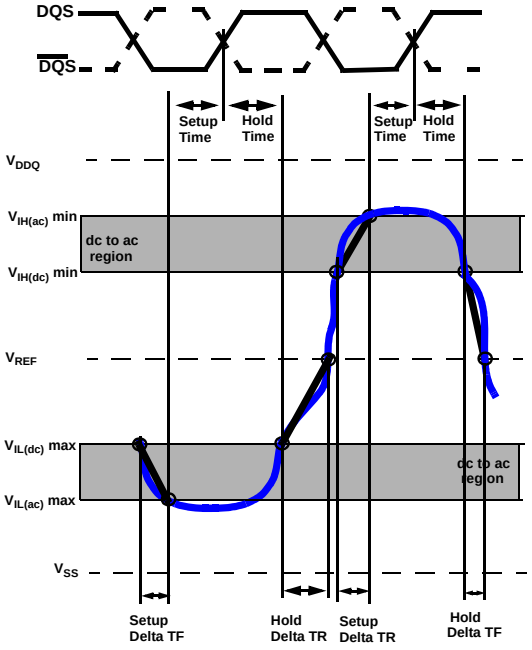
## Input AC Logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $V_{IH}$ (ac) | ac input logic high | VREF + 0.250 | - | V | |
| $V_{IL}$ (ac) | ac input logic low | - | VREF - 0.250 | V | |

## AC Input Test Conditions

| Symbol | Condition | Value | Units | Notes |
|---|---|---|---|---|
| $V_{REF}$ | Input reference voltage | 0.5 * $V_{DDQ}$ | V | 1 |
| $V_{SWING(MAX)}$ | Input signal maximum peak to peak swing | 1.0 | V | 1 |
| SLEW | Input signal minimum slew rate | 1.0 | V/ns | 2, 3 |

Note :
1. Setup (tIS & tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of Vih(ac)min. Setup (tIS & tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'dc to ac region', use nominal slew rate for derating value (see Fig a.) If the actual signal is later than the nominal slew rate line anywhere between shaded 'dc to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Fig b.)
2. Hold (tIH & tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of Vref. Hold (tIH & tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of Vref. If the actual signal is always later than the nominal slew rate line between shaded 'dc to Vref region', use nominal slew rate for derating value (see Fig a.) If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to Vref region', the slew rate of a tangent line to the actual signal from the dc level to Vref level is used for derating value (see Fig b.)Input waveform timing is referenced to the input signal crossing through the $V_{REF}$ level applied to the device under test.



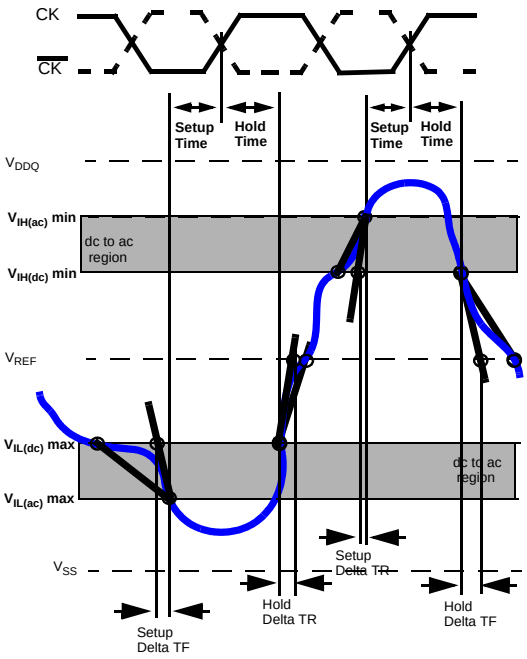

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{Vil(dc)max - Vil(ac)max}}{\text{Setup Delta TF}}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{\text{Vih(ac)min - Vih(dc)min}}{\text{Setup Delta TR}}$$

$$\text{Hold Slew Rate Rising Signal} = \frac{\text{Vref - Vil(dc)max}}{\text{Hold Delta TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{Vih(dc)min - Vref}}{\text{Hold Delta TF}}$$

<Figure. a>




$$\text{Setup Slew Rate Rising Signal} = \frac{\text{tangent line[Vih(ac)min - Vih(dc)min]}}{\text{Setup Delta TR}}$$

$$\text{Setup Slew Rate Falling Signal} = \frac{\text{tangent line[Vil(dc)max - Vil(ac)max]}}{\text{Setup Delta TF}}$$

$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line [ Vref - Vil(dc)max ]}}{\text{Hold Delta TR}}$$

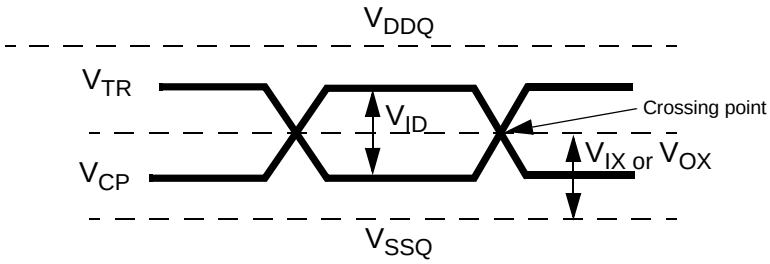
$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line [ Vih(dc)min - Vref ]}}{\text{Hold Delta TF}}$$

<Figure. b>

## Differential input AC logic Level

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $V_{ID}$ (ac) | ac differential input voltage | 0.5 | VDDQ + 0.6 | V | 1 |
| $V_{IX}$ (ac) | ac differential cross point voltage | 0.5 * VDDQ - 0.175 | 0.5 * VDDQ + 0.175 | V | 2 |

1. $V_{IN(DC)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
2. $V_{ID(DC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where $V_{TR}$ is the true input (such as CK, DQS, LDQS or UDQS) level and $V_{CP}$ is the complementary input (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$) level. The minimum value is equal to $V_{IH(DC)} - V_{IL(DC)}$.




**< Differential signal levels >**

Notes:

1. $V_{ID(AC)}$ specifies the input differential voltage $|V_{TR} - V_{CP}|$ required for switching, where $V_{TR}$ is the true input signal (such as CK, DQS, LDQS or UDQS) and $V_{CP}$ is the complementary input signal (such as $\overline{CK}$, $\overline{DQS}$, $\overline{LDQS}$ or $\overline{UDQS}$). The minimum value is equal to $V_{IH(AC)} - V_{IL(AC)}$.
2. The typical value of $V_{IX(AC)}$ is expected to be about 0.5 * VDDQ of the transmitting device and $V_{IX(AC)}$ is expected to track variations in VDDQ . $V_{IX(AC)}$ indicates the voltage at which differential input signals must cross.

## Differential AC output parameters

| Symbol | Parameter | Min. | Max. | Units | Notes |
|---|---|---|---|---|---|
| $V_{OX}$ (ac) | ac differential cross point voltage | 0.5 * VDDQ - 0.125 | 0.5 * VDDQ + 0.125 | V | 1 |

Notes:
1. The typical value of $V_{OX(AC)}$ is expected to be about 0.5 * V DDQ of the transmitting device and $V_{OX(AC)}$ is expected to track variations in VDDQ . $V_{OX(AC)}$ indicates the voltage at whitch differential output signals must cross.

## Output Buffer Levels (@ Component)

### Output AC Test Conditions

| Symbol | Parameter | Class II | Units | Notes |
|---|---|---|---|---|
| $V_{OH}$ | Minimum Required Output Pull-up under AC Test Load | $V_{TT}$ + 0.603 | V | |
| $V_{OL}$ | Maximum Required Output Pull-down under AC Test Load | $V_{TT}$ - 0.603 | V | |
| $V_{OTR}$ | Output Timing Measurement Reference Level | 0.5 * $V_{DDQ}$ | V | 1 |

1. The VDDQ of the device under test is referenced.

### Output DC Current Drive

| Symbol | Parameter | Class II | Units | Notes |
|---|---|---|---|---|
| $I_{OH(dc)}$ | Output Minimum Source DC Current | - 13.4 | mA | 1, 3, 4 |
| $I_{OL(dc)}$ | Output Minimum Sink DC Current | 13.4 | mA | 2, 3, 4 |

1. $V_{DDQ}$ = 1.7 V; $V_{OUT}$ = 1420 mV. ($V_{OUT}$ - $V_{DDQ}$)/$I_{OH}$ must be less than 21 ohm for values of $V_{OUT}$ between $V_{DDQ}$ and $V_{DDQ}$ - 280 mV.
2. $V_{DDQ}$ = 1.7 V; $V_{OUT}$ = 280 mV. $V_{OUT}$/$I_{OL}$ must be less than 21 ohm for values of $V_{OUT}$ between 0 V and 280 mV.
3. The dc value of $V_{REF}$ applied to the receiving device is set to $V_{TT}$
4. The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in Notes 1 and 2. They are used to test device drive current capability to ensure $V_{IH}$ min plus a noise margin and $V_{IL}$ max minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating point (see Section 3.3) along a 21 ohm load line to define a convenient driver current for measurement.

### OCD default characteristics

| Description | Parameter | Min | Nom | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Output impedance | | 12.6 | 18 | 23.4 | ohms | 1,2 |
| Output impedance step size for OCD calibration | | 0 | | 1.5 | ohms | 6 |
| Pull-up and pull-down mismatch | | 0 | | 4 | ohms | 1,2,3 |
| Output slew rate | | tbd | | tbd | V/ns | 1,4,5 |

Note 1: Absolute Specifications (0°C ≤ $T_{CASE}$ ≤ +tbd°C; VDD = +1.8V ±0.1V, VDDQ = +1.8V ±0.1V)

Note 2: Impedance measurement condition for output source dc current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT-VDDQ)/Ioh must be less than 23.4 ohms for values of VOUT between VDDQ and VDDQ-280mV. Impedance measurement condition for output sink dc current: VDDQ = 1.7V; VOUT = 280mV; VOUT/Iol must be less than 23.4 ohms for values of VOUT between 0V and 280mV.

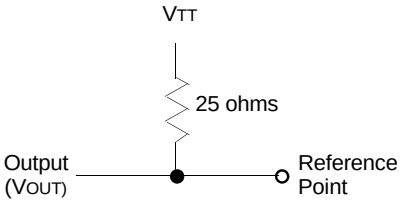
Note 3: Mismatch is absolute value between pull-up and pull-dn, both are measured at same temperature and voltage.

Note 4: Slew rate measured from vil(ac) to vih(ac).

Note 5: The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.

Note 6 : This represents the step size when the OCD is near 18 ohms at nominal conditions across all process and represents only the DRAM uncertainty. A 0 ohm value (no calibration) can only be achieved if the OCD impedance is 18 ohms +/- 0.75 ohms under nominal conditions.

Output slew rate load :




## Input/Output Capacitance(VDD=1.8V, VDDQ=1.8V, TA=25°C, f=1MHz)

| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| **Non-ECC** | | **M470T6554BG0** | | **M470T6553BG0** | | **M470T3354BG0** | | |
| Input capacitance, CK and $\overline{CK}$ | CCK0 | - | TBD | - | TBD | - | TBD | pF |
| | CCK1 | - | TBD | - | TBD | - | TBD | |
| Input capacitance, CKE and $\overline{CS}$ | $CI_1$ | - | TBD | - | TBD | - | TBD | |
| Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $CI_2$ | - | TBD | - | TBD | - | TBD | |
| Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$ | CIO | - | TBD | - | TBD | - | TBD | |
| **Non-ECC** | | **TBD** | | | | | | |
| Input capacitance, CK and $\overline{CK}$ | CCK0 | - | TBD | | | | | pF |
| | CCK1 | - | TBD | | | | | |
| | CCK2 | - | TBD | | | | | |
| Input capacitance, CKE and $\overline{CS}$ | $CI_1$ | - | TBD | | | | | |
| Input capacitance, Addr, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $CI_2$ | - | TBD | | | | | |
| Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$ | CIO | - | TBD | | | | | |

Note: DM is internally loaded to match DQ and DQS identically.

## IDD Specification Parameters Definition

**(IDD values are for full operating range of Voltage and Temperature)**

| Symbol | Proposed Conditions | | Units | Notes |
|---|---|---|---|---|
| IDD0 | **Operating one bank active-precharge current**; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD1 | **Operating one bank active-read-precharge current**; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC (IDD)}$, $t_{RAS} = t_{RASmin(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as IDD4W | | mA | |
| IDD2P | **Precharge power-down current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | | mA | |
| IDD2Q | **Precharge quiet standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING | | mA | |
| IDD2N | **Precharge standby current**; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD3P | **Active power-down current**; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING | Fast PDN Exit MRS(12) = 0mA | mA | |
| | | Slow PDN Exit MRS(12) = 1mA | mA | |
| IDD3N | **Active standby current**; All banks open; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD4W | **Operating burst write current**; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD4R | **Operating burst read current**; All banks open, Continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; $t_{CK} = t_{CK(IDD)}$, $t_{RAS} = t_{RASmax(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W | | mA | |
| IDD5B | **Burst auto refresh current**; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING | | mA | |
| IDD6 | **Self refresh current**; CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING | Normal | mA | |
| | | Low Power | mA | |
| IDD7 | **Operating bank interleave read current**; All bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = $t_{RCD(IDD)}$-1*$t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$, $t_{RCD} = 1*t_{CK(IDD)}$; CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions | | mA | |

## Operating Current Table(1-1) ($T_A$=0°C, VDD= 1.9V)

### M378T6553BG0 : 512MB(64Mx8 *8) Module

| Symbol | | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | TBD | TBD | TBD | mA | |
| IDD1 | | TBD | TBD | TBD | mA | |
| IDD2P | | TBD | TBD | TBD | mA | |
| IDD2Q | | TBD | TBD | TBD | mA | |
| IDD2N | | TBD | TBD | TBD | mA | |
| IDD3P | | TBD | TBD | TBD | mA | |
| IDD3N | | TBD | TBD | TBD | mA | |
| IDD4W | | TBD | TBD | TBD | mA | |
| IDD4R | | TBD | TBD | TBD | mA | |
| IDD5B | | TBD | TBD | TBD | mA | |
| IDD6 | Normal | TBD | TBD | TBD | mA | |
| | Low power | TBD | TBD | TBD | mA | Optional |
| IDD7 | | TBD | TBD | TBD | mA | |

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

### M378T2953BG0 : 1GB(64Mx8 *16) Module

| Symbol | | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | TBD | TBD | TBD | mA | |
| IDD1 | | TBD | TBD | TBD | mA | |
| IDD2P | | TBD | TBD | TBD | mA | |
| IDD2Q | | TBD | TBD | TBD | mA | |
| IDD2N | | TBD | TBD | TBD | mA | |
| IDD3P | | TBD | TBD | TBD | mA | |
| IDD3N | | TBD | TBD | TBD | mA | |
| IDD4W | | TBD | TBD | TBD | mA | |
| IDD4R | | TBD | TBD | TBD | mA | |
| IDD5B | | TBD | TBD | TBD | mA | |
| IDD6 | Normal | TBD | TBD | TBD | mA | |
| | Low power | TBD | TBD | TBD | mA | Optional |
| IDD7 | | TBD | TBD | TBD | mA | |

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## Operating Current Table(1-2) ($T_A$=0°C, VDD= 1.9V)

**M378T3354BG0 : 256MB(32Mx16 *4) Module**

| Symbol | | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | TBD | TBD | TBD | mA | |
| IDD1 | | TBD | TBD | TBD | mA | |
| IDD2P | | TBD | TBD | TBD | mA | |
| IDD2Q | | TBD | TBD | TBD | mA | |
| IDD2N | | TBD | TBD | TBD | mA | |
| IDD3P | | TBD | TBD | TBD | mA | |
| IDD3N | | TBD | TBD | TBD | mA | |
| IDD4W | | TBD | TBD | TBD | mA | |
| IDD4R | | TBD | TBD | TBD | mA | |
| IDD5B | | TBD | TBD | TBD | mA | |
| IDD6 | Normal | TBD | TBD | TBD | mA | |
| | Low power | TBD | TBD | TBD | mA | Optional |
| IDD7 | | TBD | TBD | TBD | mA | |

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

**M391T6553BG0 : 512MB(64Mx8 *9) ECC Module**

| Symbol | | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | TBD | TBD | TBD | mA | |
| IDD1 | | TBD | TBD | TBD | mA | |
| IDD2P | | TBD | TBD | TBD | mA | |
| IDD2Q | | TBD | TBD | TBD | mA | |
| IDD2N | | TBD | TBD | TBD | mA | |
| IDD3P | | TBD | TBD | TBD | mA | |
| IDD3N | | TBD | TBD | TBD | mA | |
| IDD4W | | TBD | TBD | TBD | mA | |
| IDD4R | | TBD | TBD | TBD | mA | |
| IDD5B | | TBD | TBD | TBD | mA | |
| IDD6 | Normal | TBD | TBD | TBD | mA | |
| | Low power | TBD | TBD | TBD | mA | Optional |
| IDD7 | | TBD | TBD | TBD | mA | |

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## Operating Current Table(1-3) ($T_A$=0°C, VDD= 1.9V)

**M391T2953BG0 : 1GB(64Mx8 *18) ECC Module**

| Symbol | | E6 (DDR2-667@CL=5) | D5 (DDR2-533@CL=4) | CC (DDR2-400@CL=3) | Unit | Notes |
|---|---|---|---|---|---|---|
| IDD0 | | TBD | TBD | TBD | mA | |
| IDD1 | | TBD | TBD | TBD | mA | |
| IDD2P | | TBD | TBD | TBD | mA | |
| IDD2Q | | TBD | TBD | TBD | mA | |
| IDD2N | | TBD | TBD | TBD | mA | |
| IDD3P | | TBD | TBD | TBD | mA | |
| IDD3N | | TBD | TBD | TBD | mA | |
| IDD4W | | TBD | TBD | TBD | mA | |
| IDD4R | | TBD | TBD | TBD | mA | |
| IDD5B | | TBD | TBD | TBD | mA | |
| IDD6 | Normal | TBD | TBD | TBD | mA | |
| | Low power | TBD | TBD | TBD | mA | Optional |
| IDD7 | | TBD | TBD | TBD | mA | |

* Module IDD was calculated on the basis of component IDD and can be differently measured according to DQ loading cap.

## Electrical Characteristics & AC Timing for DDR2-667/533/400

(0 °C ≤ $T_{CASE}$ ≤ 95 °C; $V_{DDQ}$ = 1.8V ± 0.1V; $V_{DD}$ = 1.8V ± 0.1V)

### Refresh Parameters by Device Density

| Parameter | Symbol | | 256Mb | 512Mb | 1Gb | 2Gb | 4Gb | Units |
|---|---|---|---|---|---|---|---|---|
| Refresh to active/Refresh command time | tRFC | | 75 | 105 | 127.5 | 195 | tbd | ns |
| Average periodic refresh interval | tREFI | 0 °C ≤ $T_{CASE}$ ≤ 85°C | 7.8 | 7.8 | 7.8 | 7.8 | 7.8 | µs |
| | | 85 °C < $T_{CASE}$ ≤ 95°C | 3.9 | 3.9 | 3.9 | 3.9 | 3.9 | µs |

### Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR2-667(E6) | | DDR2-533(D5) | | DDR2-400(CC) | | Units |
|---|---|---|---|---|---|---|---|
| Bin (CL - tRCD - tRP) | 5 - 5- 5 | | 4 - 4 - 4 | | 3 - 3 - 3 | | |
| Parameter | min | max | min | max | min | max | |
| tCK, CL=3 | 5 | 8 | 5 | 8 | 5 | 8 | ns |
| tCK, CL=4 | 3.75 | 8 | 3.75 | 8 | 5 | 8 | ns |
| tCK, CL=5 | 3 | 8 | - | - | - | - | ns |
| tRCD | 15 | | 15 | | 15 | | ns |
| tRP | 15 | | 15 | | 15 | | ns |
| tRC | 55 | | 55 | | 55 | | ns |
| tRAS | 40 | 70000 | 40 | 70000 | 40 | 70000 | ns |

### Timing Parameters by Speed Grade

(Refer to notes for informations related to this table at the bottom)

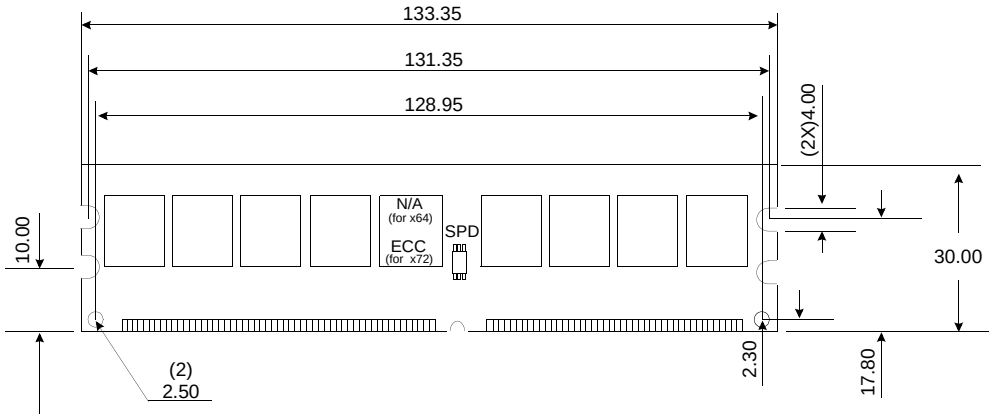
| Parameter | Symbol | DDR2-667 | | DDR2-533 | | DDR2-400 | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | min | max | min | max | min | max | | |
| DQ output access time from CK/$\overline{CK}$ | tAC | -450 | +450 | -500 | +500 | -600 | +600 | ps | |
| DQS output access time from CK/$\overline{CK}$ | tDQSCK | -400 | +400 | -450 | +450 | -500 | +500 | ps | |
| CK high-level width | tCH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK low-level width | tCL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | |
| CK half period | tHP | min(tCL, tCH) | x | min(tCL, tCH) | x | min(tCL, tCH) | x | ps | 19,20 |
| Clock cycle time, CL=x | tCK | 3000 | 8000 | 3750 | 8000 | 5000 | 8000 | ps | 23 |
| DQ and DM input hold time | tDH | tbd | x | 225 | x | 275 | x | ps | 14,15, 16 |
| DQ and DM input setup time | tDS | tbd | x | 100 | x | 150 | x | ps | 14,15, 16 |
| Control & Address input pulse width for each input | tIPW | 0.6 | x | 0.6 | x | 0.6 | x | tCK | |

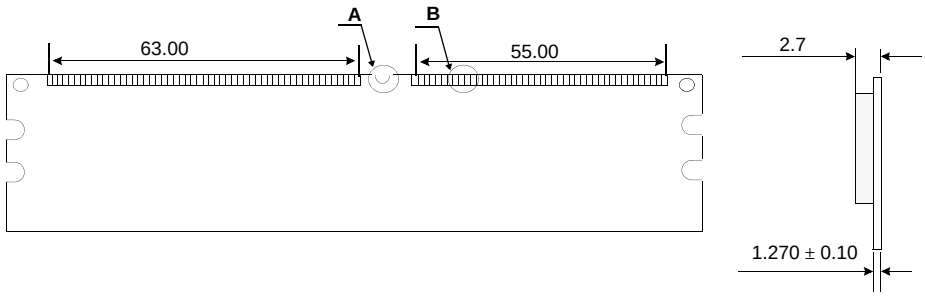
| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| DQ and DM input pulse width for each input | tDIPW | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| Data-out high-impedance time from CK/$\overline{CK}$ | tHZ | x | tAC max | x | tAC max | x | tAC max | ps | |
| Data-out low-impedance time from CK/$\overline{CK}$ | tLZ | tAC min | tAC max | tAC min | tAC max | tAC min | tAC max | ps | |
| DQS-DQ skew for DQS and associated DQ signals | tDQSQ | x | tbd | x | 300 | x | 350 | ps | 21 |
| DQ hold skew factor | tQHS | x | tbd | x | 400 | x | 450 | ps | 20 |
| DQ/DQS output hold time from DQS | tQH | tHP - tQHS | x | tHP - tQHS | x | tHP - tQHS | x | ps | |
| Write command to first DQS latching transition | tDQSS | WL - 0.25 | WL + 0.25 | WL - 0.25 | WL + 0.25 | WL - 0.25 | WL + 0.25 | tCK | |
| DQS input high pulse width | tDQSH | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| DQS input low pulse width | tDQSL | 0.35 | x | 0.35 | x | 0.35 | x | tCK | |
| DQS falling edge to CK setup time | tDSS | 0.2 | x | 0.2 | x | 0.2 | x | tCK | |
| DQS falling edge hold time from CK | tDSH | 0.2 | x | 0.2 | x | 0.2 | x | tCK | |
| Mode register set command cycle time | tMRD | 2 | x | 2 | x | 2 | x | tCK | |
| Write preamble setup time | tWPRES | 0 | x | 0 | x | 0 | x | ps | |
| Write postamble | tWPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | 18 |
| Write preamble | tWPRE | tbd | x | 0.4 | x | 0.4 | x | tCK | |
| Address and control input hold time | tIH | tbd | x | 375 | x | 475 | x | ps | 13,15, 17 |
| Address and control input setup time | tIS | tbd | x | 250 | x | 350 | x | ps | 13,15, 17 |
| Read preamble | tRPRE | 0.9 | 1.1 | 0.9 | 1.1 | 0.9 | 1.1 | tCK | |
| Read postamble | tRPST | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | tCK | |
| Active to active command period for 1KB page size products | tRRD | 7.5 | x | 7.5 | x | 7.5 | x | ns | 12 |
| Active to active command period for 2KB page size products | tRRD | 10 | x | 10 | x | 10 | x | ns | 12 |
| $\overline{CAS}$ to $\overline{CAS}$ command delay | tCCD | 2 | | 2 | | 2 | | tCK | |
| Write recovery time | tWR | 15 | x | 15 | x | 15 | x | ns | |
| Auto precharge write recovery + precharge time | tDAL | tWR+tRP* | x | tWR+tRP* | x | tWR+tRP* | x | tCK | 22 |
| Internal write to read command delay | tWTR | 7.5 | x | 7.5 | x | 10 | x | ns | |
| Internal read to precharge command delay | tRTP | 7.5 | | 7.5 | | 7.5 | | ns | 11 |
| Exit self refresh to a non-read command | tXSNR | tRFC + 10 | | tRFC + 10 | | tRFC + 10 | | ns | |

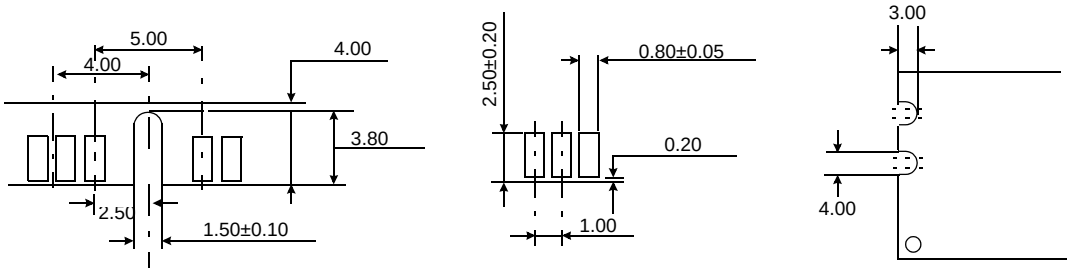
| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Exit self refresh to a read command | tXSRD | 200 | | 200 | | 200 | | tCK | |
| Exit precharge power down to any non-read command | tXP | 2 | x | 2 | x | 2 | x | tCK | |
| Exit active power down to read command | tXARD | 2 | x | 2 | x | 2 | x | tCK | 9 |
| Exit active power down to read command (Slow exit, Lower power) | tXARDS | 6 - AL | | 6 - AL | | 6 - AL | | tCK | 9, 10 |
| CKE minimum pulse width (high and low pulse width) | tCKE | 3 | | 3 | | 3 | | tCK | |
| ODT turn-on delay | tAOND | 2 | 2 | 2 | 2 | 2 | 2 | tCK | |
| ODT turn-on | tAON | tAC(min) | tAC(max) +0.7 | tAC(min) | tAC(max) +1 | tAC(min) | tAC(max) +1 | ns | 13, 24 |
| ODT turn-on(Power-Down mode) | tAONPD | tAC(min)+ 2 | 2tCK+tAC (max)+1 | tAC(min)+ 2 | 2tCK+tAC (max)+1 | tAC(min) +2 | 2tCK+tA C(max)+1 | ns | |
| ODT turn-off delay | tAOFD | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | 2.5 | tCK | |
| ODT turn-off | tAOF | tAC(min) | tAC(max) + 0.6 | tAC(min) | tAC(max)+ 0.6 | tAC(min) | tAC(max)+ 0.6 | ns | 25 |
| ODT turn-off (Power-Down mode) | tAOFPD | tAC(min)+ 2 | 2.5tCK+tA C(max)+1 | tAC(min)+ 2 | 2.5tCK+ tAC(max) +1 | tAC(min) +2 | 2.5tCK+ tAC(max) +1 | ns | |
| ODT to power down entry latency | tANPD | 3 | | 3 | | 3 | | tCK | |
| ODT power down exit latency | tAXPD | 8 | | 8 | | 8 | | tCK | |
| OCD drive mode output delay | tOIT | 0 | 12 | 0 | 12 | 0 | 12 | ns | |
| Minimum time clocks remains ON after CKE asynchronously drops LOW | tDelay | tIS+tCK+tI H | | tIS+tCK+tI H | | tIS+tCK+t IH | | ns | 23 |

## Physical Dimensions: 64Mbx8 based 64Mx64/x72 Module(1 Rank)
## (M378/91T6553BG0)

Units : Millimeters



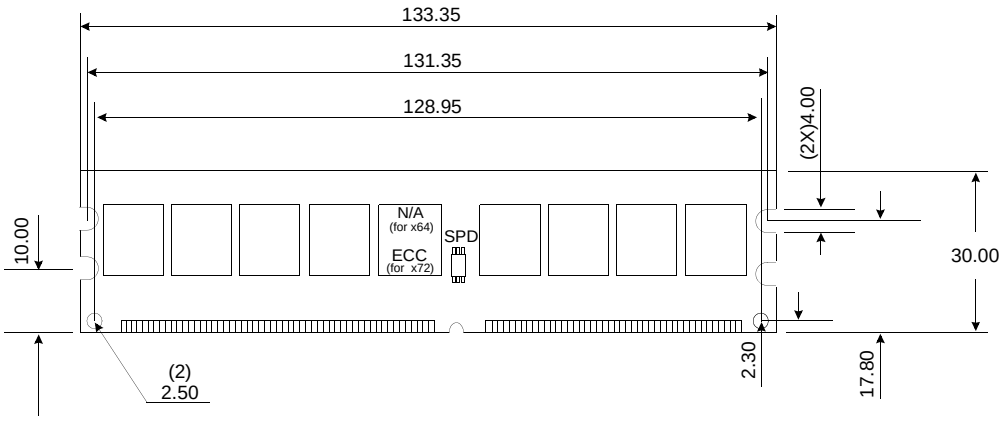



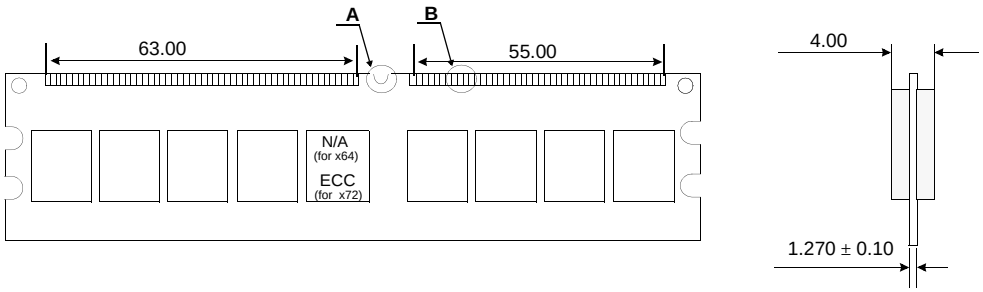

**Detail A** **Detail B**

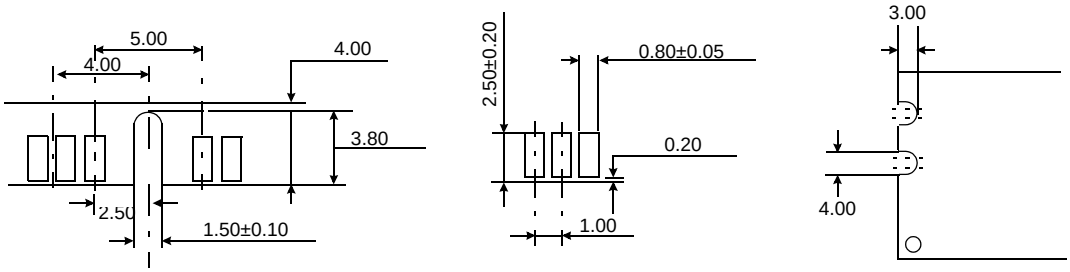
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QB-GC/L##.

## Physical Dimensions: 64Mbx8 based 128Mx64/x72 Module(2 Ranks) (M378/91T2953BG0)

Units : Millimeters



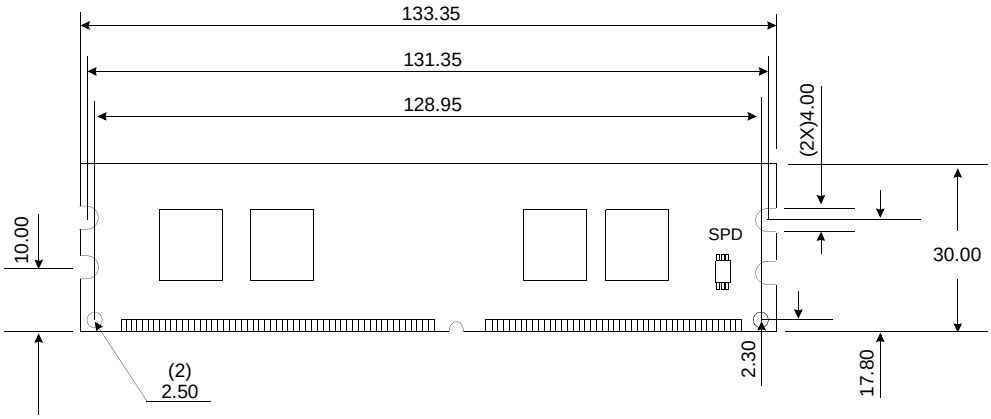



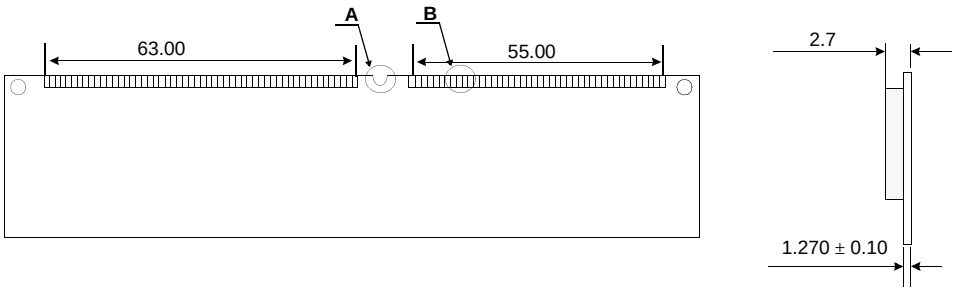

**Detail A** **Detail B**

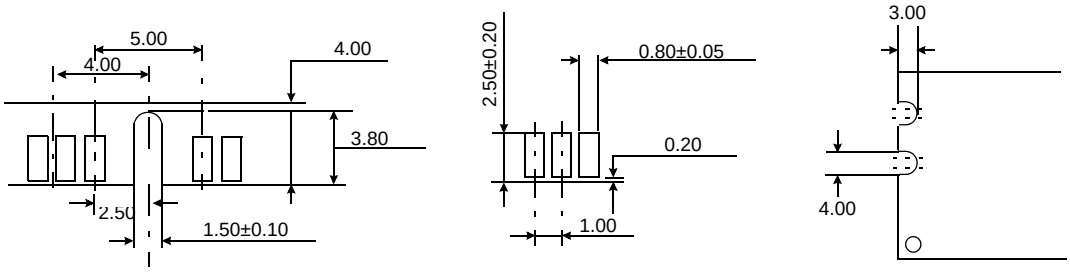
The used device is 64M x8 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51083QB-GC/L##.

## Physical Dimensions: 32Mbx16 based 32Mx64/x72 Module(1 Rank) (M378T3354BG0)

Units : Millimeters




**Detail A** **Detail B**

The used device is 32M x16 DDR2 SDRAM, FBGA.
DDR2 SDRAM Part NO : K4T51163QB-GC/L##.