32-Channel AC Plasma Display Driver

Ordering Information

Device	Package Options						
	40-Pin Ceramic DIP	40-Pin Plastic DIP	44-Pin J-Lead Ceramic Chip Carrier	44-Pin J-Lead Plastic Chip Carrier	Die	40-Pin Ceramic Dip (MIL-STD-883 Processed*)	44-Pin J-Lead Ceramic Chip Carrier (MIL-STD-883 Processed*)
HV500	HV500D	HV500P	HV500DJ	HV500PJ	HV500X	RBHV500D	RBHV500DJ

* For Hi-Rel process flows, refer to page 5-3 of the Databook.

Features

- Processed with HVCMOS® Technology
- Output voltage of up to 100V
- CMOS push-pull output buffers
- Low-power level shifting
- Source/sink current minimum of 15mA
- Shift register speed 8MHz
- CMOS compatible inputs
- Output clamp diodes to V_{PP} and GND
- Direct replacement for the SN75500 and SN55500 series devices
- 44-lead plastic and ceramic surface mount packages available
- Hi-Rel processing available

General Description

The HV500 is a monolithic low-voltage logic to high-voltage output 32-channel driver for AC plasma flat panel displays. It is manufactured using the HVCMOS process, providing the high output voltages and currents possible with DMOS structures and the low power dissipation of CMOS logic.

The HV500 is comprised of an 8-stage DMOS shift register, four groups of eight high-voltage output buffers, and logic to select which group of outputs will reflect the status of the data in the shift register and strobe functions. When the strobe input is high, all outputs are held low independent of any other logic input. When strobe is brought low, the group of outputs selected by the state of the select inputs reflects the data in the shift register, and all non-selected outputs are held low.

The high-voltage output buffers have level shifters which dissipate no DC power. These level shifters also control the rise and fall times of the outputs which have been optimized to lower system noise without compromising the current source and sink capability of the output buffers. Additionally, each output has low V_{fwd} clamp diodes to V_{PP} and GND.

Absolute Maximum Ratings

Supply voltage, V_{DD}[1]		-0.3V to +15V
Supply voltage, V_{PP}[1]		-0.3V to +100V
Logic input levels[1]		-0.3V to V_{DD} + 0.3V
Ground currrent[2]		1.2A[3]
Continuous total power dissipation[4]	Ceramic	1850mW
	Plastic	1200mW
Operating temperature range	Commercial	-40°C to +85°C
	Military	-55°C to 125°C
Storage temperature range		-65°C to +150°C

Notes:
1. All voltages are referenced to GND.
2. Duty cycle is limited by the total power dissipated in the package.
3. Consult factory for availability of 8.0A ground current version.
4. For operation above 25°C case temperature, derate linearly to 70°C at 15mW/°C.

Electrical Characteristics (over recommended operating conditions unless noted)

DC Characteristics

Symbol	Parameter		Min	Max	Units	Conditions
I_{DD}	V_{DD} quiescent supply current			1	mA	
I_{PP}	V_{PP} quiescent supply current			1	mA	HV_{out} H or L
I_{IH}	High-level input current			1	µA	$V_{IN} = V_{DD}$
I_{IL}	Low-level input current			-1	µA	$V_{IN} = V_{SS}$
V_{OH}	High-level output voltage	HV outputs	94		V	I_{OH} = -1mA[1]
			90		V	I_{OH} = -15mA[1]
		Serial out	9		V	I_{OH} = -100µA[2]
V_{OL}	Low-level output voltage	HV outputs		2	V	I_{OL} = 1mA
				5	V	I_{OL} = 15mA
		Serial out		1	V	I_{OL} = 100µA[2]
V_{OK}	High voltage output			2.5	V	I_{OK} = 20mA[3]
	Clamp voltage			-2.5	V	I_{OK} = -20mA[3]

Notes:
1. V_{PP} = 100V
2. V_{DD} = 10.8V
3. V_{PP} = 0V

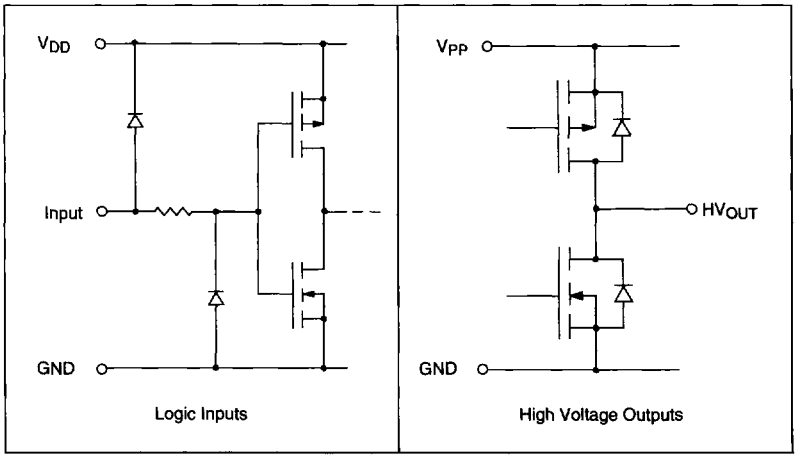
AC Characteristics (V_{DD} = 12V, V_{PP} = 100V, T_C = 25°C)

Symbol	Parameter		Min	Max	Units	Conditions
f_{MAX}	Maximum clock frequency			8	MHz	
t_W	Clock pulse width high or low		62		ns	
t_{DHL}	Delay time strobe to HV_{out} high to low			250	ns	C_L = 30pF
t_{DLH}	Delay time strobe to HV_{out} low to high			250	ns	C_L = 30pF
t_{SU}	Set-up time	Data in to clock ↑	20		ns	
		Select before strobe ↓	50		ns	
t_H	Hold time	Data after clock ↑	50		ns	
		Strobe high after clock ↑	50		ns	
		Select after strobe ↑	50		ns	
t_R	Rise time low to high HV_{out}			300	ns	C_L = 30pF
t_F	Fall time high to low HV_{out}			200	ns	C_L = 30pF

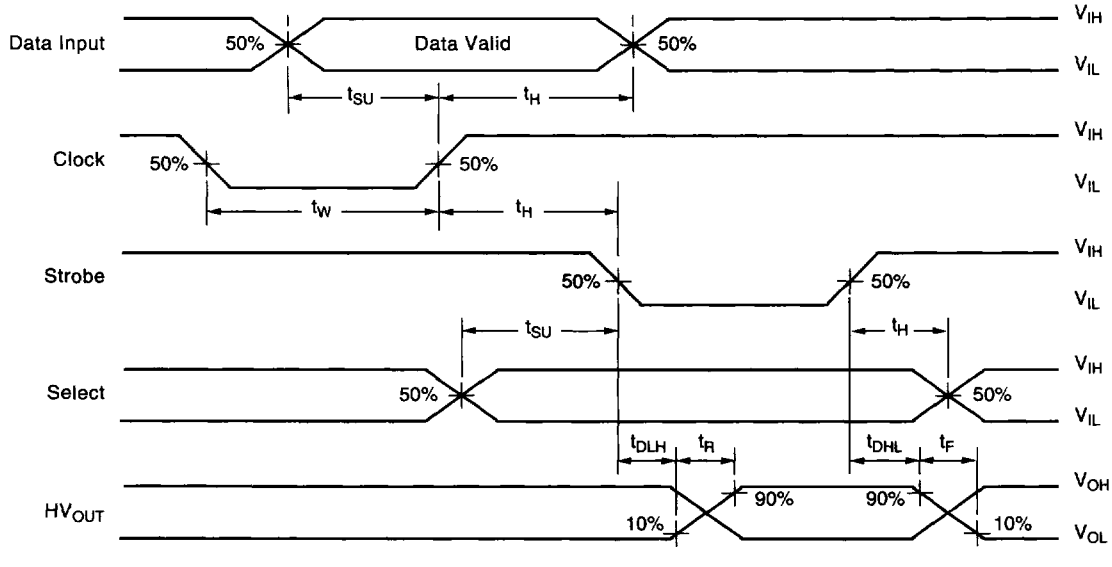
Recommended Operating Conditions

Symbol	Parameter		Min	Max	Units
V_{DD}	Logic supply voltage		10.8	13.2	V
V_{PP}	High voltage supply		0	100	V
V_{IH}	High-level input voltage		0.75 V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage		GND	0.25 V_{DD}	V
T_A	Operating free-air temperature	Commercial	-40	+85	°C
		Military Hi-Rel (RB)	-55	+125	°C

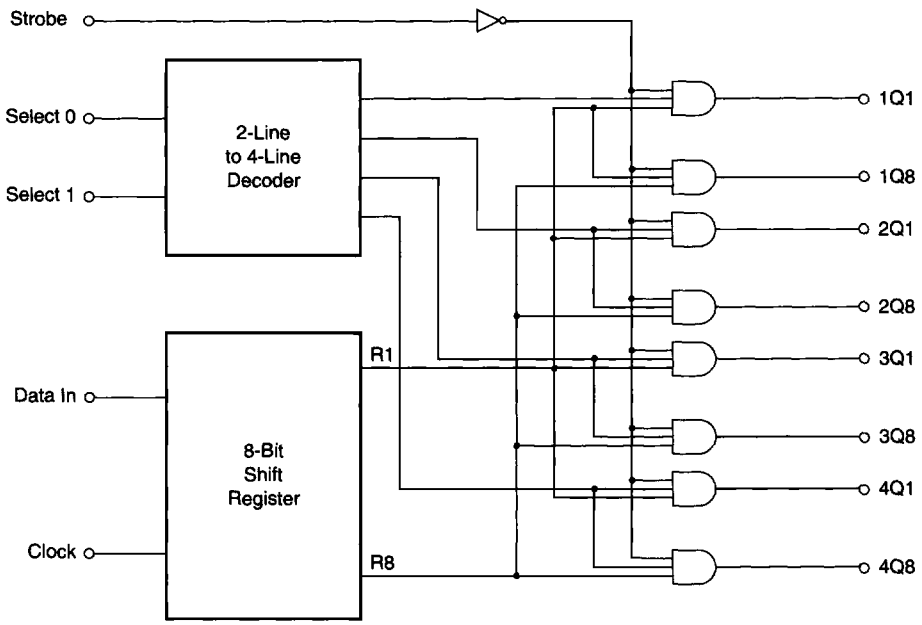
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Table

Function	Inputs					Internal Levels			HV Outputs			
			Select			Shift Register						
	Data	Clk	S1	S0	Strb	R1	R2	R3...R8	1Q1...1Q8	2Q1...2Q8	3Q1...3Q8	4Q1...4Q8
Load	H	↑	X	X	H	L	R1n	R2nºR7n	LºL	LºL	LºL	LºL
	L	↑	X	X	H	H	R1n	R2nºR7n	LºL	LºL	LºL	LºL
Strobe	X	X	X	X	H	R1n	R2n	R3nºR8n	LºL	LºL	LºL	LºL
	X	H	L	L	L	R1n	R2n	R3nºR8n	R1ºR8	LºL	LºL	LºL
	X	H	L	H	L	R1n	R2n	R3nºR8n	LºL	R1ºR8	LºL	LºL
	X	H	H	L	L	R1n	R2n	R3nºR8n	LºL	LºL	R1ºR8	LºL
	X	H	H	H	L	R1n	R2n	R3nºR8n	LºL	LºL	LºL	R1ºR8

Notes:
H = high level, L = low level, X = irrelevant, ↑ = low-to-high transition.
R1ºR8 = levels currently at internal outputs of shift registers one through eight, respectively.
R1nºR8n = levels at shift-register outputs R1 through R8, respectively, before the most recent ↑ transition of the clock.

Pin Configurations

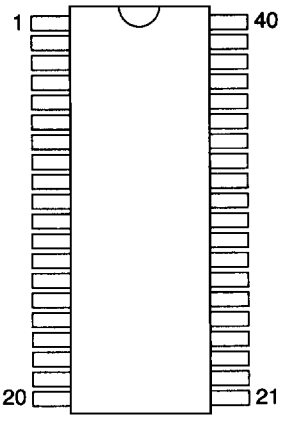
40-Pin Dual-In-Line

Pin	Function	Pin	Function
1	Select 0	21	V_{PP}
2	Data In	22	3Q8
3	Clock	23	3Q7
4	1Q1	24	3Q6
5	1Q2	25	3Q5
6	1Q3	26	3Q4
7	1Q4	27	3Q3
8	1Q5	28	3Q2
9	1Q6	29	3Q1
10	1Q7	30	4Q8
11	1Q8	31	4Q7
12	2Q1	32	4Q6
13	2Q2	33	4Q5
14	2Q3	34	4Q4
15	2Q4	35	4Q3
16	2Q5	36	4Q2
17	2Q6	37	4Q1
18	2Q7	38	Strobe
19	2Q8	39	Select 1
20	GND	40	V_{DD}

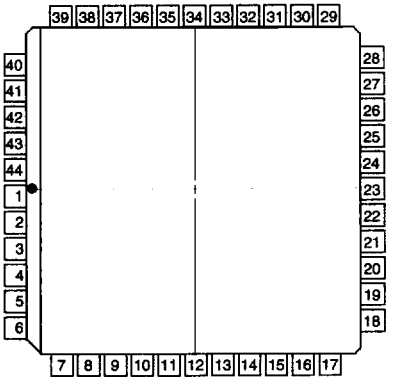
44 Pin J-Lead

Pin	Function	Pin	Function
1	N/C	23	N/C
2	Select 0	24	V_{PP}
3	Data In	25	3Q8
4	Clock	26	3Q7
5	N/C	27	3Q6
6	1Q1	28	3Q5
7	1Q2	29	3Q4
8	1Q3	30	3Q3
9	1Q4	31	3Q2
10	1Q5	32	3Q1
11	1Q6	33	4Q8
12	1Q7	34	4Q7
13	1Q8	35	4Q6
14	2Q1	36	4Q5
15	2Q2	37	4Q4
16	2Q3	38	4Q3
17	2Q4	39	4Q2
18	2Q5	40	4Q1
19	2Q6	41	N/C
20	2Q7	42	Strobe
21	2Q8	43	Select 1
22	GND	44	V_{DD}

Package Outlines



top view
40-pin DIP



top view
44-pin J-Lead Package