



256K x 16 Static RAM

Features

- Low voltage range:
 - CY62146CV25: 2.2V–2.7V
 - CY62146CV30: 2.7V–3.3V
 - CY62146CV33: 3.0V–3.6V
- Ultra-low active, standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- TTL-compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed/power

Functional Description

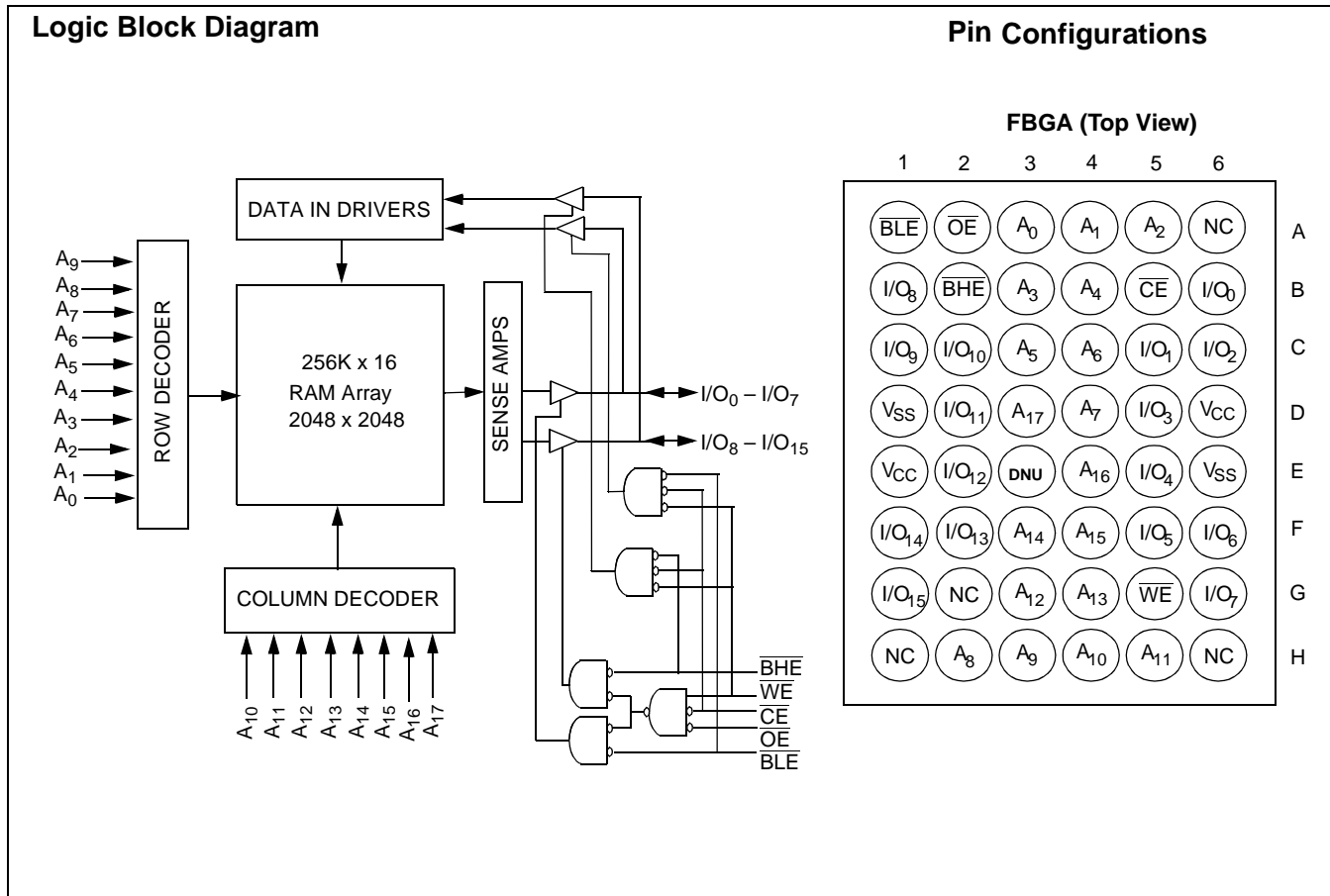
The CY62146CV25/30/33 are high-performance CMOS static RAMs organized as 262,144 words by 16 bits. These devices feature advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL™) in portable applications such as cellular telephones. The devices also have an automatic power-down feature that significantly reduces power consumption by 80% when addresses are not toggling. The device can also be put into standby mode when deselected (\overline{CE} HIGH). The input/output pins (I/O₀

through I/O₁₅) are placed in a high-impedance state when: deselected (\overline{CE} HIGH), outputs are disabled (\overline{OE} HIGH), \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₇). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₇).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O₀ to I/O₇. If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O₈ to I/O₁₅. See the truth table at the back of this data sheet for a complete description of read and write modes.

The CY62146CV25/30/33 are available in a 48-ball FBGA package. DNU on ball E3 is a “Do Not Use” pin, connecting to Vss will not affect performance.



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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied -55°C to +125°C

Supply Voltage to Ground Potential -0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State^[1] -0.5V to V_{CC} + 0.5V

DC Input Voltage^[1] -0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage >2100V (per MIL-STD-883, Method 3015)

Latch-Up Current >200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC}
CY62146CV25	Industrial	-40°C to +85°C	2.2V to 2.7V
CY62146CV30			2.7V to 3.3V
CY62146CV33			3.0V to 3.6V

Product Portfolio

Product	V _{CC} Range			Power	Power Dissipation (Industrial)			
	V _{CC(min.)}	V _{CC(typ.)} ^[2]	V _{CC(max.)}		Operating (I _{CC})		Standby (I _{SB2})	
					Typ. ^[2]	Maximum	Typ. ^[2]	Maximum
CY62146CV25	2.2V	2.5V	2.7V	LL	7 mA	15 mA	5 μA	20 μA
CY62146CV30	2.7V	3.0V	3.3V	LL	7 mA	15 mA	7 μA	20 μA
CY62146CV33	3.0V	3.3V	3.6V	LL	7 mA	15 mA	8 μA	20 μA

Notes:

- V_{L(min.)} = -2.0V for pulse durations less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ.)}, T_A = 25°C

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62146CV25			Unit
				Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -0.1 mA	V _{CC} = min.	2.0			V
V _{OL}	Output LOW Voltage	I _{OL} = 0.1 mA	V _{CC} = min.			0.4	V
V _{IH}	Input HIGH Voltage			1.8		V _{CC} + 0.3V	V
V _{IL}	Input LOW Voltage			-0.5		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels	V _{CC} = max.		7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0,$ V _{CC} = max.	LL		5	20	μA

Parameter	Description	Test Conditions		CY62146CV30			Unit
				Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = min.	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = min.			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage			-0.3		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels	V _{CC} = max.		7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0,$ V _{CC} = max.	LL		7	20	μA

Parameter	Description	Test Conditions		CY62146CV33			Unit
				Min.	Typ. ^[2]	Max.	
V _{OH}	Output HIGH Voltage	I _{OH} = -1.0 mA	V _{CC} = min.	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA	V _{CC} = min.			0.4	V
V _{IH}	Input HIGH Voltage			2.2		V _{CC} + 0.5V	V
V _{IL}	Input LOW Voltage			-0.3		0.8	V
I _{IX}	Input Load Current	GND ≤ V _I ≤ V _{CC}		-1	±1	+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _O ≤ V _{CC} , Output Disabled		-1	+1	+1	μA
I _{CC}	V _{CC} Operating Supply Current	I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC} , CMOS Levels	V _{CC} = max.		7	15	mA
		I _{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I _{SB2}	Automatic CE Power-Down Current—CMOS Inputs	$\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V, f = 0,$ V _{CC} = max.	LL		8	20	μA

Capacitance³

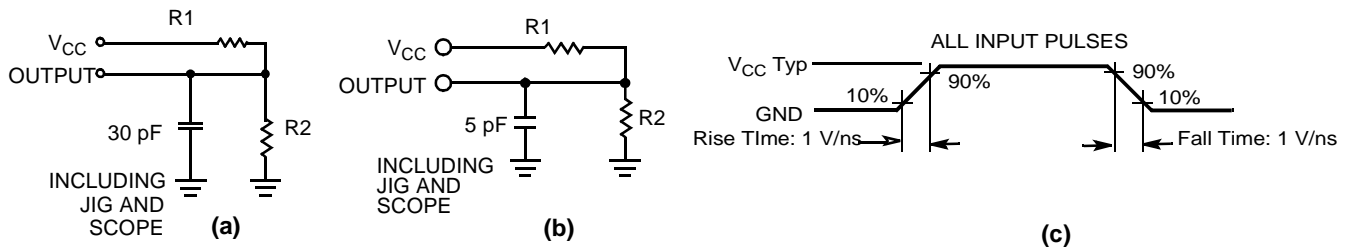
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = V _{CC} (typ.)	6	pF
C _{OUT}	Output Capacitance		8	pF

Thermal Resistance

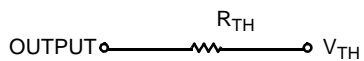
Description	Test Conditions	Symbol	BGA	Unit
Thermal Resistance (Junction to Ambient) ^[3]	Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ _{JA}	55	°C/W
Thermal Resistance (Junction to Case) ^[3]		θ _{JC}	16	°C/W

Note:

3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms


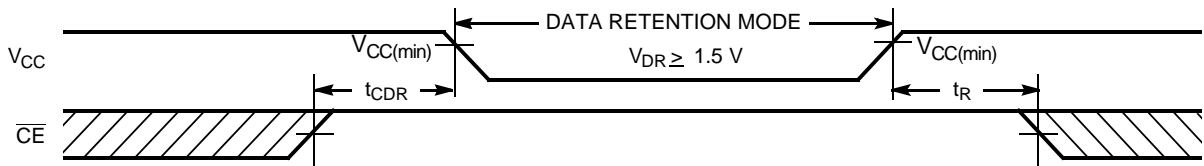
Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.5V	3.0V	3.3V	Unit
R1	16.6	1.105	1.105	KΩ
R2	15.4	1.550	1.550	KΩ
R _{TH}	8	0.645	0.645	KΩ
V _{TH}	1.20V	1.75V	1.75V	V

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions	Min.	Typ. ^[2]	Max.	Unit
V _{DR}	V _{CC} for Data Retention		1.5		2.7	V
I _{CCDR}	Data Retention Current	V _{CC} = 1.5V CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V or V _{IN} ≤ 0.3V No input may exceed V _{CC} + 0.3V	LL	3	10	μA
t _{CDR} ^[3]	Chip Deselect to Data Retention Time		0			ns
t _R ^[4]	Operation Recovery Time		70			ns

Data Retention Waveform

Note:

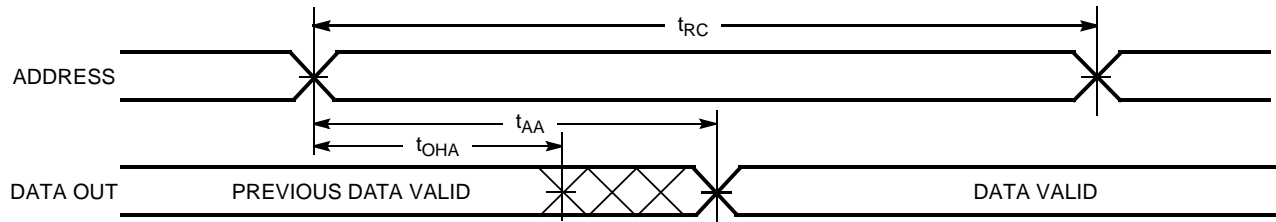
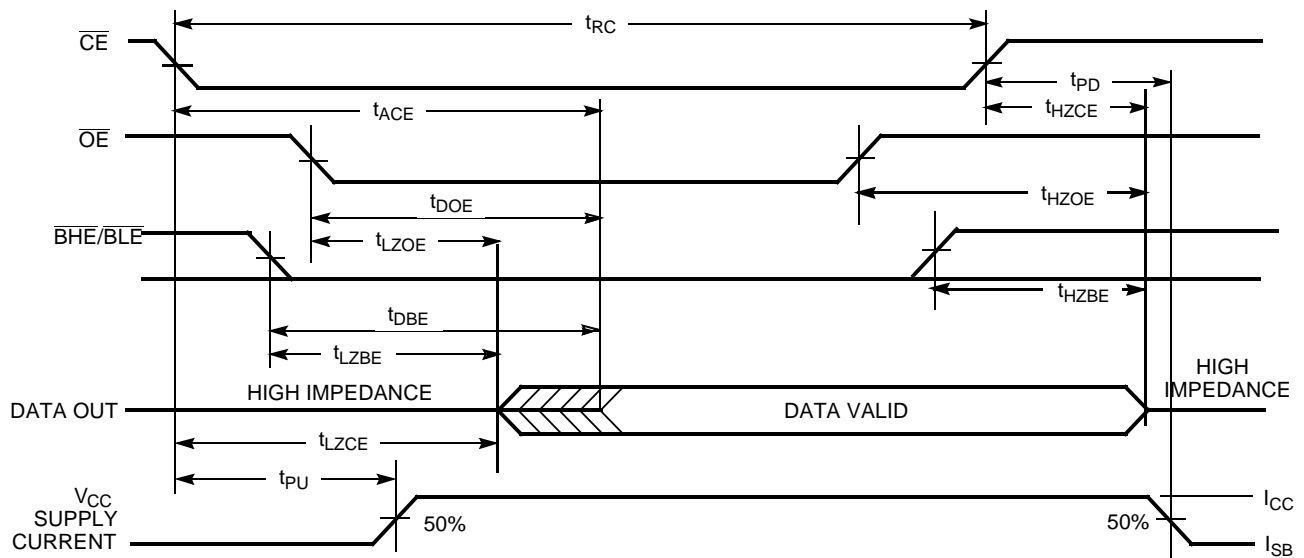
- Full Device AC operation requires linear V_{CC} ramp from V_{DR} to V_{CC(min.)} > 50 μs or stable at V_{CC(min.)} > 50 μs.

Switching Characteristics Over the Operating Range^[5]

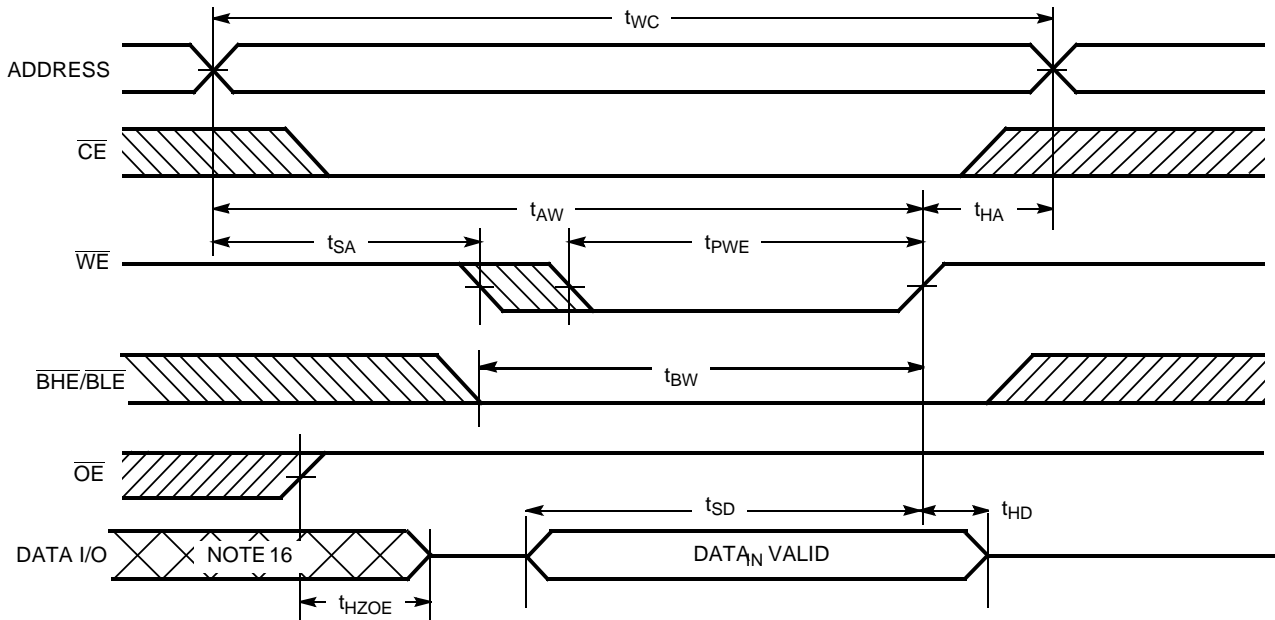
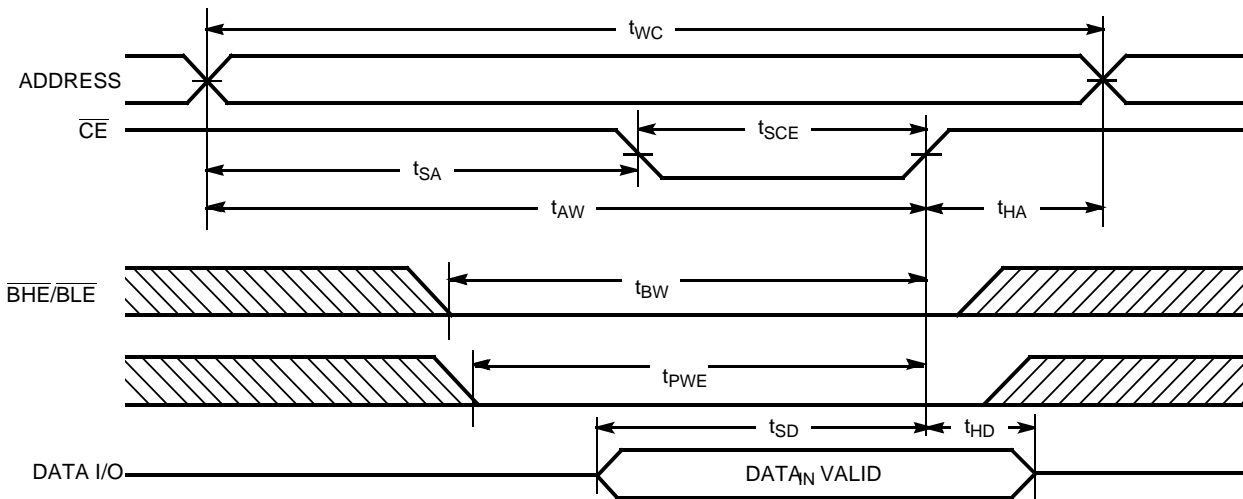
Parameter	Description	Min.	Max.	Unit
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6, 7]	5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[7]		25	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t_{PU}	\overline{CE} LOW to Power-Up	0		ns
t_{PD}	\overline{CE} HIGH to Power-Down		70	ns
t_{DBE}	$\overline{BHE} / \overline{BLE}$ LOW to Data Valid		70	ns
t_{LZBE} ^[8]	$\overline{BHE} / \overline{BLE}$ LOW to Low Z	5		ns
t_{HZBE}	$\overline{BHE} / \overline{BLE}$ HIGH to High Z		25	ns
WRITE CYCLE ^[9, 10]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	\overline{CE} LOW to Write End	60		ns
t_{AW}	Address Set-Up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-Up to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	50		ns
t_{BW}	$\overline{BHE} / \overline{BLE}$ Pulse Width	60		ns
t_{SD}	Data Set-Up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	10		ns

Notes:

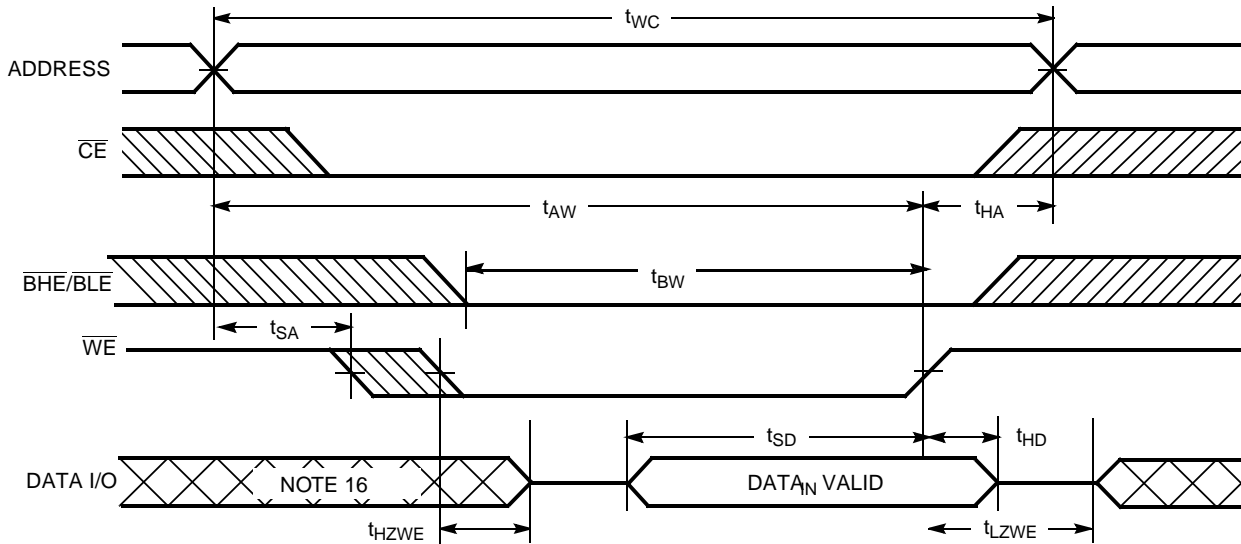
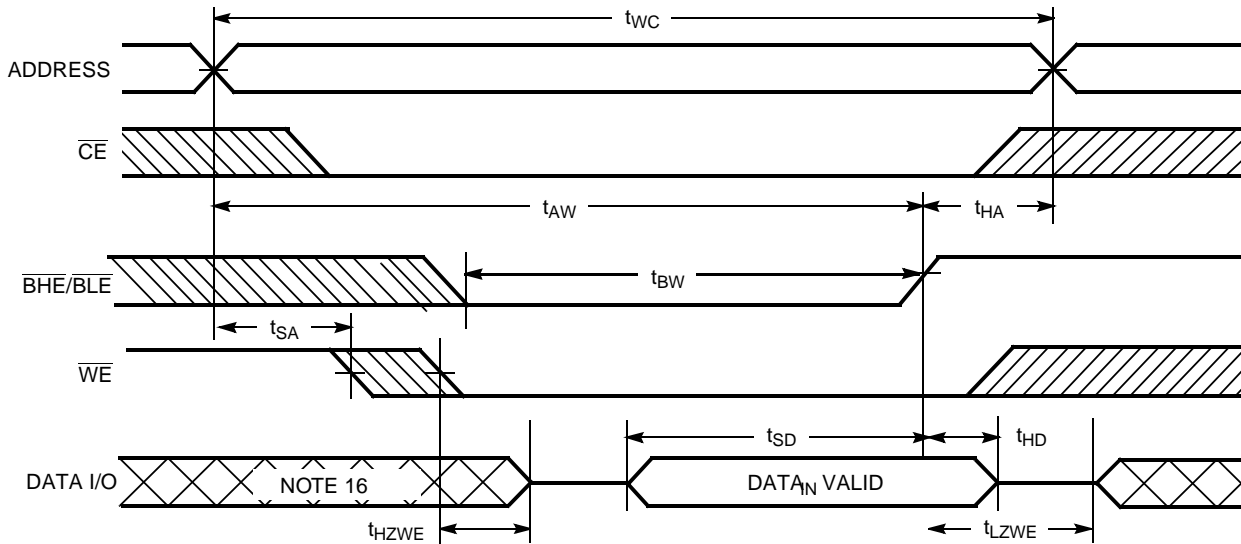
- Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with $C_L = 5$ pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- If both byte enables are toggled together this value is 10ns
- The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle #3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD} .

Switching Waveforms
Read Cycle No. 1 ^[11, 12]

Read Cycle No. 2 ^[12, 13]

Notes:

11. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
12. \overline{WE} is HIGH for read cycle.
13. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled) [9, 14, 15]

Write Cycle No. 2 (\overline{CE} Controlled) [8, 14, 15]

Notes:

14. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
15. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high-impedance state.
16. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)
Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[10, 15]

Write Cycle No. 4 (BHE/BL \overline{E} Controlled, \overline{OE} LOW)^[16]


Truth Table

CE	WE	OE	BHE	BLE	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-Down	Standby (I_{SB})
L	H	L	L	L	Data Out (I/O ₀ –I/O ₁₅)	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data Out (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	H	L	High Z	Deselect/Output Disabled	Active (I_{CC})
L	H	H	L	H	High Z	Deselect/Output Disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O ₀ –I/O ₁₅)	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O ₀ –I/O ₇); I/O ₈ –I/O ₁₅ in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data In (I/O ₈ –I/O ₁₅); I/O ₀ –I/O ₇ in High Z	Write	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62146CV25LL-70BAI	BA49	48-Ball Fine Pitch BGA	Industrial
	CY62146CV30LL-70BAI			
	CY62146CV33LL-70BAI			

Document #: 38-01124-**

Package Diagrams
48-Ball (7.00 mm x 7.00 mm) FBGA BA48
