Platform Flash In-System Programmable Configuration PROMs

DS123 (v2.1) November 18, 2003

Preliminary Product Specification

Features

- In-System Programmable PROMs for Configuration of Xilinx FPGAs
- Low-Power Advanced CMOS FLASH Process
- Endurance of 20,000 Program/Erase Cycles
- Operation over Full Industrial Temperature Range (–40°C to +85°C)
- Available in small footprint packages: VO20, VO48, and FS48
- IEEE Standard 1149.1/1532 Boundary-Scan (JTAG) Support for Programming, Prototyping, and Testing
- JTAG Command Initiation of Standard FPGA Configuration
- Cascadable for Storing Longer or Multiple Bitstreams
- Dedicated Boundary-Scan (JTAG) I/O Power Supply (V_{CCJ})
- I/O Pins Compatible with Voltage Levels Ranging From 1.5V to 3.3V
- Design Support Using the Xilinx Alliance ISE and Foundation ISE Series Software Packages
- XCF01S/XCF02S/XCF04S
  - 3.3V supply voltage
  - Serial FPGA configuration interface
- XCF08P/XCF16P/XCF32P
  - 1.8V supply voltage
  - Serial or parallel FPGA configuration interface
  - Design revision technology enables storing and accessing multiple design revisions for configuration
  - Built-in data decompressor compatible with Xilinx advanced compression technology

Table 1: **Platform Flash PROM Features**

	Density	V_{CCINT}	V_{CCO} / V_{CCJ} Range	Packages	JTAG ISP Programming	Serial Configuration	Parallel Configuration	Design Revisioning	Compression
XCF01S	1 Mbit	3.3V	1.8V - 3.3V	VO20	√	√			
XCF02S	2 Mbit	3.3V	1.8V - 3.3V	VO20	√	√			
XCF04S	4 Mbit	3.3V	1.8V - 3.3V	VO20	√	√			
XCF08P	8 Mbit	1.8V	1.5V - 3.3V	VO48 FS48	√	√	√	√	√
XCF16P	16 Mbit	1.8V	1.5V - 3.3V	VO48 FS48	√	√	√	√	√
XCF32P	32 Mbit	1.8V	1.5V - 3.3V	VO48 FS48	√	√	√	√	√

Description

Xilinx introduces the Platform Flash series of in-system programmable configuration PROMs. Available in 1 to 32 Megabit (Mbit) densities, these PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams. The Platform Flash PROM series includes both the 3.3V XCFxxS PROM and the 1.8V XCFxxP PROM. The XCFxxS version includes 4-Mbit, 2-Mbit, and 1-Mbit PROMs that support Master Serial and Slave Serial FPGA configuration modes (Figure 1). The XCFxxP version includes 32-Mbit, 16-Mbit, and 8-Mbit PROMs that support Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP FPGA configuration modes (Figure 2). A summary of the Platform Flash PROM family members and supported features is shown in Table 1.

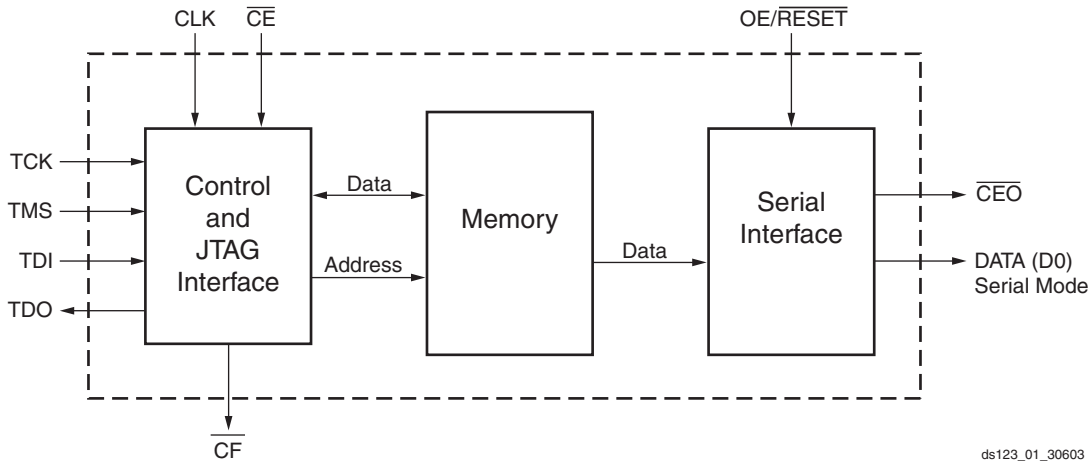


Figure 1: **XCFxxS Platform Flash Block Diagram**

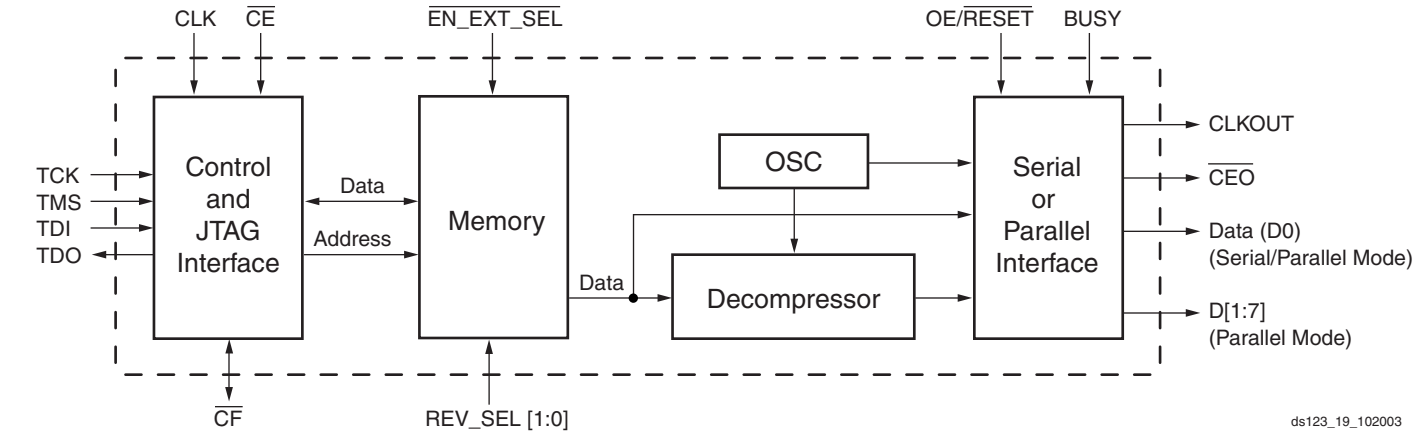


Figure 2: **XCFxxP Platform Flash Block Diagram**

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after $\overline{CE}$ and OE are enabled, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. New data is available a short access time after each rising clock edge. The FPGA generates the appropriate number of clock pulses to complete the configuration.

When the FPGA is in Slave Serial mode, the PROM and the FPGA are both clocked by an external clock source, or optionally, for the XCFxxP PROM only, the PROM can be used to drive the FPGAs configuration clock.

The XCFxxP version of the Platform Flash PROM also supports Master SelectMAP and Slave SelectMAP (or Slave Parallel) FPGA configuration modes. When the FPGA is in Master SelectMAP mode, the FPGA generates a configuration clock that drives the PROM. When the FPGA is in Slave SelectMAP Mode, either an external oscillator generates the configuration clock that drives the PROM and the FPGA, or optionally, the XCFxxP PROM can be used to drive the FPGAs configuration clock. After $\overline{CE}$ and OE are enabled, data is available on the PROMs DATA (D0-D7) pins. New data is available a short access time after each rising clock edge. The data is clocked into the FPGA on the following rising edge of the CCLK. A free-running oscillator can be used in the Slave Parallel /Slave SelecMAP mode.

The XCFxxP version of the Platform Flash PROM provides additional advanced features. A built-in data decompressor supports utilizing compressed PROM files, and design revisioning allows multiple design revisions to be stored on a single PROM or stored across several PROMs. For design revisioning, external pins or internal Control bits are used to select the active design revision.

Multiple Platform Flash PROM devices can be cascaded to support the larger configuration files required when targeting larger FPGA devices or targeting multiple FPGAs daisy chained together. When utilizing the advanced features for the XCFxxP Platform Flash PROM, such as design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced XCFxxP features are not enabled, then the cascaded chain can include both XCFxxP and XCFxxS PROMs.

The Platform Flash PROMs are compatible with all of the existing FPGA device families. A reference list of Xilinx FPGAs and the respective compatible Platform Flash PROMs is given in Table 2. A list of Platform Flash PROMs and their capacities is given in Table 3.

Table 2: **Xilinx FPGAs and Compatible Platform Flash PROMs**

FPGA	Configuration Bitstream	Platform Flash PROM(1)
Virtex-II Pro		
XC2VP2	1,305,440	XCF02S
XC2VP4	3,006,560	XCF04S
XC2VP7	4,485,472	XCF08P
XC2VP20	8,214,624	XCF08P
XC2VP30	11,589,984	XCF16P
XC2VP40	15,868,256	XCF16P
XC2VP50	19,021,408	XCF32P
XC2VP70	26,099,040	XCF32P
XC2VP100	34,292,832	XCF32P(2)
XC2VP125	43,602,784	XCF32P(2)
Virtex-II		
XC2V40	360,096	XCF01S
XC2V80	635,296	XCF01S
XC2V250	1,697,184	XCF02S
XC2V500	2,761,888	XCF04S
XC2V1000	4,082,592	XCF04S
XC2V1500	5,659,296	XCF08P
XC2V2000	7,492,000	XCF08P
XC2V3000	10,494,368	XCF16P
XC2V4000	15,659,936	XCF16P
XC2V6000	21,849,504	XCF32P
XC2V8000	29,063,072	XCF32P
Virtex-E		
XCV50E	630,048	XCF01S
XCV100E	863,840	XCF01S
XCV200E	1,442,016	XCF02S
XCV300E	1,875,648	XCF02S
XCV400E	2,693,440	XCF04S
XCV405E	3,430,400	XCF04S
XCV600E	3,961,632	XCF04S
XCV812E	6,519,648	XCF08P
XCV1000E	6,587,520	XCF08P
XCV1600E	8,308,992	XCF08P
XCV2000E	10,159,648	XCF16P
XCV2600E	12,922,336	XCF16P
XCV3200E	16,283,712	XCF16P

Table 2: **Xilinx FPGAs and Compatible Platform Flash PROMs *(Continued)***

FPGA	Configuration Bitstream	Platform Flash PROM(1)
Virtex		
XCV50	559,200	XCF01S
XCV100	781,216	XCF01S
XCV150	1,040,096	XCF01S
XCV200	1,335,840	XCF02S
XCV300	1,751,808	XCF02S
XCV400	2,546,048	XCF04S
XCV600	3,607,968	XCF04S
XCV800	4,715,616	XCF08P
XCV1000	6,127,744	XCF08P
Spartan-3		
XC3S50	439,264	XCF01S
XC3S200	1,047,616	XCF01S
XC3S400	1,699,136	XCF02S
XC3S1000	3,223,488	XCF04S
XC3S1500	5,214,784	XCF08P
XC3S2000	7,673,024	XCF08P
XC3S4000	11,316,864	XCF16P
XC3S5000	13,271,936	XCF16P
Spartan-IIE		
XC2S50E	630,048	XCF01S
XC2S100E	863,840	XCF01S
XC2S150E	1,134,496	XCF02S
XC2S200E	1,442,016	XCF02S
XC2S300E	1,875,648	XCF02S
XC2S400E	2,693,440	XCF04S
XC2S600E	3,961,632	XCF04S
Spartan-II		
XC2S15	197,696	XCF01S
XC2S30	336,768	XCF01S
XC2S50	559,200	XCF01S
XC2S100	781,216	XCF01S
XC2S150	1,040,096	XCF01S
XC2S200	1,335,840	XCF02S

Notes:
1. If design revisioning or other advanced feature support is required, the XCFxxP can be used as an alternative to the XCF01S, XCF02S, or XCF04S.
2. Assumes compression used.

Table 3: **Platform Flash PROM Capacity**

Platform Flash PROM	Configuration Bits	Platform Flash PROM	Configuration Bits
XCF01S	1,048,576	XCF08P	8,388,608
XCF02S	2,097,152	XCF16P	16,777,216
XCF04S	4,194,304	XCF32P	33,554,432

Programming

In-System Programming

In-System Programmable PROMs can be programmed individually, or two or more can be daisy-chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 3. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The programming data sequence is delivered to the device using either Xilinx iMPACT software and a Xilinx download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The iMPACT software also outputs serial vector format (SVF) files for use with any tools that accept SVF format, including automatic test equipment. During in-system programming, the $\overline{CEO}$ output is driven High. All other outputs are held in a high-impedance state or held at clamp levels during in-system programming. In-system programming is fully supported across the recommended operating voltage and temperature ranges.

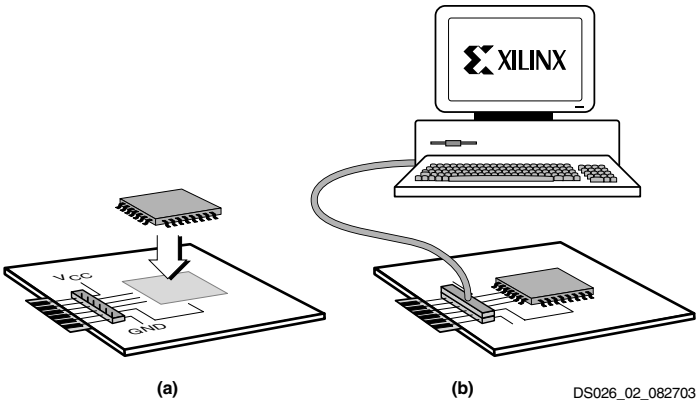


Figure 3: **JTAG In-System Programming Operation**
(a) Solder Device to PCB
(b) Program Using Download Cable

OE/$\overline{RESET}$

The 1/2/4 Mbit XCFxxS Platform Flash PROMs in-system programming algorithm requires issuance of a reset that causes OE/$\overline{RESET}$ to pulse Low.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx MultiPRO Desktop Tool or a third-party device programmer. This provides the added flexibility of using pre-programmed devices with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 20,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable Platform Flash PROM devices incorporate advanced data security features to fully protect the FPGA programming data against unauthorized reading via JTAG. The XCFxxP PROMs can also be programmed to prevent inadvertent writing via JTAG. Table 4 and Table 5 show the security settings available for the XCFxxS PROM and XCFxxP PROM, respectively.

Read Protection

The read protect security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. Read protection does not prevent write operations. For the XCFxxS PROM, the read protect security bit is set for the entire device, and resetting the read protect security bit requires erasing the entire device. For the XCFxxP PROM the read protect security bit can be set for individual design revisions, and resetting the read protect bit requires erasing the particular design revision.

Write Protection

The XCFxxP PROM device also allows the user to write protect (or lock) a particular design revision to prevent inadvertent erase or program operations. Once set, the write protect security bit for an individual design revision must be reset (using the UNLOCK command followed by ISC_ERASE command) before an erase or program operation can be performed.

Table 4: **XCFxxS Device Data Security Options**

Read Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)			
Set	√		

Table 5: **XCFxxP Design Revision Data Security Options**

Read Protect	Write Protect	Read/Verify Inhibited	Program Inhibited	Erase Inhibited
Reset (default)	Reset (default)			
Reset (default)	Set		√	√
Set	Reset (default)	√		
Set	Set	√	√	√

IEEE 1149.1 Boundary-Scan (JTAG)

The Platform Flash PROM family is IEEE Standard 1532 in-system programming compatible, and is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG, which is a subset of IEEE Std. 1532 Boundary-Scan. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the Platform Flash PROM device. Table 6 lists the required and optional boundary-scan instructions supported in the Platform Flash PROMs. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Instruction Register

The Instruction Register (IR) for the Platform Flash PROM is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI.

XCFxxS Instruction Register (8 bits wide)

The Instruction Register (IR) for the XCFxxS PROM is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Figure 4.

The instruction capture pattern shifted out of the XCFxxS device includes IR[7:0]. IR[7:5] are reserved bits and are set to a logic "0". The ISC Status field, IR[4], contains logic "1" if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic "0". The Security field, IR[3], contains logic "1" if the device has been programmed with the security option turned on; otherwise, it contains logic "0". IR[2] is unused, and is set to '0'. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

XCFxxP Instruction Register (16 bits wide)

The Instruction Register (IR) for the XCFxxP PROM is sixteen bits wide and is connected between TDI and TDO during an instruction scan sequence. The detailed composition of the instruction capture pattern is illustrated in Figure 5.

The instruction capture pattern shifted out of the XCFxxP device includes IR[15:0]. IR[15:9] are reserved bits and are set to a logic "0". The ISC Error field, IR[8:7], contains a "10" when an ISC operation is a success, otherwise a "01" when an In-System Configuration (ISC) operation fails The Erase/Program (ER/PROG) Error field, IR[6:5], contains a "10" when an erase or program operation is a success, otherwise a "01" when an erase or program operation fails. The Erase/Program (ER/PROG) Status field, IR[4], contains a logic "1" when the device is busy performing an erase or programming operation, otherwise, it contains a logic "0". The ISC Status field, IR[3], contains logic "1" if the device is currently in In-System Configuration (ISC) mode; otherwise, it contains logic "0". The DONE field, IR[2], contains logic "1" if the sampled design revision has been successfully programmed; otherwise, a logic "0" indicates incomplete programming. The remaining bits IR[1:0] are set to '01' as defined by IEEE Std. 1149.1.

Table 6: **Platform Flash PROM Boundary Scan Instructions**

Boundary-Scan Command	XCFxxS IR[7:0] (hex)	XCFxxP IR[15:0] (hex)	Instruction Description
Required Instructions			
BYPASS	FF	FFFF	Enables BYPASS
SAMPLE/PRELOAD	01	0001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00	0000	Enables boundary-scan EXTEST operation

Table 6: **Platform Flash PROM Boundary Scan Instructions *(Continued)***

Boundary-Scan Command	XCFxxS IR[7:0] (hex)	XCFxxP IR[15:0] (hex)	Instruction Description
Optional Instructions			
CLAMP	FA	00FA	Enables boundary-scan CLAMP operation
HIGHZ	FC	00FC	Places all outputs in high-impedance state simultaneously
IDCODE	FE	00FE	Enables shifting out 32-bit IDCODE
USERCODE	FD	00FD	Enables shifting out 32-bit USERCODE
Platform Flash PROM Specific Instructions			
CONFIG	EE	00EE	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low once. (For the XCFxxP this command also resets the selected design revision based on either the external REV_SEL[1:0] pins or on the internal design revision selection bits.)(1)

Notes:
1. For more information see Initiating FPGA Configuration.

TDI →	IR[7:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Status	Security	0	0 1	

Figure 4: **XCFxxS Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

TDI →	IR[15:9]	IR[8:7]	IR[6:5]	IR[4]	IR[3]	IR[2]	IR[1:0]	→ TDO
	Reserved	ISC Error	ER/PROG Error	ER/PROG Status	ISC Status	DONE	0 1	

Figure 5: **XCFxxP Instruction Capture Values Loaded into IR as part of an Instruction Scan Sequence**

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/PRELOAD, and CLAMP instructions. Each output pin on the Platform Flash PROM has two register stages which contribute to the boundary-scan register, while each input pin has only one register stage. The bidirectional pins have a total of three register stages which contribute to the boundary-scan register. For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the High-Z enable state of the output pin. For each input pin, a single register stage controls and observes the input state of the pin. The bidirectional pin combines the three bits, the input stage bit is first, followed by the output stage bit and finally the output enable stage bit. The output enable stage bit is closest to TDO.

See the XCFxxS/XCFxxP Pin Names and Descriptions Tables in the **Pinouts and Pin Descriptions** section for the boundary-scan bit order for all connected device pins, or see the appropriate BSDL file for the complete boundary-scan bit order description under the "attribute BOUNDARY_REGISTER" section in the BSDL file. The bit assigned to boundary-scan cell "0" is the LSB in the boundary-scan register, and is the register bit closest to TDO.

Identification Registers

IDCODE Register

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32 bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG. Table 7 lists the IDCODE register values for the Platform Flash PROMs.

The IDCODE register has the following binary format:

```
vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number
f = the PROM family code
a = the specific Platform Flash PROM product ID
c = the Xilinx manufacture's ID

The LSB of the IDCODE register is always read as logic "1" as defined by IEEE Std. 1149.1.

Table 7: **IDCODES Assigned to Platform Flash PROMs**

Device	IDCODE(1) (hex)
XCF01S	05044093
XCF02S	05045093
XCF04S	05046093
XCF08P	05057093
XCF16P	05058093
XCF32P	05059093

Notes:
1. The first four bits indicate the die version number, and may vary.

USERCODE Register

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the Platform Flash PROM. If the device is blank or was not loaded during programming, the USERCODE register contains FFFFFFFFh.

Customer Code Register

For the XCFxxP Platform Flash PROM, in addition to the USERCODE, a unique 32-byte Customer Code can be assigned to each design revision enabled for the PROM. The Customer Code is set during programming, and is typically used to supply information about the design revision contents. A private JTAG instruction is required to read the Customer Code. If the PROM is blank, or the Customer Code for the selected design revision was not loaded during programming, or if the particular design revision is erased, the Customer Code will contain all ones.

Platform Flash PROM TAP Characteristics

The Platform Flash PROM family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the Platform Flash PROM TAP are described as follows.

TAP Timing

Figure 6 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

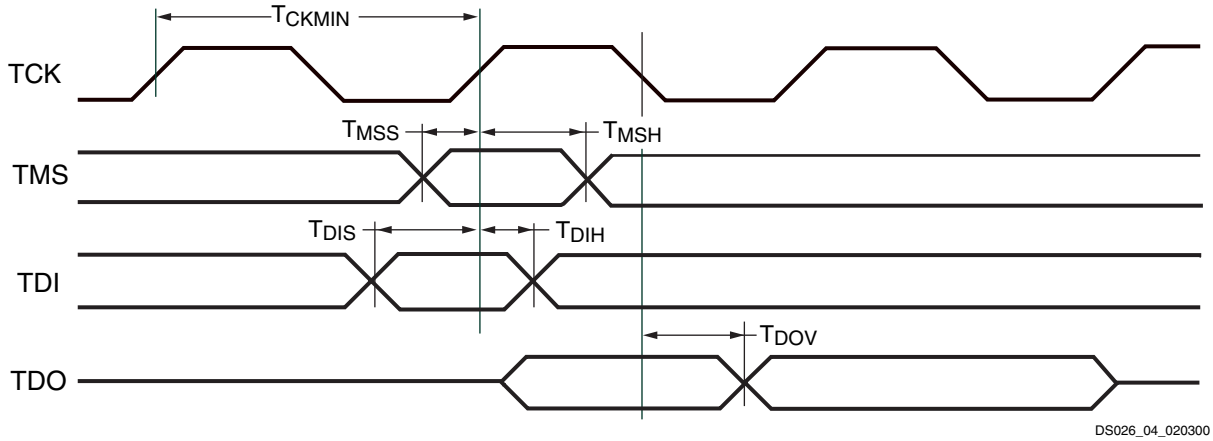


Figure 6: **Test Access Port Timing**

TAP AC Parameters

Table 8 shows the timing parameters for the TAP waveforms shown in Figure 6.

Table 8: **Test Access Port Timing Parameters**

Symbol	Parameter	Min	Max	Units
T_{CKMIN1}	TCK minimum clock period when V_{CCJ} = 2.5V or 3.3V	100	-	ns
T_{CKMIN2}	TCK minimum clock period, Bypass Mode, when V_{CCJ} = 2.5V or 3.3V	50	-	ns
T_{MSS}	TMS setup time when V_{CCJ} = 2.5V or 3.3V	10	-	ns
T_{MSH}	TMS hold time when V_{CCJ} = 2.5V or 3.3V	25	-	ns
T_{DIS}	TDI setup time when V_{CCJ} = 2.5V or 3.3V	10	-	ns
T_{DIH}	TDI hold time when V_{CCJ} = 2.5V or 3.3V	25	-	ns
T_{DOV}	TDO valid delay when V_{CCJ} = 2.5V or 3.3V	-	30	ns

Additional Features for the XCFxxP

Internal Oscillator

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include an optional internal oscillator which can be used to drive the CLKOUT and DATA pins on FPGA configuration interface. The internal oscillator can be enabled during device programming, and can be set to either the default frequency or to a slower frequency (**AC Characteristics Over Operating Conditions When Cascading**).

CLKOUT

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include the programmable option to enable the CLKOUT signal which allows the PROM to provide a source synchronous clock aligned to the data on the configuration interface. The CLKOUT signal is derived from one of two clock sources: the CLK input pin or the internal oscillator. The input clock source is selected during the PROM programming sequence. Output data is available on the rising edge of CLKOUT.

The CLKOUT signal is enabled during programming, and is active when $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High. When disabled, the CLKOUT pin is put into a high-impedance state and should be pulled High externally to provide a known state.

When cascading Platform Flash PROMs with CLKOUT enabled, after completing it's data transfer, the first PROM disables CLKOUT and releases the $\overline{CEO}$ pin enabling the next PROM in the PROM chain. The next PROM will begin driving the CLKOUT signal once that PROM is enabled and data is available for transfer.

During high-speed parallel configuration without compression, the FPGA drives the BUSY signal on the configuration interface. When BUSY is asserted High, the PROMs internal address counter stops incrementing, and the current data value is held on the data outputs. While BUSY is High, the PROM will continue driving the CLKOUT signal to the FPGA, clocking the FPGAs configuration logic. When the FPGA deasserts BUSY, indicating that it is ready to receive additional configuration data, the PROM will begin driving new data onto the configuration interface.

Decompression

The 8/16/32 Mbit XCFxxP Platform Flash PROMs include a built-in data decompressor compatible with Xilinx advanced compression technology. Compressed Platform Flash PROM files are created from the target FPGA bitstream(s) using the iMPACT software. Only Slave Serial and Slave SelectMAP (parallel) configuration modes are supported for FPGA configuration when using a XCFxxP PROM programmed with a compressed bitstream. Compression rates will vary depending on several factors, including the target device family and the target design contents.

The decompression option is enabled during the PROM programming sequence. The PROM decompresses the stored data before driving both clock and data onto the FPGA's configuration interface. If Decompression is enabled, then the Platform Flash clock output pin (CLKOUT) must be used as the clock signal for the configuration interface, driving the target FPGA's configuration clock input pin (CCLK). Either the PROM's CLK input pin or the internal oscillator must be selected as the source for CLKOUT. Any target FPGA connected to the PROM must operate as slave in the configuration chain, with the configuration mode set to Slave Serial mode or Slave SelectMap (parallel) mode.

When decompression is enabled, the CLKOUT signal becomes a controlled clock output with a reduced maximum frequency and remains Low when decompressed data is not ready.

The BUSY input is automatically disabled when decompression is enabled.

Design Revisioning

Design Revisioning allows the user to create up to four unique design revisions on a single PROM or stored across

multiple cascaded PROMs. Design Revisioning is supported for the 8/16/32 Mbit XCFxxP Platform Flash PROMs in both serial and parallel modes. Design Revisioning can be used with compressed PROM files, and also when the CLKOUT feature is enabled. The PROM programming files along with the revision information files (.cfi) are created using the iMPACT software. The .cfi file is required to enable design revision programming in iMPACT.

A single design revision requires at least 8 Mbits of memory, but a larger design revision can span several devices. A single 32 Mbit PROM can store from one to four separate design revisions: one 32 Mbit design revision, two 16 Mbit design revisions, three 8 Mbit design revisions, or four 8 Mbit design revisions. A single 16 Mbit PROM can store up to two separate design revisions: one 16 Mbit design revision, two 8 Mbit design revisions. A single 8 Mbit PROM can store only one 8 Mbit design revision. Larger design revisions can be split over several cascaded PROMs.

During the PROM file creation, each design revision is assigned a revision number:

Revision 0 = '00'
Revision 1 = '01'
Revision 2 = '10'
Revision 3 = '11'

After programming the Platform Flash PROM, a particular design revision can be selected using the external REV_SEL[1:0] pins or using the internal programmable design revision control bits. The $\overline{\text{EN\_EXT\_SEL}}$ pin determines if the external pins or internal bits are used to select the design revision. When $\overline{\text{EN\_EXT\_SEL}}$ is Low, design revision selection is controlled by the external Revision Select pins, REV_SEL[1:0]. When $\overline{\text{EN\_EXT\_SEL}}$ is High, design revision selection is controlled by the internal programmable Revision Select control bits. During power up, the design revision selection inputs (pins or control bits) are sampled internally. After power up, the design revision selection inputs are sampled again after the rising edge of the $\overline{\text{CF}}$ pulse. The data from the selected design revision is then presented on the FPGA configuration interface.

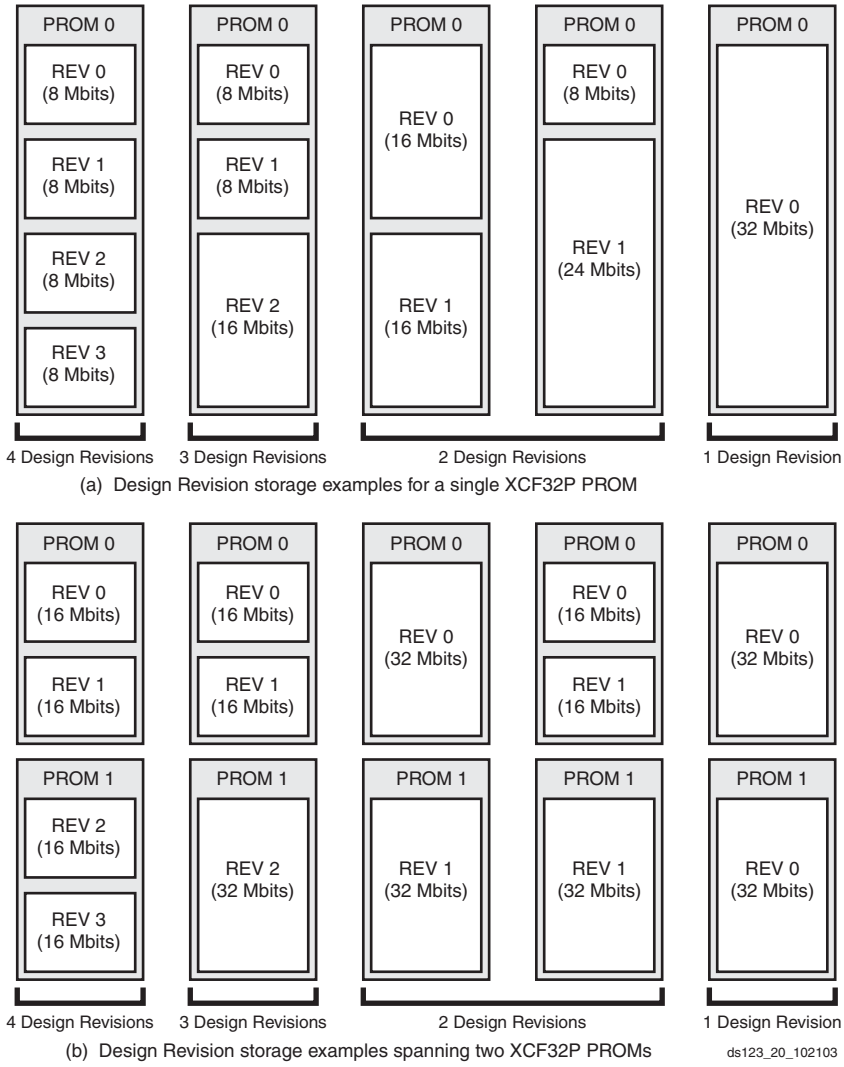


Figure 7: **Design Revision Storage Examples**

PROM to FPGA Configuration Mode and Connections Summary

The FPGA's I/O, logical functions, and internal interconnections are established by the configuration data contained in the FPGAs bitstream. The bitstream is loaded into the FPGA either automatically upon power up, or on command, depending on the state of the FPGA's mode pins. Xilinx Platform Flash PROMs are designed to download directly to the FPGA configuration interface. FPGA configuration modes which are supported by the XCFxxS Platform Flash PROMs include: Master Serial and Slave Serial. FPGA configuration modes which are supported by the XCFxxP Platform Flash PROMs include: Master Serial, Slave Serial, Master SelectMAP, and Slave SelectMAP. Below is a short summary of the supported FPGA configuration modes. See the respective FPGA data sheet for device configuration details, including which configuration modes are supported by the targeted FPGA device.

FPGA Master Serial Mode

In Master Serial mode, the FPGA automatically loads the configuration bitstream in bit-serial form from external memory synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master Serial configuration mode. Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be setup at the FPGAs DIN input pin a short time before each rising edge of the FPGA's internally generated CCLK signal.

Typically, a wide range of frequencies can be selected for the FPGA's internally generated CCLK which always starts at a slow default frequency. The FPGAs bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master Serial configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master Serial Configuration Mode (Figure 8):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s)
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

FPGA Slave Serial Mode

In Slave Serial mode, the FPGA loads the configuration bitstream in bit-serial form from external memory synchronized by an externally supplied clock. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave Serial configuration mode. Slave Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines (INIT and DONE) are required to configure an FPGA. Data from the PROM is read out sequentially on a single data line (DIN), accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The serial bitstream data must be setup at the FPGAs DIN input pin a short time before each rising edge of the externally provided CCLK.

Connecting the FPGA device to the configuration PROM for Slave Serial Configuration Mode (Figure 9):

- The DATA output of the PROM(s) drive the DIN input of the lead FPGA device.
- The PROM CLKOUT (for XCFxxP only) or an external clock source drives the FPGA's CCLK input.
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B (or INIT) pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

Serial Daisy Chain

Multiple FPGAs can be daisy-chained for serial configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed internally

to the FPGAs DOUT pin. Typically the data on the DOUT pin changes on the falling edge of CCLK, although for some devices the DOUT pin changes on the rising edge of CCLK. Consult the respective device data sheets for detailed information on a particular FPGA device. For clocking the daisy-chained configuration, either the first FPGA in the chain can be set to Master Serial, generating the CCLK, with the remaining devices set to Slave Serial (Figure 10), or all the FPGA devices can be set to Slave Serial and an externally generated clock can be used to drive the FPGA's configuration interface.

FPGA Master SelectMAP (Parallel) Mode(1)

In Master SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by the configuration clock (CCLK) generated by the FPGA. Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Master SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGAs Chip Select, Write, and BUSY pins must be correctly controlled to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be setup at the FPGAs [D0..D7] input pins a short time before each rising edge of the FPGA's internally generated CCLK signal. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. An external data source or external pull-down resistors must be used to enable the FPGA's active Low Chip Select ($\overline{CS}$ or CS_B) and Write ($\overline{WRITE}$ or RDWR_B) signals to enable the FPGA's SelectMAP configuration process.

The Master SelectMAP configuration interface is clocked by the FPGA's internal oscillator. Typically, a wide range of frequencies can be selected for the internally generated CCLK which always starts at a slow default frequency. The FPGAs bitstream contains configuration bits which can switch CCLK to a higher frequency for the remainder of the Master SelectMAP configuration sequence. The desired CCLK frequency is selected during bitstream generation.

Connecting the FPGA device to the configuration PROM for Master SelectMAP (Parallel) Configuration Mode (Figure 11):

- The DATA outputs of the PROM(s) drive the [D0..D7] input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s)
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output. This connection assures that the PROM is only enabled when the FPGA is ready for the next configuration data byte.
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

FPGA Slave SelectMAP (Parallel) Mode(2)

In Slave SelectMAP mode, byte-wide data is written into the FPGA, typically with a BUSY flag controlling the flow of data, synchronized by an externally supplied configuration clock (CCLK). Upon power-up or reconfiguration, the FPGA's mode select pins are used to select the Slave SelectMAP configuration mode. The configuration interface typically requires a parallel data bus, a clock line, and two control lines (INIT and DONE). In addition, the FPGAs Chip Select, Write, and BUSY pins must be correctly controlled to enable SelectMAP configuration. The configuration data is read from the PROM byte by byte on pins [D0..D7], accessed via the PROM's internal address counter which is incremented on every valid rising edge of CCLK. The bitstream data must be setup at the FPGAs [D0..D7] input pins a short time before each rising edge of the provided CCLK. If BUSY is asserted (High) by the FPGA, the configuration data must be held until BUSY goes Low. An external data source or external pull-down resistors must be used to enable the FPGA's active Low Chip Select ($\overline{CS}$ or CS_B) and Write ($\overline{WRITE}$ or RDWR_B) signals to enable the FPGA's SelectMAP configuration process.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained using the persist option.

Connecting the FPGA device to the configuration PROM for Slave SelectMAP (Parallel) Configuration Mode (Figure 12):

1. The Master SelectMAP (Parallel) FPGA configuration mode is supported only by the XCFxxP Platform Flash PROM. This mode is not supported by the XCFxxS Platform Flash PROM.

2. The Slave SelectMAP (Parallel) FPGA configuration mode is supported only by the XCFxxP Platform Flash PROMs.This mode is not supported by the XCFxxS Platform Flash PROM.

- The DATA outputs of the PROM(s) drives the [D0..D7] inputs of the lead FPGA device.
- The PROM CLKOUT (for XCFxxP only) or an external clock source drives the FPGA's CCLK input
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ pins of all PROMs are connected to the INIT_B pins of all FPGA devices. This connection assures that the PROM address counter is reset before the start of any (re)configuration.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of all target FPGA devices, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary I_{CC} active supply current (**DC Characteristics Over Operating Conditions**).
- For high-frequency parallel configuration, the BUSY pins of all PROMs are connected to the FPGA's BUSY output. This connection assures that the PROM is only enabled when the FPGA is ready for the next configuration data byte.
- The PROM $\overline{CF}$ pin is typically connected to the FPGA's PROG_B (or $\overline{PROGRAM}$) input.

FPGA SelectMAP (Parallel) Device Chaining(1)

Multiple Virtex-II FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, DONE, INIT, Data ([D0..D7]), Write ($\overline{WRITE}$ or RDWR_B), and BUSY pins of all the devices in parallel. If all devices are to be configured with the same bitstream, readback is not being used, and the CCLK frequency selected does not require the use of the BUSY signal, the CS_B pins can be connected to a common line so all of the devices are configured simultaneously (Figure 13).

With additional control logic, the individual devices can be loaded separately by asserting the CS_B pin of each device in turn and then enabling the appropriate configuration data. The PROM can also store the individual bitstreams for each FPGA for SelectMAP configuration in separate design revisions. When design revisioning is utilized, additional control logic can be used to select the appropriate bitstream by asserting the $\overline{EN\_EXT\_SEL}$ pin, and using the REV_SEL[1:0] pins to select the required bitstream, while asserting the CS_B pin for the FPGA the bitstream is targeting (Figure 14).

1. The SelectMAP (Parallel) FPGA configuration modes are supported only by the XCFxxP Platform Flash PROM.These modes are not supported by the XCFxxS Platform Flash PROM.

For clocking the parallel configuration chain, either the first FPGA in the chain can be set to Master SelectMAP, generating the CCLK, with the remaining devices set to Slave SelectMAP, or all the FPGA devices can be set to Slave SelectMAP and an externally generated clock can be used to drive the configuration interface. Again, the respective device data sheets should be consulted for detailed information on a particular FPGA device, including which configuration modes are supported by the targeted FPGA device.

Cascading Configuration PROMs

When configuring multiple FPGAs in a serial daisy chain, configuring multiple FPGAs in a SelectMAP parallel chain, or configuring a single FPGA requiring a larger configuration bitstream, cascaded PROMs provide additional memory (Figure 10, Figure 13, Figure 14, and Figure 15). Multiple Platform Flash PROMs can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the downstream device. The clock signal and the data outputs of all Platform Flash PROMs in the chain are interconnected. After the last data from the first PROM is read, the first PROM asserts its $\overline{CEO}$ output Low and drives its outputs to a high-impedance state. The second PROM recognizes the Low level on its $\overline{CE}$ input and immediately enables its outputs.

After configuration is complete, address counters of all cascaded PROMs are reset if the PROM OE/$\overline{RESET}$ pin goes Low or $\overline{CE}$ goes High.

When utilizing the advanced features for the XCFxxP Platform Flash PROM, including the clock output (CLKOUT) option, decompression option, or design revisioning, programming files which span cascaded PROM devices can only be created for cascaded chains containing only XCFxxP PROMs. If the advanced features are not used, then cascaded PROM chains can contain both XCFxxP and XCFxxS PROMs.

Initiating FPGA Configuration

The options for initiating FPGA configuration via the Platform Flash PROM include:

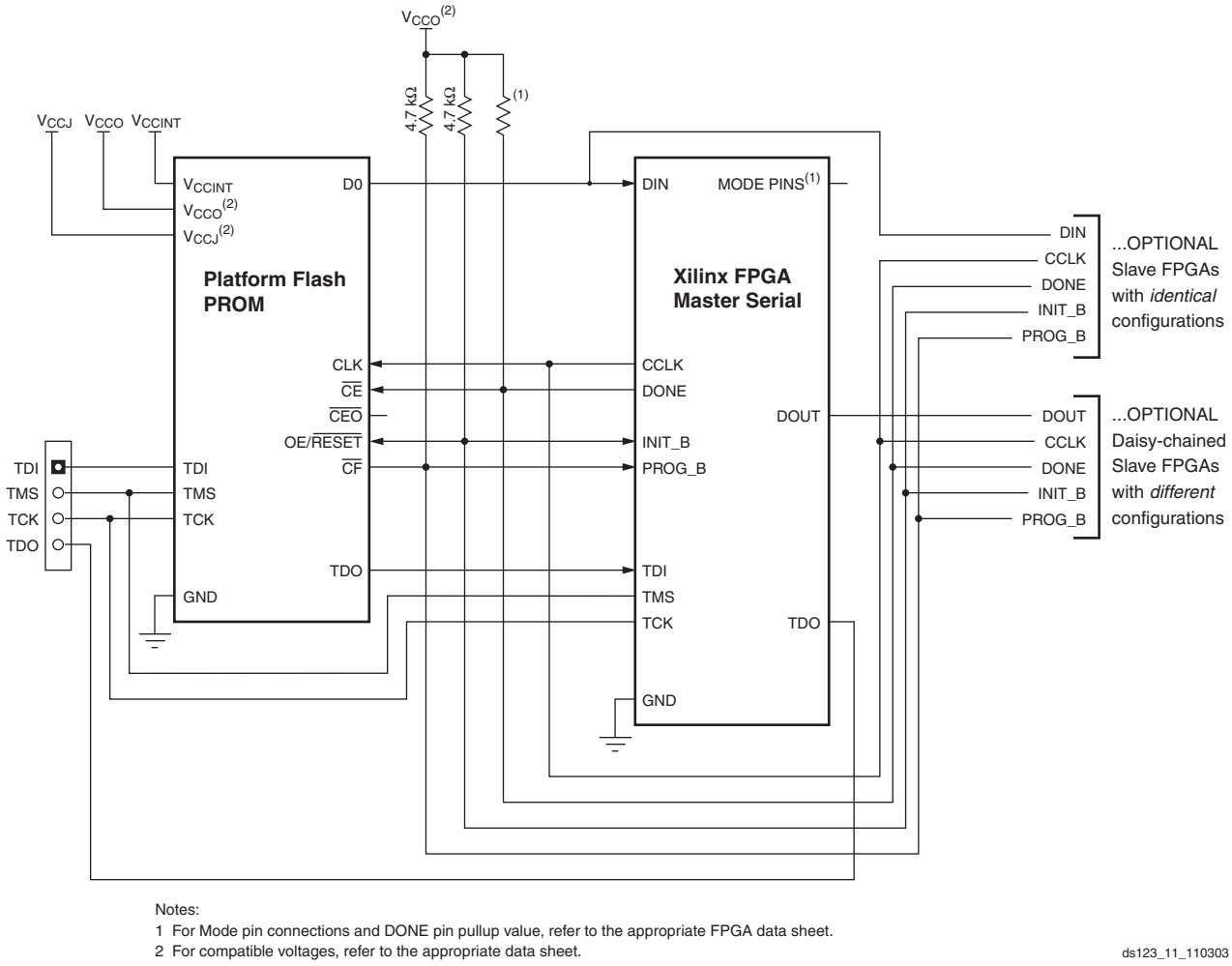
1. Automatic configuration on power up
2. Applying an external PROG_B (or $\overline{PROGRAM}$) pulse
3. Applying the JTAG CONFIG instruction

Following the FPGA's power-on sequence or the assertion of the PROG_B (or $\overline{PROGRAM}$) pin the FPGAs configuration memory is cleared, the configuration mode is selected, and the FPGA is ready to accept a new configuration bitstream. The FPGA's PROG_B pin can be controlled by an external source, or alternatively, the Platform Flash PROMs incorporate a $\overline{CF}$ pin that can be tied to the FPGAs PROG_B pin. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ output Low once for 300-500 ns, resetting the FPGA and initiating configuration. The iMPACT soft-

ware can issue the JTAG CONFIG command to initiate FPGA configuration by setting the "Load FPGA" option.

When using the XCFxxP Platform Flash PROM with design revisioning enabled, the $\overline{CF}$ pin should always be connected to the PROG_B (or $\overline{PROGRAM}$) pin on the FPGA to ensure that the current design revision selection is sampled when the FPGA is reset. The XCFxxP PROM samples the current design revision selection from the external REV_SEL pins or the internal programmable Revision Select bits on the rising edge of $\overline{CF}$. When the JTAG CONFIG command is executed, the XCFxxP will sample the new design revision before initiating the FPGA configuration sequence.

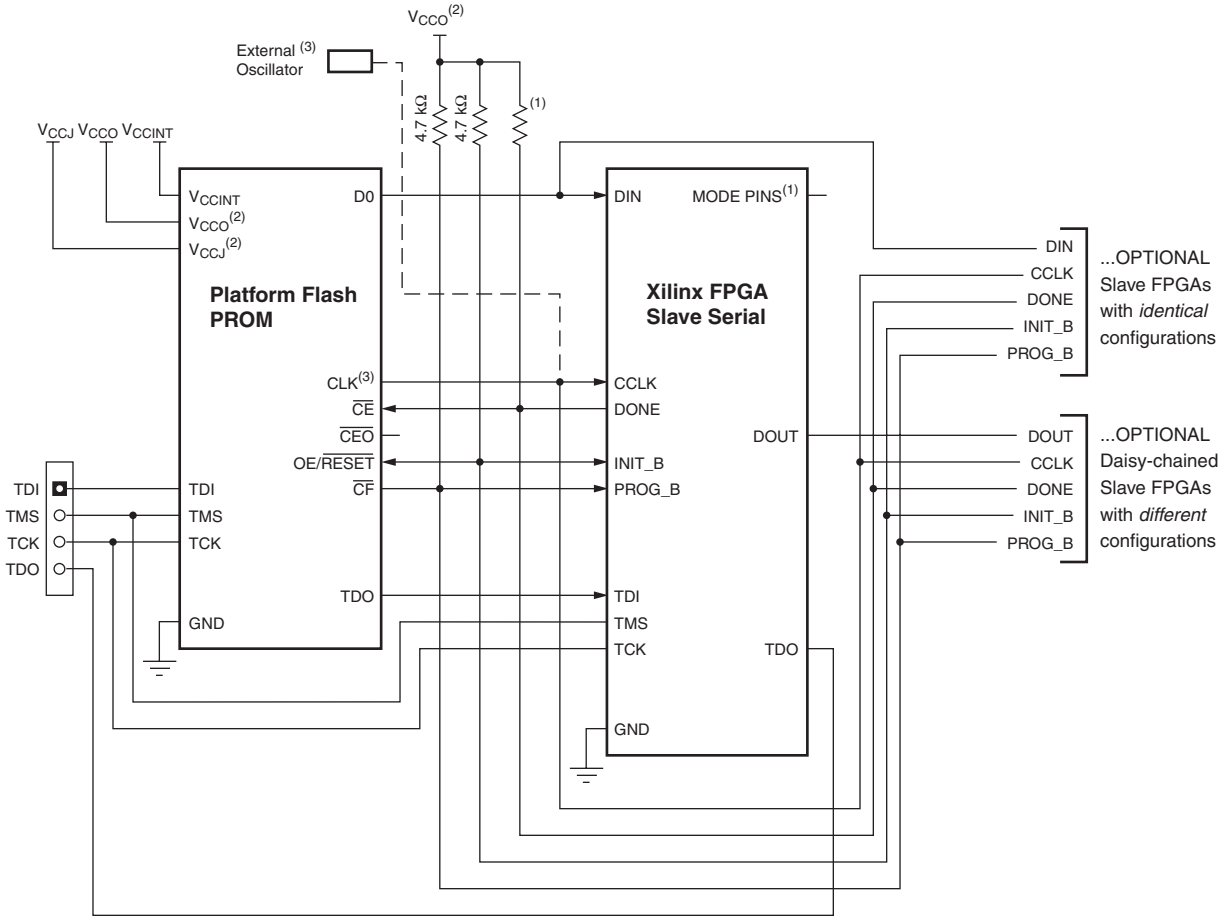
Configuration PROM to FPGA Device Interface Connection Diagrams



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.

ds123_11_110303

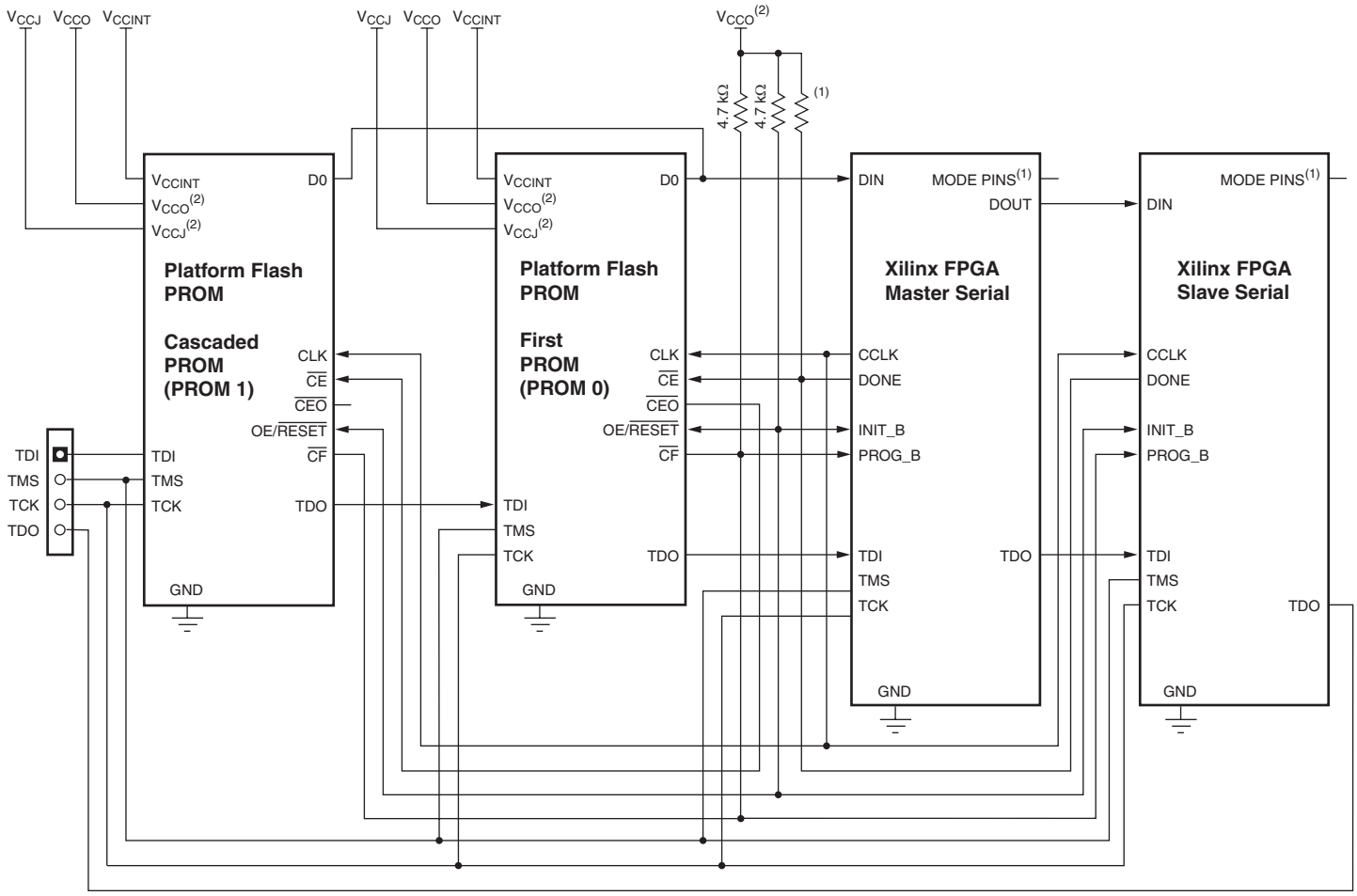
Figure 8: **Configuring in Master Serial Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally—for the XCFxxP Platform Flash PROM only—the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then it must be tied to a 4.7KΩ resistor pulled up to V_{CCO}.

ds123_12_110303

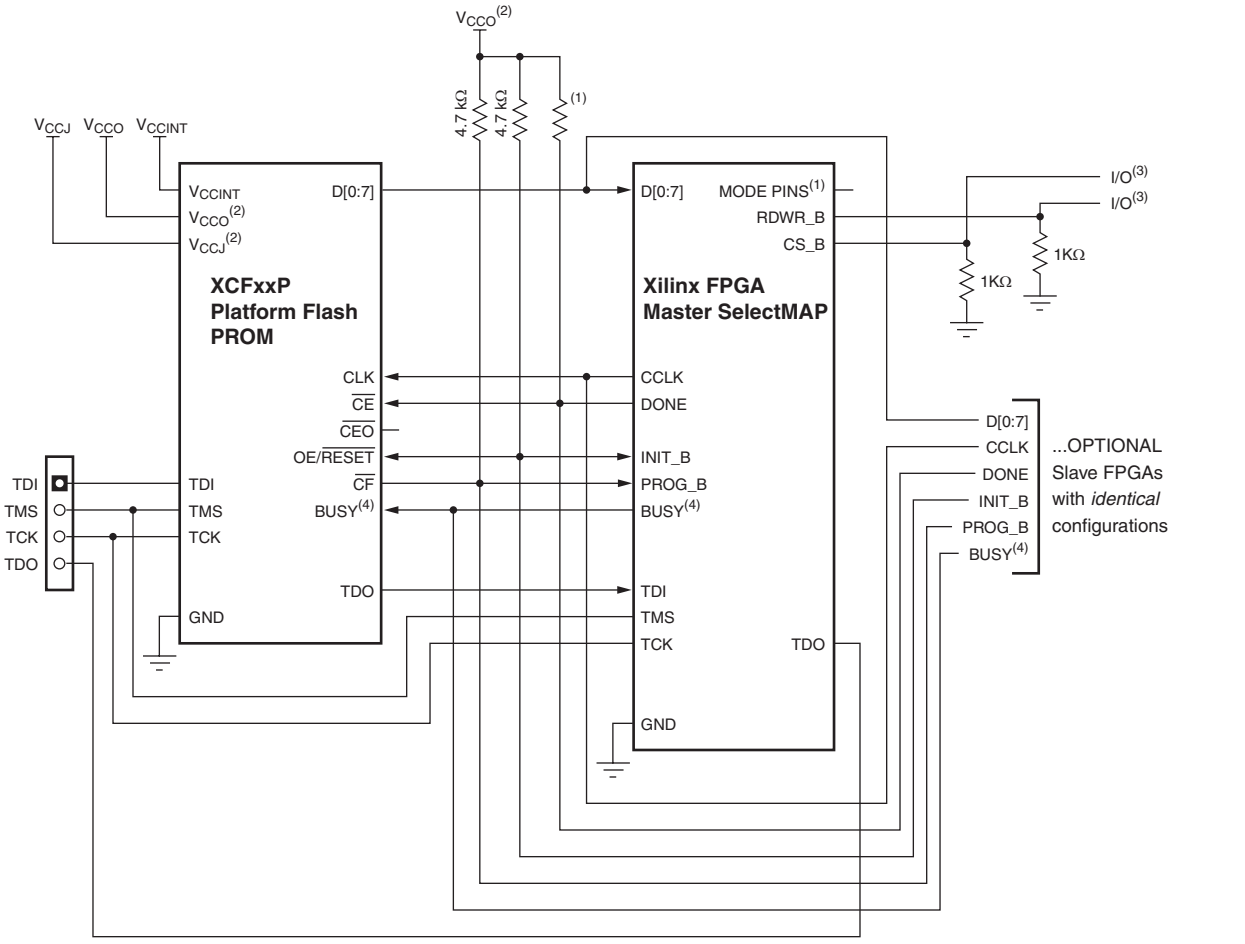
Figure 9: **Configuring in Slave Serial Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.

ds123_13_110303

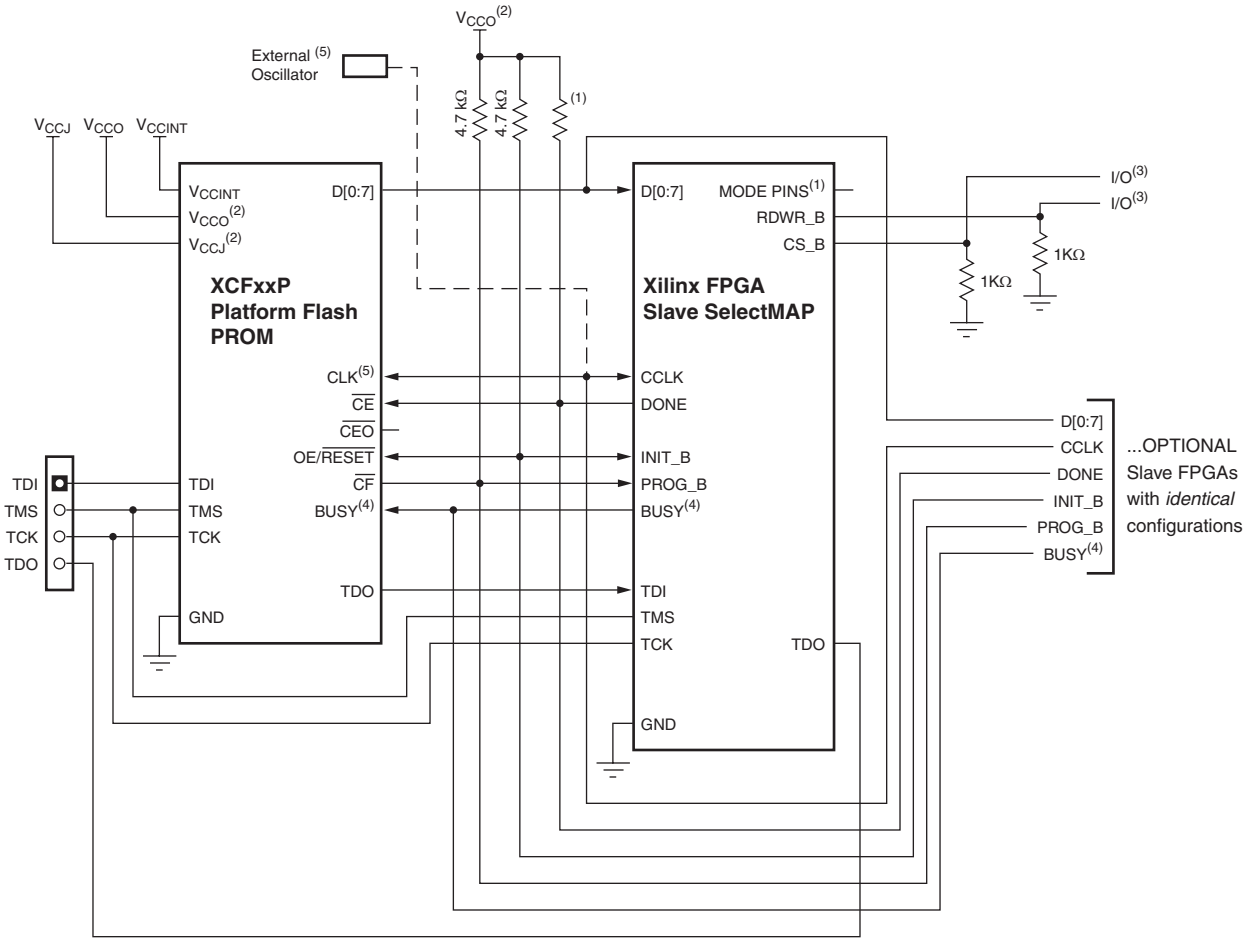
Figure 10: **Configuring Multiple Devices Master/Slave Serial Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 CS_B (or $\overline{CS}$) and RDWR_B (or $\overline{WRITE}$) must be either driven Low or pulled down exernally. One option is shown.
4 The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.

ds123_14_110303

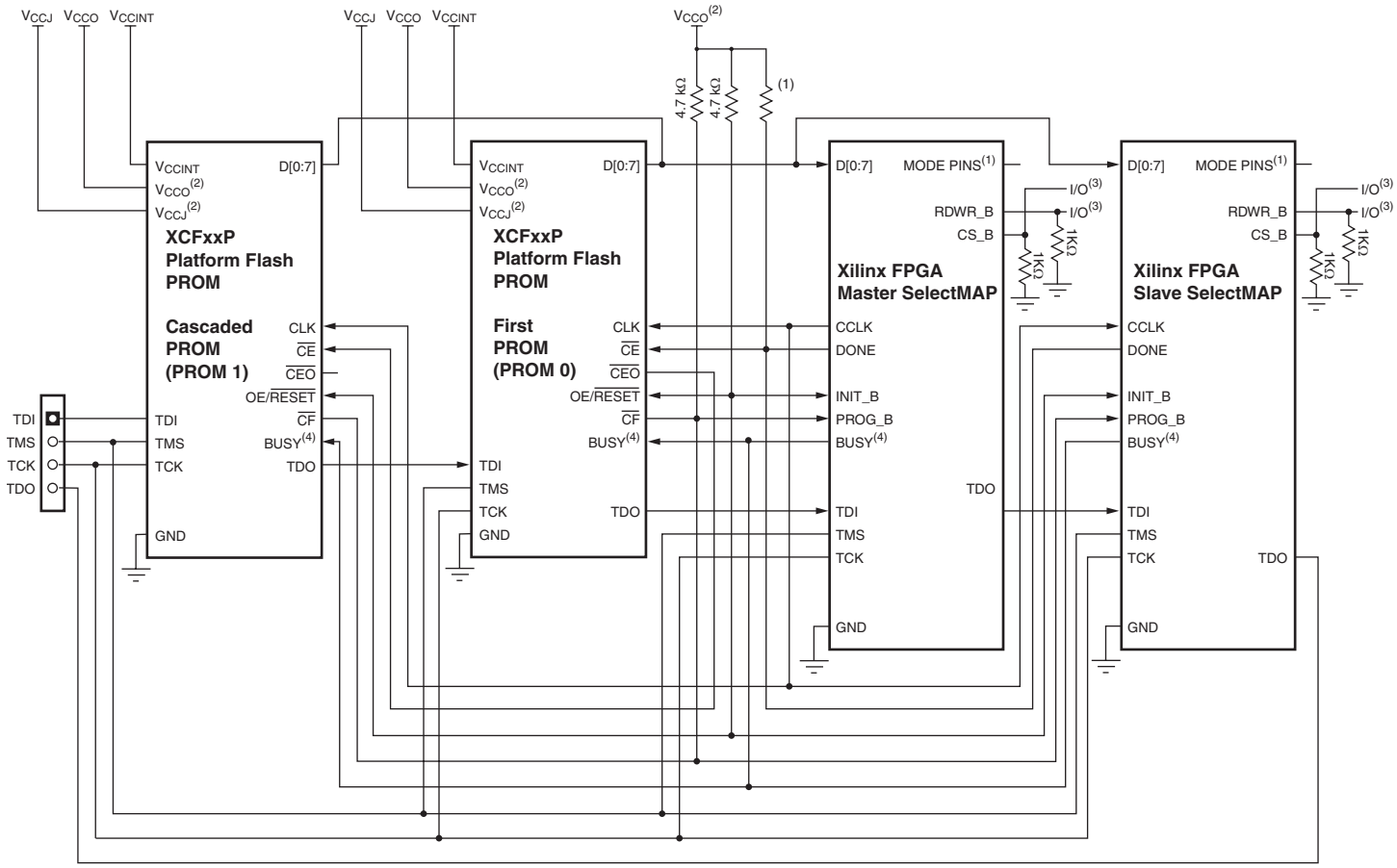
Figure 11: **Configuring in Master SelectMAP Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 CS_B (or $\overline{CS}$) and RDWR_B (or $\overline{WRITE}$) must be either driven Low or pulled down exernally. One option is shown.
4 The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.
5 If the XCFxxP Platform Flash PROM is not used with CLKOUT enabled to drive CCLK, then an external clock is required for Slave SelectMAP (or Slave Parallel) modes. If CLKOUT is used, then it must be tied to a 4.7KΩ resistor pulled up to V_{CCO}.

ds123_15_110303

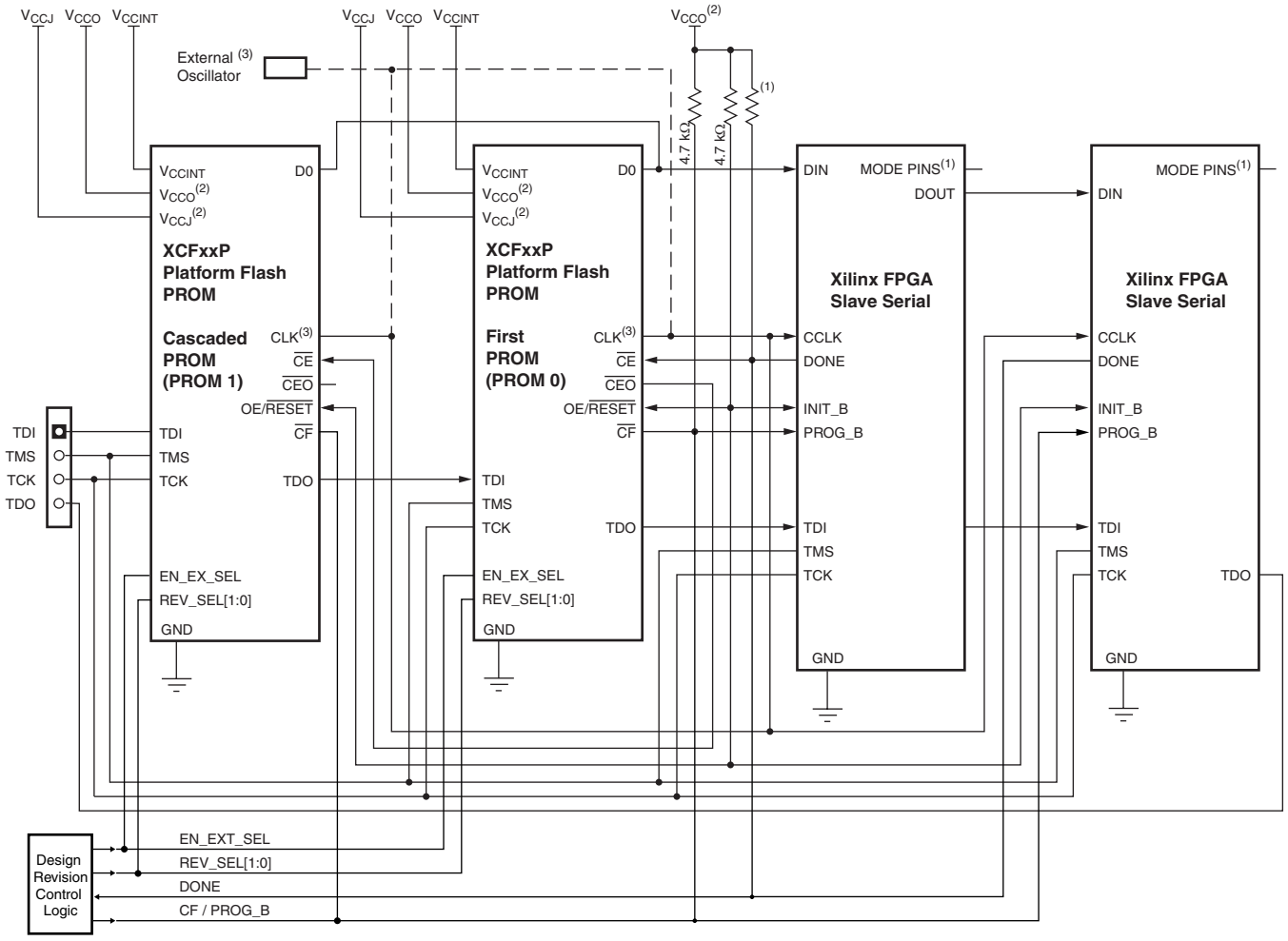
Figure 12: **Configuring in Slave SelectMAP Mode**



Notes:
1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 CS_B (or $\overline{CS}$) and RDWR_B (or $\overline{WRITE}$) must be either driven Low or pulled down exernally. One option is shown.
4 The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high-frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.

ds123_16_110303

Figure 13: **Configuring Multiple Devices with Identical Patterns in Master/Slave SelectMAP Mode**

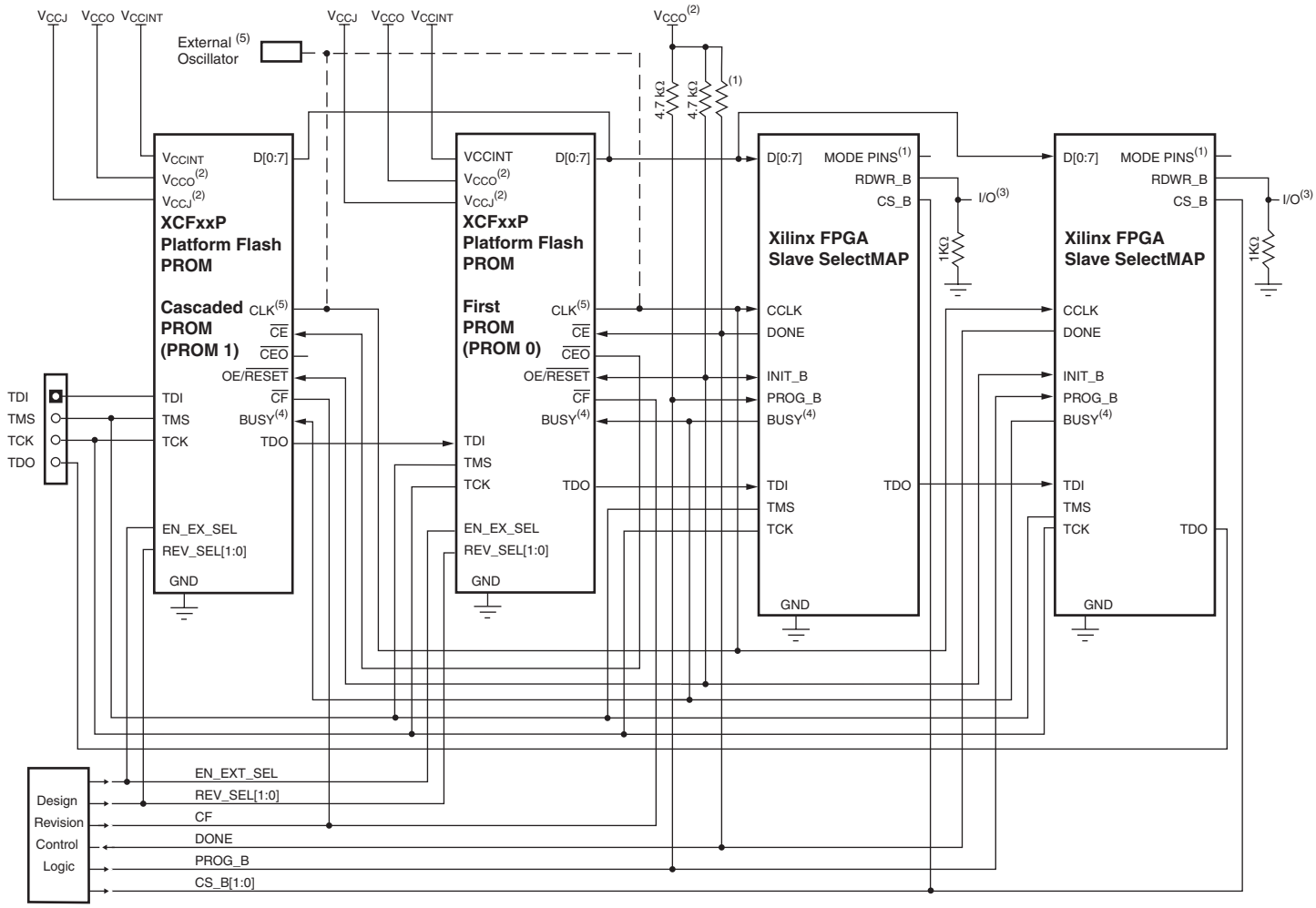


Notes:

1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.
2 For compatible voltages, refer to the appropriate data sheet.
3 In Slave Serial mode, the configuration interface can be clocked by an external oscillator, or optionally the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then it must be tied to a 4.7KΩ resistor pulled up to V_{CCO}.

ds123_17_110503

Figure 14: **Configuring Multiple Devices with Design Revisioning in Slave Serial Mode**



Notes:

1 For Mode pin connections and DONE pin pullup value, refer to the appropriate FPGA data sheet.

2 For compatible voltages, refer to the appropriate data sheet.

3 RDWR_B (or $\overline{\text{WRITE}}$) must be either driven Low or pulled down exernally. One option is shown.

4 The BUSY pin is only available with the XCFxxP Platform Flash PROM, and the connection is only required for high frequency SelectMAP mode configuration. For BUSY pin requirements, refer to the appropriate FPGA data sheet.

5 In Slave SelectMAP mode, the configuration interface can be clocked by an external oscillator, or optionally the CLKOUT signal can be used to drive the FPGA's configuration clock (CCLK). If the XCFxxP PROM's CLKOUT signal is used, then it must be tied to a 4.7KΩ resistor pulled up to V_{CCO}.

ds123_18_110303

Figure 15: **Configuring Multiple Devices with Design Revisioning in Slave SelectMAP Mode**

Reset and Power-On Reset Activation

At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified V_{CCINT} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on reset properly. During the power-up sequence, OE/$\overline{RESET}$ is held Low by the PROM. Once the required supplies have reached their respective POR (Power On Reset) thresholds, the OE/$\overline{RESET}$ release is delayed (T_{OER} minimum) to allow more margin for the power supplies to stabilize before initiating configuration. The OE/$\overline{RESET}$ pin is connected to an external pull-up resistor and also to the target FPGA's INIT pin. For systems utilizing slow-rising power supplies, an additional power monitoring circuit can be used to delay the target configuration until the system power reaches minimum operating voltages by holding the OE/$\overline{RESET}$ pin Low. When OE/$\overline{RESET}$ is released, the FPGAs INIT pin is pulled High allowing the FPGA's configuration sequence to begin. If the power drops below the power-down threshold (V_{CCPD}), the PROM resets and OE/$\overline{RESET}$ is again held Low until the after the POR threshold is reached. OE/$\overline{RESET}$ polarity is not programmable. These power-up requirements are shown graphically in Figure 16.

For a fully powered Platform Flash PROM, a reset occurs whenever OE/$\overline{RESET}$ is asserted (Low) or $\overline{CE}$ is deasserted (High). The address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state.

Notes:

1. The XCFxxS PROM only requires V_{CCINT} to rise above its POR threshold before releasing OE/$\overline{RESET}$.
2. The XCFxxP PROM requires both V_{CCINT} to rise above its POR threshold and for V_{CCO} to reach the recommended operating voltage level before releasing OE/$\overline{RESET}$.

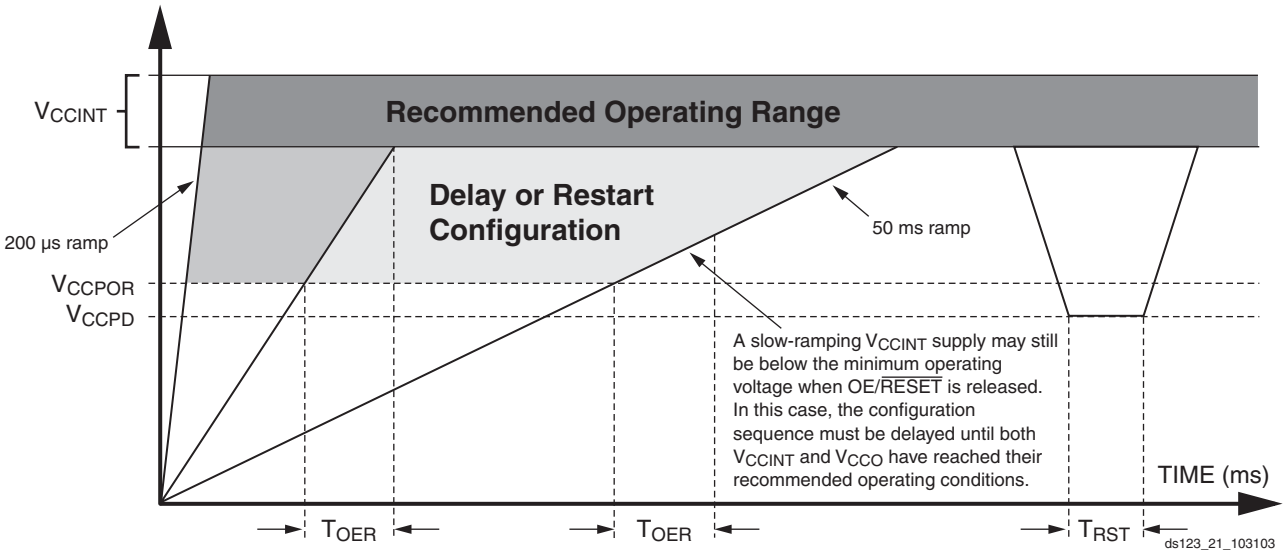


Figure 16: **Platform Flash PROM Power-Up Requirements**

I/O Input Voltage Tolerance and Power Sequencing

The I/Os on each re-programmable Platform Flash PROM are fully 3.3V-tolerant. This allows 3V CMOS signals to connect directly to the inputs without damage. The V_{CCINT} power can be applied before or after 3V CMOS signals are applied to the I/Os. The core power supply (V_{CCINT}), JTAG pin power supply (V_{CCJ}), and output power supply (V_{CCO}) can be applied in any order. The PROM should not be partially powered, with one supply left unpowered while another supply is fully powered. Failure to power the PROM correctly may result in damage to the device.

Additionally, for the XCFxxS PROM only, when V_{CCO} is supplied at 2.5V or 3.3V and V_{CCINT} is supplied at 3.3V, the I/Os are 5V-tolerant. This allows 5V CMOS signals to connect directly to the inputs on a powered XCFxxS PROM without damage.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is deasserted (High). In standby mode, the address counter is reset, $\overline{CEO}$ is driven High, and the remaining outputs are placed in a high-impedance state regardless of the state of the OE/$\overline{RESET}$ input. For the device to remain in the low-power standby mode, the JTAG pins TMS, TDI, and TDO must not be pulled Low, and TCK must be stopped (High or Low).

Table 9: **Truth Table for XCFxxS PROM Control Inputs**

Control Inputs		Internal Address	Outputs		
OE/$\overline{\text{RESET}}$	$\overline{\text{CE}}$		DATA	$\overline{\text{CEO}}$	ICC
High	Low	If address < TC(2) : increment	Active	High	Active
		If address = TC(2) : don't change	High-Z	Low	Reduced
Low	Low	Held reset	High-Z	High	Active
X(1)	High	Held reset	High-Z	High	Standby

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

Table 10: **Truth Table for XCFxxP PROM Control Inputs**

Control Inputs			Internal Address	Outputs			
OE/$\overline{\text{RESET}}$	$\overline{\text{CE}}$	BUSY		DATA	$\overline{\text{CEO}}$	CLKOUT	ICC
High	Low	Low	If address < TC(2) and address < EA(3) : increment	Active	High	Active	Active
			If address < TC(2) and address = EA(3) : don't change	High-Z	High	High-Z	Reduced
			Else if address = TC(2) : don't change	High-Z	Low	High-Z	Reduced
High	Low	High	Unchanged	Active and Unchanged	High	Active	Active
Low	Low	X	Held reset(4)	High-Z	High	High-Z	Active
X(1)	High	X	Held reset(4)	High-Z	High	High-Z	Standby

Notes:
1. X = don't care.
2. TC = Terminal Count = highest address value.
3. For the XCFxxP with Design Revisioning enabled, EA = end address (last address in the selected design revision).
4. For the XCFxxP with Design Revisioning enabled, Held Reset = address reset to the beginning address of the selected bank. If Design Revisioning is not enabled, then Held Reset = address reset to address 0.

DC Electrical Characteristics

AC Electrical Characteristics

Absolute Maximum Ratings

Symbol	Description		XCF01S, XCF02S, XCF04S	XCF08P, XCF16P, XCF32P	Units
V_{CCINT}	Internal supply voltage relative to GND		–0.5 to +4.0	–0.5 to +2.7	V
V_{CCO}	I/O supply voltage relative to GND		–0.5 to +4.0	–0.5 to +4.0	V
V_{CCJ}	JTAG I/O supply voltage relative to GND		–0.5 to +4.0	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	$V_{CCO} < 2.5V$	–0.5 to +3.6	–0.5 to V_{CCO} + 0.5	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	–0.5 to V_{CCO} + 0.5	V
V_{TS}	Voltage applied to High-Z output	$V_{CCO} < 2.5V$	–0.5 to +3.6	–0.5 to V_{CCO} + 0.5	V
		$V_{CCO} \geq 2.5V$	–0.5 to +5.5	–0.5 to V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	–65 to +150	°C
T_{SOL}(3)	Maximum soldering temperature (10s @ 1/16 in.)		+220	+220	°C
T_J	Junction temperature		+125	+125	°C

Notes:
1. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins can undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.
2. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time adversely affects device reliability.
3. For soldering guidelines, see the information on "Packaging and Thermal Characteristics" at www.xilinx.com.

Supply Voltage Requirements for Power-On Reset and Power-Down

Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
V_{CCPOR}	POR threshold for the V_{CCINT} supply	1	-	TBD	-	V
T_{OER}	OE/$\overline{RESET}$ release delay following POR(4)	0	1	0	TBD	ms
T_{VCC}	V_{CCINT} rise time from 0V to nominal voltage	0.2	50	0.2	50	ms
T_{RST}	Time required to trigger a device reset when the V_{CCINT} supply drops below the maximum V_{CCPD} threshold	10	-	10	-	ms
V_{CCPD}	Power-down threshold for V_{CCINT} supply	-	1	-	TBD	V

Notes:
1. V_{CCINT}, V_{CCO}, and V_{CCJ} supplies may be applied in any order.
2. At power up, the device requires the V_{CCINT} power supply to monotonically rise to the nominal operating voltage within the specified T_{VCC} rise time. If the power supply cannot meet this requirement, then the device might not perform power-on-reset properly. See Figure 16, page 21.
3. If the V_{CCINT} and V_{CCO} supplies do not reach their respective recommended operating conditions before the OE/$\overline{RESET}$ pin is released, then the configuration data from the PROM will not be available at the recommended threshold levels. The configuration sequence must be delayed until both V_{CCINT} and V_{CCO} have reached their recommended operating conditions.

Recommended Operating Conditions

Symbol	Description		XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
			Min	Max	Min	Max	
V_{CCINT}	Internal voltage supply		3.0	3.6	1.65	2.0	V
V_{CCO}/V_{CCJ}	Supply voltage for output drivers	3.3V Operation	3.0	3.6	3.0	3.6	V
		2.5V Operation	2.3	2.7	2.3	2.7	V
		1.8V Operation	1.7	2.0	1.7	2.0	V
		1.5V Operation	-	-	TBD	TBD	V
V_{IL}	Low-level input voltage	2.5V or 3.3V Operation	0	0.8	0	0.8	V
		1.8V Operation	0	20% V_{CCO}	0	20% V_{CCO}	V
V_{IH}	High-level input voltage	2.5V or 3.3V Operation	2.0	5.5	2.0	3.6	V
		1.8V Operation	70% V_{CCO}	3.6	70% V_{CCO}	3.6	V
V_O	Output voltage		0	V_{CCO}	0	V_{CCO}	V
T_A	Operating ambient temperature		–40	85	–40	85	°C

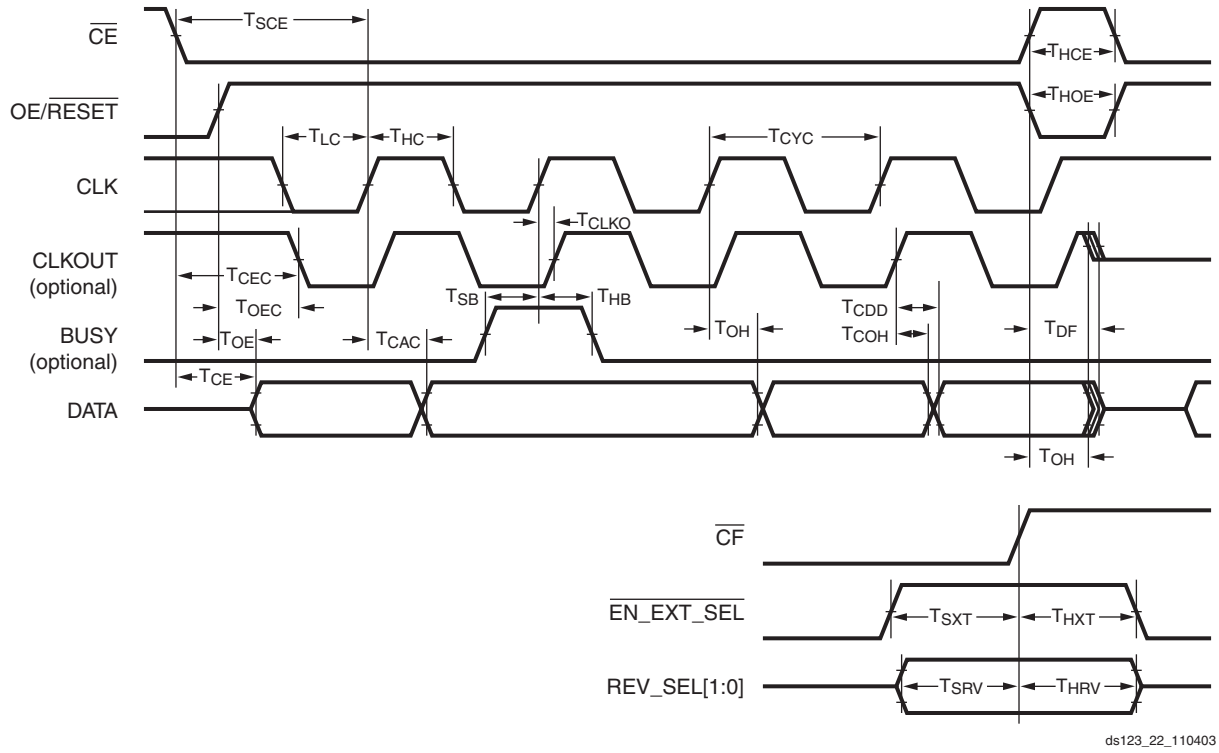
Quality and Reliability Characteristics

Symbol	Description	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/erase cycles (Endurance)	20,000	-	Cycles
V_{ESD}	Electrostatic discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Symbol	Description	XCF01S, XCF02S, XCF04S			XCF08P, XCF16P, XCF32P			Units
		Test Conditions	Min	Max	Test Conditions	Min	Max	
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4	-	I_{OH} = TBD	TBD	-	V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	V_{CCO} – 0.4	-	I_{OH} = TBD	TBD	-	V
	High-level output voltage for 1.8V outputs	I_{OH} = –50 µA	V_{CCO} – 0.4	-	I_{OH} = TBD	TBD	-	V
	High-level output voltage for 1.5V outputs	-	-	-	I_{OH} = TBD	TBD	-	V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA	-	0.4	I_{OL} = TBD	-	TBD	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA	-	0.4	I_{OL} = TBD	-	TBD	V
	Low-level output voltage for 1.8V outputs	I_{OL} = 50 µA	-	0.4	I_{OL} = TBD	-	TBD	V
	Low-level output voltage for 1.5V outputs	-	-	-	I_{OL} = TBD	-	TBD	V
I_{CCINT}	Internal voltage supply current, active mode	33 MHz	-	10	TBD	-	10	mA
I_{CCO}	Output driver supply current, active mode	TBD	-	TBD	TBD	-	TBD	mA
I_{CCJ}	JTAG supply current, active mode	TBD	-	TBD	TBD	-	TBD	mA
I_{CCINTS}	Internal voltage supply current, standby mode	-	-	1	-	-	TBD	mA
I_{CCOS}	Output driver supply current, standby mode	TBD	-	TBD	TBD	-	TBD	mA
I_{CCJS}	JTAG supply current, standby mode	TBD	-	TBD	TBD	-	TBD	mA
I_{ILJ}	JTAG pins TMS, TDI, and TDO pull-up current	V_{CCJ} = max V_{IN} = GND	-	100	V_{CCJ} = max V_{IN} = GND	-	TBD	µA
I_{IL}	Input leakage current	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	–10	10	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	TBD	TBD	µA
I_{IH}	Input and output High-Z leakage current	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	–10	10	V_{CCINT} = max V_{IN} = GND or V_{CCINT}	TBD	TBD	µA
C_{IN}	Input capacitance	V_{IN} = GND f = 1.0 MHz	-	8	V_{IN} = GND f = 1.0 MHz	-	TBD	pF
C_{OUT}	Output capacitance	V_{IN} = GND f = 1.0 MHz	-	14	V_{IN} = GND f = 1.0 MHz	-	TBD	pF

AC Characteristics Over Operating Conditions



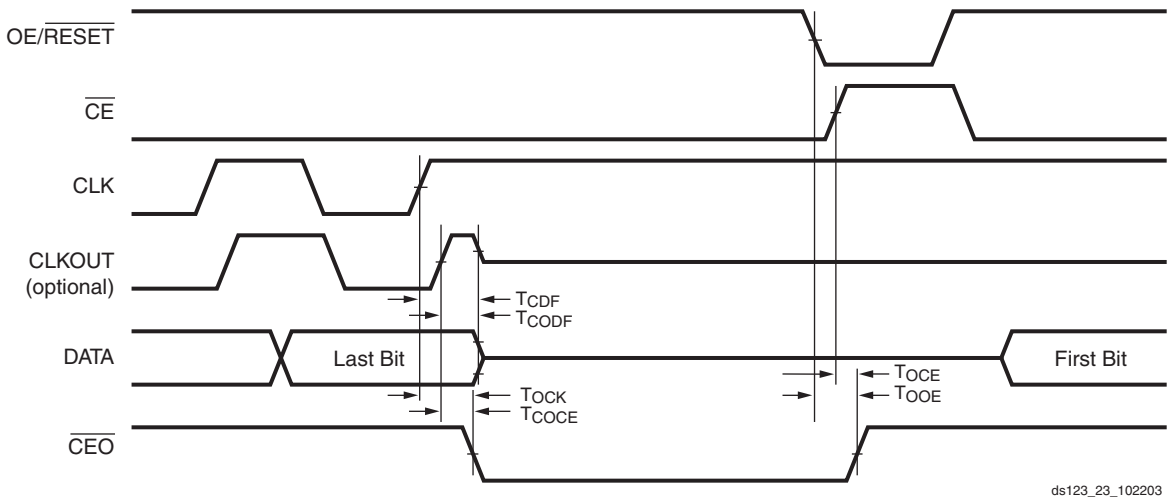
Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{OE}	OE/$\overline{RESET}$ to data delay[6] when V_{CCO} = 3.3V or 2.5V	-	10	TBD	TBD	ns
	OE/$\overline{RESET}$ to data delay[6] when V_{CCO} = 1.8V	-	30	TBD	TBD	ns
T_{CE}	$\overline{CE}$ to data delay[5] when V_{CCO} = 3.3V or 2.5V	-	15	TBD	TBD	ns
	$\overline{CE}$ to data delay[5] when V_{CCO} = 1.8V	-	30	TBD	TBD	ns
T_{CAC}	CLK to data delay when V_{CCO} = 3.3V or 2.5V	-	15	TBD	TBD	ns
	CLK to data delay when V_{CCO} = 3.3V or 2.5V	-	30	TBD	TBD	ns
T_{OH}	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or CLK when V_{CCO} = 3.3V or 2.5V	0	-	TBD	TBD	ns
	Data hold from $\overline{CE}$, OE/$\overline{RESET}$, or CLK when V_{CCO} = 1.8V	0	-	TBD	TBD	ns
T_{DF}	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay[2] when V_{CCO} = 3.3V or 2.5V	-	25	TBD	TBD	ns
	$\overline{CE}$ or OE/$\overline{RESET}$ to data float delay[2] when V_{CCO} = 1.8V	-	30	TBD	TBD	ns
T_{CYC}	Clock period[7] when V_{CCO} = 3.3V or 2.5V	30	-	TBD	TBD	ns
	Clock period when V_{CCO} = 1.8V	67	-	TBD	TBD	ns
T_{LC}	CLK Low time[3] when V_{CCO} = 3.3V or 2.5V	10	-	TBD	TBD	ns
	CLK Low time[3] when V_{CCO} = 1.8V	15	-	TBD	TBD	ns

Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{HC}	CLK High time(3) when V_{CCO} = 3.3V or 2.5V	10	-	TBD	TBD	ns
	CLK High time(3) when V_{CCO} = 1.8V	15	-	TBD	TBD	ns
T_{SCE}	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 3.3V or 2.5V	20	-	TBD	TBD	ns
	$\overline{CE}$ setup time to CLK (guarantees proper counting)(3) when V_{CCO} = 1.8V	30		TBD	TBD	ns
T_{HCE}	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 3.3V or 2.5V	250	-	TBD	TBD	ns
	$\overline{CE}$ hold time (guarantees counters are reset)(5) when V_{CCO} = 1.8V	250	-	TBD	TBD	ns
T_{HOE}	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 3.3V or 2.5V	250	-	TBD	TBD	ns
	OE/$\overline{RESET}$ hold time (guarantees counters are reset)(6) when V_{CCO} = 1.8V	250	-	TBD	TBD	ns
T_{SB}	BUSY setup time to CLK when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	BUSY setup time to CLK when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{HB}	BUSY hold time to CLK when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	BUSY hold time to CLK when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{CLKO}	CLK input to CLKOUT output delay when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	CLK input to CLKOUT output delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{CEC}	$\overline{CE}$ to CLKOUT delay when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	$\overline{CE}$ to CLKOUT delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{OEC}	OE/$\overline{RESET}$ to CLKOUT delay when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	OE/$\overline{RESET}$ to CLKOUT delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{CDD}	CLKOUT to data delay when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	CLKOUT to data delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{COH}	Data hold from CLKOUT when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	Data hold from CLKOUT when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{SXT}	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	$\overline{EN\_EXT\_SEL}$ setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{HXT}	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	$\overline{EN\_EXT\_SEL}$ hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{SRV}	REV_SEL setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	REV_SEL setup time to $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	TBD	TBD	ns

Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{HRV}	REV_SEL hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 3.3V or 2.5V	-	-	TBD	TBD	ns
	REV_SEL hold time from $\overline{CF}$ (rising edge) when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{FF}	CLKOUT default (fast) frequency	-	-	TBD	TBD	ns
	CLKOUT default (fast) frequency with compression	-	-	TBD	TBD	ns
T_{SF}	CLKOUT alternate (slower) frequency	-	-	TBD	TBD	ns
	CLKOUT alternate (slower) frequency with compression	-	-	TBD	TBD	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.
6. If T_{HOE} Low < 2 µs, T_{OE} = 2 µs.
7. Minimum possible T_{CYC}. Actual T_{CYC} = T_{CAC} + FPGA data setup time. If FPGA data setup time = 15 ns, actual T_{CYC} = 15 ns +15 ns = 30 ns.

AC Characteristics Over Operating Conditions When Cascading



Symbol	Description	XCF01S, XCF02S, XCF04S		XCF08P, XCF16P, XCF32P		Units
		Min	Max	Min	Max	
T_{CDF}	CLK to output float delay(2,3) when V_{CCO} = 2.5V or 3.3V	-	25	TBD	TBD	ns
	CLK to output float delay(2,3) when V_{CCO} = 1.8V	-	35	TBD	TBD	ns
T_{OCK}	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 2.5V or 3.3V	-	20	TBD	TBD	ns
	CLK to $\overline{CEO}$ delay(3,5) when V_{CCO} = 1.8V	-	35	TBD	TBD	ns
T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	TBD	TBD	ns
	$\overline{CE}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	35	TBD	TBD	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 2.5V or 3.3V	-	20	TBD	TBD	ns
	OE/$\overline{RESET}$ to $\overline{CEO}$ delay(3) when V_{CCO} = 1.8V	-	35	TBD	TBD	ns
T_{COCE}	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 2.5V or 3.3V	-	-	TBD	TBD	ns
	CLKOUT to $\overline{CEO}$ delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns
T_{CODF}	CLKOUT to output float delay when V_{CCO} = 2.5V or 3.3V	-	-	TBD	TBD	ns
	CLKOUT to output float delay when V_{CCO} = 1.8V	-	-	TBD	TBD	ns

Notes:
1. AC test load = 50 pF.
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. For cascaded PROMs minimum, $T_{CYC} = T_{OCK}$ + FPGA Data setup time.

Pinouts and Pin Descriptions

The XCFxxS Platform Flash PROM is available in the VO20 package. The XCFxxP Platform Flash PROM is available in the VO48 and FS48 packages. This section includes:

Notes:

1. VO20 denotes a 20-pin (TSSOP) Plastic Thin Shrink Small Outline Package
2. VO48 denotes a 48-pin (TSOP) Plastic Thin Small Outline Package.
3. FS48 denotes a 48-pin (TFBGA) Plastic Thin Fine Pitch Ball Grid Array (0.8 mm pitch).

XCFxxS Pinouts and Pin Descriptions

Table 11 provides a list of the pin names and descriptions for the XCFxxS 20-pin VO20 package.

Table 11: **XCFxxS Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	20-pin TSSOP (VO20)
D0	4	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped).	1
	3	Output Enable		
CLK	0	Data In	Configuration Clock Input. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High.	3
OE/$\overline{RESET}$	20	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA output is in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is not programmable.	8
	19	Data Out		
	18	Output Enable		
$\overline{CE}$	15	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA pins are put in a high-impedance state.	10
$\overline{CF}$	22	Data Out	Configuration Pulse (Open-Drain Output). Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	7
	21	Output Enable		
$\overline{CEO}$	12	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	13
	11	Output Enable		
TMS		Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	5

Table 11: **XCFxxS Pin Names and Descriptions *(Continued)***

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	20-pin TSSOP (VO20)
TCK		Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	6
TDI		Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	4
TDO		Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the system if the pin is not driven.	17
VCCINT			+3.3V Supply. Positive 3.3V supply voltage for internal logic.	18
VCCO			+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	19
VCCJ			+3.3V, 2.5V, or 1.8V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	20
GND			Ground	11
DNC			Do not connect. (These pins must be left unconnected.)	2, 9, 12, 14, 15, 16

XCFxxS Pinout Diagram

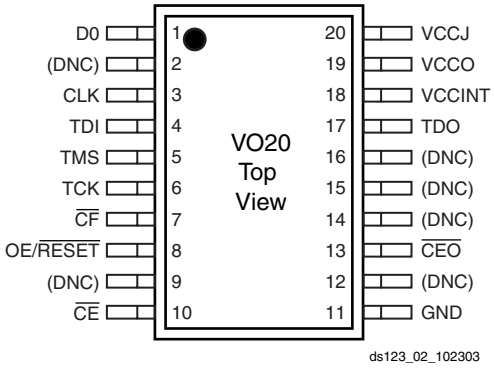


Figure 17: **VO20 Pinout Diagram (Top View) with Pin Names**

XCFxxP Pinouts and Pin Descriptions

Table 12 provides a list of the pin names and descriptions for the XCFxxP 48-pin VO48 and 48-pin FS48 packages.

Table 12: **XCFxxP Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP (VO48)	48-pin TFBGA (FS48)
D0	28	Data Out	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode. D0-D7 are the DATA output pins to provide parallel data for configuring a Xilinx FPGA in SelectMap (parallel) mode. The D0 output is set to a high-impedance state during ISPEN (when not clamped). The D1-D7 outputs are set to a high-impedance state during ISPEN (when not clamped) and when serial mode is selected for configuration. The D1-D7 pins can be left unconnected when the PROM is used in serial mode.	28	H6
	27	Output Enable			
D1	26	Data Out		29	H5
	25	Output Enable			
D2	24	Data Out		32	E5
	23	Output Enable			
D3	22	Data Out		33	D5
	21	Output Enable			
D4	20	Data Out		43	C5
	19	Output Enable			
D5	18	Data Out		44	B5
	17	Output Enable			
D6	16	Data Out		47	A5
	15	Output Enable			
D7	14	Data Out		48	A6
	13	Output Enable			
CLK	01	Data In	Configuration Clock Input. An internal programmable control bit selects between the internal oscillator and the CLK input pin as the clock source to control the configuration sequence. Each rising edge on the CLK input increments the internal address counter if the CLK input is selected, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High.	12	B3
OE/$\overline{RESET}$	04	Data In	Output Enable/Reset (Open-Drain I/O). When Low, this input holds the address counter reset and the DATA and CLKOUT outputs are placed in a high-impedance state. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is not programmable.	11	A3
	03	Data Out			
	02	Output Enable			
$\overline{CE}$	00	Data In	Chip Enable Input. When $\overline{CE}$ is High, the device is put into low-power standby mode, the address counter is reset, and the DATA and CLKOUT outputs are placed in a high-impedance state.	13	B4
$\overline{CF}$	11	Data In	Configuration Pulse (Open-Drain I/O). As an output, this pin allows JTAG CONFIG instruction to initiate FPGA configuration without powering down the FPGA. This is an open-drain signal that is pulsed Low by the JTAG CONFIG command. As an input, when Low, this signal enables the device to sample the current design revision selection.	6	D1
	10	Data Out			
	09	Output Enable			

Table 12: **XCFxxP Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP (VO48)	48-pin TFBGA (FS48)
$\overline{CEO}$	06	Data Out	Chip Enable Output. Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. $\overline{CEO}$ returns to High when OE/$\overline{RESET}$ goes Low or $\overline{CE}$ goes High.	10	D2
	05	Output Enable			
$\overline{EN\_EXT\_SEL}$	31	Data In	Enable External Selection Input. When this pin is Low, design revision selection is controlled by the Revision Select pins. When this pin is High, design revision selection is controlled by the internal programmable Revision Select control bits. $\overline{EN\_EXT\_SEL}$ has an internal 50KΩ resistive pull-up to V_{CCO} to provide a logic "1" to the device if the pin is not driven.	25	H4
REV_SEL0	30	Data In	Revision Select[1:0] Inputs. When the $\overline{EN\_EXT\_SEL}$ is Low, the Revision Select pins are used to select the design revision to be enabled, overriding the internal programmable Revision Select control bits. The Revision Select[1:0] inputs have an internal 50KΩ resistive pull-up to VCCO to provide a logic "1" to the device if the pins are not driven.	26	G3
REV_SEL1	29	Data In		27	G4
BUSY	12	Data In	Busy Input. The BUSY input is enabled when parallel mode is selected for configuration. When BUSY is High, the internal address counter stops incrementing and the current data remains on the data pins. On the first rising edge of CLK after BUSY transitions from High to Low, the data for the next address is driven on the data pins. When serial mode or decompression is enabled during device programming, the BUSY input is disabled. BUSY has an internal 50KΩ resistive pull-down to GND to provide a logic "0" to the device if the pin is not driven.	5	C1
CLKOUT	08	Data Out	Configuration Clock Output. An internal Programmable control bit enables the CLKOUT signal which is sourced from either the internal oscillator or the CLK input pin. Each rising edge on the selected clock source increments the internal address counter if data is available, $\overline{CE}$ is Low, and OE/$\overline{RESET}$ is High. Output data is available on the rising edge of CLKOUT. CLKOUT remains Low when data is not ready. When CLKOUT is not enabled , the CLKOUT pin is put into a high-impedance state.	9	C2
	07	Output Enable			
TMS		Mode Select	JTAG Mode Select Input. The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	21	E2
TCK		Clock	JTAG Clock Input. This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	20	H3
TDI		Data In	JTAG Serial Data Input. This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the device if the pin is not driven.	19	G1

Table 12: **XCFxxP Pin Names and Descriptions**

Pin Name	Boundary Scan Order	Boundary Scan Function	Pin Description	48-pin TSOP (VO48)	48-pin TFBGA (FS48)
TDO		Data Out	JTAG Serial Data Output. This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50KΩ resistive pull-up to V_{CCJ} to provide a logic "1" to the system if the pin is not driven.	22	E6
VCCINT			+1.8V Supply. Positive 1.8V supply voltage for internal logic.	4, 15, 34	B1, E1, G6
VCCO			+3.3V, 2.5V, or 1.8V I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the output voltage drivers and input buffers.	8, 30, 38, 45	B2, C6, D6, G5
VCCJ			+3.3V, 2.5V, or 1.8V JTAG I/O Supply. Positive 3.3V, 2.5V, or 1.8V supply voltage connected to the TDO output voltage driver and TCK, TMS, and TDI input buffers.	24	H2
GND			Ground	2, 7, 17, 23, 31, 36, 46	A1, A2, B6, F1, F5, F6, H1
DNC			Do Not Connect. (These pins must be left unconnected.)	1, 3, 14, 16, 18, 35, 37, 39, 40, 41, 42	A4, C3, C4, D3, D4, E3, E4, F2, F3, F4, G2

XCFxxP Pinout Diagrams

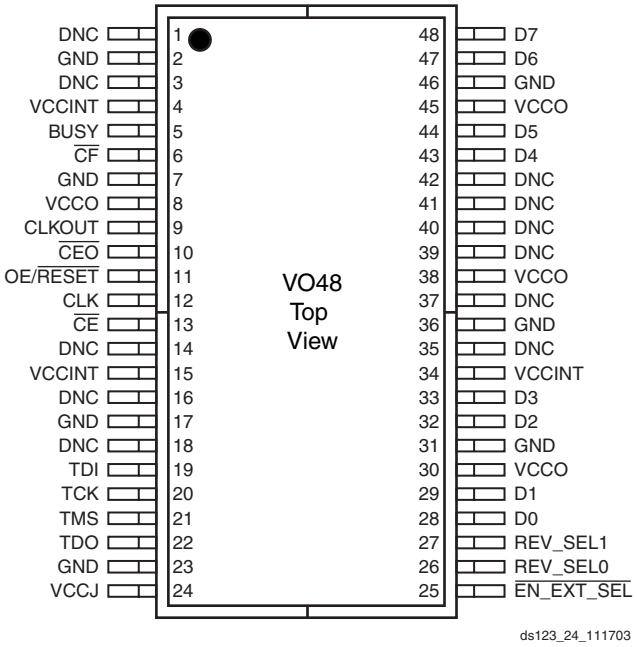


Figure 18: **VO48 Pinout Diagram (Top View) with Pin Names**

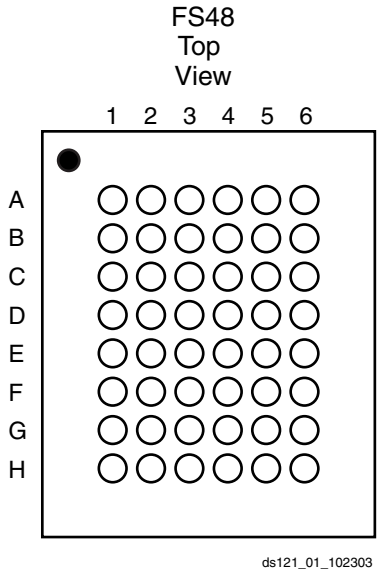
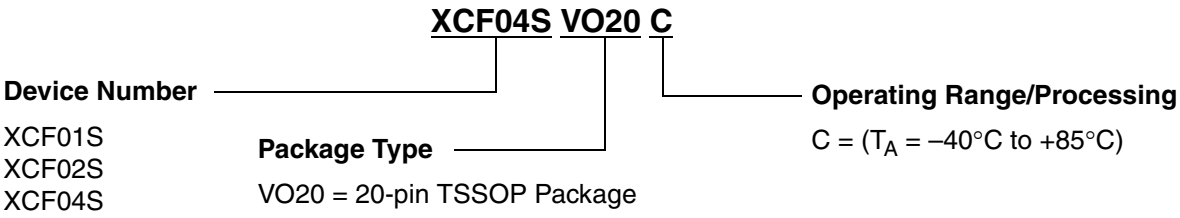


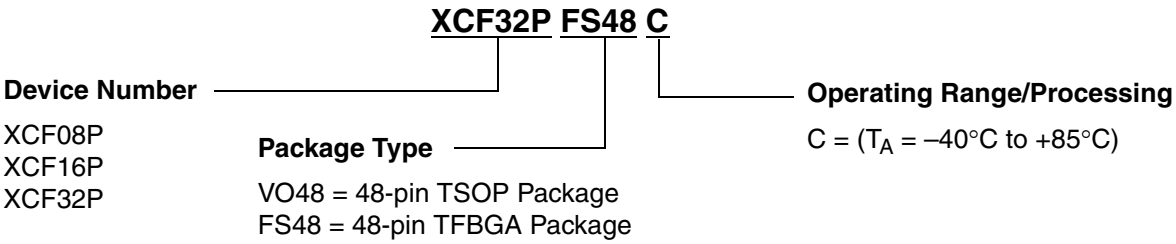
Figure 19: **FS48 Pinout Diagram (Top View)**

Table 13: **FS48 Pin Number/Name Reference**

Pin Number	Pin Name	Pin Number	Pin Name
A1	GND	E1	VCCINT
A2	GND	E2	TMS
A3	OE/$\overline{\text{RESET}}$	E3	DNC
A4	DNC	E4	DNC
A5	D6	E5	D2
A6	D7	E6	TDO
B1	VCCINT	F1	GND
B2	VCCO	F2	DNC
B3	CLK	F3	DNC
B4	$\overline{\text{CE}}$	F4	DNC
B5	D5	F5	GND
B6	GND	F6	GND
C1	BUSY	G1	TDI
C2	CLKOUT	G2	DNC
C3	DNC	G3	REV_SEL0
C4	DNC	G4	REV_SEL1
C5	D4	G5	VCCO
C6	VCCO	G6	VCCINT
D1	$\overline{\text{CF}}$	H1	GND
D2	$\overline{\text{CEO}}$	H2	VCCJ
D3	DNC	H3	TCK
D4	DNC	H4	$\overline{\text{EN\_EXT\_SEL}}$
D5	D3	H5	D1
D6	VCCO	H6	D0

Ordering Information

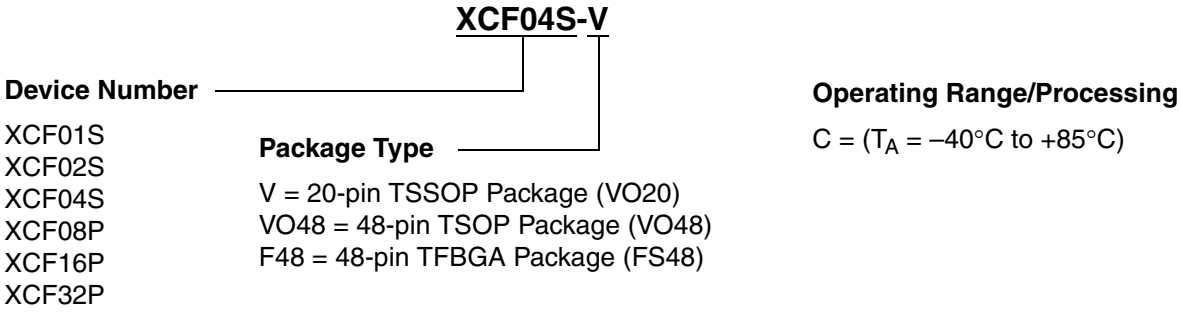




Valid Ordering Combinations

XCF01SVO20 C	XCF08PVO48 C	XCF08PFS48 C
XCF02SVO20 C	XCF16PVO48 C	XCF16PFS48 C
XCF04SVO20 C	XCF32PVO48 C	XCF32PFS48 C

Marking Information



Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/29/03	1.0	Xilinx Initial Release.
06/03/03	1.1	Made edits to all pages.
11/05/03	2.0	Major revision.
11/18/03	2.1	Pinout corrections as follows: • Table 12: - For VO48 package, removed 38 from VCCINT and added it to VCCO. - For FS48 package, removed pin D6 from VCCINT and added it to VCCO. • Table 13 (FS48 package): - For pin D6, changed name from VCCINT to VCCO. - For pin A4, changed name from GND to DNC. • Figure 18 (VO48 package): For pin 38, changed name from VCCINT to VCCO.