

# NCP1217

## Enhanced PWM Current-Mode Controller for High-Power Universal Off-Line Supplies

Housed in an SO-8 or PDIP-7 package, the NCP1217 represents the enhanced version of the NCP1203-based controllers. Thanks to its high drive capability, NCP1217 drives large gate-charge MOSFETs, which together with internal ramp compensation and built-in overvoltage protection, ease the design of modern AC/DC adapters. NCP1217 offers a true alternative to UC384X-based designs.

With an internal structure operating at different fixed frequencies (65–100–133 kHz), the controller features a high-voltage start-up FET, which ensures a clean and loss less start-up sequence. Its current-mode control topology provides an excellent input audio-susceptibility and inherent pulse-by-pulse control. Internal ramp compensation easily prevents subharmonic oscillations from taking place in continuous conduction mode designs.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so-called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1217 features two efficient protective circuitries: 1) In presence of an overcurrent condition, the output pulses are disabled and the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto-recovers. 2) If an external signal (e.g. a temperature sensor) pulls pin1 above 3.2 V, output pulses are immediately stopped and the NCP1217 stays latched in this position. Reset occurs when the  $V_{CC}$  collapses to ground, e.g. the user unplugs the power supply.

### Features

- Current-Mode with Adjustable Skip-Cycle Capability
- Built-in Internal Ramp Compensation
- Auto-Recovery Internal Output Short-Circuit Protection
- Full Latch-Off if Adjustment Pin is Brought High
- Extremely Low No-Load Standby Power
- Internal Temperature Shutdown
- 500 mA Peak Current Capability
- Fixed Frequency Versions at 65 kHz, 100 kHz and 133 kHz
- Direct Optocoupler Connection
- Internal Leading Edge Blanking
- SPICE Models Available for TRANSient and AC Analysis

### Typical Applications

- High Power AC/DC Converters for TVs, Set-Top Boxes, etc.
- Offline Adapters for Notebooks
- Telecom DC-DC Converters
- All Power Supplies

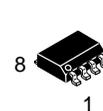


ON Semiconductor®

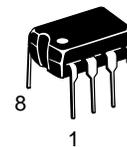
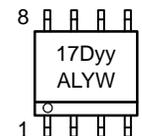
<http://onsemi.com>

## MINIATURE PWM CONTROLLER FOR HIGH POWER AC/DC WALL ADAPTERS AND OFFLINE BATTERY CHARGERS

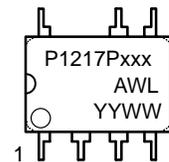
### MARKING DIAGRAMS



SO-8  
D SUFFIX  
CASE 751

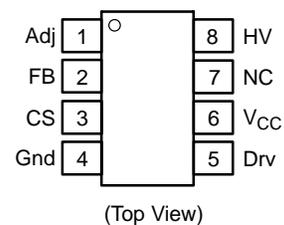


PDIP-7  
P SUFFIX  
CASE 626B



xxx = Device Code: 065, 100 or 133  
yy = Device Code:  
06 for 65  
10 for 100  
13 for 133  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week

### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

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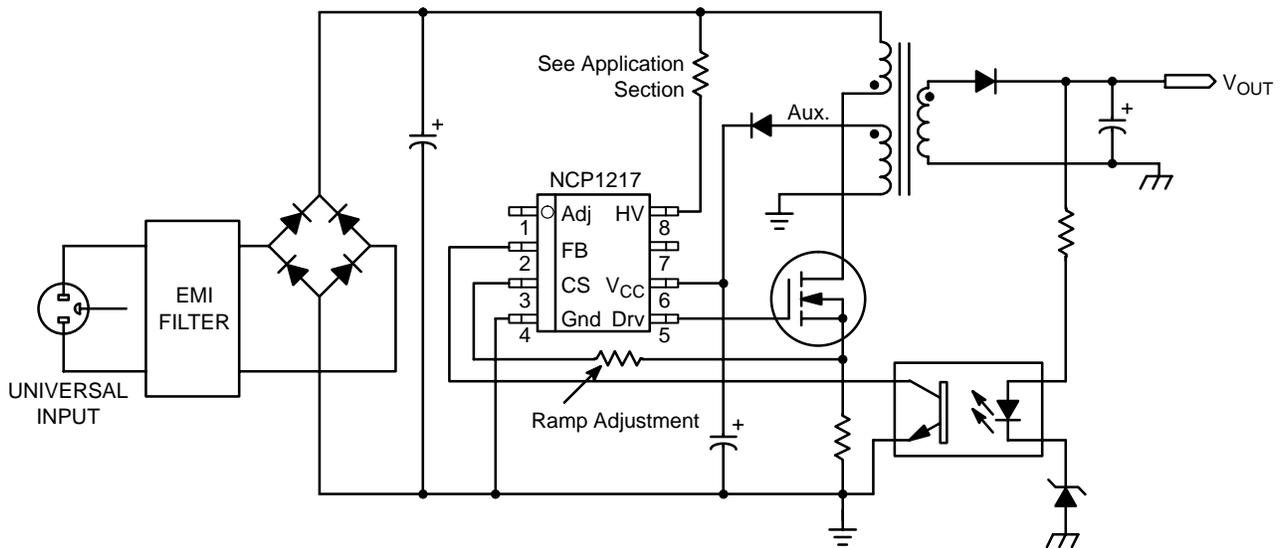
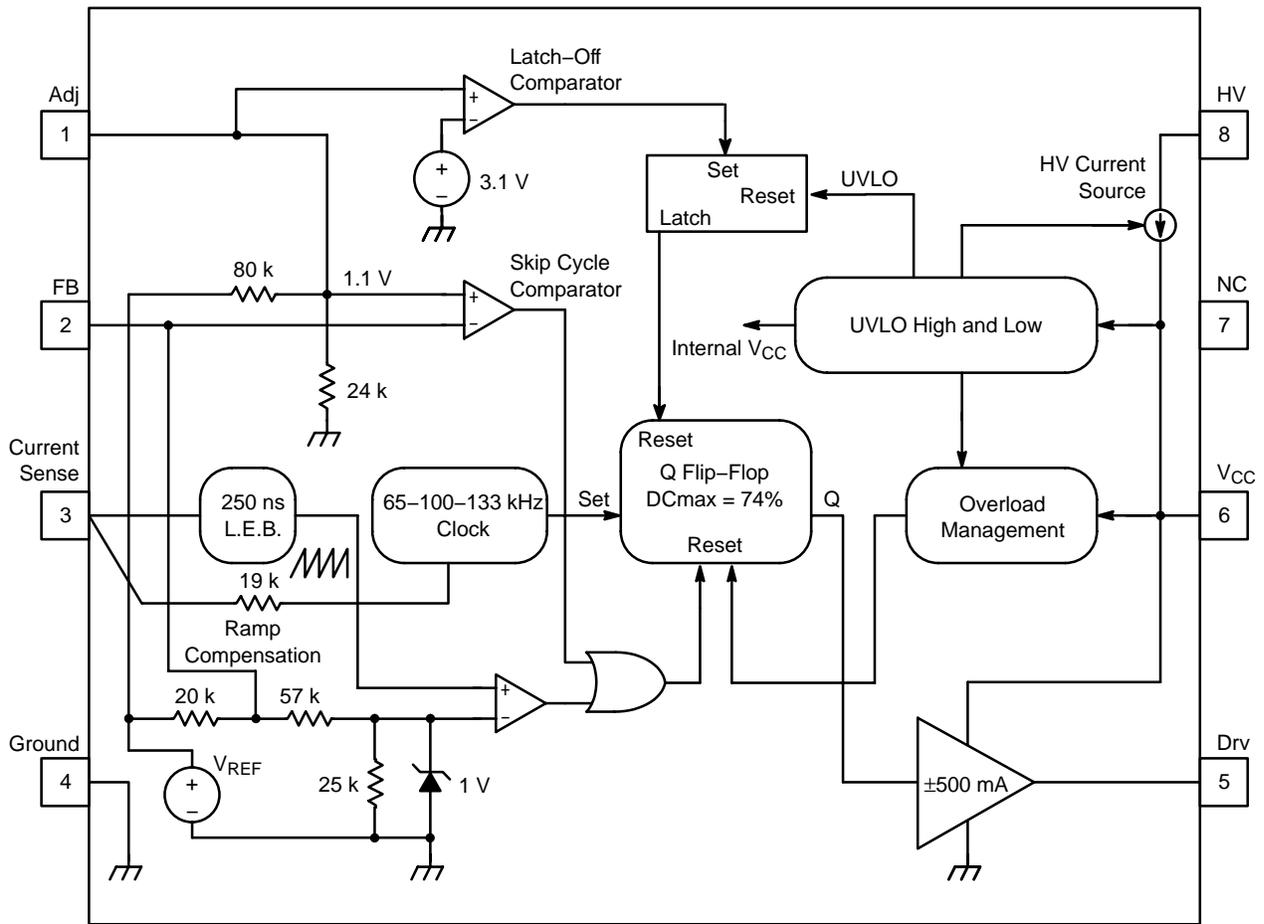


Figure 1. Typical Application Example

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Description
1	Adj	Adjust the skipping peak current	This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground permanently disables the skip cycle feature. By bringing this pin above 3.1 V, you permanently shut off the device.
2	FB	Sets the peak current setpoint	By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand.
3	CS	Current sense input	This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the amount of ramp compensation you need.
4	Gnd	The IC ground	-
5	Drv	Driving pulses	The driver's output to an external MOSFET.
6	V <sub>CC</sub>	Supplies the IC	This pin is connected to an external bulk capacitor of typically 22 μF.
7	NC	-	This unconnected pin ensures adequate creepage distance.
8	HV	Ensures a clean and lossless start-up sequence	Connected to the high-voltage rail, this pin injects a constant current into the V <sub>CC</sub> capacitor during the start-up sequence.

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**Figure 2. Internal Circuit Architecture**

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC}$	16	V
Power Supply Voltage on All Other Pins Except Pin 8 (HV), Pin 6 ( $V_{CC}$ ) and Pin 5 (Drv)	–	–0.3 to 10	V
Maximum Voltage on Pin 8 (HV), Pin 6 ( $V_{CC}$ ) Decoupled to Ground with 10 $\mu$ F	$V_{HV}$	500	V
Maximum Voltage on Pin 8 (HV), Pin 6 ( $V_{CC}$ ) Grounded	$V_{HV}$	450	V
Maximum Current into All Pins Except $V_{CC}$ (6) and HV (8) when 10 V ESD Diodes are Activated	–	5.0	mA
Thermal Resistance, Junction-to-Case	$R_{\theta J-C}$	57	$^{\circ}$ C/W
Thermal Resistance, Junction-to-Air, PDIP-7 Version	$R_{\theta J-A}$	100	$^{\circ}$ C/W
Thermal Resistance, Junction-to-Air, SO-8 Version	$R_{\theta J-A}$	178	$^{\circ}$ C/W
Maximum Junction Temperature	$T_{JMAX}$	150	$^{\circ}$ C
Temperature Shutdown	–	155	$^{\circ}$ C
Hysteresis in Shutdown	–	30	$^{\circ}$ C
Storage Temperature Range	–	–60 to +150	$^{\circ}$ C
ESD Capability, HBM Model (All Pins Except $V_{CC}$ and HV)	–	2.0	kV
ESD Capability, Machine Model	–	200	V

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**ELECTRICAL CHARACTERISTICS** (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+125^\circ\text{C}$ , Max  $T_J = 150^\circ\text{C}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
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## SUPPLY SECTION (All frequency versions, unless otherwise noted)

Turn-On Threshold Level, $V_{CC}$ Going Up	6	$V_{CC_{ON}}$	11.8	12.8	13.8	V
Minimum Operating Voltage After Turn-On	6	$V_{CC_{min}}$	6.9	7.6	8.3	V
$V_{CC}$ Decreasing Level at which the Latch-Off Phase Ends	6	$V_{CC_{latch}}$	–	5.6	–	V
Internal IC Consumption, No Output Load on Pin 5, $F_{SW} = 65\text{ kHz}$	6	ICC1	–	960	1110 (Note 1)	$\mu\text{A}$
Internal IC Consumption, No Output Load on Pin 5, $F_{SW} = 100\text{ kHz}$	6	ICC1	–	1020	1180 (Note 1)	$\mu\text{A}$
Internal IC Consumption, No Output Load on Pin 5, $F_{SW} = 133\text{ kHz}$	6	ICC1	–	1060	1200 (Note 1)	$\mu\text{A}$
Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW} = 65\text{ kHz}$	6	ICC2	–	1.7	2.0 (Note 1)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW} = 100\text{ kHz}$	6	ICC2	–	2.1	2.4 (Note 1)	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW} = 133\text{ kHz}$	6	ICC2	–	2.4	2.9 (Note 1)	mA
Internal IC Consumption, Latch-Off Phase, $V_{CC} = 6.0\text{ V}$	6	ICC3	–	230	–	$\mu\text{A}$

## INTERNAL START-UP CURRENT SOURCE ( $T_J > 0^\circ\text{C}$ )

High-Voltage Current Source, $V_{CC} = 10\text{ V}$	8	IC1	3.5 (Note 2)	6.0	7.8	mA
High-Voltage Current Source, $V_{CC} = 0$	8	IC2	–	7.0	–	mA

## DRIVE OUTPUT

Output Voltage Rise-Time @ $CL = 1.0\text{ nF}$ , 10–90% of a 12 V Output Signal	5	$T_r$	–	60	–	ns
Output Voltage Fall-Time @ $CL = 1.0\text{ nF}$ , 10–90% of a 12 V Output Signal	5	$T_f$	–	20	–	ns
Source Resistance	5	$R_{OH}$	15	20	35	$\Omega$
Sink Resistance	5	$R_{OL}$	5.0	10	18	$\Omega$

## CURRENT COMPARATOR (Pin 5 Unloaded)

Input Bias Current @ 1.0 V Input Level on Pin 3	3	$I_{IB}$	–	0.02	–	$\mu\text{A}$
Maximum Internal Current Setpoint	3	$I_{Limit}$	0.9	1.0	1.1	V
Default Internal Current Setpoint for Skip Cycle Operation	3	$I_{Lskip}$	–	330	–	mV
Propagation Delay from Current Detection to Gate OFF State	3	$T_{DEL}$	–	90	150	ns
Leading Edge Blanking Duration	3	$T_{LEB}$	–	250	–	ns

## INTERNAL OSCILLATOR ( $V_{CC} = 11\text{ V}$ , Pin 5 Loaded by 1.0 k $\Omega$ )

Oscillation Frequency, 65 kHz Version	–	$f_{OSC}$	58.5	65	71.5	kHz
Oscillation Frequency, 100 kHz Version	–	$f_{OSC}$	90	100	110	kHz
Oscillation Frequency, 133 kHz Version	–	$f_{OSC}$	120	133	146	kHz
Maximum Duty-Cycle, NCP1217	–	$D_{max}$	69	74	80	%

1. Maximum Value @  $T_J = 0^\circ\text{C}$ .
2. Minimum Value @  $T_J = 125^\circ\text{C}$ .

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**ELECTRICAL CHARACTERISTICS** (continued) (For typical values  $T_J = 25^\circ\text{C}$ , for min/max values  $T_J = 0^\circ\text{C}$  to  $+125^\circ\text{C}$ , Max  $T_J = 150^\circ\text{C}$ ,  $V_{CC} = 11\text{ V}$  unless otherwise noted.)

Characteristic	Pin	Symbol	Min	Typ	Max	Unit
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**FEEDBACK SECTION** ( $V_{CC} = 11\text{ V}$ , Pin 5 Loaded by  $1.0\text{ k}\Omega$ )

Internal Pull-Up Resistor	2	Rup	–	19	–	$\text{k}\Omega$
Pin 2 (FB) to Internal Current Setpoint Division Ratio	–	Iratio	–	3.3	–	–

**SKIP CYCLE GENERATION**

Default Skip Mode Level	1	Vskip	0.93	1.1	1.26	V
Pin 1 Internal Output Impedance	1	Zout	–	27	–	$\text{k}\Omega$

**INTERNAL RAMP COMPENSATION**

Internal Ramp Level @ $25^\circ\text{C}$ (Note 3)	3	Vramp	2.6	2.9	3.2	V
Internal Ramp Resistance to CS Pin	3	Rramp	–	19	–	$\text{k}\Omega$

**ADJUSTMENT LATCH-OFF LEVEL**

Latching Level	1	Vlatch	2.69	3.10	3.42	V
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3. A  $1.0\text{ M}\Omega$  resistor is connected to the ground for the measurement.

## TYPICAL CHARACTERISTICS

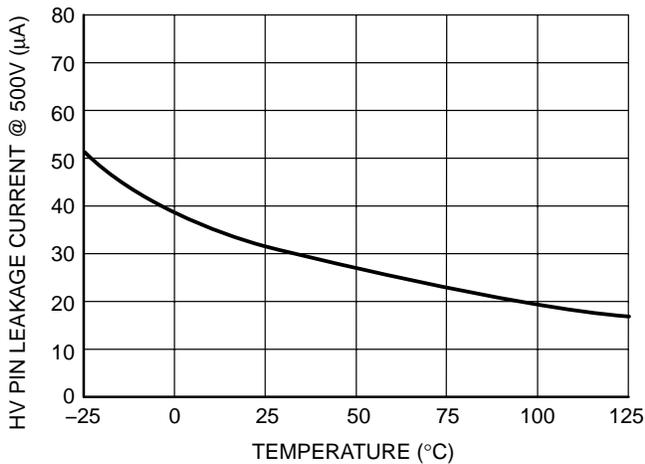


Figure 3. High Voltage Pin Leakage Current vs. Temperature

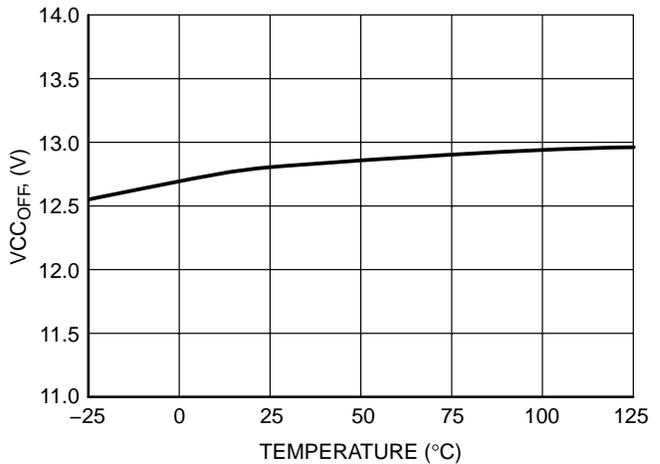


Figure 4.  $V_{CCOFF}$  vs. Temperature

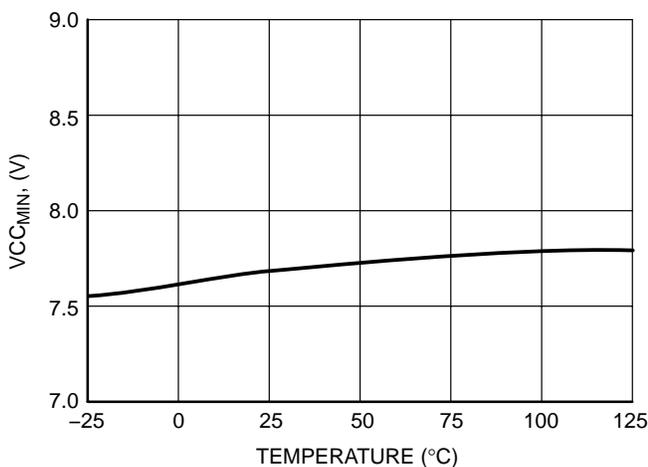


Figure 5.  $V_{CCMIN}$  vs. Temperature

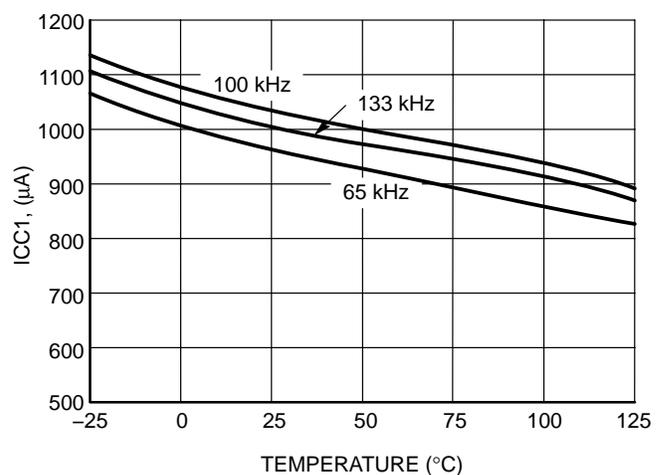


Figure 6.  $ICC1$  (@  $V_{CC} = 11\text{ V}$ ) vs. Temperature

TYPICAL CHARACTERISTICS (continued)

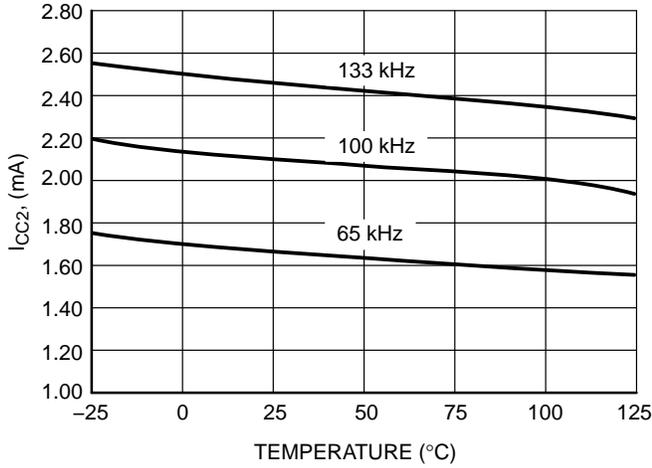


Figure 7. ICC2 vs. Temperature

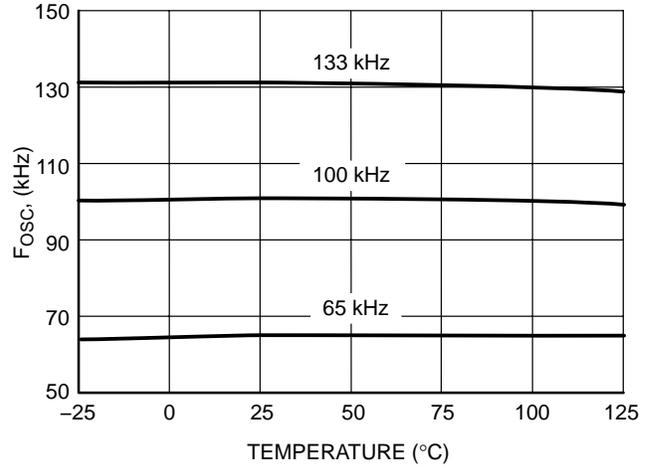


Figure 8. Switching Frequency vs. Temperature

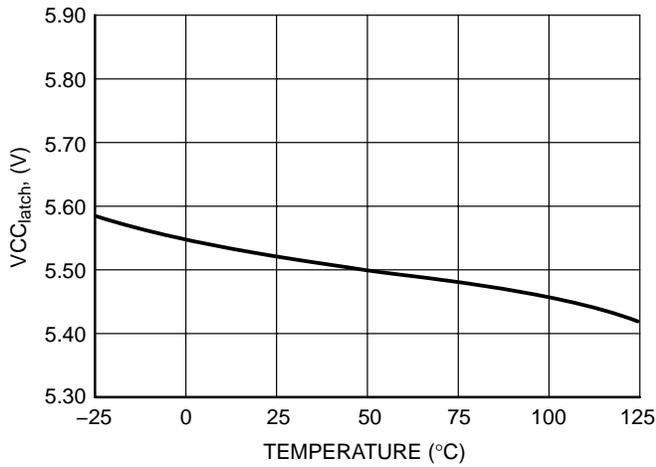


Figure 9. VCC\_latch vs. Temperature

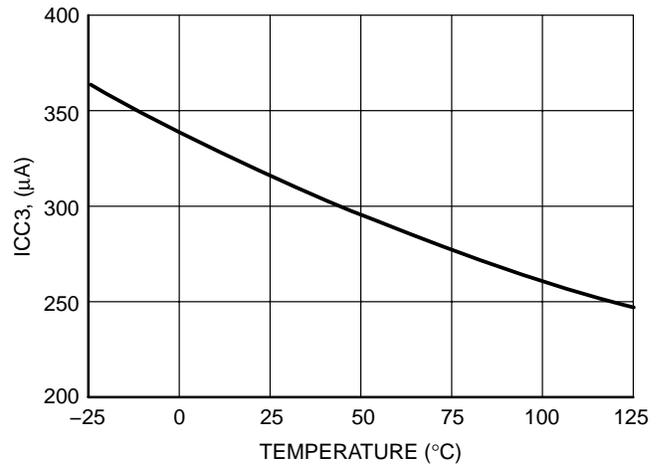


Figure 10. ICC3 vs. Temperature

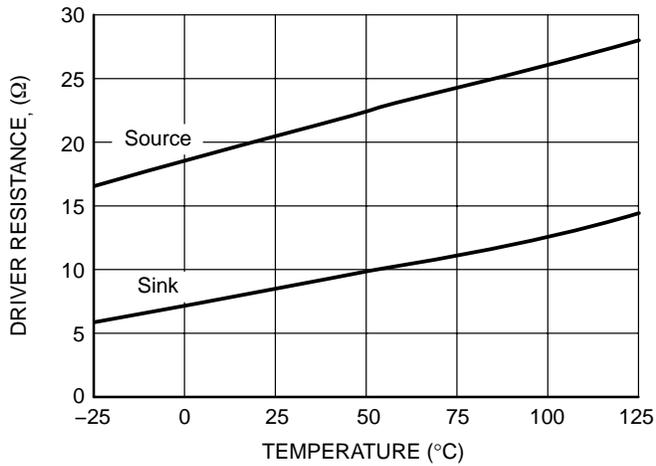


Figure 11. Drive Sink and Source Resistance vs. Temperature

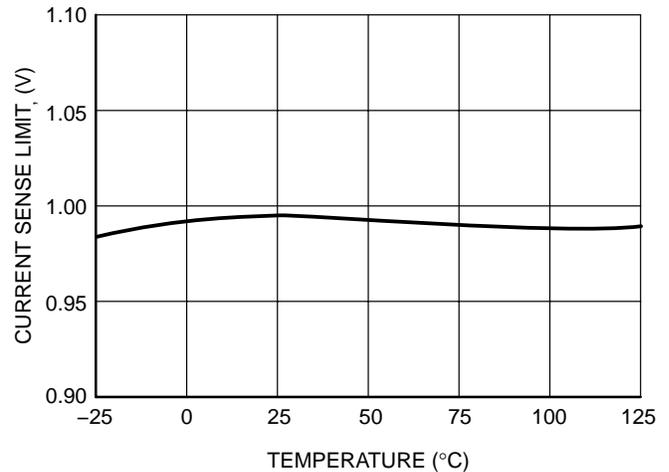


Figure 12. Current Sense Limit vs. Temperature

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## TYPICAL CHARACTERISTICS (continued)

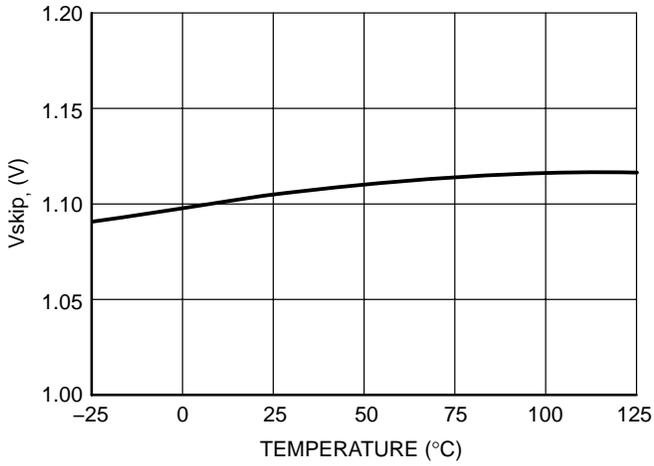


Figure 13. Vskip vs. Temperature

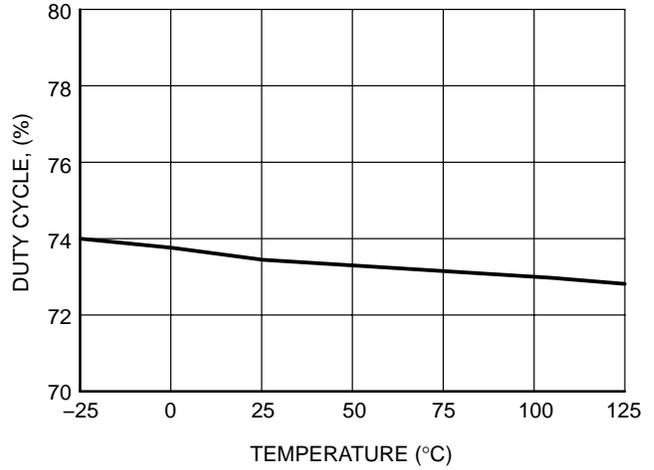


Figure 14. Max Duty-Cycle vs. Temperature

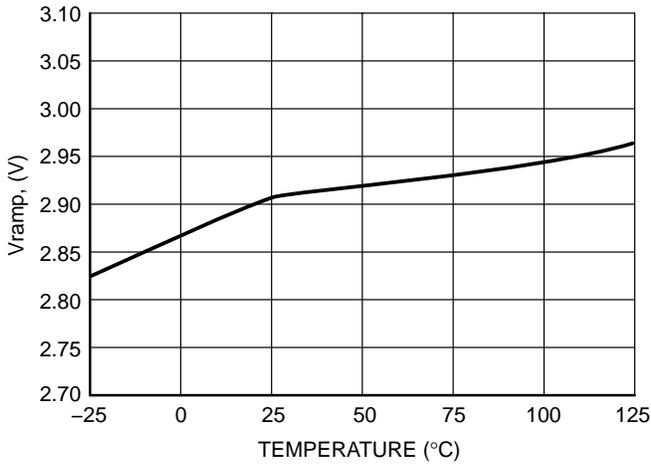


Figure 15. Vramp vs. Temperature

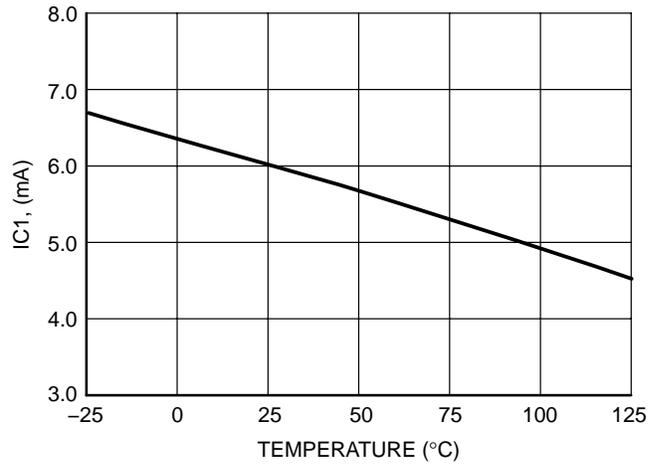


Figure 16. High Voltage Current Source (@ Vcc=10V) vs. Temperature

## APPLICATION INFORMATION

**Introduction**

The NCP1217 implements a standard current mode architecture where the switch-off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part-count is the key parameter, particularly in low-cost AC/DC adapters, TV power supplies, etc. Due to its high-performance High-Voltage technology, the NCP1217 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low-pass filter and start-up device but also enhances the original component by offering: 1) an externally triggerable latch-off 2) ramp compensation and finally, 3) short-circuit protection. Due to its high-voltage current source, ON Semiconductor's NCP1217 does not need an external start-up resistance but supplies the start-up current directly from the high-voltage rail. On the other hand, more and more applications are requiring low no-load standby power, e.g. for AC/DC adapters, VCRs, etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1217 elegantly solves this problem by skipping unwanted switching cycles at a user-adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise-free operation:

**Current-Mode Operation:** As the UC384X series, the NCP1217 features a well-known current mode control architecture which provides superior input audio-susceptibility compared to traditional voltage-mode controllers. Primary current pulse-by-pulse checking together with a fast over current comparator offers greater security in the event of a difficult fault condition, e.g. a saturating transformer.

**Ramp Compensation:** By inserting a resistor between the current-sense (CS) pin and the actual sense resistor, it becomes possible to inject a given amount of ramp compensation since the internal saw tooth clock is routed to the CS pin. Subharmonic oscillations in Continuous Conduction Mode (CCM) can thus be compensated via a single resistor.

**Adjustable Skip Cycle Level:** By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise-free operation with cheap transformers. Skip cycle offers a proven mean to reduce the standby power in no or light loads situations.

**Wide Switching-Frequency Offer:** Three different options are available: 65 kHz-100 kHz-133 kHz. Depending on the application, the designer can pick up the right device to help

reducing magnetics or improve the EMI signature before reaching the 150 kHz starting point.

**Over Current Protection (OCP):** By continuously monitoring the Vcc auxiliary winding voltage, NCP1217 enters burst mode as soon as the power supply undergoes an overload: when the Vcc voltage goes down until it crosses the undervoltage lockout level (Vccmin). When the NCP1217 reaches this level (typically 7.6 V), it stops the switching pulses until the Vcc pin voltage reaches Vcclatch (5.6 V). At Vcclatch, the NCP1217 attempts to restart. As soon as the default disappears, the power supply resumes operation.

**Over Voltage Protection (OVP):** If pin1 is brought to a level higher than the internal 3.2 V reference voltage, the controller is permanently shut down until the user cycles the VCC OFF and ON again. This allows the building of efficient and low-cost over voltage protection circuits.

**Wide Duty-Cycle Operation:** Wide mains operation requires a large duty-cycle excursion. The NCP1217 can go up to 74% typically.

**Low Standby-Power:** If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP1217 drastically reduces the power wasted during light load conditions. In no-load conditions, the NPC1217 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.

**No Acoustic Noise While Operating:** Instead of skipping cycles at high peak currents, the NCP1217 waits until the peak current demand falls below a user-adjustable 1/3 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer ... You can thus select cheap magnetic components free of noise problems.

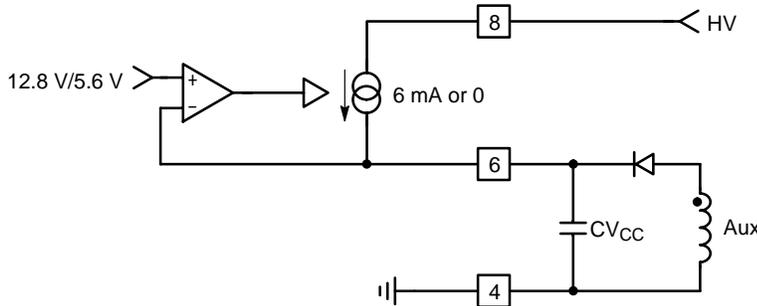
**External MOSFET Connection:** By leaving the external MOSFET external to the IC, you can select avalanche proof devices, which in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).

**SPICE Model:** A dedicated model to run transient cycle-by-cycle simulations is available but also an averaged version to help you closing the loop. Ready-to-use templates can be downloaded in OrCAD's Pspice and INTUSOFT's IsSpice from ON Semiconductor web site, NCP1217 related section.

**Start-Up Sequence**

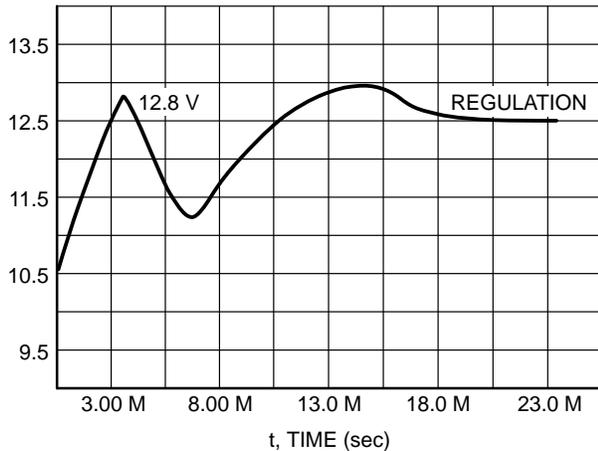
When the power supply is first powered from the mains outlet, the internal current source (typically 7.0 mA) is biased and charges up the  $V_{CC}$  capacitor. When the voltage on this  $V_{CC}$  capacitor reaches the  $V_{CC_{ON}}$  level (typically

12.8 V), the current source turns off and no longer wastes any power. At this time, the  $V_{CC}$  capacitor only supplies the controller and the auxiliary supply is supposed to take over before  $V_{CC}$  collapses below  $V_{CC_{min}}$ . Figure 17 shows the internal arrangement of this structure.



**Figure 17. The Current Source Brings  $V_{CC}$  Above 12.8 V and then Turns Off**

Once the power supply has started, the  $V_{CC}$  shall be constrained below 16 V, which is the maximum rating on pin 6. Figure 18 portrays a typical start-up sequence with a  $V_{CC}$  regulated at 12.5 V.



**Figure 18. A Typical Start-Up Sequence for the NCP1217**

**Overload Operation**

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short-circuit protection. A short-circuit actually forces the output voltage to be at a low

level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1217 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty-cycle. The system auto-recovers when the fault condition disappears.

During the start-up phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self-supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage lockout level of typically 7.6 V. When this happens, NCP1217 immediately stops the switching pulses and unbiases all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the  $V_{CC}$  slowly falls down. As soon as  $V_{CC}$  reaches typically 5.6 V, the start-up source turns-on again and a new start-up sequence occurs, bringing  $V_{CC}$  toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 19 portrays the typical operating signals in short circuit.

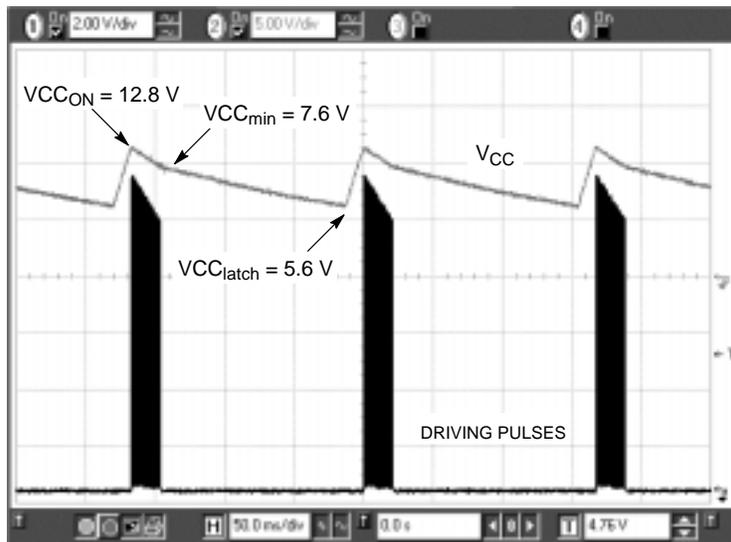


Figure 19. Typical Waveforms in Short Circuit Conditions

**Calculating the V<sub>CC</sub> Capacitor**

The V<sub>CC</sub> capacitor can be calculated knowing the IC consumption as soon as V<sub>CC</sub> reaches 12.8 V. Suppose that a NCP1217P065 is used and drives a MOSFET with a 30 nC total gate charge (Q<sub>g</sub>). The total average current is thus made of I<sub>CC1</sub> (750 μA) plus the driver current, F<sub>sw</sub> \* Q<sub>g</sub> = 1.95 mA. The total current is therefore 2.7 mA. The ΔV available to fully start-up the circuit (e.g. never reach the 8.2 V V<sub>CC\_min</sub> during power on) is 13.7–8.2 = 5.5 V best case or 4.9 V worse case (11.9–7.0). We have a capacitor that then needs to supply the NCP1217 with 2.7 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms. CV<sub>CC</sub> is calculated using the equation  $C = \frac{\Delta t \cdot i}{\Delta V}$  or  $C \geq 8.3 \mu\text{F}$ . Select a 22 μF/25 V and this will fit.

**Skipping Cycle Mode**

The NCP1217 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (V<sub>pin 1</sub>), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so-called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 21). Suppose we have the following component values:

- L<sub>p</sub>, primary inductance = 350 μH
- F<sub>sw</sub>, switching frequency = 65 kHz
- I<sub>p skip</sub> = 600 mA (or 333 mV/R<sub>sense</sub>)

The theoretical power transfer is therefore:  $\frac{1}{2} \cdot L_p \cdot I_p^2 \cdot F_{sw} = 4.1 \text{ W}$ . If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: 4.1 \* 0.1 = 410 mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight.

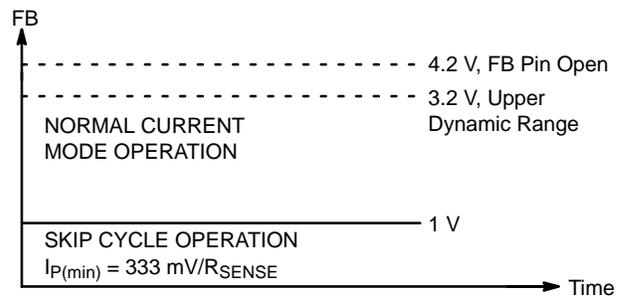


Figure 20.

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/R<sub>sense</sub>. When the IC enters the skip cycle mode, the peak current cannot go below V<sub>pin1</sub>/3.3. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. In this later case, care must be taken to keep sufficient margin between this pin 1 adjustment level and the latch-off level. Grounding pin 1 permanently invalidates the skip cycle operation.

# NCP1217

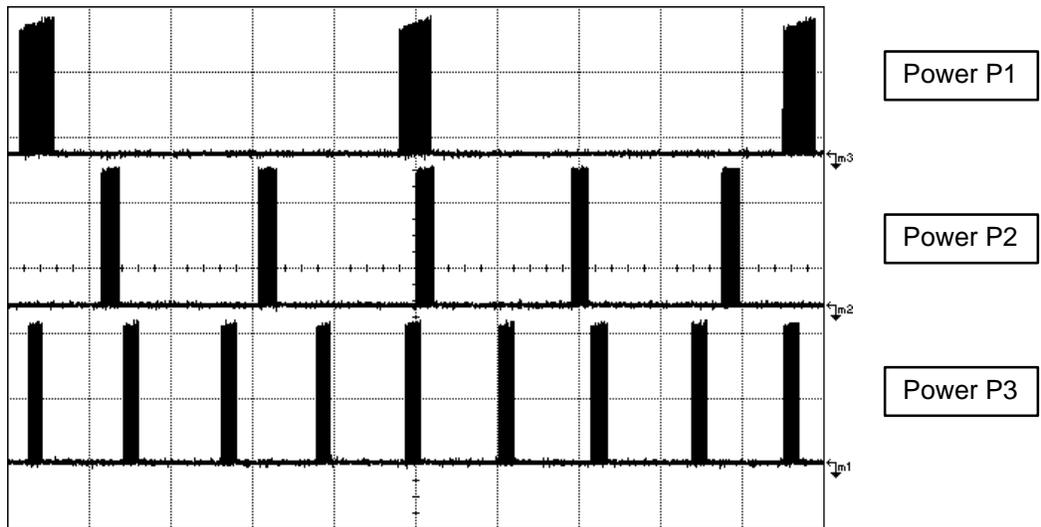


Figure 21. Output Pulses at Various Power Levels (X = 5.0  $\mu$ s/div) P1 < P2 < P3

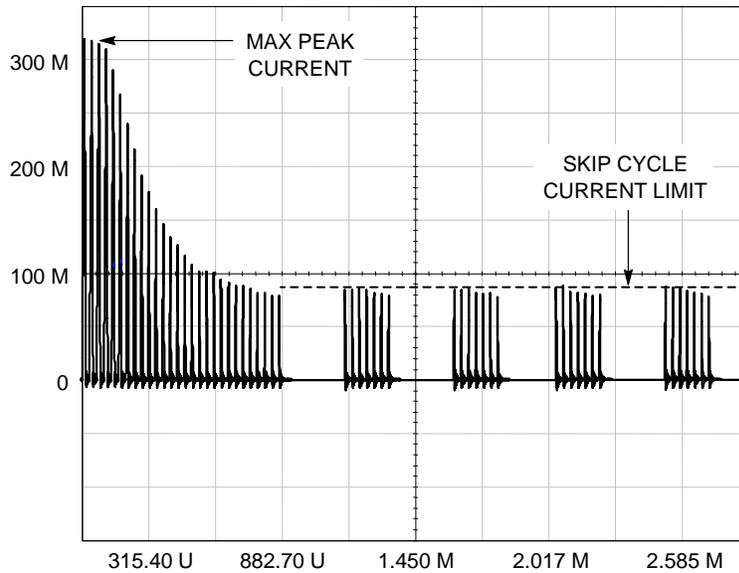


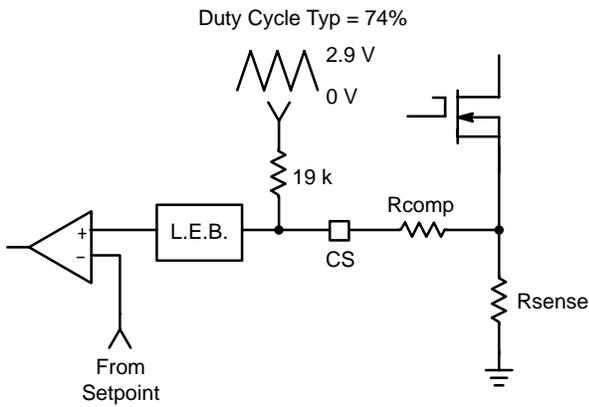
Figure 22. The Skip Cycle Takes Place at Low Peak Currents which Guarantees Noise-Free Operation

Sufficient margin shall be kept between normal pin1 level and the latch-off point in order to avoid false triggering.

### Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during

Continuous Conduction Mode (CCM) with a duty-cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor down-slope. Figure 23 depicts how internally the ramp is generated.



**Figure 23. Inserting a Resistor in Series with the Current Sense Information Brings Ramp Compensation**

In the NCP1217, the ramp features a swing of 2.9 V with a duty cycle max at 74%. Over a 65 kHz frequency, for instance, it corresponds to a 254 mV/μs ramp. In our FLYBACK design, let's suppose that our primary inductance  $L_p$  is 350 μH, delivering 12 V with a  $N_p:N_s$  ratio of 1:0.1. The OFF time primary current slope is thus given

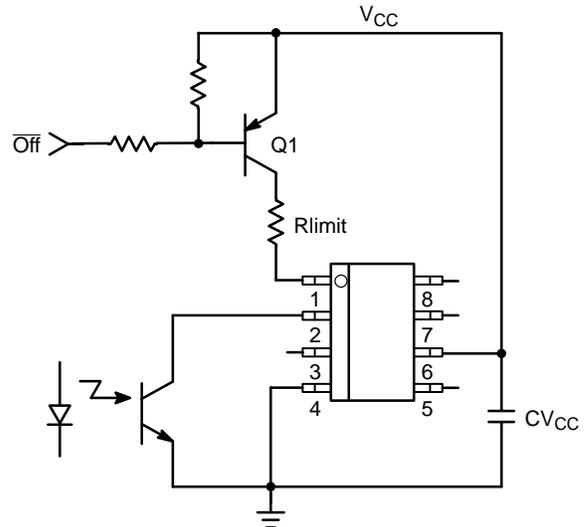
$$\text{by: } \frac{(V_{out} + V_f) \cdot \frac{N_p}{N_s}}{L_p} = 371 \text{ mA}/\mu\text{s} \text{ or } 37 \text{ mV}/\mu\text{s} \text{ when}$$

projected over an  $R_{sense}$  of 0.1 Ω, for instance. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 27 mV/μs. Our internal compensation being of 254 mV/μs, the divider ratio (*divratio*) between  $R_{comp}$  and the 19 kΩ is 0.106.

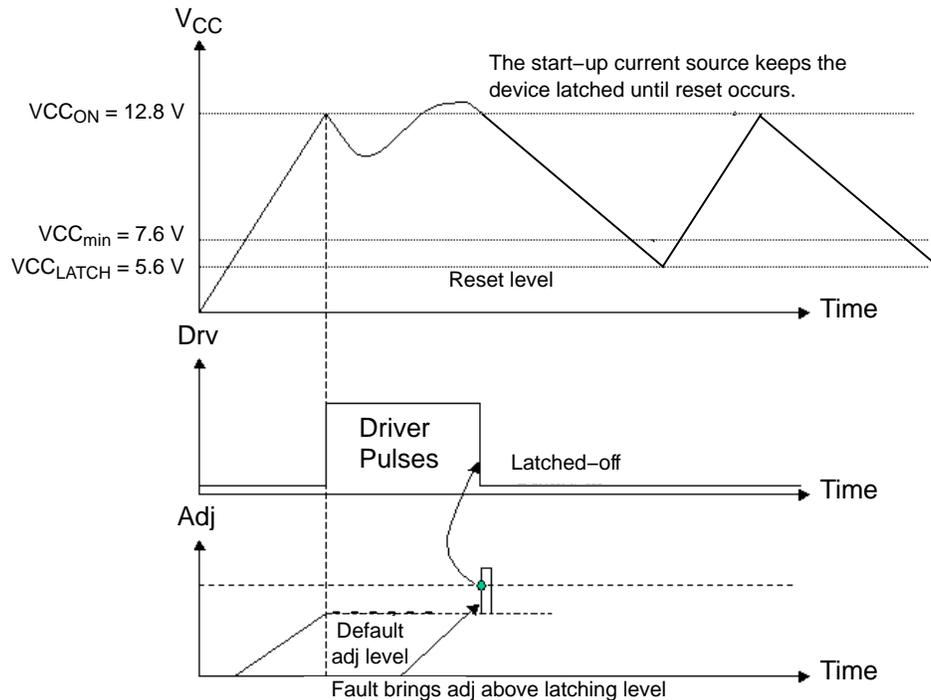
$$\frac{19 \text{ k} \cdot \text{divratio}}{(1 - \text{divratio})} = 2.26 \text{ k}\Omega.$$

**Latching Off the NCP1217**

Total latched shutdown can easily be implemented through a simple PNP bipolar transistor as depicted by Figure 24. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the ADJ pin toward  $V_{CC}$  and permanently latches-off the IC as soon  $V_{adj}$  goes above the latching level (typical 3.1 V). Figure 24 shows how to wire the bipolar transistor to activate the latch-off. A typical candidate for Q1 could be an MMBT3906 from ON Semiconductor.

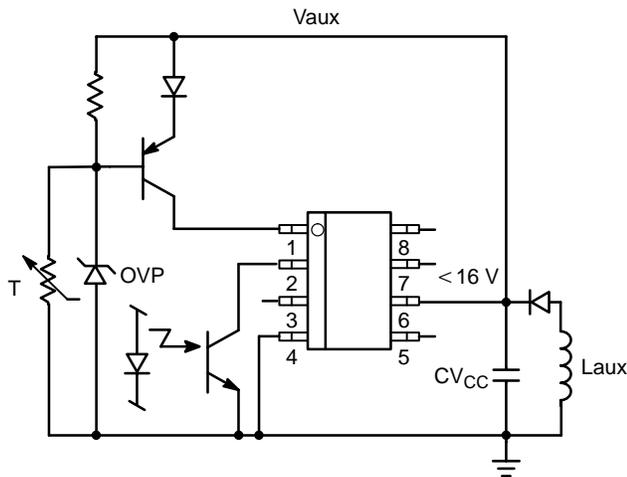


**Figure 24. A Simple Bipolar Transistor Totally Disables the IC**



**Figure 25. When  $V_{adj}$  is Pulled Above 3.1 V, NCP1217 Permanently Latches-Off the Output Pulses**

In normal operation, the Adj pin level is kept at a fixed level, the default one or lower. As soon as some external signal pulls this Adj pin level above 3.1 V typical, the output pulses are permanently disabled. Care must be taken to limit the injected current into pin 1 to less than 2.0 mA, e.g. through a series resistor of 5.6 k with a 10 V  $V_{CC}$ . The start-up switch is activated every time  $V_{CC}$  reaches 5.6 V and maintains a  $V_{CC}$  voltage ramping up and down between 5.6 V and 12.8 V. Reset occurs when  $V_{CC}$  falls below 5.6 V, e.g. when the user cycle the SMPS down. Figure 26 illustrates the operation. Adding a zener diode from Q1 base to ground makes a cheap OVP, protecting the supply from any lethal open-loop operation. If a thermistor (NTC) is added in parallel with the zener-diode, overtemperature protection is also ensured.

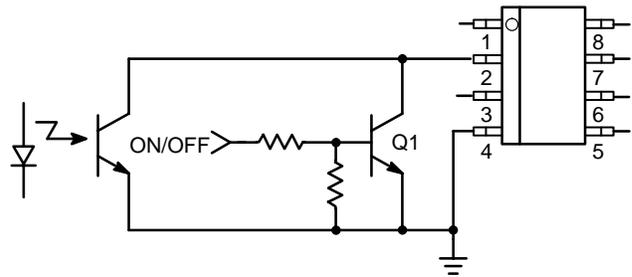


**Figure 26. A Thermistor and a Zener Diode Offer Both OVP and Overtemperature Latched-Off Protection**

**Non-Latching Shutdown**

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj pin 1 level, the

output pulses are disabled as long as FB is pulled below pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 27 depicts the application example.



**Figure 27. Another Way of Shutting Down the IC Without a Definitive Latch-Off State**

**Protecting the Controller Against Negative Spikes**

As with any controller built upon a CMOS technology, it is the designer’s duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irreparable damages to the IC if a low impedance path is offered between  $V_{CC}$  and GND. If the current sense pin is often the seat of such spurious signals, the high-voltage pin can also be the source of problems in certain circumstances. During the turn-off sequence, e.g. when the user unplugs the power supply, the controller is still fed by its  $V_{CC}$  capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by  $R_{sense}$ . Unfortunately, if the quality coefficient  $Q$  of the resonating network formed by  $L_p$  and  $C_{bulk}$  is low (e.g. the MOSFET  $R_{dson} + R_{sense}$  are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge ( $Q = I * t$ ) immediately latches the controller that brutally discharges its  $V_{CC}$  capacitor. If this  $V_{CC}$  capacitor is of sufficient value, its stored energy damages the controller. Figure 28 depicts a typical negative shot occurring on the HV pin where the brutal  $V_{CC}$  discharge testifies for latch-up.

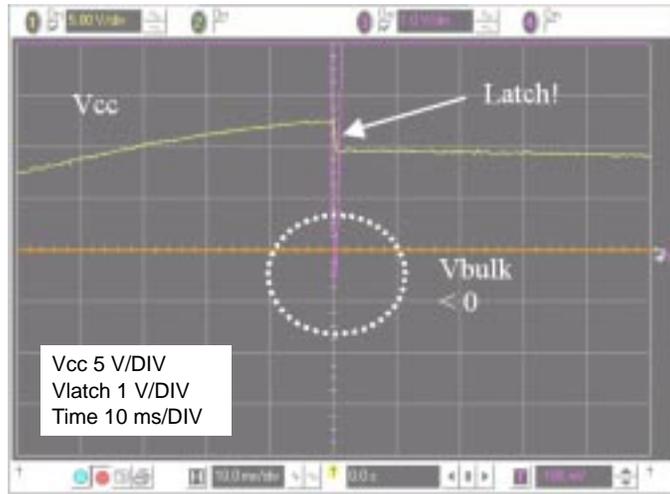


Figure 28. A Negative Spike Takes Place on the Bulk Capacitor at the Switch-Off Sequence

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high-voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 29). Please note that the negative spike is clamped to  $(-2 \cdot V_f)$  thanks to the diode bridge. Also, the power dissipation of this resistor is extremely small since it only heats up during the startup sequence.

Another option (Figure 30) consists in wiring a diode from  $V_{CC}$  to the bulk capacitor to force  $V_{CC}$  to reach  $V_{CC_{ON}}$  sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

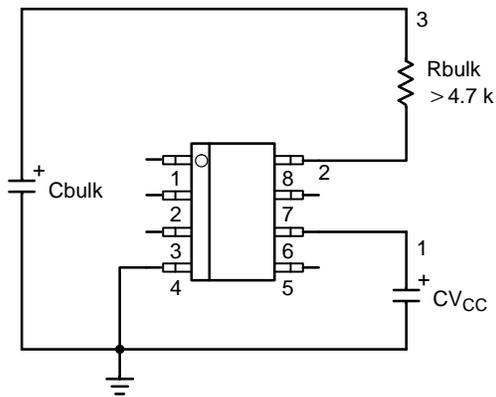


Figure 29. A simple resistor in series avoids any latch-up in the controller . . .

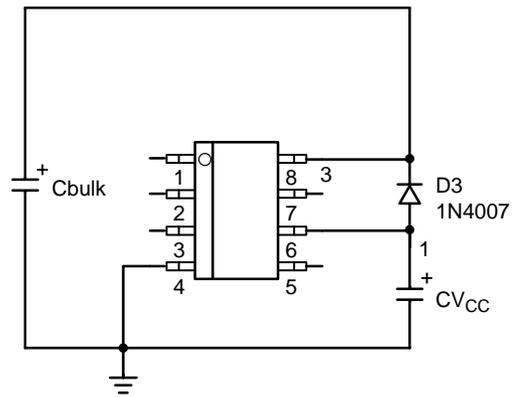


Figure 30. . . or one diode forces  $V_{CC}$  to reach  $V_{CC_{ON}}$  sooner.

# NCP1217

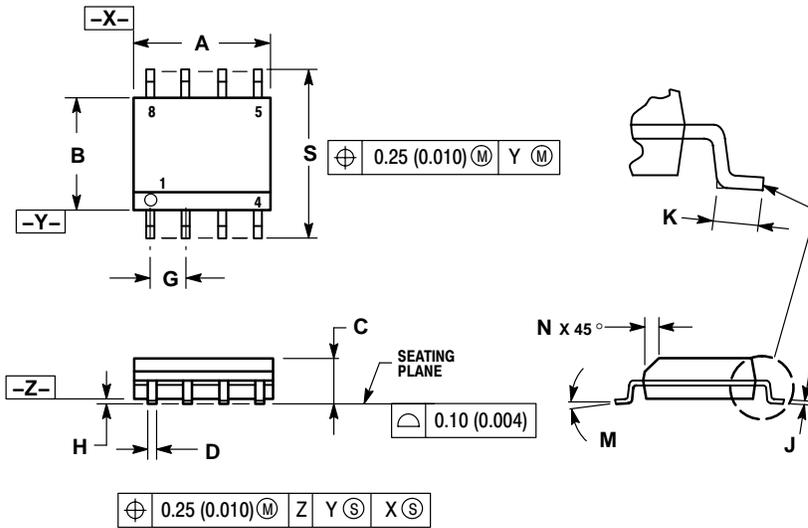
## ORDERING INFORMATION

Device	Version	Marking	Package	Shipping
NCP1217P065	65 kHz	P1217P065	PDIP-7	50 Units/Rail
NCP1217D065	65 kHz	17D06	SO-8	2500 Units/Reel
NCP1217P100	100 kHz	P1217P100	PDIP-7	50 Units/Rail
NCP1217D100	100 kHz	17D10	SO-8	2500 Units/Reel
NCP1217P133	133 kHz	P1217P133	PDIP-7	50 Units/Rail
NCP1217D133	133 kHz	17D13	SO-8	2500 Units/Reel

# NCP1217

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
CASE 751-07  
ISSUE AA



### NOTES:

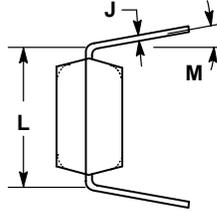
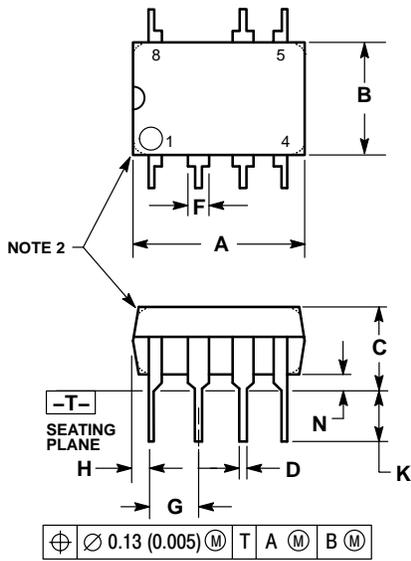
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

# NCP1217

## PACKAGE DIMENSIONS

PDIP-7  
P SUFFIX  
CASE 626B-01  
ISSUE A



### NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
5. DIMENSIONS A AND B ARE DATUMS.

MILLIMETERS		
DIM	MIN	MAX
A	9.40	10.16
B	6.10	6.60
C	3.94	4.45
D	0.38	0.51
F	1.02	1.78
G	2.54 BSC	
H	0.76	1.27
J	0.20	0.30
K	2.92	3.43
L	7.62 BSC	
M	---	10 °
N	0.76	1.01

# NCP1217

The product described herein (NCP1217), may be covered by the following U.S. patents: 6,271,735, 6,362,067, 6,385,060, 6,429,709, 6,587,357. There may be other patents pending.

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