MOTOROLA

MCM6836E16
MCM6836R16

Advance Information

128K-BIT COMBINATION ROM/EEPROM MEMORY UNIT

The MCM6836E16/MCM6836R16 Combination ROM/EEPROM Memory (CREEM) is a 16K byte combination memory device with 14K bytes of mask programmable ROM and 2K bytes of electrically erasable programmable ROM (EEPROM). It is designed for handling data in applications requiring nonvolatile memory and in-system reprogramming to a portion of the memory. The MCM6836 saves time and money because of the in-system erase and reprogram capability of its 2K bytes of EEPROM. The industry standard pinout in a 28-pin dual-in-line package makes the MCM6836( )16 compatible with 128K-bit ROMs and EPROMs.

For easy use, the MCM6836( )16 device operates in the read mode from a single power supply and has a static power down mode. The MCM6836R16 version has a 256 byte user programmable redundancy EEPROM on chip. It can be programmed by the user to replace any page of 256 bytes of memory in the mask ROM or EEPROM sections.

The following are some of the major features of the MCM6836( )16.

- 128K-Bit ROM/EEPROM Combination Memory Organized as 16,384 × 8 Bytes
- Lowest Order 2K Bytes are Bulk Erasable EEPROM
- Remaining 14K Bytes are Mask Programmed ROM
- Packaged in Standard 28-Pin DIP
- Pin Compatible with 128K-Bit ROMs and EEPROMs
- In the Read Operating Mode Only +5 V Power Supply is Required
- +21 Vdc Programming Power Supply
- Bulk Erase
- 256 Bytes of Spare Memory are Included on Chip (MCM6836R16 Only)
- Seven Operating Modes: Read, Standby, Program, Erase, Verify, Replace (MCM6836R16 Only), and Erase-of-Replace (MCM6836R16 Only)

ORDERING INFORMATION (T_A = 0°C to 70°C)

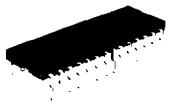
Package Type	Order Number
Cerdip S Suffix	MCM6836E16S MCM6836R16S
Plastic P Suffix	MCM6836E16P MCM6836R16P

This document contains information on a new product. Specifications and information herein are subject to change without notice.

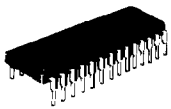
HMOS

HIGH-DENSITY N-CHANNEL PROCESS

128K-BIT COMBINATION ROM/EEPROM MEMORY

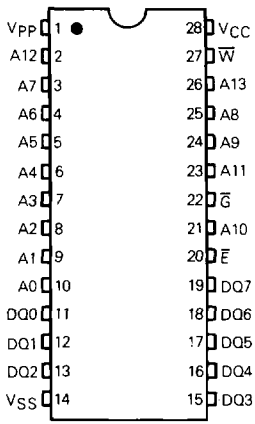


S SUFFIX
CERDIP PACKAGE
CASE 733



P SUFFIX
PLASTIC PACKAGE
CASE 710

PIN ASSIGNMENT



Pin Names

A0-A13	Address
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write
DQ0-DQ7	Data
V_{PP}	Program Voltage
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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FIGURE 1 – MCM6836E/R16 EEPROM MEMORY UNIT BLOCK DIAGRAM

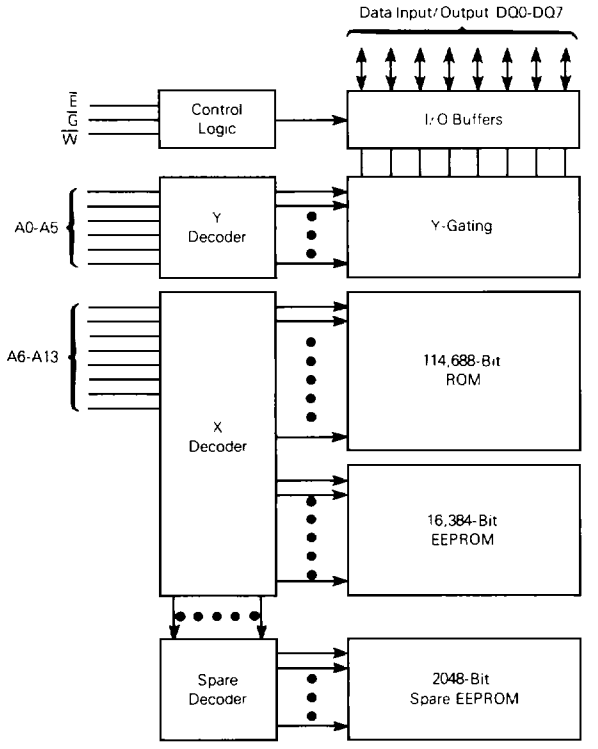
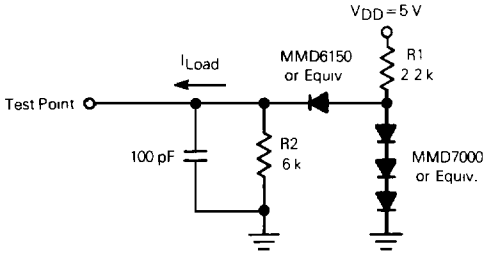


FIGURE 2 – AC TEST LOAD



MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Ratings	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Programming Voltage	V_{PP}	−0.3 to +22	V
Input Voltage Mode Programming Pin All Other Inputs	 V_{IHH} V_{in}	 −0.3 to +19 −0.3 to +7	 V V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages of electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{CC}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance Cerdip Plastic	θ_{JA}	 60 100	°C/W

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POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

OPERATING DC ELECTRICAL CHARACTERISTICS ($V_{CC} = V_{PP} = 5.0$ V ± 10%, $V_{SS} = 0$ Vdc, $T_A = 0°$ to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Output High Voltage ($I_{Load} = -400\ \mu A$)	V_{OH}	2.4	–	V
Output Low Voltage ($I_{Load} = 2.1$ mA)	V_{OL}	–	0.4	V
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage All Inputs (Except V_{PP})	V_{IL}	−0.1	0.8	V
Input High Voltage V_{PP} (Normal Operating Mode)	V_{IH}	V_{CC}	V_{CC}	V
Supply Current Measured at $T_A = 0°C$ in Read Mode Operation ($V_{CC} = 4.5$ to 5.5 V)	I_{CC}	–	100	mA
Input Low Current ($V_{IL} = 0$)	I_{IL}	–	−10	μA
Input High Current ($V_{IH} = 5.25$ V)	I_{IH}	–	10	μA
Hi-Z Output Leakage Current Low ($V_{out} = 0.4$ V)	I_{OZL}	–	−10	μA
Hi-Z Output Leakage Current High ($V_{out} = 5.5$ V)	I_{OZH}	–	10	μA
Capacitance Output ($V_{out} = 0$) Input ($V_{in} = 0$)	 C_{out} C_{in}	 – –	 12 10	 pF pF
V_{PP} Current	I_{PP}	–	12	mA
Supply Current During Standby, Measured at $T_A = 0°C$ ($V_{CC} = 4.5$ to 5.5 V, $\overline{E} \ge V_{IH}$, $\overline{G} \ge V_{IH}$)	$I_{CC(SB)}$	–	25	mA

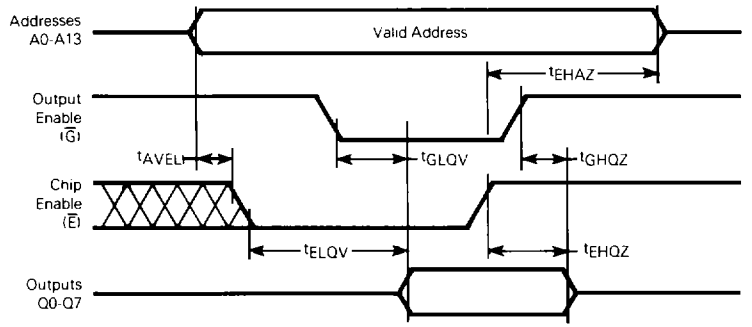
NOTES: 1. In normal read operation, if the V_{PP} pin is connected to V_{CC}, then the total I_{CC} current will be the sum of the total supply and the V_{PP} current.

2. In all cases, V_{CC} and V_{IHH} must be applied simultaneously with or prior to V_{PP}, V_{CC} and V_{IHH} must be switched off simultaneously with or after V_{PP}.

READ MODE AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Unit
Access Time (From Chip Enable)	t_{ELQV}	–	250	ns
Access Time (From Output Enable)	t_{GLQV}	–	100	ns
Address Hold Time (From Chip Enable)	t_{EHAZ}	0	–	ns
Address Setup Time	t_{AVEL}	0	–	ns
Disable Time (From Output Enable)	t_{GHQZ}	0	80	ns
Disable Time (From Chip Enable)	t_{EHQZ}	10	80	ns

READ MODE TIMING DIAGRAM



NOTES. 1 Voltage levels shown are $V_{OL} \leq 0.4$ V and $V_{OH} \geq 2.4$ V unless otherwise specified
2 Timing level measurement points are 0.8 V and 2.0 V unless otherwise specified.
3 $\overline{G}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{E}$ without impact on t_{ELQV}

PROGRAMMING OPERATION DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage (V_{PP} Pin)	V_{PP}	20	21	22	V
Input High Voltage For Data	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	– 0.1	–	0.8	V
Address, $\overline{E}$, $\overline{G}$, and $\overline{W}$ Sink Current (V_{in} = 5.25 V/0.4 V)	I_{leak}	–	–	10	μA
V_{PP} Supply Current (V_{PP} = 21 ± 1 V, $\overline{W} = V_{IH}$)	I_{PP1}	–	–	10	mA
V_{PP} Programming Pulse Supply Current (V_{PP} = 21 ± 1 V, $\overline{W} = V_{IL}$)	I_{PP2}	–	–	10	mA
V_{CC} Supply Current	I_{CC}	–	–	115	mA

PROGRAMMING OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 V, T_A = 25°C)

Characteristic	Symbol	Min	Max	Unit
V_{PP} Rise Time	t_{PLPH}	50	–	ns
V_{PP} Fall Time	t_{PHPL}	50	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	µs
V_{PP} Hold Time	t_{WHPL}	2.0	–	µs
Address Setup Time	t_{AVWL}	2.0	–	µs
Address Hold Time	t_{WHAX}	2.0	–	µs
Output Enable High to Program Pulse	t_{GHWL}	2.0	–	µs
Output Enable Hold Time	t_{WHGL}	2.0	–	µs
Chip Enable Setup Time	t_{EHWL}	2.0	–	µs
Output Disable to Hi-Z Output	t_{GHQX}	0.1	100	ns
Data Setup Time	t_{DVWL}	2.0	–	µs
Data Hold Time	t_{WHDX}	2.0	–	µs
Program Pulse Width	$t_{W(WL)1}$	1.0	10	ms
Output Enable to Valid Data	t_{GLDV}	–	200	ns

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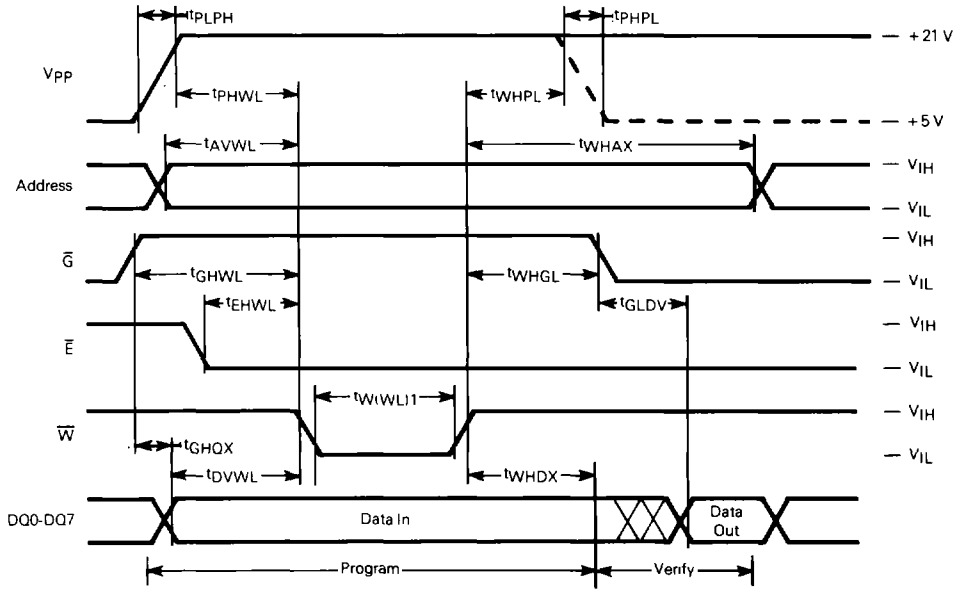
PROGRAMMING OPERATION TIMING DIAGRAM



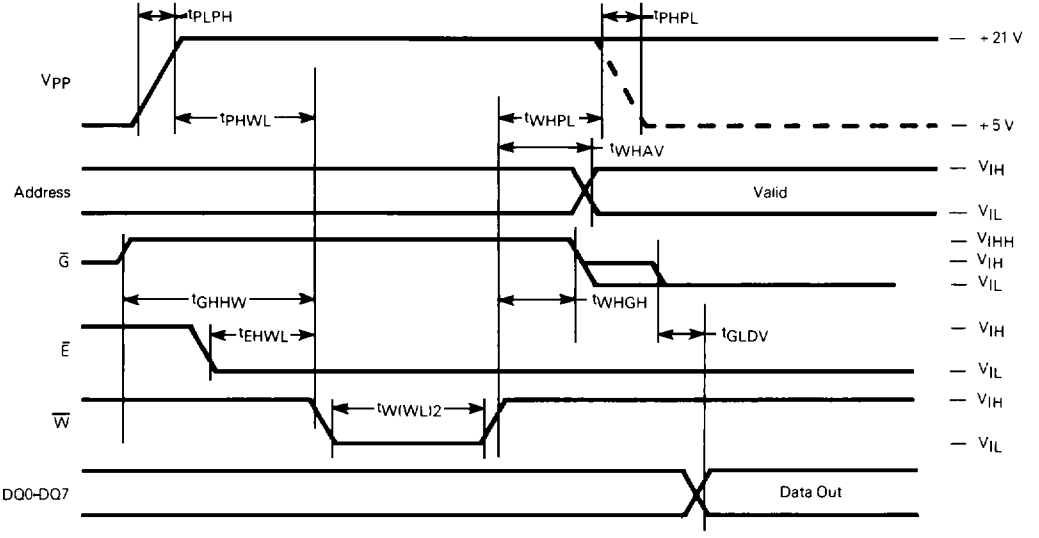
ERASE OPERATION DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current for Any Input @ V_{in}	I_{leak}	–	–	10	μA
V_{CC} Supply Current (Outputs Open, $\overline{W} = V_{IL}$)	I_{CC}	–	–	115	mA
V_{PP} Supply Current ($\overline{W} = V_{IL}$)	I_{PP}	–	5	10	mA
Input Low Level	V_{IL}	−0.1	–	0.8	V
Input High Level	V_{IH}	2.0	–	V_{CC}	V
Input Mode Select High	V_{IHH}	12	15	19	V

ERASE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Rise Time	t_{PLPH}	50	–	–	ns
V_{PP} Fall Time	t_{PHPL}	50	–	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	μs
V_{PP} Hold Time	t_{WHPL}	2.0	–	–	μs
Address Delay Time	t_{WHAV}	2.0	–	–	μs
Output Enable Setup Time	t_{GHHWL}	2.0	–	–	μs
Output Enable Hold Time	t_{WHGH}	2.0	–	–	μs
Chip Enable Setup Time	t_{EHWL}	2.0	–	–	μs
Erase Pulse Width	$t_{W(WL)2}$	1.0	10	100	ms
Output Enable to Invalid Data	t_{GLDV}	–	–	200	ns

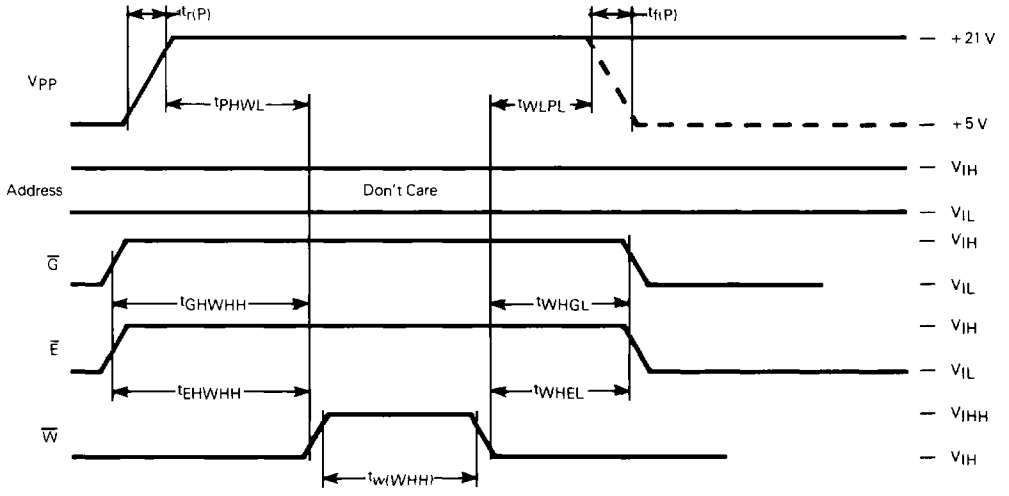
ERASE OPERATION TIMING DIAGRAM



ERASE-OF-REPLACE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Rise Time	$t_{r(P)}$	50	–	–	ns
V_{PP} Fall Time	$t_{f(P)}$	50	–	–	ns
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	µs
V_{PP} Hold Time	t_{WLPL}	2.0	–	–	µs
Output Enable Setup Time	t_{GHWHH}	2.0	–	–	µs
Output Enable Hold Time	t_{WHGL}	2.0	–	–	µs
Chip Enable Setup Time	t_{EHWHH}	2.0	–	–	µs
Chip Enable Hold Time	t_{WHEL}	2.0	–	–	µs
Erase-of-Replace Pulse Width	$t_{w(WHH)}$	10	–	–	ms

ERASE-OF-REPLACE OPERATION TIMING DIAGRAM



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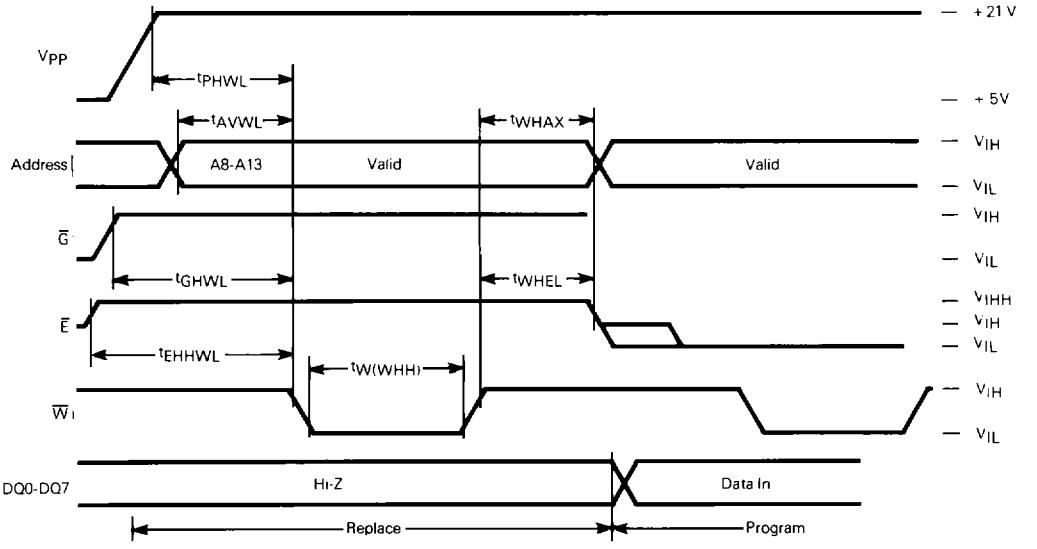
REPLACE OPERATION AC TIMING CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, V_{PP} = 21 ± 1 Vdc, T_A = 25°C)

Characteristic	Symbol	Min	Typ	Max	Unit
V_{PP} Setup Time	t_{PHWL}	2.0	–	–	µs
Address Setup Time	t_{AVWL}	2.0	–	–	µs
Address Hold Time	t_{WHAX}	2.0	–	–	µs
Output Enable Setup Time	t_{GHWL}	2.0	–	–	µs
Chip Enable Setup Time	t_{EHHWL}	2.0	–	–	µs
Chip Enable Hold Time	t_{WHEH}	2.0	–	–	µs
Replace Pulse Width	$t_{w(WL)3}$	50	100	–	ms

REPLACE OPERATION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

INTRODUCTION

The MCM6836( )16 Combination ROM/EEPROM (CREEM) is a 128K bit memory device containing 2K bytes of EEPROM and 14K bytes of mask programmed ROM. The EEPROM is located in the lower 2K byte section of memory, at addresses $0000 to $07FF, and the mask ROM is located in the upper 14K byte section of memory at addresses $0800 to $3FFF. The MCM6836R16 contains an additional 256 bytes of spare memory. This redundant memory allows for the replacement of a 256 byte block of memory in either mask ROM or EEPROM. The MCM6836E16, without redundancy, is also available. The MCM6836( )16 is contained in a standard 28-pin dual in-line package.

The MCM6836( )16 incorporates several operating modes which make the device easy to use and test. These modes which are illustrated in Figure 3 include: Read, Standby, Program, Erase, Verify, Replace, and Erase-Of-Replace (Replace and Erase-Of-Replace modes are used in the MCM6836R16 only). The pin voltages (signals) required for each mode are also illustrated in Figure 3 and a functional description of each operating mode is provided below. The read and standby modes allow the device to be used as a conventional ROM, the program mode allows programming of individual bytes in the EEPROM, and the erase mode allows the entire EEPROM contents to be erased to the logic high state in approximately 10 milliseconds.

In the MCM6836R16, the replace mode allows substitution of any 256-byte page in the mask ROM or EEPROM memory space with an erased page of EEPROM which can then be programmed. The substitution is performed as a single block of memory, and on-chip logic determines if mask ROM or EEPROM has been replaced. If EEPROM has been replaced, the redundant memory and the memory it has replaced are erased when the standard EEPROM is erased. If the substitution is for mask ROM, the spare memory is erased only by the erase replace mode which has unique control functions. This allows the spare memory to contain the same characteristics as the normal memory for which it is substituted.

OPERATING MODES

The MCM6836E16/MCM6836R16 (CREEM) incorporates five common operating modes, plus two more modes for the MCM6836R16, which make the device easy to use and test. The following paragraphs provide a detailed discussion of each of these modes. In addition, Figure 3 provides a chart illustrating how the various pins are affected during each of the operating modes.

NOTE

It is possible to erase spare EEPROM even if it is used as ROM (or isn't being used) when the following erroneous pin connections are made: E and $\overline{G} = V_{IHH}$, $V_{PP} = V_{PP}$, and $\overline{W} = V_{IL}$.

Read Mode — this mode allows the MCM6836( )16 to be used like any conventional mask ROM. In order to read the device in this mode, E and $\overline{G}$ must be held low (V_{IL}), V_{PP} is connected to V_{CC}, and a valid address accessed for data output. The W pin can be in either state (don't care). Some characteristics of the read mode are:

1. Data is available 250 nanoseconds after valid addresses or after the falling edge of $\overline{E}$.
2. Data is valid 100 nanoseconds after the trailing edge of $\overline{G}$ provided $\overline{E}$ and stable addresses have been present for 150 nanoseconds or more.
3. Current is less than 100 milliamperes at 0°C.

Standby Mode — In this mode the MCM6836( )16 is disabled. In order to enter this mode, $\overline{E}$ and $\overline{G}$ must be at a logic high level (V_{IH}), and V_{PP} must be connected to V_{CC}. The $\overline{W}$ and address line can be at any state ("don't care") and the data bus will be in the high-impedance state. (Hi-Z). Some characteristics of the standby mode are:

1. Data outputs are high impedance.
2. Current is reduced 75% to less than 25 milliamperes at 0°C.

Program Mode — In this mode, individual bytes (memory locations) in the EEPROM may be programmed in approximately 10 milliseconds. (A memory location must be erased to the all ones state before it can be programmed.) In order to enter this mode and program the EEPROM, $\overline{E}$ must be at a logic low (V_{IL}), $\overline{G}$ at a logic high (V_{IH}), and V_{PP} must be held at +21 Vdc. A 10 millisecond negative-going pulse on $\overline{W}$ will then allow the input data to be programmed into the addresses accessed in the EEPROM. Some characteristics of the program mode are:

1. Although only zeros are programmed into the device, both ones and zeros can be present in the data word.
2. Requires +21 Vdc programming voltage supply.

FIGURE 3 — OPERATING MODES AND CONTROL VOLTAGES

	$\overline{E}$	$\overline{G}$	V_{PP}	$\overline{W}$	Address	Data
Read	V_{IL}	V_{IL}	V_{CC}	X	Valid	D_{out}
Standby	V_{IH}	V_{IH}	V_{CC}	X	X	Hi-Z
Program	V_{IL}	V_{IH}	V_{PP}	⎍ V_{IH}	Valid	D_{in}
Erase	V_{IL}	V_{IHH}	V_{PP}	⎍ V_{IH}	X	Hi-Z
Verify	V_{IL}	V_{IL}	V_{PP}	V_{IH}	Valid	D_{out}
Replace#	V_{IHH}	V_{IH}	V_{PP}	⎍ V_{IH}	Valid	Hi-Z
Erase-of-Replace#	V_{IH}	V_{IH}	V_{PP}	⎍ V_{IHH}	X	Hi-Z

# Indicates used in MCM6836R only.

NOTE: It is possible to erase spare EPROM even if it is used as ROM (or isn't being used) when the following erroneous pin connections are made: $\overline{E}$ and $\overline{G} = V_{IHH}$, $V_{PP} = V_{PP}$, and $\overline{W} = V_{IL}$.

Erase Mode – This mode allows the contents of the EEPROM to be erased to all ones. In order to enter this mode and erase the EEPROM, $\overline{E}$ must be held low (V_{IL}), $\overline{G}$ must be held at V_{IHH}, and V_{PP} must be held at +21 Vdc. A 10 millisecond negative-going pulse on $\overline{W}$ will then erase the EEPROM to the all ones state. Address lines can be in any state and the data bus will be in the high-impedance state (Hi-Z). Some characteristics of the erase mode are:

1. Bulk erase returns the entire EEPROM array to all ones.
2. A +21 Vdc programming voltage supply is required.

Verify Mode – In this mode the contents of the EEPROM can be verified as all ones after erasure and the contents of the data byte can be verified after programming. In order to enter this mode and verify EEPROM and/or data byte contents, $\overline{E}$ and $\overline{G}$ must be held at V_{IL}, and V_{PP} must be held at +21 Vdc. The $\overline{W}$ line must be held high (V_{IH}) and a valid address must be applied to the address lines accessing the EEPROM locations (to obtain data output). Some characteristics of the verify mode are:

1. Allows quick verification of the data byte which was written during the previous cycle.
2. Verification may be performed after each program or erase cycle.
3. Verification is accomplished by performing a read cycle with V_{PP} at +21 Vdc and $\overline{W}$ held at V_{IH}.

Replace Mode (MCM6836R16 only) – The replace mode allows for substitution of any 256 byte page in the mask ROM or EEPROM memory with an erased page of EEPROM which can then be programmed. The substitution is performed as a single block of memory and on-chip logic determines if mask ROM or EEPROM is to be replaced. If EEPROM is replaced, the redundant memory and the memory it has replaced is erased when the standard EEPROM is erased. If the substitution is for mask ROM, the spare memory can be erased only in the erase-of-replace mode, which has unique control functions. Thus, the spare memory assumes the same characteristics as the normal memory for which it was substituted.

To replace a block of memory, $\overline{E}$ must be held at V_{IHH}, $\overline{G}$ must be held at V_{IH}, and V_{PP} must be held at +21 Vdc. Then, a 100 millisecond negative-going pulse on $\overline{W}$ will substitute the spare memory when the beginning address of the section of memory to be replaced is set on address lines A8-A13.

The replace operation programs special EEPROM devices which: (1) program replacement addresses into a spare row decoder, (2) determine if the address space is in mask ROM or EEPROM, (3) enable the spare memory, and (4) prevent "overprogramming" the replacement address. Data is then programmed into the spare memory by using the program mode. If this section of memory is addressed during the read or program mode, a signal is generated that disables all normal row decoders.

Some characteristics of the replace mode are:

1. Substitutes 256 bytes of spare EEPROM for 256 bytes of either mask ROM or EEPROM.
2. Performed as a single block of memory.
3. On-chip logic determines if mask ROM or EEPROM is to be replaced.
4. When in the replace mode, special EEPROM devices are programmed which:
   A. Program replacement addresses into a spare row decoder,
   B. Determine if the address space is in mask ROM or EEPROM,
   C. Enable the spare memory, and
   D. Prevent "overprogramming" the replacement address.

Data is then programmed into spare memory using the program mode.

Erase-Of-Replace Mode (MCM6836R16 only) – This mode is used, when spare memory (redundancy) is being used, to erase the replace mask ROM. To erase the spare memory to all ones, $\overline{E}$ and $\overline{G}$ must be held at V_{IH}, and V_{PP} must be held at +21 Vdc. Then, a 10 millisecond positive-going (to V_{IHH}) pulse on $\overline{W}$ will erase the spare memory to the all ones state. This mode also erases the programmed address to the redundancy EEPROM. During the erase-of-replace mode, the address lines can be at any state and the data bus is in the high-impedance state. Some characteristics of the erase-of-replace mode are:

1. Returns the device to its original condition by erasing the replace circuitry, spare decoder, and spare memory.
2. Needed only for a device which contains redundancy as a user option.
3. False erasure of redundancy memory is unlikely due to unique control function ($\overline{W}$ pulse).

NOTE

The erase-of-replace mode need only be used if spare memory is being used to replace a section of mask ROM. This operation erases the replacement circuitry, spare decoder, and spare memory after which the device is returned to its original condition.

FUNCTIONAL PIN DESCRIPTION

V_{PP}

This pin is used as the +21 Vdc input voltage during EEPROM programming and erasing operations. It is connected to V_{CC} in the normal operating read and standby modes. V_{PP} should not, in any case, be applied before the device has been powered by V_{CC} or after V_{CC} has been removed from the device.

WRITE ($\overline{W}$)

The active low state (V_{IL}) of this input pin is used to program and erase the EEPROM. It is also used as a mode select pin for the erase-of-replace mode when V_{IHH} is applied to its input. In the normal read and standby operating modes, this pin is a "don't care".

CHIP ENABLE ($\overline{E}$)

The active low state (V_{IL}) of this input pin is used as a chip select signal for the read, program, erase, and verify operating modes. It is also used as a mode select input signal for the replace mode when V_{IHH} is applied. It is used as a mode select signal for the standby and erase-of-replace modes when V_{IH} is applied.

OUTPUT ENABLE ($\overline{G}$)

The active low state (V_{IL}) of this input pin is used in conjunction with $\overline{E}$ to enable the output buffer of this device. It is also used as a mode select signal for the erase mode when V_{IHH} is applied.

DATA BUS (DQ0-DQ7)

These eight pins provide a bidirectional data link to the system bus.

ADDRESS INPUTS (A0-A13)

These 14 address inputs allow any of the 14K bytes of mask ROM and 2K bytes of EEPROM to be uniquely selected in the read mode. Addresses $0000 to $07FF are designated as EEPROM, and addresses $0800 to $3FFF are designated as the mask programmable ROM. These address inputs are also used to select an address byte for programming, verifying, and replacing.