Document Title

512Kx8 Bit High Speed Static RAM(3.3V Operating), Revolutionary Pin out. Operated at Commercial Temperature Range.

Revision History

Rev No.	History	Draft Data	Remark
Rev. 0.0	Initial release with Design Target.	Jun. 14th, 1996	Design Target
Rev. 0.5	Release to Preliminary Data Sheet. 0.1. Replace Design Target to Preliminary. 0.2. Delete 12ns part but add 17ns part. 0.3. Relax D.C and A.C parameters and insert new parameter(I_{CC1}) with the test condition. 0.3.1. Insert I_{CC1} parameter with the test condition as address is increased with binary count. 0.3.2. Relax D.C and A.C parameters.	Sep. 16th, 1996	Preliminary
Rev. 1.0	Release to Final Data Sheet. 1.1. Delete Preliminary. 1.2. Delete Icc1 parameter with the test condition. 1.3. Update D.C parameters.	Jun. 5th, 1997	Final

0.3.2. Relax D.C and A.C parameters.

Items	Previous spec. (15/ –/20ns part)	Relaxed spec. (15/17/20ns part)
I_{CC}	170/ –/160mA	200/195/190mA
t_{CW}	10/ –/12ns	12/13/14ns
t_{AW}	10/ –/12ns	12/13/14ns
t_{WP}($\overline{OE}$=H)	10/ –/12ns	12/13/14ns
t_{WP1}($\overline{OE}$=L)	12/ –/14ns	15/17/20ns
t_{DW}	7/ –/9ns	8/9/10ns

1.3. Update D.C parameters.

Items	Previous spec. (15/17/20ns part)	Updated spec. (15/17/20ns part)
I_{CC}	200/195/190mA	160/155/150mA

1.4. Add timing diagram to define t_{WP} as "**(Timing Wave Form of Write Cycle($\overline{CS}$=Low fixed)**"

512K x 8 Bit High-Speed CMOS Static RAM

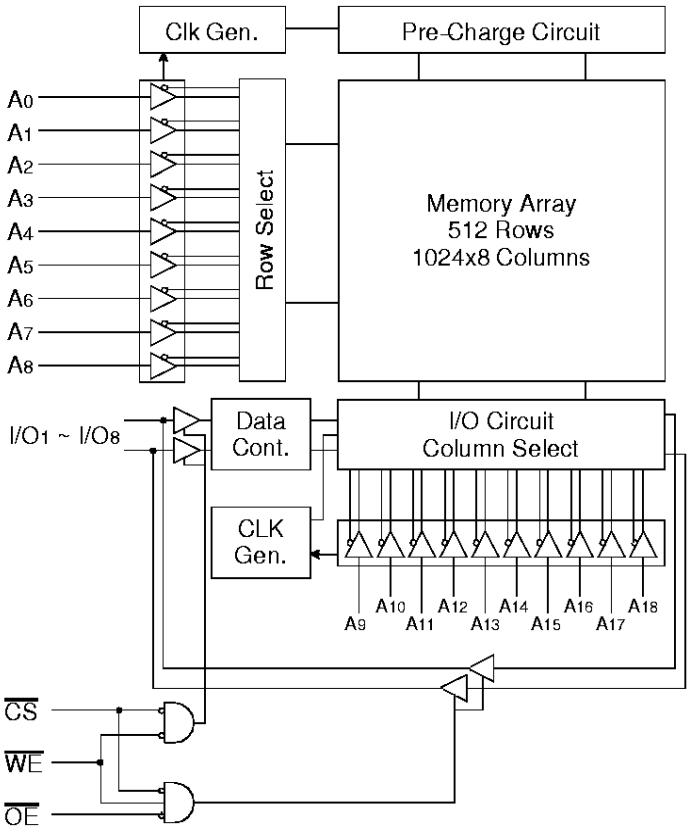
FEATURES

- Fast Access Time 15,17,20§ (Max.)
- Low Power Dissipation
  - Standby (TTL) : 50§ (Max.)
  - (CMOS) : 10§ (Max.)
  - Operating KM68V4002A-15 : 160§ (Max.)
  - KM68V4002A-17 : 155§ (Max.)
  - KM68V4002A-20 : 150§ (Max.)
- Single 3.3V±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- Standard Pin Configuration
  - KM68V4002AJ : 36-SOJ-400

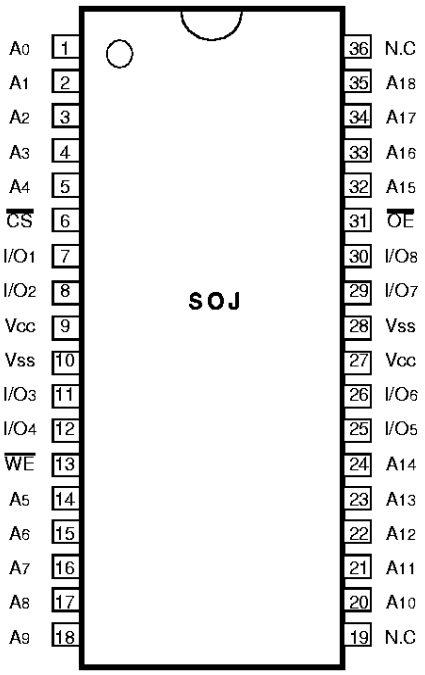
GENERAL DESCRIPTION

The KM68V4002A is a 4,194,304-bit high-speed Static Random Access Memory organized as 524,288 words by 8 bits. The KM68V4002A uses 8 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM68V4002A is packaged in a 400 mil 36-pin plastic SOJ.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top View)



PIN FUNCTION

Pin Name	Pin Function
A0 ~ A18	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O1 ~ I/O8	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

LECTRONICS

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss	V_{CC}	-0.5 to 4.6	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Ground	V_{SS}	0	0	0	V
Input Low Voltage	V_{IH}	2.2	-	V_{CC}+0.3**	V
Input Low Voltage	V_{IL}	-0.3*	-	0.8	V

* V_{IL}(Min) = -2.0V a.c(Pulse Width≤10ns) for I≤20§

** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width≤10ns) for I≤20§

DC AND OPERATING CHARACTERISTICS(T_A=0 to 70°C, V_{CC}=3.3V±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = Vss to V_{CC}		-2	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT} = Vss to V_{CC}		-2	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT}=0mA	15ns	-	160	§
			17ns	-	155	
			20ns	-	150	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}		-	50	§
	I_{SB1}	f=0MHz, $\overline{CS}$≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V		-	10	§
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

CAPACITANCE*(T_A =25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF

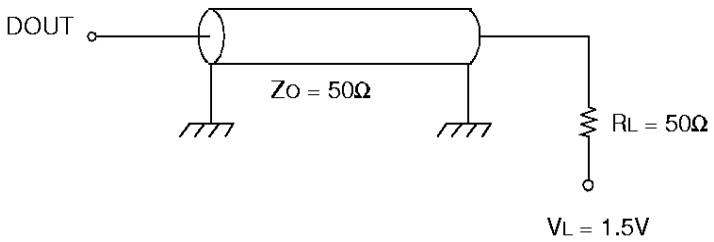
* NOTE : Capacitance is sampled and not 100% tested.

AC CHARACTERISTICS (T_A=0 to 70°C, V_{CC}=3.3V±0.3V, unless otherwise noted.)

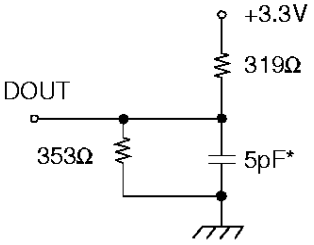
TEST CONDITIONS

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3§
Input and Output timing Reference Levels	1.5V
Output Loads	See below

Output Loads(A)



Output Loads(B)
for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Including Scope and Jig Capacitance

READ CYCLE

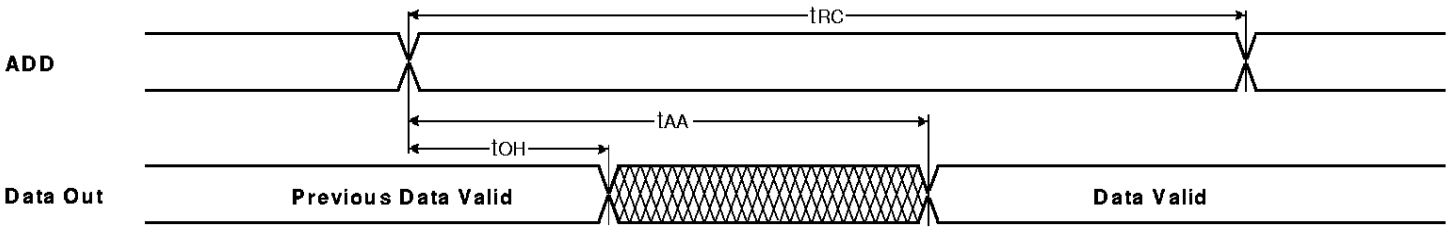
Parameter	Symbol	KM68V4002A-15		KM68V4002A-17		KM68V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	15	–	17	–	20	–	§
Address Access Time	tAA	–	15	–	17	–	20	§
Chip Select to Output	tCO	–	15	–	17	–	20	§
Output Enable to Valid Output	tOE	–	7	–	8	–	9	§
Chip Enable to Low-Z Output	tLZ	3	–	3	–	3	–	§
Output Enable to Low-Z Output	tOLZ	0	–	0	–	0	–	§
Chip Disable to High-Z Output	tHZ	0	7	0	8	0	9	§
Output Disable to High-Z Output	tOHZ	0	7	0	8	0	9	§
Output Hold from Address Change	tOH	3	–	3	–	3	–	§
Chip Selection to Power Up Time	tPU	0	–	0	–	0	–	§
Chip Selection to Power DownTime	tPD	–	15	–	17	–	20	§

WRITE CYCLE

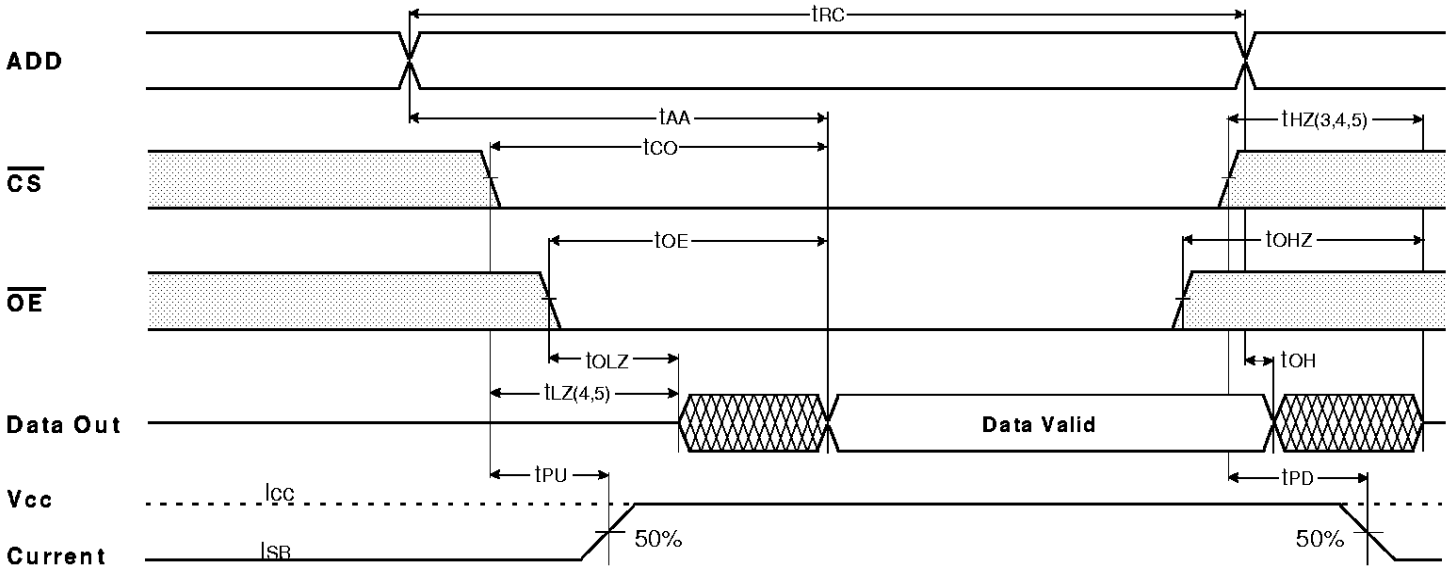
Parameter	Symbol	KM68V4002A-15		KM68V4002A-17		KM68V4002A-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	tWC	15	–	17	–	20	–	§
Chip Select to End of Write	tCW	12	–	13	–	14	–	§
Address Set-up Time	tAS	0	–	0	–	0	–	§
Address Valid to End of Write	tAW	12	–	13	–	14	–	§
Write Pulse Width($\overline{OE}$ High)	tWP	12	–	13	–	14	–	§
Write Pulse Width($\overline{OE}$ Low)	tWP1	15	–	17	–	20	–	§
Write Recovery Time	tWR	0	–	0	–	0	–	§
Write to Output High-Z	tWHZ	0	7	0	8	0	9	§
Data to Write Time Overlap	tDW	8	–	9	–	10	–	§
Data Hold from Write Time	tDH	0	–	0	–	0	–	§
End Write to Output Low-Z	tOW	3	–	3	–	3	–	§

TIMING DIAGRAMS

TIMING WAVE FORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



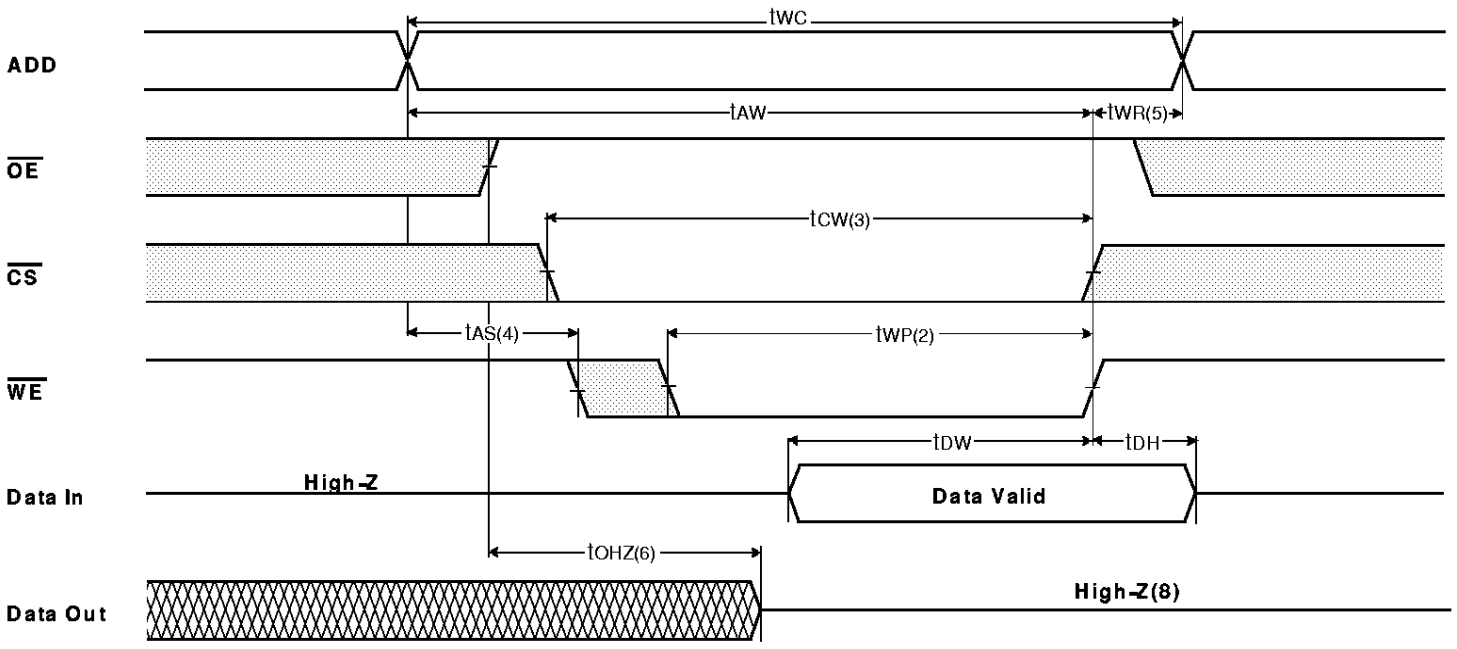
TIMING WAVE FORM OF READ CYCLE(2)($\overline{WE}$=V_{IH})



NOTES(READ CYCLE)

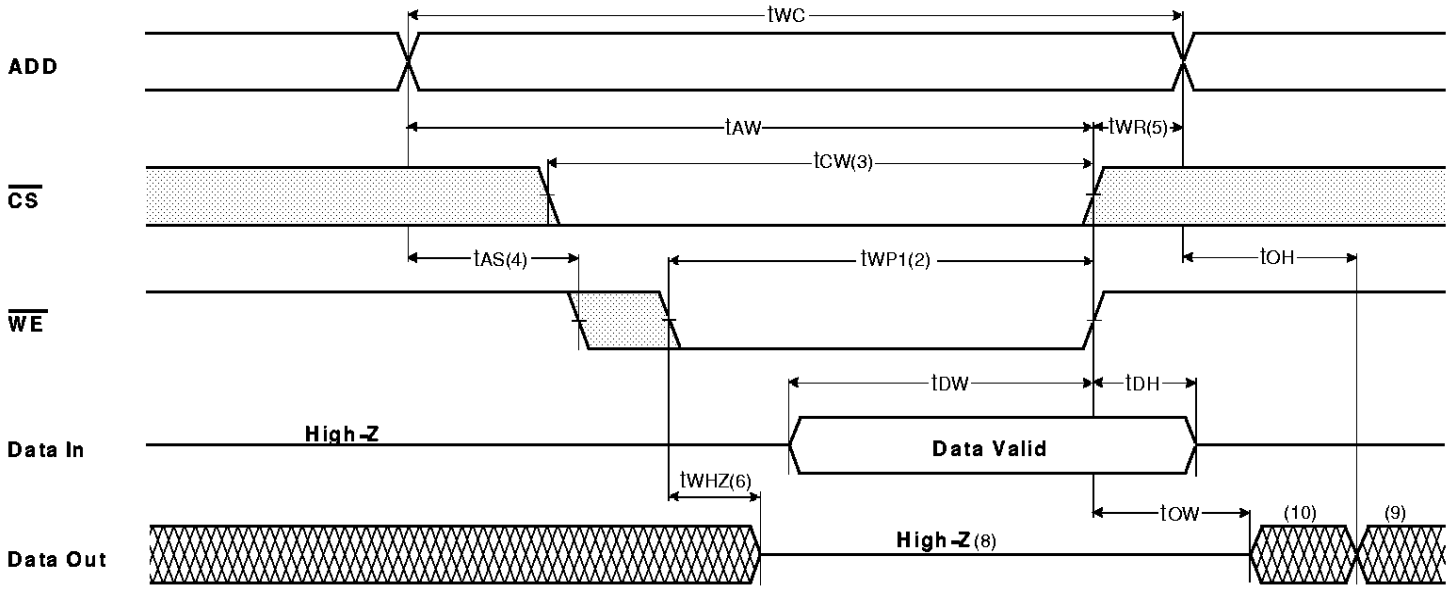
1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} Levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ} (Min.) both for a given device and from device to device.
5. Transition is measured ±200§˘ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycl e.

TIMING WAVE FORM OF WRITE CYCLE(1)($\overline{OE}$=Clock)

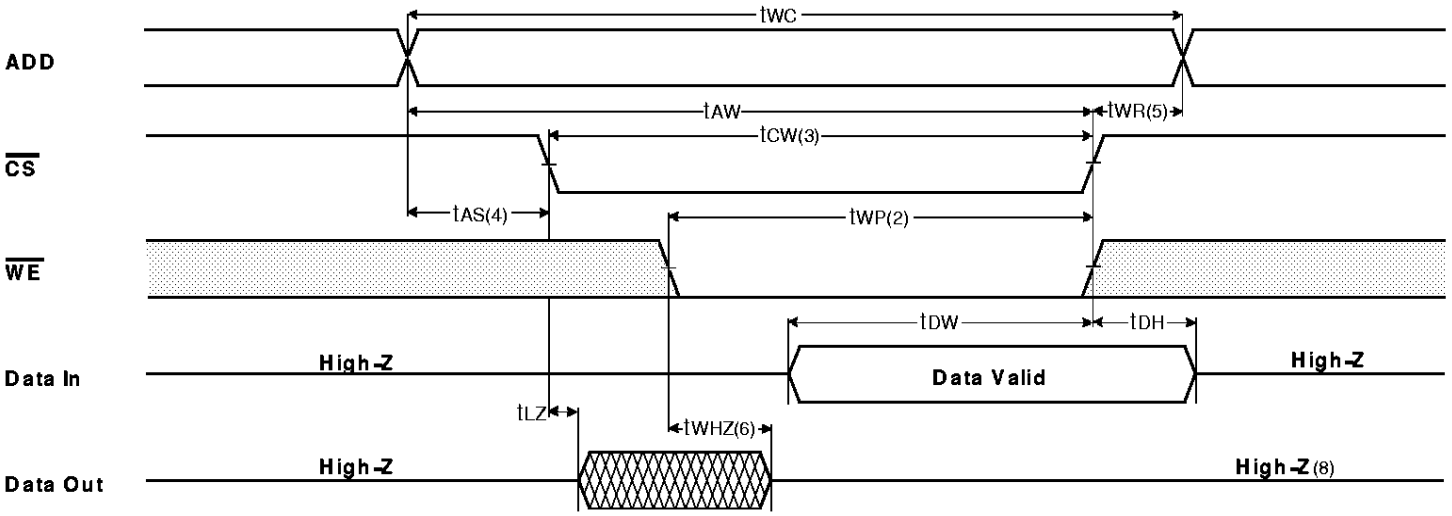


LECTRONICS

TIMING WAVE FORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



TIMING WAVE FORM OF WRITE CYCLE(3) ($\overline{CS}$=Controlled)



LECTRONICS

NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

* NOTE : X means Don't Care.

PACKAGE DIMENSIONS

36-SOJ-400

Units : Inches (millimeters)