CMOS PARALLEL-TO-SERIAL FIFO
256 x 16, 512 x 16, 1024 x 16

IDT72105
IDT72115
IDT72125

Integrated Device Technology, Inc.

FEATURES:

- 25ns parallel port access time, 35ns cycle time
- 45MHz serial output shift rate
- Wide x16 organization offering easy expansion
- Low power consumption (50mA typical)
- Least/Most Significant Bit first read selected by asserting the FL/DIR pin
- Four memory status flags: Empty, Full, Half-Full, and Almost-Empty/Almost-Full
- Dual-Port zero fall-through architecture
- Available in 28-pin 300 mil plastic DIP, 28-pin SOIC, and 32-pin PLCC

DESCRIPTION:

The IDT72105/72115/72125s are very high-speed, low-power, dedicated, parallel-to-serial FIFOs. These FIFOs possess a 16-bit parallel input port and a serial output port with 256, 512 and 1K word depths, respectively.

The ability to buffer wide word widths (x16) make these FIFOs ideal for laser printers, FAX machines, local area networks (LANs), video storage and disk/tape controller applications.

Expansion in width and depth can be achieved using multiple chips. IDT's unique serial expansion logic makes this possible using a minimum of pins.

The unique serial output port is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant Bit can be read first by programming the DIR pin after a reset.

Monitoring the FIFO is eased by the availability of four status flags: Empty, Full, Half-Full and Almost-Empty/Almost-Full. The Full and Empty flags prevent any FIFO data overflow or underflow conditions. The Half-Full Flag is available in both single and expansion mode configurations. The Almost-Empty/Almost-Full Flag is available only in a single device mode.

The IDT72105/15/25 are fabricated using IDT's leading edge, submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of Mil-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM
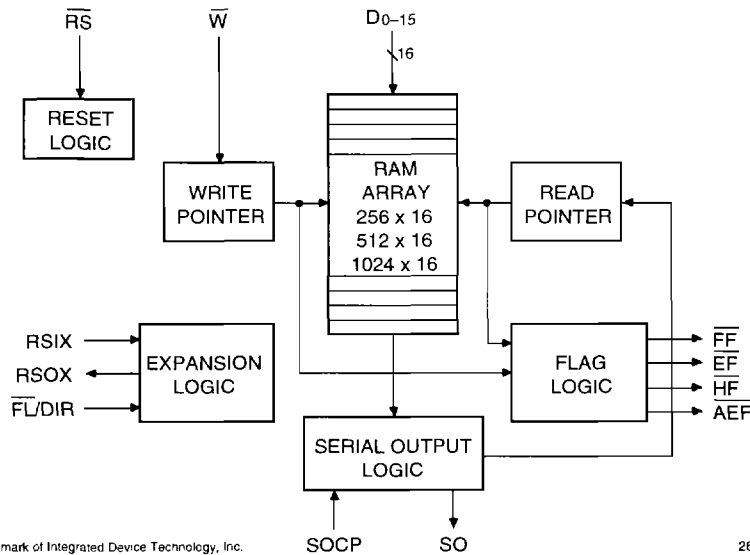
The IDT logo is a registered trademark of Integrated Device Technology, Inc.
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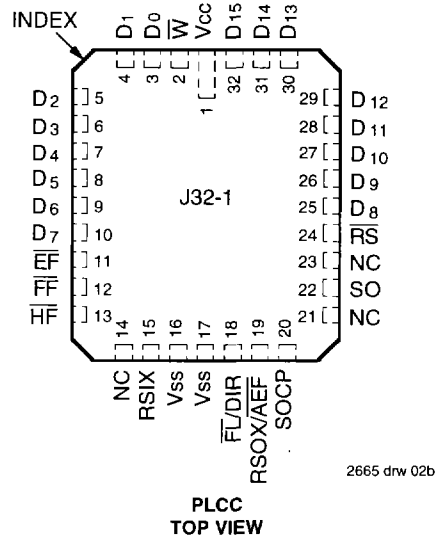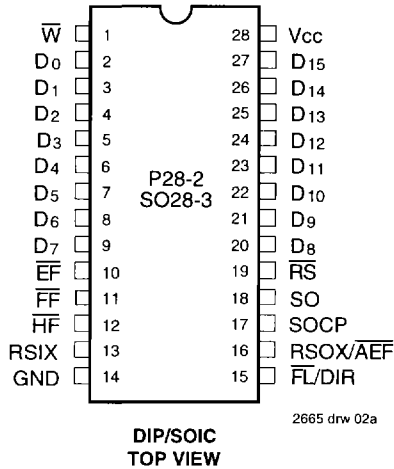
2665 drw 01

COMMERCIAL TEMPERATURE RANGE   **AUGUST 1993**

DSC-2038/4

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PIN CONFIGURATIONS

DIP/SOIC
TOP VIEW

2665 drw 02a

PLCC
TOP VIEW

2665 drw 02b

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0–D_{15}	Inputs	I	Data inputs for 16-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{FL}$/DIR	First Load/ Direction	I	This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) pin controls shift direction after Reset and tells the device whether to read out the Least Significant or Most Significant bit first.
RSIX	Read Serial In Expansion	I	In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty.
$\overline{HF}$	Half-Full Flag	O	When $\overline{HF}$ is LOW, the device is more than half-full. When $\overline{HF}$ is HIGH, the device is empty to half-full.
RSOX/$\overline{AEF}$	Read Serial Out Expansion Almost-Empty, Almost-Full Flag	O	This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty-to-(1/8 full -1) or (7/8 full +1)-to-full. When $\overline{AEF}$ is HIGH, the device is 1/8-full up to 7/8-full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion.
Vcc	Power Supply		Single power supply of 5V.
GND	Ground		Single ground of 0V.

2665 tbl 01

STATUS FLAGS

Number of Words in FIFO			$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
IDT72105	IDT72115	IDT72125				
0	0	0	H	L	H	L
1–31	1–63	1–127	H	L	H	H
32–128	64–256	128–512	H	H	H	H
129–224	257–448	513–896	H	H	L	H
225–255	449–511	897–1023	H	L	L	H
256	512	1024	L	L	L	H

2665 tbl 02

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to + 7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	−55 to +125	°C
T_{STG}	Storage Temperature	−55 to + 125	°C
I_{OUT}	DC Output Current	50	mA

NOTE: 2665 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}[1]	Input Low Voltage	—	—	0.8	V

NOTE: 2665 tbl 04
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS
(Commercial Vcc = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72105/IDT72115/ IDT72125 Commercial			Unit
		Min.	Typ.	Max.	
I_{IL}[1]	Input Leakage Current (Any Input)	−1	—	1	μA
I_{OL}[2]	Output Leakage Current	−10	—	10	μA
V_{OH}	Output Logic "1" Voltage I_{OUT} = −2mA[5]	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA[6]	—	—	0.4	V
I_{CC1} [3]	Power Supply Current	—	50	100	mA
I_{CC2} [3]	Average Standby Current ($\overline{W} = \overline{RS} = \overline{FL}/DIR = V_{IH})(SOCP = V_{IL})$	—	4	8	mA
I_{CC3} [3,4,7]	Power Down Current	—	1	6	mA

NOTES: 2665 tbl 05
1. Measurements with $0.4V \leq V_{IN} \leq V_{CC}$.
2. $SOCP = V_{IL}$, $0.4 \leq V_{OUT} \leq V_{CC}$.
3. Icc measurements are made with outputs open.
4. $\overline{RS} = \overline{FL}/DIR = \overline{W} = V_{CC}$ - 0.2V; SOCP = 0.2V; all other inputs ≥ Vcc - 0.2 or ≤ 0.2V.
5. For SO, I_{OUT} = -4mA.
6. For SO, I_{OUT} = 16mA.
7. Measurements are made after reset.

AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC} = 5V\pm10\%$, $T_A = 0°C$ to $+70°C$)

Symbol	Parameter	Figure	COM'L 72105L25 72115L25 72125L25 Min.	Max.	COM'L 72105L50 72115L50 72125L50 Min.	Max.	Unit
ts	Parallel Shift Frequency	—	—	28.5	—	15	MHz
tsocp	Serial Shift Frequency	—	—	50	—	40	MHz
PARALLEL INPUT TIMINGS							
twc	Write Cycle Time	2	35	—	65	—	ns
twpw	Write Pulse Width	2	25	—	50	—	ns
twR	Write Recovery Time	2	10	—	15	—	ns
tDS	Data Set-up Time	2	12	—	15	—	ns
tDH	Data Hold Time	2	0	—	2	—	ns
tWEF	Write High to $\overline{EF}$ HIGH	5, 6	—	35	—	45	ns
tWFF	Write Low to $\overline{FF}$ LOW	4, 7	—	35	—	45	ns
tWF	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
tWPF	Write Pulse Width After $\overline{FF}$ HIGH	7	25	—	50	—	ns
SERIAL OUTPUT TIMINGS							
tsocp	Serial Clock Cycle Time	3	20	—	25	—	ns
tsocw	Serial Clock Width HIGH/LOW	3	8	—	10	—	ns
tsopd	SOCP Rising Edge to SO Valid Data	3	—	14	—	15	ns
tsoHZ	SOCP Rising Edge to SO at High-Z[1]	3	3	14	3	15	ns
tsoLZ	SOCP Rising Edge to SO at Low-Z[1]	3	3	14	3	15	ns
tsocEF	SOCP Rising Edge to $\overline{EF}$ LOW	5, 6	—	35	—	45	ns
tsocFF	SOCP Rising Edge to $\overline{FF}$ HIGH	4, 7	—	35	—	45	ns
tsocF	SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$	8	—	35	—	45	ns
tREFSO	SOCP Delay After $\overline{EF}$ HIGH	6	35	—	65	—	ns
RESET TIMINGS							
tRSC	Reset Cycle Time	1	35	—	65	—	ns
tRS	Reset Pulse Width	1	25	—	50	—	ns
tRSS	Reset Set-up Time	1	25	—	50	—	ns
tRSR	Reset Recovery Time	1	10	—	15	—	ns
EXPANSION MODE TIMINGS							
tFLS	$\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge	9	7	—	8	—	ns
tFLH	$\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge	9	0	—	2	—	ns
tDIRS	DIR Set-up Time to SOCP Rising Edge	9	10	—	12	—	ns
tDIRH	DIR Hold Time from SOCP Rising Edge	9	5	—	5	—	ns
tsoXD1	SOCP Rising Edge to RSOX Rising Edge	9	—	15	—	17	ns
tsoXD2	SOCP Rising Edge to RSOX Falling Edge	9	—	15	—	17	ns
tsIXS	RSIX Set-up Time to SOCP Rising Edge	9	5	—	8	—	ns
tsIXPW	RSIX Pulse Width	9	10	—	15	—	ns

NOTE:
1. Values guaranteed by design.

2665 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2665 tbl 07

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	12	pF

NOTE: 2665 tbl 08
1. This parameter is sampled and not 100% tested.
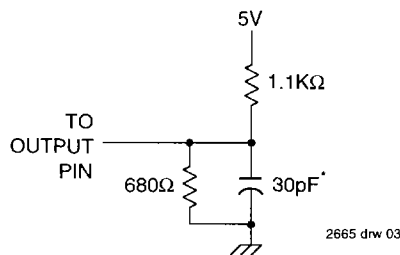
or equivalent circuit

Figure A. Output Load

*Includes jig and scope capacitances.

FUNCTIONAL DESCRIPTION

Parallel Data Input

The device must be reset before beginning operation so that all flags are set to their initial state. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the D_{0-15} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is internally inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first, depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.
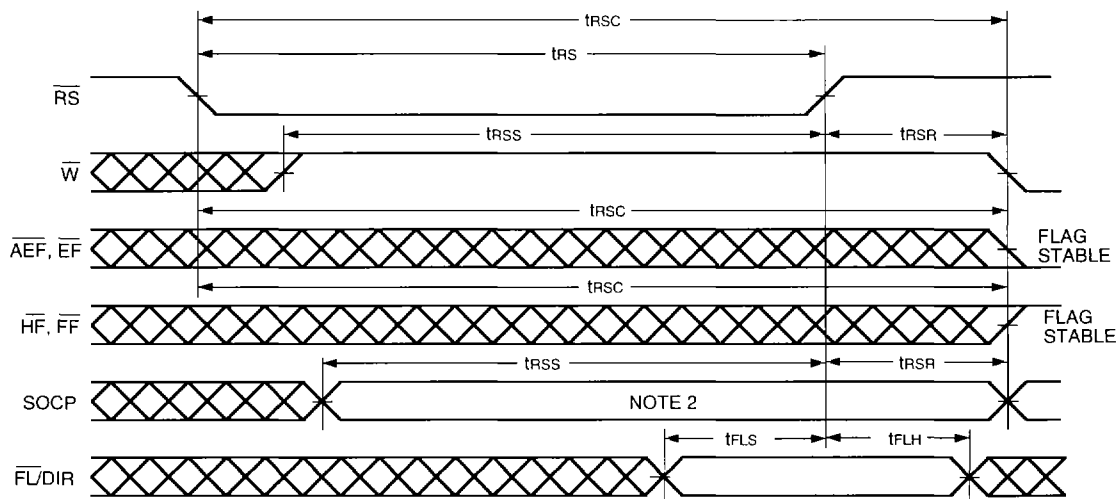
NOTES:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at t_{RSC}.
2. SOCP should be in the steady LOW or HIGH during t_{RSS}. The first LOW-HIGH (or HIGH-LOW) transition can begin after t_{RSR}.
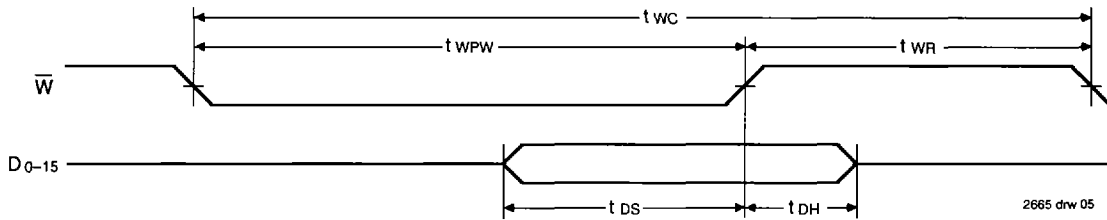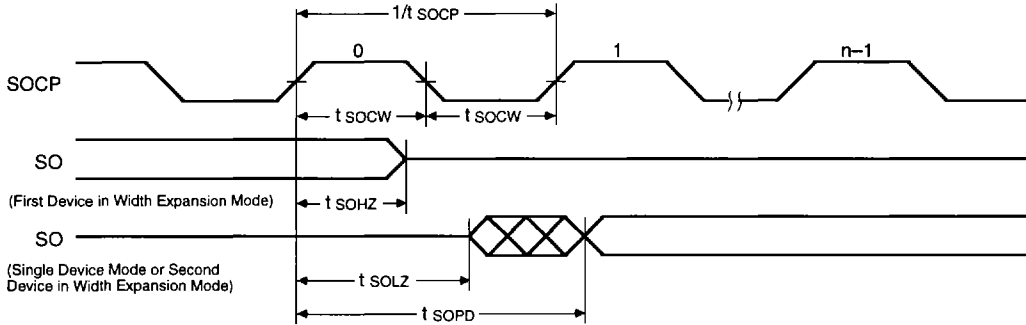
Figure 1. Reset

Figure 2. Write Operation

NOTE:
1. In Single Device Mode, SO will not tri-state except after reset.

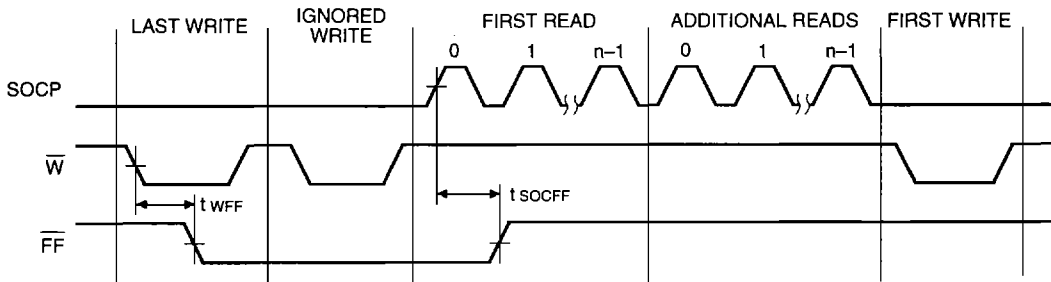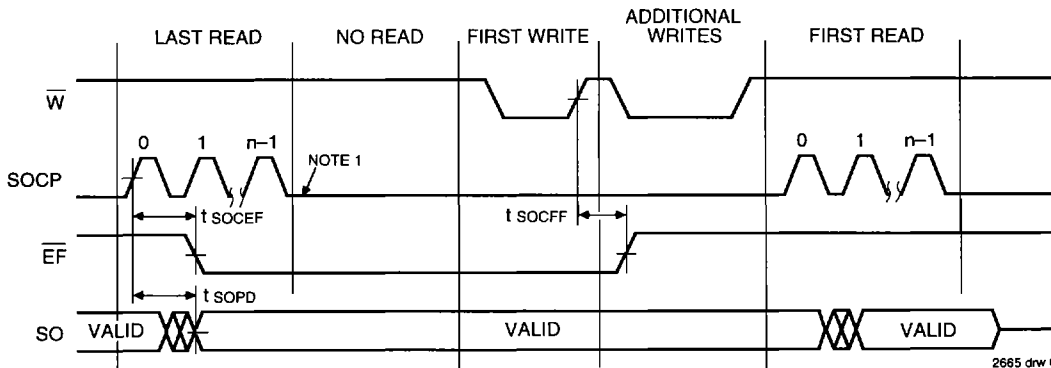Figure 3. Read Operation

Figure 4. Full Flag from Last Write to First Read

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 5. Empty Flag from Last Read to First Write

NOTE:
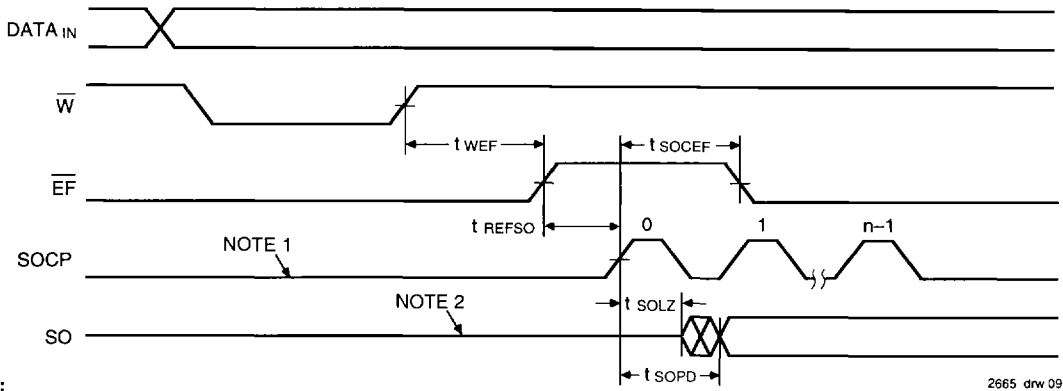1. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.
2. In Single Device Mode, SO will not tri-state except after Reset. It will retain the last valid data.

Figure 6. Empty Boundary Condition Timing

NOTE:
1. Single Device Mode will not tri-state but will retain the last valid data.
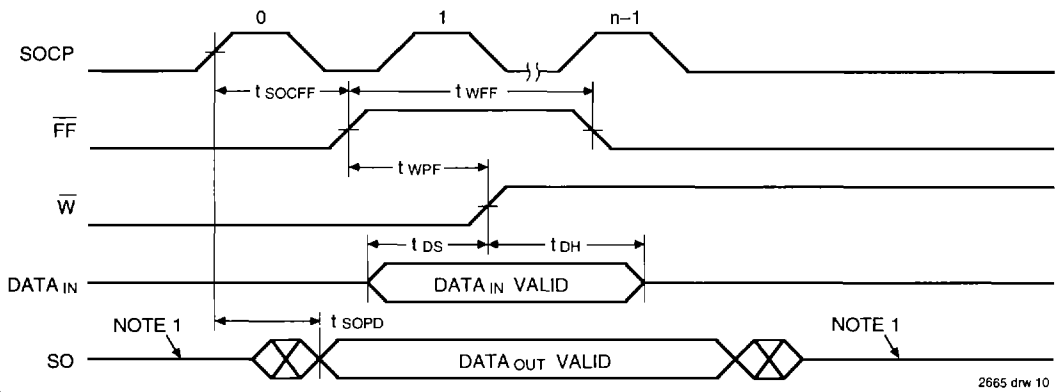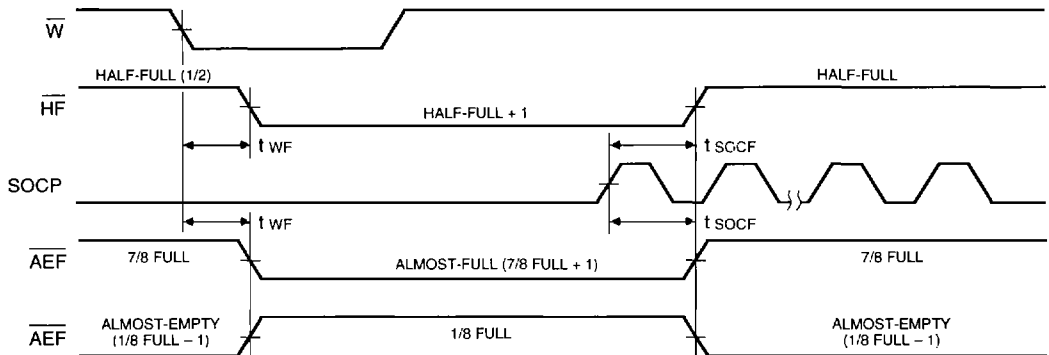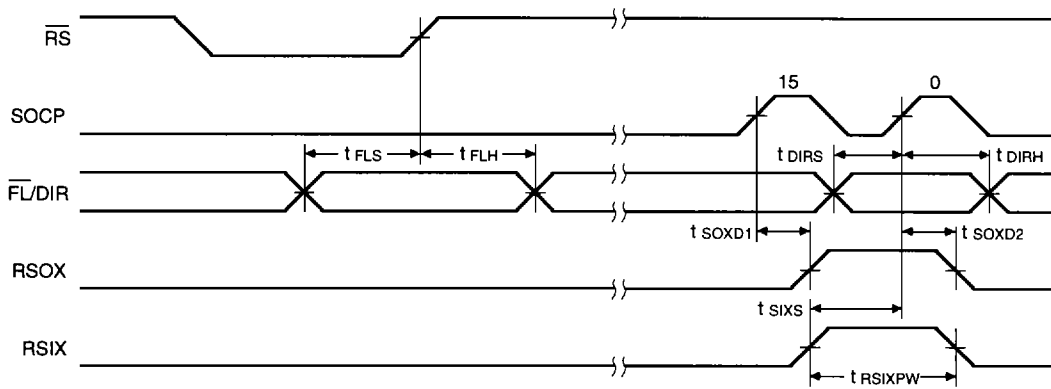
Figure 7. Full Boundary Condition Timing

Figure 8. Half-Full, Almost-Full and Almost-Empty Timings

Figure 9. Serial Read Expansion

OPERATING CONFIGURATIONS

Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$ and outputs the Almost-Empty and Almost-Full Flag.

Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together, as shown in Figure 11, and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.
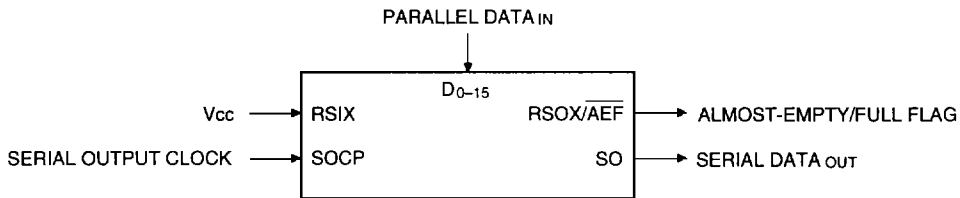
Figure 10. Single Device Configuration

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{AEF}, \overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	X	Location Zero	Location Zero	0	1	1
Read/Write	1	X	0,1	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

2665 tbl 09

Table 1. Reset and First Load Truth Table–Single Device Configuration

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half-Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost-Empty/Almost-Full flag is not available. The RSOX pin is used for expansion.
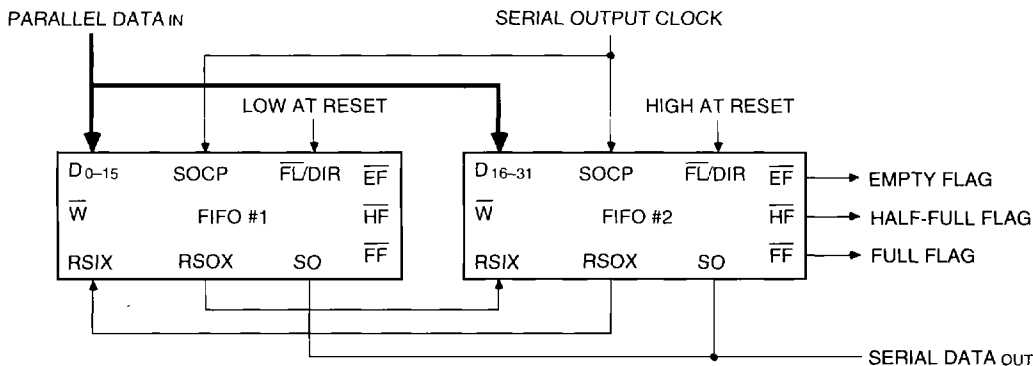

Figure 11. Width Expansion for 32-bit Parallel Data In

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Depth Expansion (Daisy Chain) Mode

The IDT72105/15/25 can easily be adapted to applications requiring greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25s and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO is being written. A word of data must be written sequentially into each FIFO so that the data will be read in the correct sequence. The IDT72105/15/25 operates in the Depth Expansion Mode when the following conditions are met:

1. The first device must be programmed by holding $\overline{FL}$ LOW at Reset. All other devices must be programmed by holding $\overline{FL}$ HIGH at reset.
2. The Read Serial Out Expansion pin (RSOX) of each device must be tied to the Read Serial In Expansion pin (RSIX) of the next device (see Figure 12).

3. External logic is needed to generate composite Empty, Half-Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost-Empty and Almost-Full Flag is not available due to using the RSOX pin for expansion.

Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant Device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.
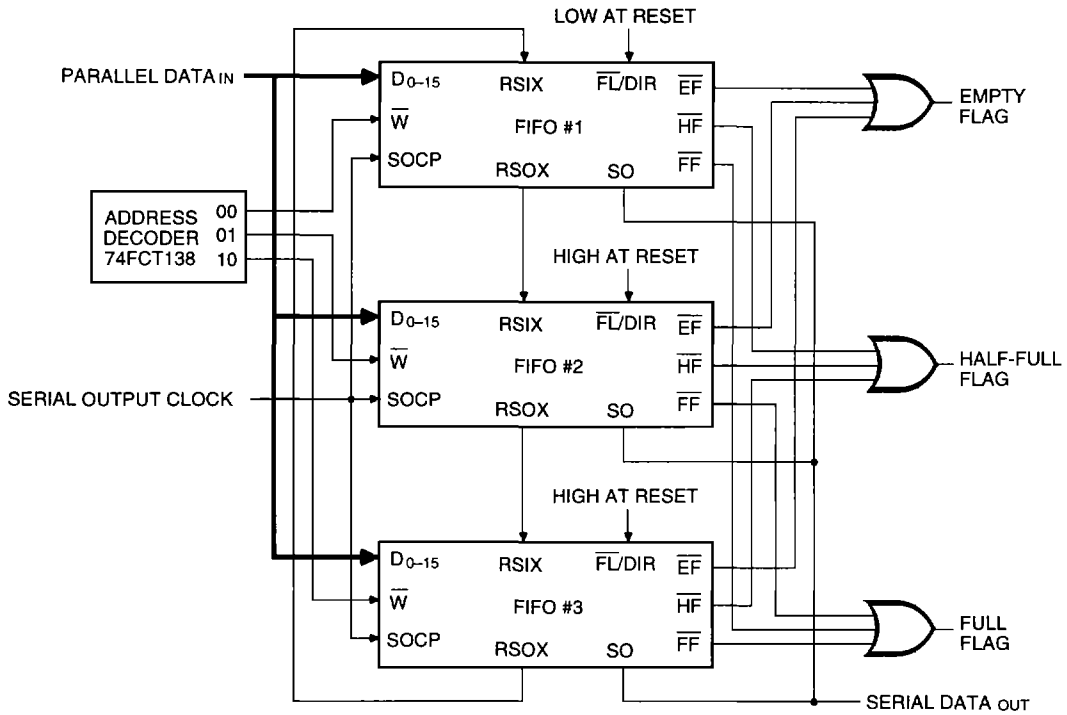
2665 drw 15

Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	DIR	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{HF}, \overline{FF}$
Reset-First Device	0	0	X	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	X	Location Zero	Location Zero	0	1
Read/Write	1	X	0,1	X	X	X	X

NOTE:
1.　$\overline{RS}$ = Reset Input, $\overline{FL}$/FIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half- Full Flag Output, $\overline{FF}$ = Full Flag Output.

2665 tbl 10

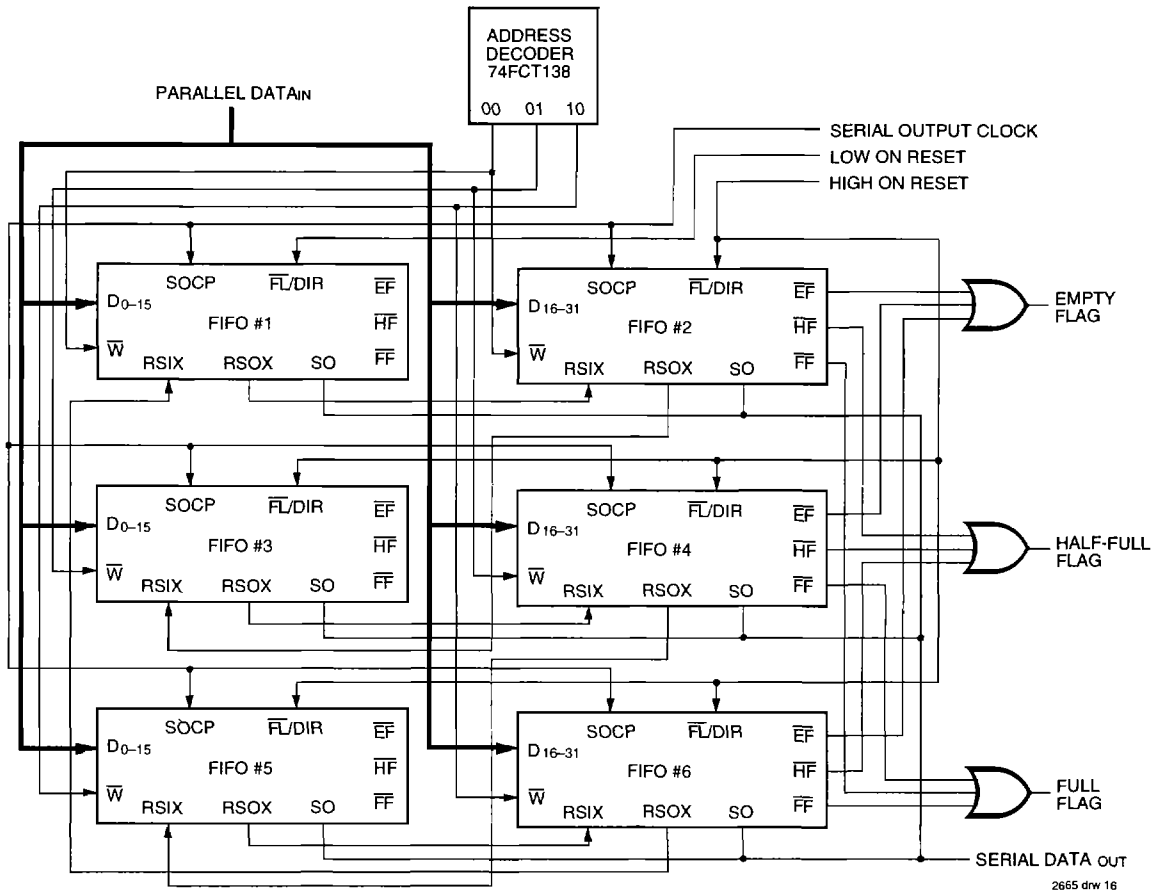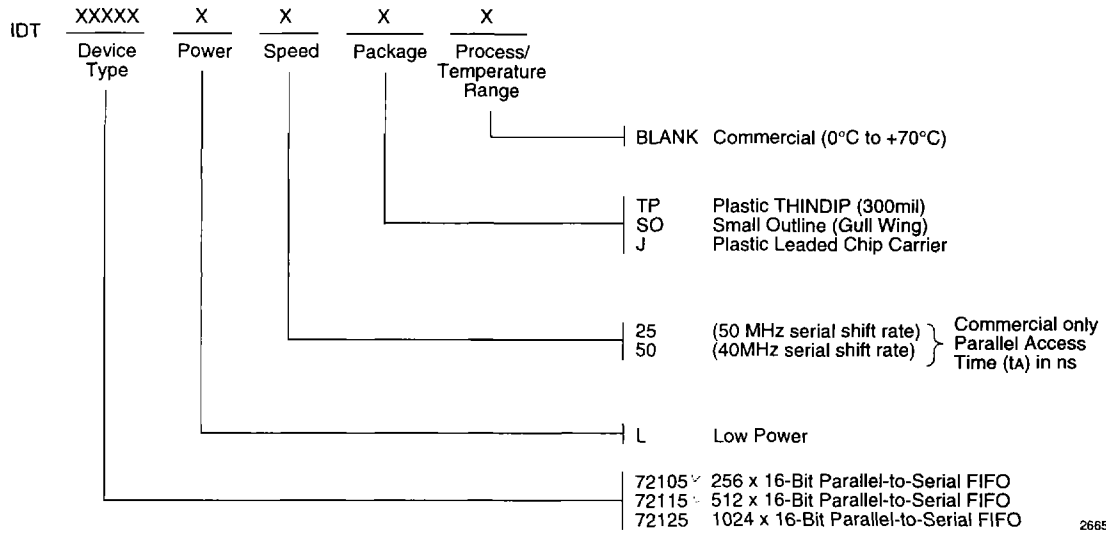**Table 2. Reset and First Load Truth Table–Width/Depth Compound Expansion Mode**

Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125

2665 drw 16

ORDERING INFORMATION

IDT   XXXXX   X   X   X   X

Device Type   Power   Speed   Package   Process/ Temperature Range

BLANK	Commercial (0°C to +70°C)

TP	Plastic THINDIP (300mil)
SO	Small Outline (Gull Wing)
J	Plastic Leaded Chip Carrier

25	(50 MHz serial shift rate)	Commercial only Parallel Access Time (tA) in ns
50	(40MHz serial shift rate)	

L	Low Power

72105	256 x 16-Bit Parallel-to-Serial FIFO
72115	512 x 16-Bit Parallel-to-Serial FIFO
72125	1024 x 16-Bit Parallel-to-Serial FIFO

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