# CY7C170A

## 4K x 4 Static RAM

### Features

- **CMOS for optimum speed/power**
- **High speed**
  - **— $t_{AA}$ = 15 ns**
  - **— $t_{ACS}$ = 10 ns**
- **Low active power**
  - **— 495 mW (commercial)**
  - **— 660 mW (military)**
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**
- **Output enable**
- **$V_{IH}$ of 2.2V**

### Functional Description

The CY7C170A is a high-performance CMOS static RAM organized as 4096 words by 4 bits. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$), an active LOW output enable ($\overline{OE}$) and three-state drivers.

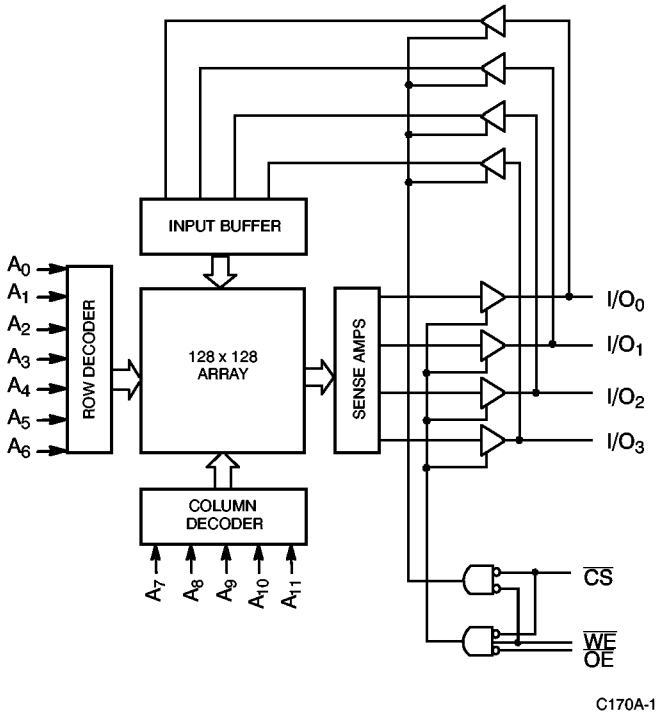
Writing to the device is accomplished when the chip select ($\overline{CS}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input/output pins ($I/O_0$ through $I/O_3$) is written into the memory location specified on the address pins ($A_0$ through $A_{11}$).

Reading the device is accomplished by taking chip select ($\overline{CS}$) and output enable ($\overline{OE}$) LOW, while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in high-impedance state when chip select ($\overline{CS}$) or output enable ($\overline{OE}$) is HIGH, or write enable ($\overline{WE}$) is LOW.

A die coat is used to insure alpha immunity.

### Logic Block Diagram

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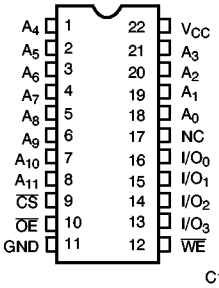
### Pin Configurations

**DIP**
**Top View**

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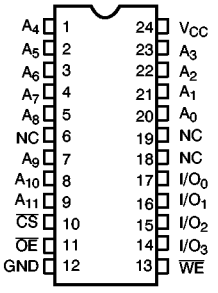
**SOJ**
**Top View**

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### Selection Guide

| | | 7C170A–15 | 7C170A–20 | 7C170A–25 | 7C170A–35 |
|---|---|---|---|---|---|
| Maximum Access Time (ns) | | 15 | 20 | 25 | 35 |
| Maximum Operating Current (mA) | Commercial | 115 | 90 | 90 | 90 |
| | Military | | | 120 | |

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 22 to Pin 21) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Commercial | 0°C to +70°C | 5V ± 10% |
| Military[1] | −55°C to +125°C | 5V ± 10% |

## Electrical Characteristics Over the Operating Range[2]

| Parameter | Description | Test Conditions | | 7C170A−15 Min. | 7C170A−15 Max. | 7C170A−20, 25, 35, 45 Min. | 7C170A−20, 25, 35, 45 Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min., $I_{OH}$ = −4.0 mA | | 2.4 | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min., $I_{OL}$ = 8.0 mA | | | 0.4 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.2 | $V_{CC}$ | 2.2 | $V_{CC}$ | V |
| $V_{IL}$ | Input LOW Voltage | | | −3.0 | 0.8 | −3.0 | 0.8 | V |
| $I_{IX}$ | Input Load Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | −10 | +10 | −10 | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_O$ ≤ $V_{CC}$, Output Disabled | | −10 | +10 | −10 | +10 | µA |
| $I_{OS}$ | Output Short Circuit Current[3] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | | −350 | | −350 | mA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | $V_{CC}$ = Max. $I_{OUT}$ = 0 mA | Com'l | | 115 | | 90 | mA |
| | | | Mil | | | | 120 | mA |

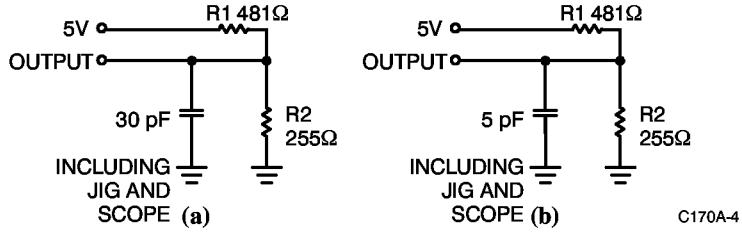
## Capacitance[4]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 5.0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

**Notes:**

1. $T_A$ is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

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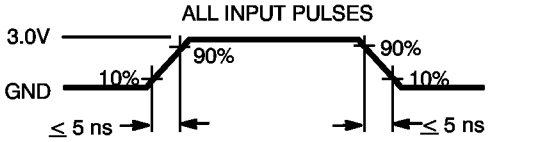


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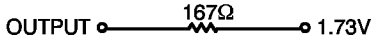
Equivalent to: THÉVENIN EQUIVALENT



## Switching Characteristics Over the Operating Range[2, 5]

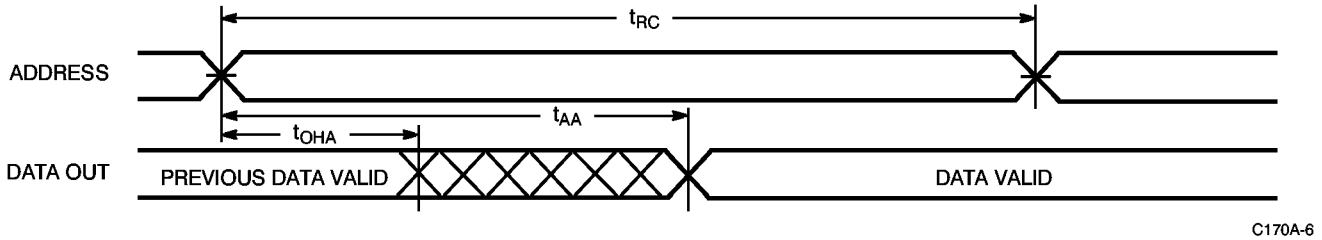
| Parameter | Description | 7C170A–15 | | 7C170A–20 | | 7C170A–25 | | 7C170A–35 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| **READ CYCLE** | | | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 15 | | 20 | | 25 | | 35 | | ns |
| $t_{AA}$ | Address to Data Valid | | 15 | | 20 | | 25 | | 35 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{ACS}$ | $\overline{CS}$ LOW to Data Valid | | 10 | | 15 | | 15 | | 25 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 10 | | 10 | | 12 | | 15 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z | 3 | | 3 | | 3 | | 3 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[6] | | 8 | | 8 | | 10 | | 12 | ns |
| $t_{LZCS}$ | $\overline{CS}$ LOW to Low Z[7] | 5 | | 5 | | 5 | | 5 | | ns |
| $t_{HZCS}$ | $\overline{CS}$ HIGH to High Z[6, 7] | | 8 | | 8 | | 10 | | 15 | ns |
| **WRITE CYCLE**[8] | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 15 | | 20 | | 20 | | 25 | | ns |
| $t_{SCS}$ | $\overline{CS}$ LOW to Write End | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{AW}$ | Address Set-Up to Write End | 12 | | 15 | | 20 | | 25 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 12 | | 15 | | 15 | | 20 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 10 | | 10 | | 10 | | 15 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ HIGH to High Z | | 7 | | 7 | | 7 | | 10 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z | 5 | | 5 | | 5 | | 5 | | ns |

**Notes:**

5. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified $I_{OI}/I_{OH}$, and 30-pF load capacitance.
6. $t_{HZCE}$ and $t_{HZWE}$ are tested with $C_L$ = 5pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
7. At any given temperature and voltage condition, $t_{HZCS}$ is less than $t_{LZCS}$ for any given device. These parameters are sampled and not 100% tested.
8. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CS}$ = $V_{IL}$ and $\overline{OE}$ = $V_{IL}$.

## Switching Waveforms

**Read Cycle No. 1**[9, 10]

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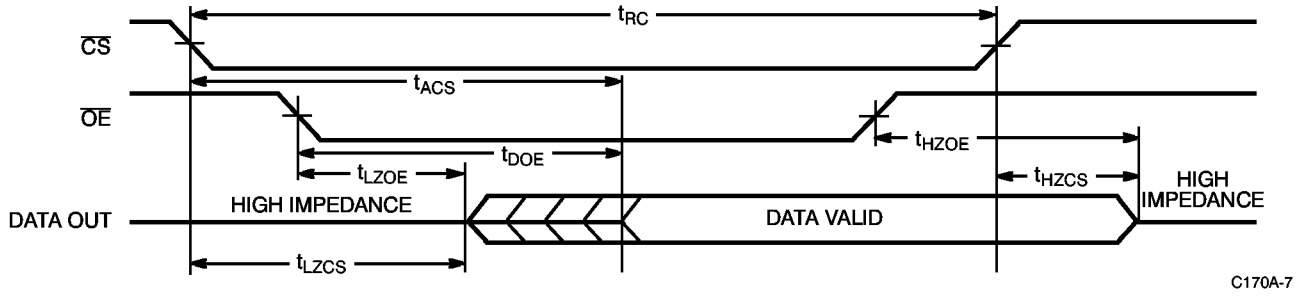
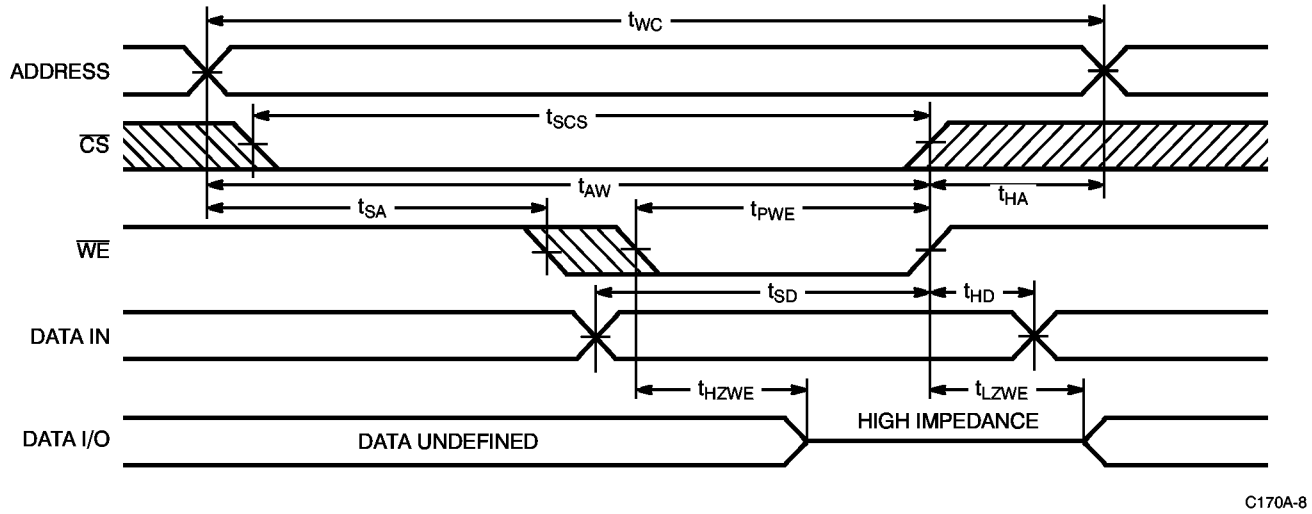
## Switching Waveforms (continued)

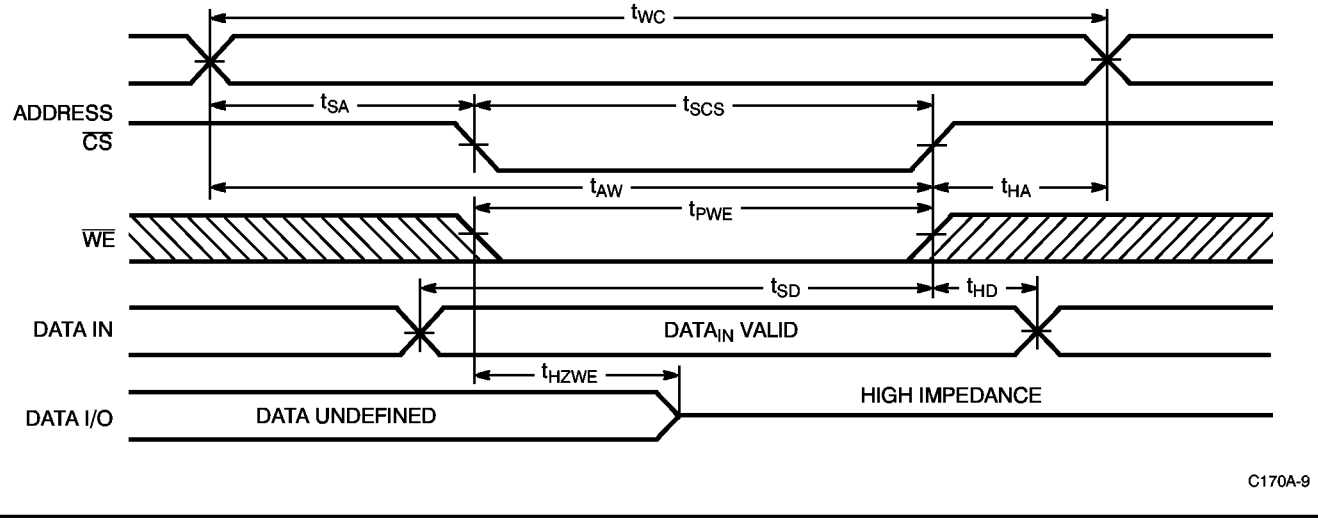
### Read Cycle No. 2[9, 11]




### Write Cycle No. 1[8, 12]




### Write Cycle No. 2[8, 12, 13]




**Notes:**
11. Data I/O will be high-impedance if $\overline{OE}$ = $V_{IH}$.
12. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
13. If $\overline{CS}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C170A−15PC | P9 | 22-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C170A−15VC | V13 | 24-Lead Molded SOJ | |
| 20 | CY7C170A−20PC | P9 | 22-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C170A−20VC | V13 | 24-Lead Molded SOJ | |
| 25 | CY7C170A−25PC | P9 | 22-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C170A−25VC | V13 | 24-Lead Molded SOJ | |
| | CY7C170A−25DMB | D10 | 22-Lead (300-Mil) CerDIP | Military |
| 35 | CY7C170A−35PC | P9 | 22-Lead (300-Mil) Molded DIP | Commercial |
| | CY7C170A−35VC | V13 | 24-Lead Molded SOJ | |

## MILITARY SPECIFICATIONS

### Group A Subgroup Testing

#### DC Characteristics

| Parameter | Subgroups |
|---|---|
| $V_{OH}$ | 1, 2, 3 |
| $V_{OL}$ | 1, 2, 3 |
| $V_{IH}$ | 1, 2, 3 |
| $V_{IL}$ Max. | 1, 2, 3 |
| $I_{IX}$ | 1, 2, 3 |
| $I_{OZ}$ | 1, 2, 3 |
| $I_{CC}$ | 1, 2, 3 |

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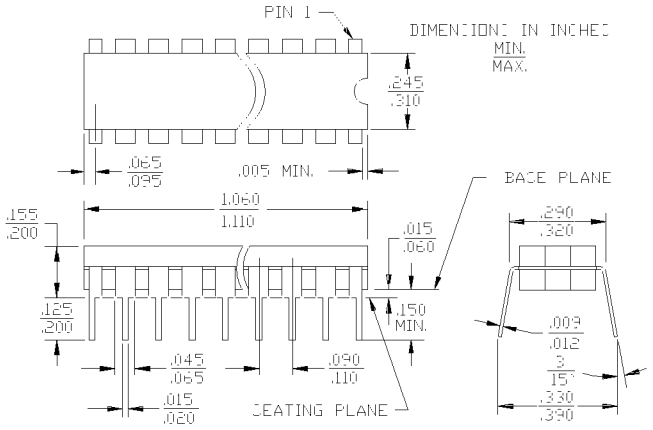
#### Switching Characteristics

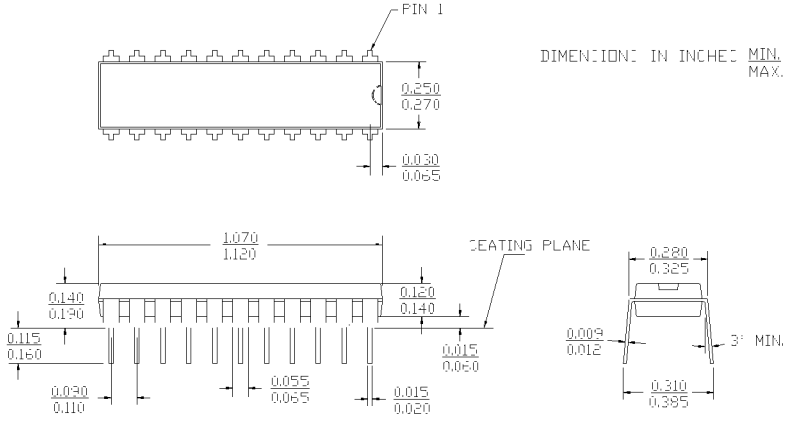
| Parameter | Subgroups |
|---|---|
| **READ CYCLE** | |
| $t_{RC}$ | 7, 8, 9, 10, 11 |
| $t_{AA}$ | 7, 8, 9, 10, 11 |
| $t_{OHA}$ | 7, 8, 9, 10, 11 |
| $t_{ACS}$ | 7, 8, 9, 10, 11 |
| $t_{DOE}$ | 7, 8, 9, 10, 11 |
| **WRITE CYCLE** | |
| $t_{WC}$ | 7, 8, 9, 10, 11 |
| $t_{SCS}$ | 7, 8, 9, 10, 11 |
| $t_{AW}$ | 7, 8, 9, 10, 11 |
| $t_{HA}$ | 7, 8, 9, 10, 11 |
| $t_{SA}$ | 7, 8, 9, 10, 11 |
| $t_{PWE}$ | 7, 8, 9, 10, 11 |
| $t_{SD}$ | 7, 8, 9, 10, 11 |
| $t_{HD}$ | 7, 8, 9, 10, 11 |

## Package Diagrams

**22-Lead (300-Mil) CerDIP D10**

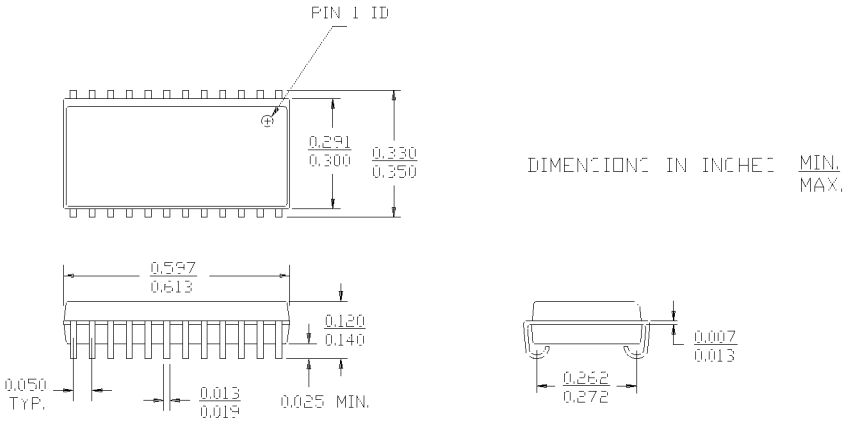



**22-Lead (300-Mil) Molded DIP P9**



## Package Diagrams (continued)

**24-Lead Molded SOJ V13**

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