FEATURES	CPS-1848	CPS-1432	CPS/SPS-1616	CPS-6Q	/10Q	CPS-8	/12	/16	Tsi572	/574	/578	Tsi577	Tsi620
Performance and Configurability													
Serial RapidIO specifications	2.1	2.1	2.1	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
Aggregate peak throughput (Gbps)	240	160	80	60	100	20	30	40	30	40	80	40	50
Full mesh non-blocking fabric	√	√	√	√		√	√	√	√	√	√	√	√
Asymmetric non-blocking fabric					√								
Maximum of number of x4 ports	12	8	4	6	10	2	3	4	2	4	8	4	3
Maximum of number of x2 ports	18	14	8										
Maximum of number of x1 port	18	14	16	16	16	8	12	16	8	8	16	16	6
Cut-through latency (ns)	100	100	100	190	190	190	190	190	110	110	110	110	110
Store and forward mode	√	√	√	√	√	√	√	√	√	√	√	√	√
Configurable by speed	Each Quad	Each Quad	CPS/SPS - Each Lane	Each Quad	Each Quad	Each Lane Pair			Each MAC			Each Quad	Each MAC
SerDes and Power													
Power per 10 Gbps link (typical, mW)	<300	<385	CPS/SPS <440	<500		<500			<500			<500	<500
Identical long and short reach power									√	√	√	√	√
Per port power down	√	√	√	√	√	√	√	√	√	√	√	√	√
Programmable transmit drive strength and pre-emphasis	√	√	√	√	√	√	√	√	√	√	√	√	√
Programmable receive equalization	√	√	√						√	√	√	√	√
On-die scope capability									√	√	√	√	√
Multicast and Routing													
Per port multicast architecture	√	√	√	√	√	√	√	√					
Parallel multicast engine with QoS support									√	√	√	√	√
Per port multicast masks/groups	40	40	40	40	40	10	10	10	8	8	8	8	8
8- and 16-bit addressing	√	√	√	√	√	√	√	√	√	√	√	√	√
Programmable watermarks on ingress buffers	√	√	√	√	√	√	√	√	√	√	√	√	√
RapidIO Standard and Non-Standard Features													
Packet/trace/mirror/ filter for debug	√	√	√	√	√	√	√	√					
Traffic management through user selectable scheduling algorithms	√	√	√						√	√	√	√	√
Receiver controlled flow control	√	√	√	√	√	√	√	√	√	√	√	√	√
Transmitter controlled flow control	√	√	√										
Performance counters/monitors	√	√	√	√	√	√	√	√	√	√	√	√	√
Dedicated maintenance path for "5th priority"	√	√	√	√	√	√	√	√					
Error Management features exceeding S-RIO specification	√	√	√						√	√	√	√	√
Error log (history) and broad error detection coverage	√	√	√	√	√	√	√	√					
Link-layer AES-128 encryption			SPS on 4 1x Ports										
BOM Reduction and Clocking Options													
Clocking options (MHz)	156	156	156	156		156			156 or 125			156 or 125	156 or 125
No power-up sequence or ramp rate requirements				√	√	√	√	√					
Run RapidIO at CPRI and OBSAI speeds									√	√	√	√	√
Lane swap for board design simplification									√	√	√	√	√
Debug packet generator	√	√	√						√	√	√	√	√
Debug packet capture	√	√	√										√
Other Bridging and Unique features													
Built-in hardware bridging from RapidIO to PCI													√
Built-in bridging options to non-SerDes FPGA													√
Package (mm)	29 X 29	25 x 25	21 X 21	27 X 27	27 X 27	19 X 19	19 X 19	19 X 19	21 X 21	21 X 21	27 X 27	21 X 21	27 X 27

GD_S-RIO Switches_REVB0311