

Ultrahigh Speed Phase/Frequency Discriminator

AD9901

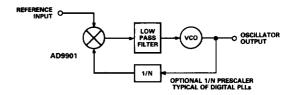
FEATURES

Phase and Frequency Detection
ECL/TTL/CMOS Compatible
Linear Transfer Function
No "Dead Zone"
MIL-STD-883 Compliant Versions Available

APPLICATIONS

Low Phase Noise Reference Loops
Fast-Tuning "Agile" IF Loops
Secure "Hopping" Communications
Coherent Radar Transmitter/Receiver Chains

PHASE-LOCKED LOOP



GENERAL DESCRIPTION

The AD9901 is a digital phase/frequency discriminator capable of directly comparing phase/frequency inputs up to 200MHz. Processing in a high speed trench-oxide isolated process, combined with an innovative design, gives the AD9901 a linear detection range, free of indeterminate phase detection zones common to other digital designs.

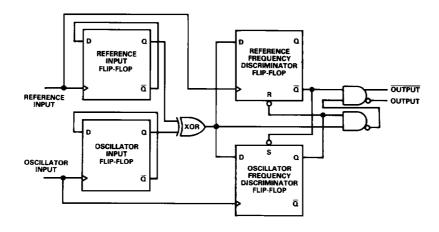
With a single +5V supply, the AD9901 can be configured to operate with TTL or CMOS logic levels; it can also operate with ECL inputs when operated with a -5.2V supply. The open-collector outputs allow the output swing to be matched to post-filtering input requirements. A simple current setting resistor controls the output stage current range, permitting a reduction in power when operated at lower frequencies.

A major feature of the AD9901 is its ability to compare phase-/frequency inputs at standard IF frequencies without prescalers. Excessive phase uncertainty which is common with standard PLL configurations is also eliminated. The AD9901 provides the locking speed of traditional phase/frequency discriminators, with the phase stability of analog mixers.

The AD9901 is available as a commercial temperature range device, 0°C to +70°C, and as a military temperature device, -55°C to +125°C. The commercial versions are packaged in a 14-pin ceramic DIP and a 20-pin PLCC.

The AD9901 Phase/Frequency Discriminator is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD9901/883B data sheet for specifications.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most recent version or complete data sheet, call our fax retrieval system at 1-800-446-6212.

AD9901 — SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS ¹	Operating Temperature Range
Positive Supply Voltage (+V _S for TTL Operation) +7V	AD9901KQ/KP0°C to +70°C
Negative Supply Voltage (-V _S for ECL Operation)7V	Storage Temperature Range65°C to +150°C
Input Voltage Range (TTL Operation) 0V to +5.5V	Junction Temperature ²
Differential Input Voltage (ECL Operation) 4.0V	Plastic
I _{SET} Current	Ceramic
Output Current	Lead Soldering Temperature (10sec)+300°C

ELECTRICAL CHARACTERISTICS $(\pm V_s = +5.0V \text{ [for TTL] or } -5.2V \text{ [for ECL], unless otherwise noted)}$

	Тетр		Commercial Temperature 0°C to +70°C AD9901KQ/KP			
		Test Level	Min	Тур	Max	Units
INPUT CHARACTERISTICS						
TTL Input Logic "1" Voltage	Full	VI	2.0			v
TTL Input Logic "0" Voltage	Full	VI			0.8	v
TTL Input Logic "1" Current ³	Full	VI			0.6	mA
TTL Input Logic "0" Current ³	Full	VI	1		1.6	mA
ECL Differential Switching Volt.	Full	VI	300			mV
ECL Input Current	Full	VI			20	μA
OUTPUT CHARACTERISTICS						
Peak-to-Peak Output Voltage Swing ⁴	Full	VI	1.6	1.8	2.0	v
TTL Output Compliance Range	Full	V		37		v
ECL Output Compliance Range	Full	v	Ì	±2		l v
I _{OUT} Range	Full	V		0.9–11		mA
Internal Reference Voltage	Full	VI	0.42	0.47	0.52	V
AC CHARACTERISTICS						
Linear Phase Detection Range ⁴			ĺ			Ì
40kHz	+25°C	V		360		Degrees
30MHz	+25°C	V	1	320		Degrees
70 MH z	+25°C	V	}	270		Degrees
Functionality @ 70MHz	+25°C	I		Pass/Fail		
POWER SUPPLY CHARACTERISTICS						
TTL Supply Current (+5.0V) ^{5, 6}	+25℃	I		43.5	54.0	mA
	Full	I		43.5	54.0	mA
ECL Supply Current (-5.2V) ^{5, 6}	+25℃	I		42.5	52.5	mA.
	Full	I		42.5	52.5	mA
Nominal Power Dissipation	+25°C	V		218		mW

Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

where:

PD = power dissipation

 θ_{JA} = thermal impedance from junction to air (°C/W)

 θ_{JC} = thermal impedance from junction to case (°C/W)

t_A = ambient temperature (°C)

 t_C = case temperature (°C)

typical thermal impedances:

AD9901 Ceramic DIP = θ_{JA} = 74°C/W; θ_{JC} = 21°C/W AD9901 LCC = θ_{JA} = 80°C/W; θ_{JC} = 19°C/W AD9901 PLCC = θ_{JA} = 88.2°C/W; θ_{JC} = 45.2°C/W $^{3}V_{L}$ = +0.4V; V_{R} = +2.4V.

 ${}^{4}R_{SET} = 47.5\Omega; R_{L} = 182\Omega.$

⁵Includes load current of 10mA (load resistors = 182Ω).

⁶Supply should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Description	Package Option ¹
AD9901KQ	0°C to +70°C	14-Pin Ceramic DIP	Q-14
AD9901KP	0°C to +70°C	20-Pin PLCC	P-20A
AD9901TQ/8832		14-Pin Ceramic DIP	Q-14
AD9901TE/883 ²	−55°C to +125°C	20-Contact Ceramic LCC	E-20A

¹E = Leadless Ceramic Chip Carrier; P = Plastic Leaded Chip Carrier; Q = Cerdip. For outline information see Package Information section.

²For specifications, refer to Analog Devices Military Products Databook.

²Maximum junction temperature should not exceed +175°C for ceramic packages, +150°C for plastic packages. Junction temperature can be calculated by: $t_{J} = PD(\theta_{JA}) + t_{A} = PD(\theta_{JC}) + t_{C}$

EXPLANATION OF TEST LEVELS

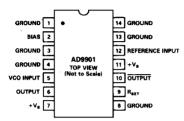
Test Level

- 100% production tested.
- II 100% production tested at +25°C, and sample tested at VI specified temperatures.
- III Sample tested only.
- IV Parameter is guaranteed by design and characterization
 - testing.

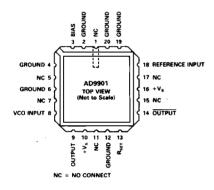
- ATION OF TEST EETEES
 - Parameter is a typical value only.
 All devices are 100% production tested at +25°C.
 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

PIN CONFIGURATIONS

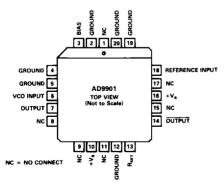
TTL DIP Pinouts



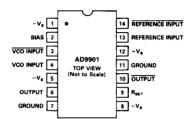
TTL LCC Pinouts



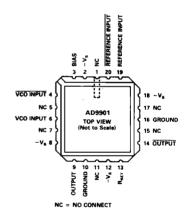
TTL PLCC Pinouts



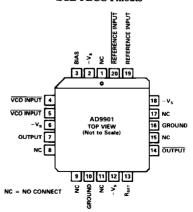
ECL DIP Pinouts



ECL LCC Pinouts



ECL PLCC Pinouts



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