Am99C68/Am99CL68

4096 x 4 CMOS Static R/W Random-Access Memory

DISTINCTIVE CHARACTERISTICS

- High speed — access times as fast as 45 ns
- Fully static storage and interface circuitry
- No clocks or timing signals required
- Automatic power down when deselected
- Low power dissipation:
  - Active: 660 mW Max.
  - Standby: 11 mW Max. (Am99C68)
    275 μW Max. (Am99CL68)
- Standard 20-pin, .300-inch dual-in-line package
- TTL-compatible interface levels
- 2-V data retention

GENERAL DESCRIPTION

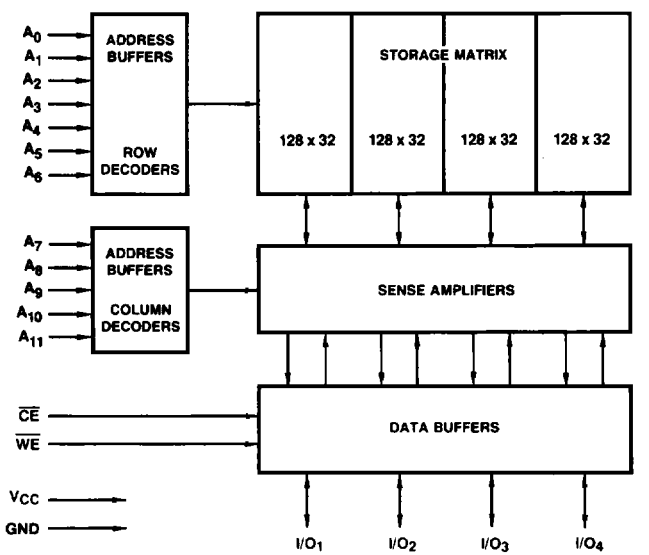
The Am99C68 and Am99CL68 are high-performance CMOS static random- access memories. Organized as 4096 words of 4 bits, the device operation is from a single +5-volt supply and all input/output levels are TTL compatible.

Both devices enter the standby power mode when $\overline{CE}$ is taken HIGH. They go into a full standby mode when, in addition to $\overline{CE}$ being HIGH, V_{IN} is either greater than (V_{CC} −0.2 V) or less than 0.2 V. In the full standby power mode, the Am99C68 draws 2 mA and the Am99CL68 draws only 50 μA.

Both devices have a data retention mode which allows them to maintain memory when V_{CC} is as low as 2.0 V.

Data readout is not destructive and has the same polarity as data input.

BLOCK DIAGRAM



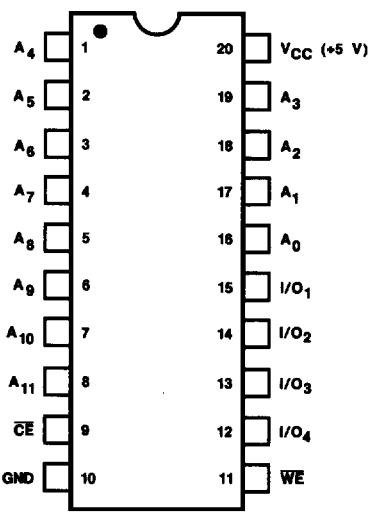
BD006040

PRODUCT SELECTOR GUIDE

Family Part Number		Am99C68/Am99CL68							
Ordering Part Number		99C68-35	99CL68-35	99C68-45	99CL68-45	99C68-55	99CL68-55	99C68-70	99CL68-70
Maximum Access Time (ns)		TBD*		45		55		70	
I_{CC} Max. (mA)	C Devices	TBD		100		100		100	
	M Devices	TBD		120		120		120	
I_{SB} Max. (mA)		TBD		20		20		20	
I_{SBI} Max. (μA)		TBD	TBD	2000	50	2000	50	2000	50
I_{CCDR} Max. (μA)		TBD	TBD	1600	40	1600	40	1600	40

*TBD = To Be Determined.

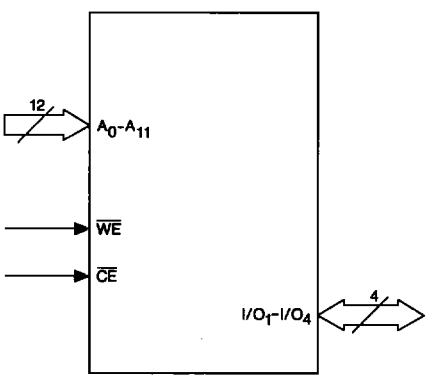
CONNECTION DIAGRAM
Top View



CD009350

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002320

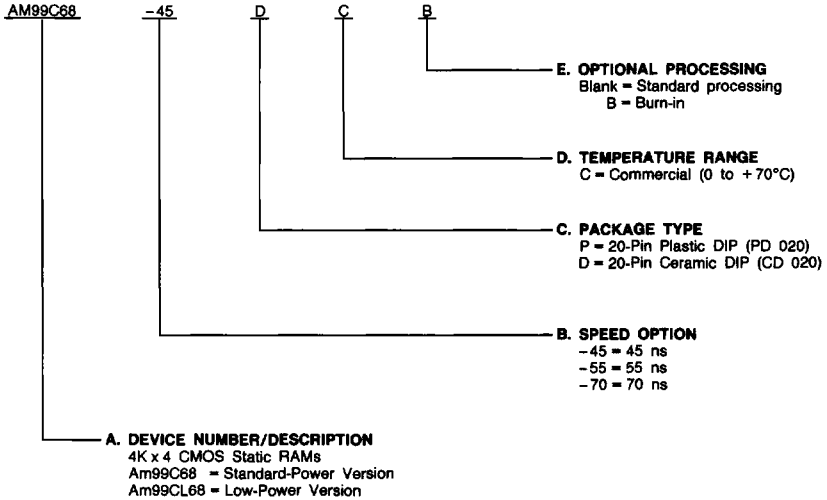
V_{CC} = +5-V Power Supply
GND = Ground

ORDERING INFORMATION (Cont'd.)

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

A. Device Number
B. Speed Option (if applicable)
C. Package Type
D. Temperature Range
E. Optional Processing



Valid Combinations	
AM99C68-45	DC, DCB, PC, PCB
AM99CL68-45	
AM99C68-55	
AM99CL68-55	
AM99C68-70	
AM99CL68-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

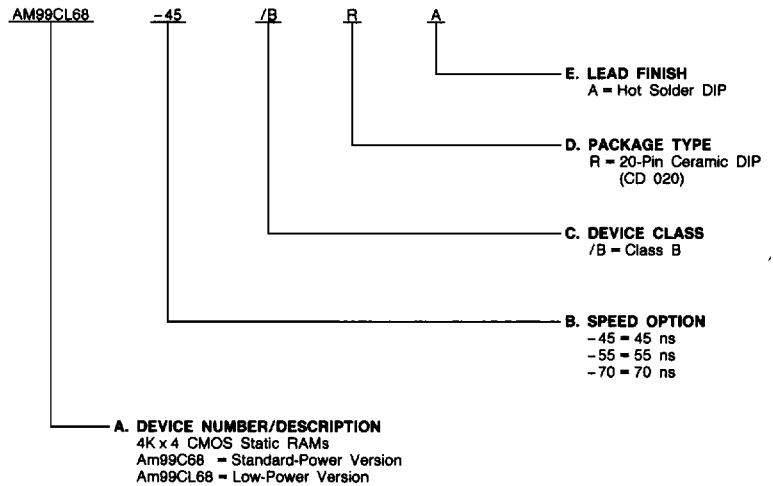
4

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. CPL (Controlled Products List) products are processed in accordance with MIL-STD-883C, but are inherently non-compliant because of package, solderability, or surface treatment exceptions to those specifications. The order number (Valid Combination) for APL products is formed by a combination of: **A. Device Number**

B. Speed Option (if applicable)
C. Device Class
D. Package Type
E. Lead Finish



Valid Combinations	
AM99C68-45	/BRA
AM99CL68-45	
AM99C68-55	
AM99CL68-55	
AM99C68-70	
AM99CL68-70	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

PIN DESCRIPTION

$A_0 - A_{11}$ Address Line (Inputs)
These inputs select the desired location (memory cell) that data is read from or written to.

$\overline{WE}$ Write Enable (Input, Active LOW)
This input enables data to be written into the memory location selected by the address when $\overline{CE}$ is active.

$\overline{CE}$ Chip Enable (Input, Active LOW)
$\overline{CE}$ acts as a general enable for the part. When $\overline{CE}$ is active LOW and $\overline{WE}$ is HIGH, data will be read. When $\overline{CE}$ is active HIGH and $\overline{WE}$ is LOW, data will be written.

$I/O_1 - I/O_4$ Data In/Out Bus (Bidirectional, active HIGH)
These I/O lines provide the path for data to be read from or written to the selected memory cell.

V_{CC} +5-Volt Power Supply

GND 0-Volt Ground

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
- Ceramic DIPs ..... −65 to +150°C
- Plastic DIPs ..... −55 to +150°C

Ambient Temperature with Power Applied
- Ceramic DIPs ..... −55 to +125°C
- Plastic DIPs ..... −10 to +85°C

Supply Voltage with Respect to Ground ..... −0.5 to +7.0 V

All Signal Voltages with Respect to Ground ..... −0.5 to +7.0 V

DC Output Short-Circuit Current, into Outputs (Note 1) ..... 25 mA

Notes: 1. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
- Temperature (T_A) ..... 0 to +70°C
- Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military (M) Devices
- Temperature (T_A) ..... −55 to +125°C
- Supply Voltage (V_{CC}) ..... +4.50 to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (Note 4)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
I_{OH}	Output HIGH Current	V_{OH} = 2.4 V, V_{CC} = 4.5 V		−4.0		mA
I_{OL}	Output LOW Current	V_{OL} = 0.4 V	C Devices	8.0		mA
			M Devices	8.0		
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{IL}	Input LOW Voltage	(Note 3)		−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−5.0	5.0	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−5.0	5.0	μA
I_{CC}	V_{CC} Operating Supply Current	Max. V_{CC}, $\overline{CE}$ ≤ V_{IL} Output Open, Max. Frequency	C Devices		100.0	mA
			M Devices		120.0	
I_{SB}	Automatic Power-Down Current	Max. V_{CC}, ($\overline{CE}$ ≥ V_{IH})			20.0	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ (V_{CC} −0.2 V) or ≤ 0.2 V	Am99C68		2,000	μA
			Am99CL68		50.0	

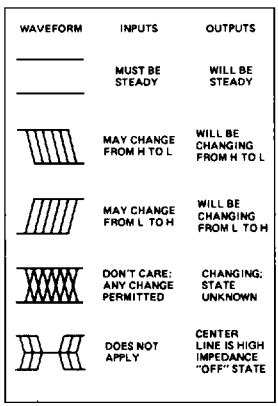
CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_I	Input Capacitance	Test Frequency = 1.0 MHz, T_A = 25°C, All pins at 0 V, V_{CC} = 5 V (Note 7)		6.0	pF
$C_{I/O}$	Input/Output Capacitance			7.0	

Notes*: 1. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance. Output timing reference is 1.5 V.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
3. V_{IL} voltages of less than −0.5 V on the I/O pins will cause the output current to exceed the maximun rating. −0.1-V and −3.0-V pulses can be tolerated for up to 50 ns and 10 ns respectively.
4. For test and correlation purposes, ambient temperature is defined as the stabilized case temperature.
5. At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} and t_{WZ} is less than t_{OW} for all devices. Transition is measured from the inputs at 1.5 V to the outputs at 1.0 V, and 0.9 V using the load shown in Test Circuit B (see Switching Test Circuits). C_L = 5 pF.
6. The minimum limit is not tested and is included as user-guidelines only.
7. These parameters are not tested, but are guaranteed by characterization.

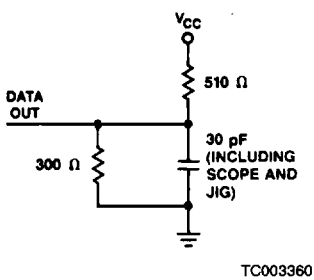
*Notes listed also correspond to references made in Switching Characteristics table.

KEY TO SWITCHING WAVEFORMS



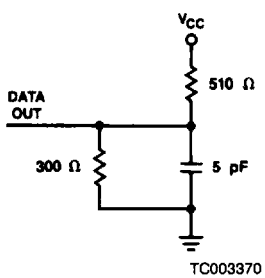
KS000010

SWITCHING TEST CIRCUITS



TC003360

A. Output Load

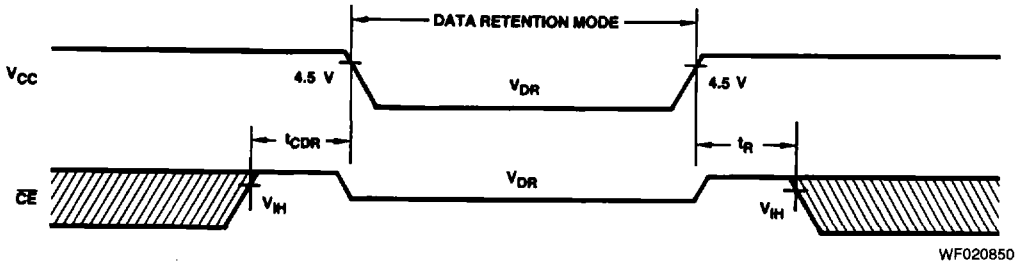


TC003370

B. Output Load for t_{HZ}, t_{LZ}, t_{OW}, t_{WZ}

Data Retention Characteristics

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2$ V	Am99C68		1600	µA
			Am99CL68		40	
t_{CDR}	Chip Deselect to Data Retention Time (Note 1)	$V_{IN} \geq (V_{CC} - 0.2\ V)$ or ≤ 0.2 V		0		ns
t_R	Operation Recovery Time (Note 1)			t_{RC}		ns



Data Retention Waveform (Note 2)

Notes: 1. Parameter is not tested, but is guaranteed by design.
2. Waveforms shown are not actual and may vary in use.

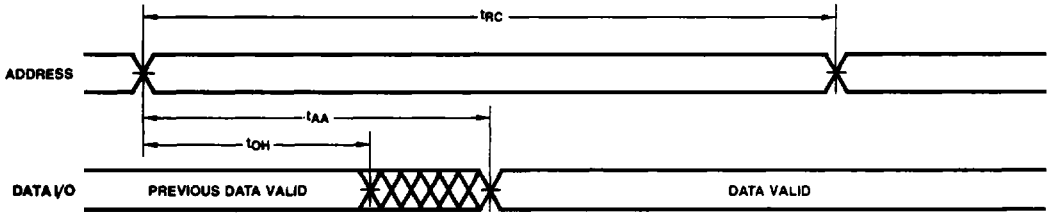
4

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 1)

Parameter No.	Parameter Symbol	Parameter Description	Am99C68-35 Am99CL68-35		Am99C68-45 Am99CL68-45		Am99C68-55 Am99CL68-55		Am99C68-70 Am99CL68-70		Units
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE											
1	t_{RC}	Address Valid to Address Do Not Care Time (Read Cycle Time)	TBD*		45		55		70		ns
2	t_{AA}	Address Valid to Data-Out Valid Delay (Address Access Time)		TBD		45		55		70	ns
3	t_{ACS}	Chip Enable LOW to Data-Out Valid (Chip Enable Access Time)		TBD		45		55		70	ns
4	t_{LZ}	Chip Enable LOW to Data-Out On (Note 5)	TBD		5		5		5		ns
5	t_{HZ}	Chip Enable HIGH to Data-Out Off (Notes 5 & 6)		TBD	0	20	0	25	0	30	ns
6	t_{OH}	Address Unknown to Data-Out Unknown Time	TBD		5		5		5		ns
7	t_{PD}	Chip Enable HIGH to Power-Down Delay (Note 7)		TBD		45		55		70	ns
8	t_{PU}	Chip Enable LOW to Power-On Delay (Note 7)	TBD		0		0		0		ns
WRITE CYCLE											
9	t_{WC}	Address Valid to Address Do Not Care (Write Cycle Time)	TBD		40		50		60		ns
10	t_{WP}	Write Enable LOW to Write Enable HIGH (Note 2)	TBD		35		45		60		ns
11	t_{WR}	Write Enable HIGH to Address Do Not Care			0		0		0		ns
12	t_{WZ}	Write Enable LOW to Output in High Z (Notes 5 & 6)		TBD	0	20	0	25	0	30	ns
13	t_{DW}	Data In Valid to Write Enable HIGH	TBD		15		20		30		ns
14	t_{DH}	Data Hold Time	TBD		3		3		3		ns
15	t_{AS}	Address Valid to Write Enable LOW			0		0		0		ns
16	t_{CW}	Chip Enable LOW to Write Enable HIGH (Note 2)	TBD		35		45		60		ns
17	t_{OW}	Write Enable HIGH to Output In Low Z (Note 5)	TBD		5		5		5		ns
18	t_{AW}	Address Valid to End of Write	TBD		35		45		60		ns

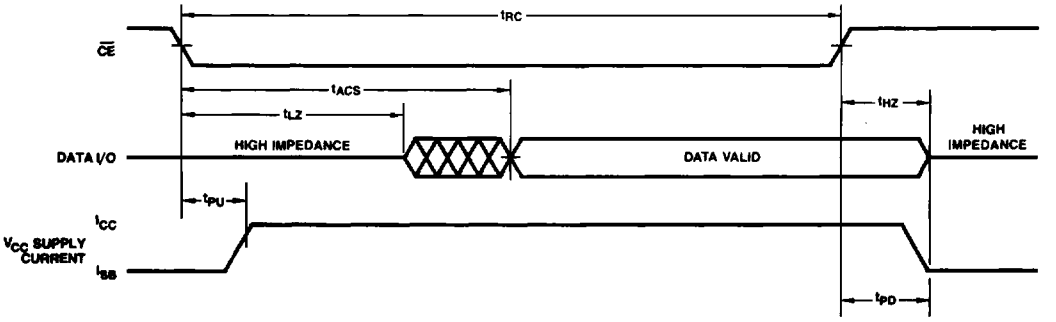
Notes: See notes following DC Characteristics table.
*TBD = To Be Determined.

SWITCHING WAVEFORMS (Cont'd.)



WF020860

Read Cycle No. 1 — $\overline{WE}$ HIGH, $\overline{CE}$ LOW

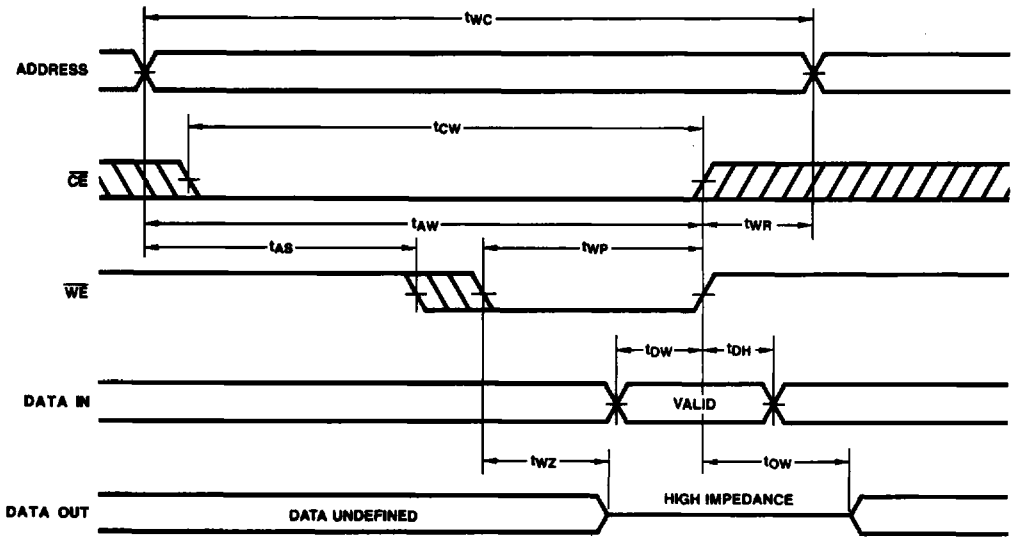


WF020870

Read Cycle No. 2 — $\overline{WE}$ HIGH, Address Valid Prior to $\overline{CE}$ Transition to LOW

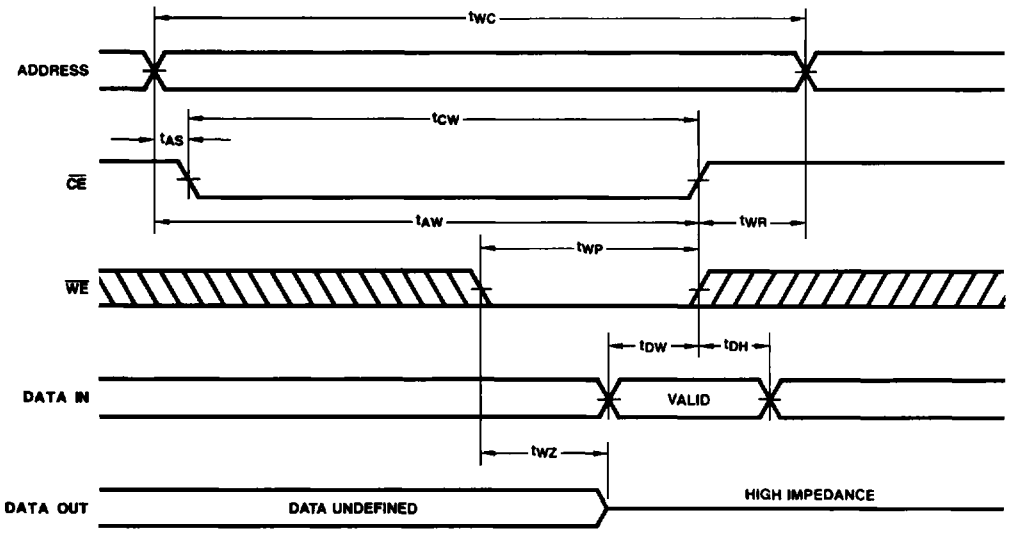
4

SWITCHING WAVEFORMS



WF020881

Write Cycle No. 1 — $\overline{WE}$ Controlled, $\overline{CE}$ Active Prior to $\overline{WE}$



WF020891

Write Cycle No. 2 — $\overline{CE}$ Controlled

Note: If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.