256Kx32 SRAM MODULE *ADVANCED**

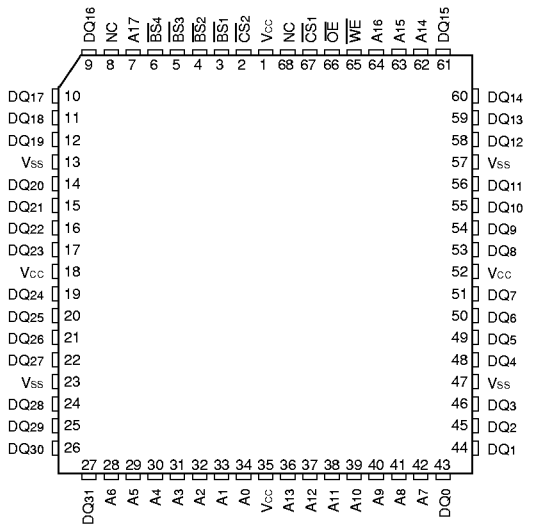
FEATURES

- Access Times
  - BiCMOS: 12, 15ns
  - CMOS: 17, 20, 25ns
- Packaging
  - 68 Lead, Plastic PLCC, 25.15mm (0.990 inch) square (Package 706)
- Organized as 256Kx32, User Configurable as 512Kx16
- Upgradeable to 512Kx32 for Future Expansion
- Individual Byte Selects
- Commercial and Industrial Temperature Ranges
- TTL Compatible Inputs and CMOS Outputs
- I/O Compatible with 3.3V Devices
- 5 Volt Power Supply
- Low Power
- Multiple Ground Pins for Low Noise Operation

* *This data sheet describes a product that may or may not be under development, and is subject to change or cancellation without notice.*

FIG. 1 PIN CONFIGURATION FOR WPS256K32-XPJX

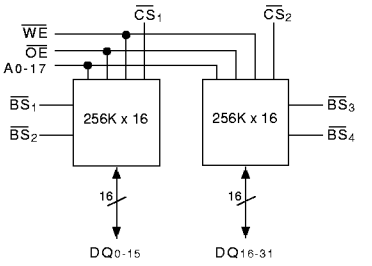
TOP VIEW



PIN DESCRIPTION

DQ0-31	Data Inputs/Outputs
A0-17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}_{1-2}$	Chip Selects
$\overline{OE}$	Output Enable
$\overline{BS}_1$-$\overline{BS}_4$	Byte Selects
Vcc	Power Supply
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature (Com.)	T_A	0	+70	°C
Operating Temperature (Ind.)	T_A	-40	+85	°C
Storage Temperature	T_{STG}	-55	+125	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc + 0.5	V
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

$\overline{CS}_{1-2}$	$\overline{OE}$	$\overline{WE}$	$\overline{BS}_{1-4}$	Mode	Data I/O	Power
H	X	X	X	Standby	High Z	Standby
L	H	H	X	Out Disable	High Z	Active
L	X	X	H	Out Disable	High Z	Active
L	L	H	L	Read	Data Out	Active
L	X	L	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Com.)	T_A	0	+70	°C
Operating Temp (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(@ T_A = +25°C)

Parameter	Symbol	Condition	Max	Unit
$\overline{OE}$ Capacitance	C_{OE}	V_{IN} = 0V, f = 1.0MHz	20	pF
$\overline{WE}$ Capacitance	C_{WE}	V_{IN} = 0V, f = 1.0MHz	20	pF
$\overline{CS}$ Capacitance	C_{CS}	V_{IN} = 0V, f = 1.0MHz	12	pF
DQ Capacitance	$C_{I/O}$	V_{IN} = 0V, f = 1.0MHz	12	pF
Address Input Capacitance	C_{AD}	V_{IN} = 0V, f = 1.0MHz	20	pF
Byte Select Capacitance	C_{BS}	V_{IN} = 0V, f = 1.0MHz	12	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC}= 5V, V_{SS} = 0V, T_A = -40 to +85°C)

Parameter	Symbol	Conditions	12 & 15		17, 20, 25		Units
			Min	Max	Min	Max	
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vss to Vcc		10		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = Vss to Vcc		10		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		540		520	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, Vcc = 5.5		50		34	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA, Vcc = 4.5		0.4		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA, Vcc = 4.5	2.4		2.4		V

NOTE: DC test conditions: V_{IH} = Vcc -0.3V, V_{IL} = 0.3V

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	-12		-15		-17		-20		-25		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	12		15		17		20		25		ns
Address Access Time	t_{AA}		12		15		17		20		25	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		12		15		17		20		25	ns
Output Enable to Output Valid	t_{OE}		8		10		10		12		15	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		7		9		9		10		12	ns
Output Disable to Output in High Z	t_{OHZ}[1]		7		9		9		10		12	ns
Byte Select Access Time	t_{BA}		8		10		10		12		14	ns
Byte Select Enable to Low Z Output	t_{BLZ}[1]	0		0		0		0		0		ns
Byte Select Disable to High Z Output	t_{BHZ}[1]		7		9		9		10		12	ns

1. This parameter is guaranteed by design but not tested.

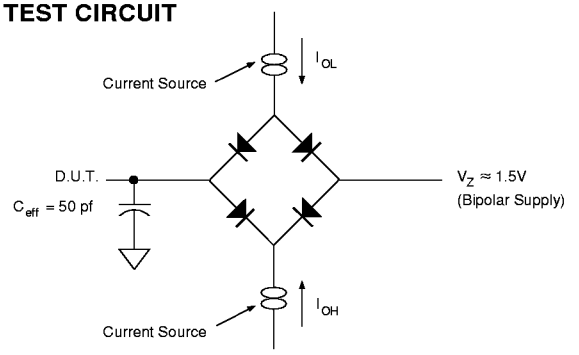
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -40°C to +85°C)

Parameter	Symbol	-12		-15		-17		-20		-25		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	12		15		17		20		25		ns
Chip Select to End of Write	t_{CW}	10		12		14		17		20		ns
Address Valid to End of Write	t_{AW}	10		12		14		17		20		ns
Data Valid to End of Write	t_{DW}	8		10		10		12		15		ns
Write Pulse Width	t_{WP}	10		12		14		17		20		ns
Address Setup Time	t_{AS}	0		0		0		0		0		ns
Address Hold Time	t_{AH}	0		0		2		2		2		ns
Output Active from End of Write	t_{OW}[1]	0		0		0		0		0		ns
Write Enable to Output in High Z	t_{WHZ}[1]		7		8		9		10		10	ns
Data Hold Time	t_{DH}	0		0		0		0		0		ns
Byte Select Valid to End of Write	t_{BW}	10		12		14		17		20		ns

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT

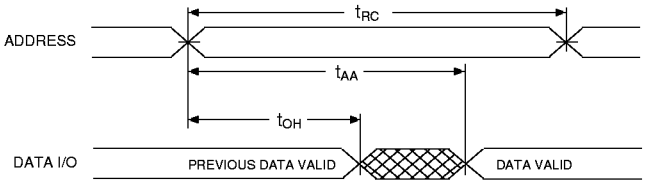


AC TEST CONDITIONS

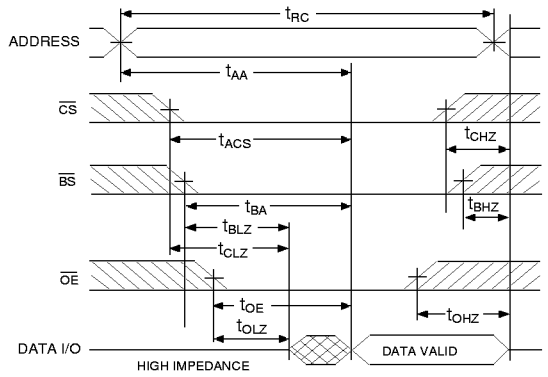
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

TIMING WAVEFORM - READ CYCLE

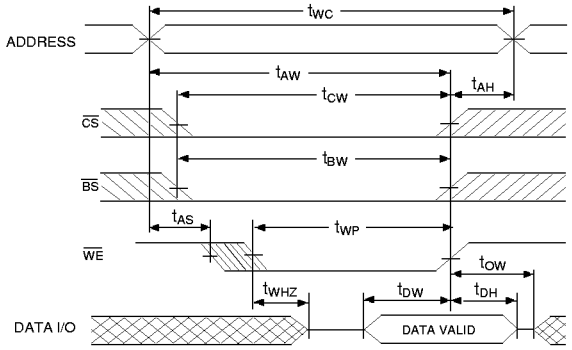


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{BS}$ = V_{IL}, $\overline{WE}$ = V_{IH})



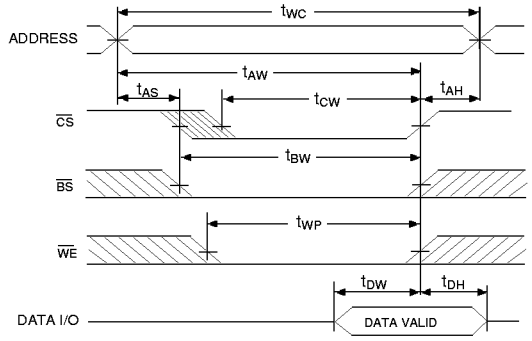
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

WRITE CYCLE - $\overline{WE}$ CONTROLLED



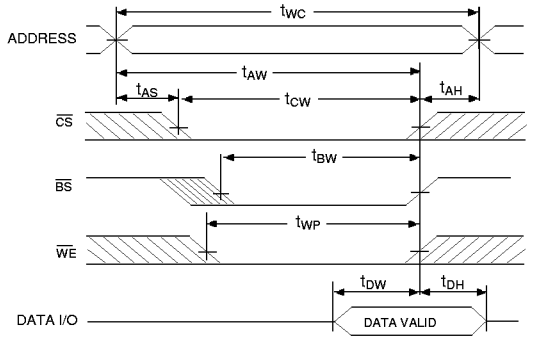
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

WRITE CYCLE - $\overline{CS}$ CONTROLLED



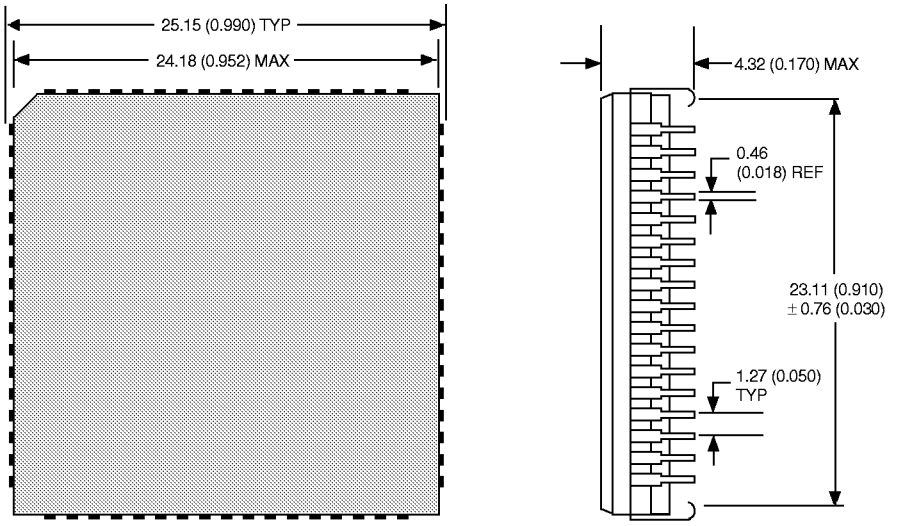
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

WRITE CYCLE - $\overline{BS}$ CONTROLLED



WRITE CYCLE 3, $\overline{BS}$ CONTROLLED

PACKAGE 706: 68 LEAD PLCC



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P S 256K 32 X - XX PJ X

DEVICE GRADE:
C = Commercial 0°C to +70°C
I = Industrial -40°C to +85°C

PACKAGE TYPE:
PJ = 68 Lead Plastic PLCC (Package 706)

ACCESS TIME (ns)

IMPROVEMENT MARK:
B = BiCMOS
Blank = CMOS

ORGANIZATION, 256K x 32

SRAM

Plastic Encapsulated Multichip Module

WHITE MICROELECTRONICS