

Preliminary W26L04A



256K × 16 HIGH-SPEED CMOS STATIC RAM

GENERAL DESCRIPTION

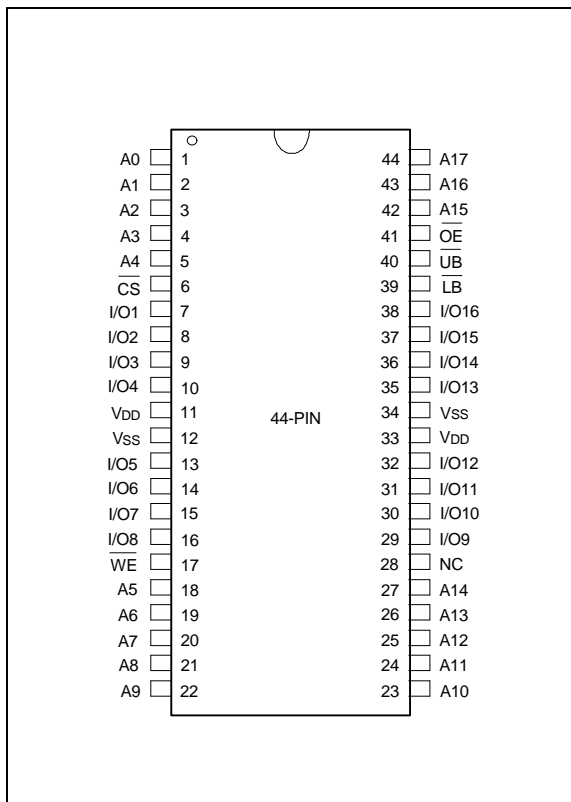
The W26L04A is a high-speed, low-power CMOS static RAM organized as 262,144 × 16 bits that operates on a single 3.3-volt power supply.

The W26L04A has an active low chip select, separate upper and lower byte selects, and a fast output enable. No clock or refreshing is required. Separate byte select controls ($\overline{\text{LB}}$ and $\overline{\text{UB}}$) allow individual bytes to be written and read. $\overline{\text{LB}}$ controls I/O1-I/O8, the lower byte. $\overline{\text{UB}}$ controls I/O9-I/O16, the upper byte. This device is well suited for use in high-density, high-speed system applications.

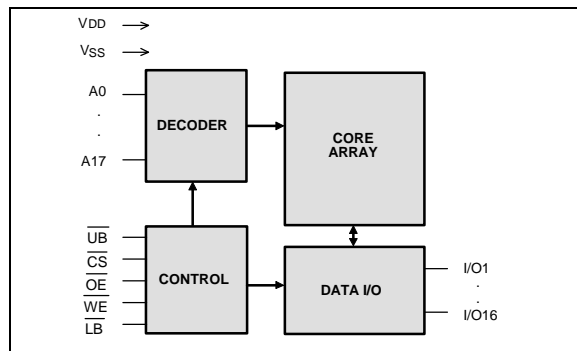
FEATURES

- High speed access time: 10/12 nS (max.)
- Low power consumption:
 - Active: 660 mW (max.)
- Single +3.3V power supply
- Fully static operation
 - No clock or refreshing
- Industrial operating temperature grade available
- All inputs and outputs directly TTL compatible
- Three-state outputs
- Data byte control
 - $\overline{\text{LB}}$ (I/O1-I/O8), $\overline{\text{UB}}$ (I/O9-I/O16)
- Available packages: 44-pin 400 mil SOJ and 44-pin TSOP(II)

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0-A17	Address Inputs
I/O1-I/O16	Data Inputs/Outputs
$\overline{\text{CS}}$	Chip Select Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$	Lower Byte Select I/O1-I/O8
$\overline{\text{UB}}$	Upper Byte Select I/O9-I/O16
VDD	Power Supply
VSS	Ground
NC	No Connection

Preliminary W26L04A



TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	$\overline{\text{LB}}$	$\overline{\text{UB}}$	MODE	I/O1- I/O8	I/O9- I/O16	V _{DD} CURRENT
H	X	X	X	X	Not Selected	High Z	High Z	ISB, ISB1
L	H	H	X	X	Output Disable	High Z	High Z	IDD
L	L	H	L	L	2 Bytes Read	DOUT	DOUT	IDD
L	L	H	L	H	Lower Byte Read	DOUT	High Z	IDD
L	L	H	H	L	Upper Byte Read	High Z	DOUT	IDD
L	X	L	L	L	2 Bytes Write	DIN	DIN	IDD
L	X	L	L	H	Lower Byte Write	DIN	High Z	IDD
L	X	L	H	L	Upper Byte Write	High Z	DIN	IDD
L	X	X	H	H	Output Disable	High Z	High Z	IDD

DC CHARACTERISTICS

Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Supply Voltage to V _{SS} Potential	-0.5 to +4.6	V
Input/Output to V _{SS} Potential	-0.5 to V _{DD} +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to +150	°C
Operating Temperature	Commercial	0 to +70
	Industrial	-40 to +85

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

Operating Characteristics

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = -40 to 85° C for Industrial Grade, T_A = 0 to 70° C for Commercial Grade)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Low Voltage	V _{IL}	-	-0.5	-	+0.8	V
Input High Voltage	V _{IH}	-	+2.0	-	V _{DD} +0.3	V
Input Leakage Current	I _{LI}	V _{IN} = V _{SS} to V _{DD}	-10	-	+10	μA
Output Leakage Current	I _{LO}	V _{I/O} = V _{SS} to V _{DD} Output Pins in High Z, See Truth Table	-10	-	+10	μA
Output Low Voltage	V _{OL}	I _{OL} = +8.0 mA	-	-	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA	2.4	-	-	V

Preliminary W26L04A



Operating Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT		
Operating Power	IDD	$\overline{CS} = V_{IL} (\text{max.}),$ Cycle = min.	10 nS	Commercial	-	-	200	mA
				Industrial			260	
Supply Current		I/O = Open, Duty = 100%	12 nS	Commercial	-	-	190	mA
				Industrial			250	
Standby Power	ISB	$\overline{CS} = V_{IH} (\text{min.}),$ Cycle = min.	-	-	30	mA		
Supply Current	ISB1	$\overline{CS} = V_{DD} - 0.2V,$ I/O = open All other pins = $V_{DD} - 0.2V/GND$	-	-	10	mA		

Note: Typical characteristics are evaluated at $V_{DD} = 3.3V,$ $T_A = 25^\circ C.$

CAPACITANCE

($V_{DD} = 3.3V,$ $T_A = 25^\circ C,$ $f = 1 \text{ MHz}$)

PARAMETER	SYM.	CONDITIONS	MAX.	UNIT
Input Capacitance	CIN	$V_{IN} = 0V$	6	pF
Input/Output Capacitance	C _{I/O}	$V_{OUT} = 0V$	8	pF

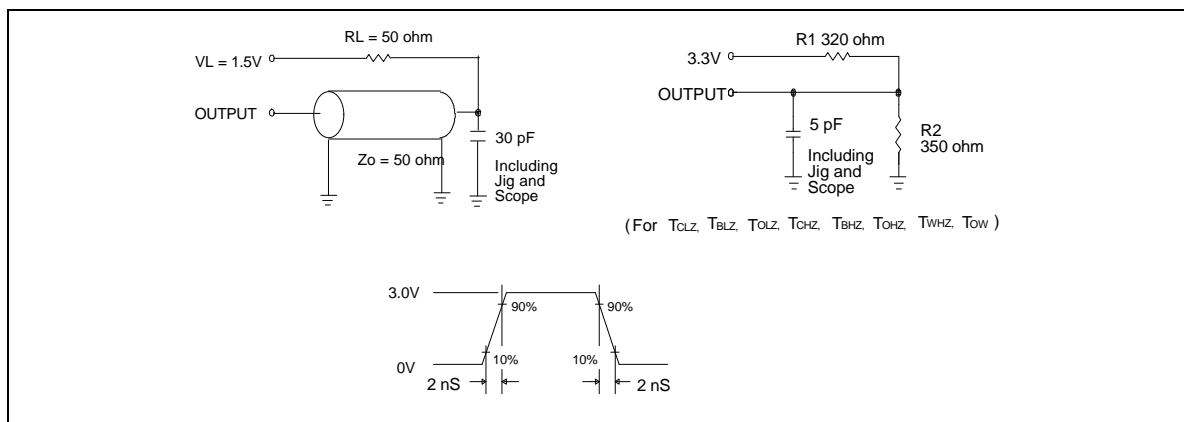
Note: These parameters are sampled but not 100% tested.

AC CHARACTERISTICS

AC Test Conditions

PARAMETER	CONDITIONS
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	2 nS
Input and Output Timing Reference Level	1.5V
Output Load	$CL = 30 \text{ pF},$ $I_{OH}/I_{OL} = -4 \text{ mA}/8 \text{ mA}$

AC Test Loads and Waveform



Publication Release Date: October 1999

Preliminary W26L04A



AC Characteristics, continued

(V_{DD} = 3.3V ±5%, V_{SS} = 0V, T_A = -40 to +85° C for Industrial Grade, T_A = 0 to 70° C for Commercial Grade)

Read Cycle

PARAMETER	SYM.	W26L04A-10		W26L04A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	TRC	10	-	12	-	nS
Address Access Time	TAA	-	10	-	12	nS
Chip Select Access Time	TACS	-	10	-	12	nS
Output Enable to Output Valid	TOE	-	5	-	6	nS
\overline{UB} , \overline{LB} Access Time	TBA	-	5	-	6	nS
Output Hold from Address Change	TOH	3	-	3	-	nS
Chip Select to Output in Low Z	TCLZ*	3	-	3	-	nS
Chip Deselect to Output in High Z	TCHZ*	-	5	-	6	nS
Output Enable to Output in Low Z	TOLZ*	0	-	0	-	nS
Output Disable to Output in High Z	TOHZ*	-	5	-	6	nS
\overline{UB} , \overline{LB} Select to Output in Low Z	TBLZ*	0	-	0	-	nS
\overline{UB} , \overline{LB} Deselect to Output in High Z	TBHZ*	-	5	-	6	nS

* These parameters are sampled but not 100% tested.

Write Cycle

PARAMETER	SYM.	W26L04A-10		W26L04A-12		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	TWC	10	-	12	-	nS
Chip Select to End of Write	TCW	9	-	10	-	nS
Address Valid to End of Write	TAW	9	-	10	-	nS
Address Setup Time	TAS	0	-	0	-	nS
\overline{UB} , \overline{LB} Select to End of Write	TBW	9	-	10	-	nS
Write Pulse Width	TWP	9	-	10	-	nS
Write Recovery Time	\overline{CS} , \overline{WE} TWR	0	-	0	-	nS
Data Valid to End of Write	TDW	6	-	7	-	nS
Data Hold from End of Write	TDH	0	-	0	-	nS
Write to Output in High Z	TWHZ*	-	6	-	7	nS
End of Write to Output Active	TOW*	3	-	3	-	nS

* These parameters are sampled but not 100% tested.

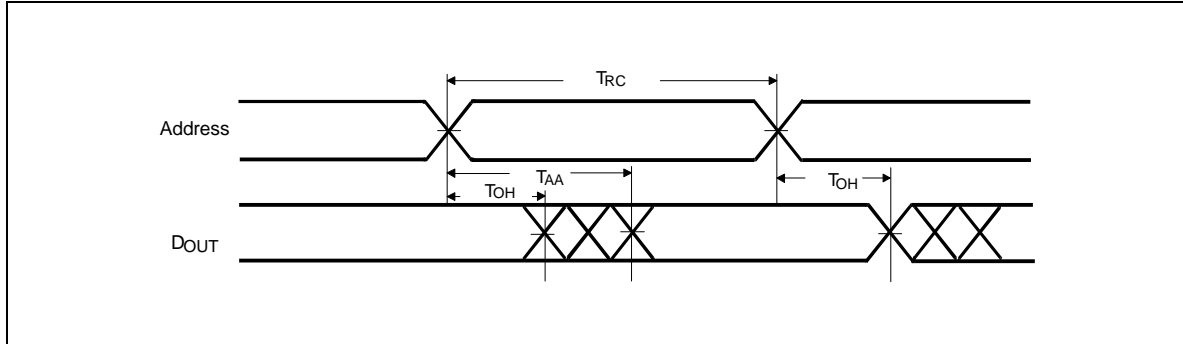
Preliminary W26L04A



TIMING WAVEFORMS

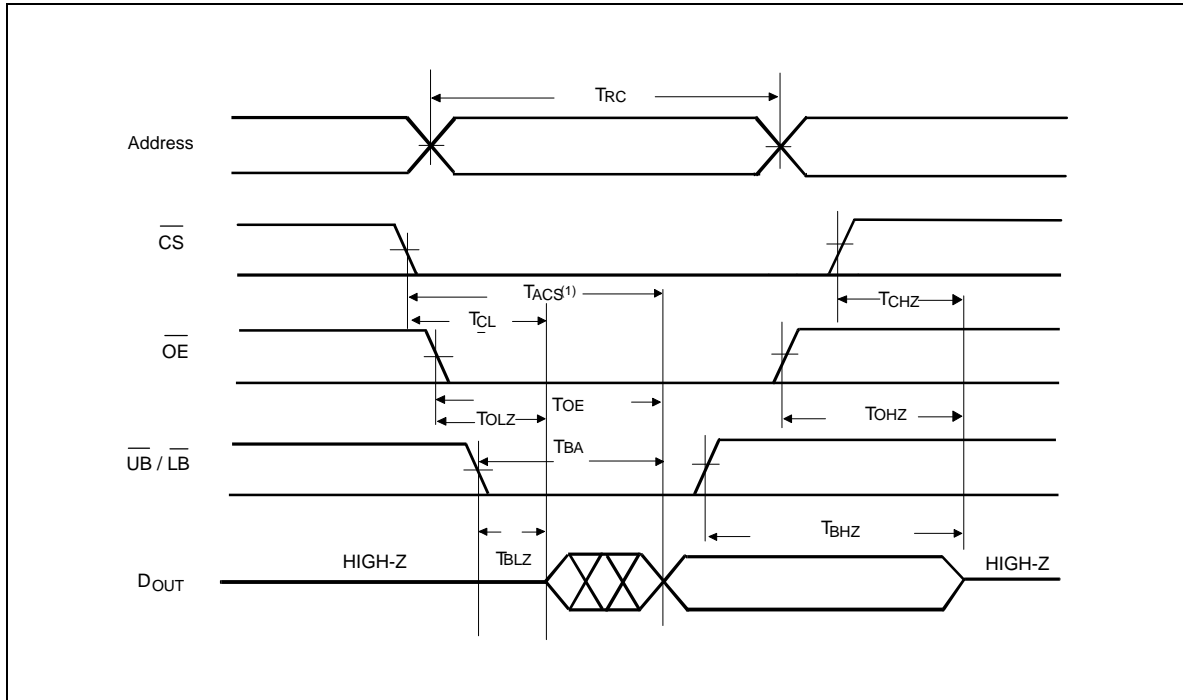
Read Cycle 1

(Address Controlled, $\overline{CS} = \overline{OE} = \overline{UB} = \overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)



Read Cycle 2

(Chip Select Controlled, $\overline{WE} = V_{IH}$)



Note (1) : Address valid prior to or coincident with \overline{CS} transition low.

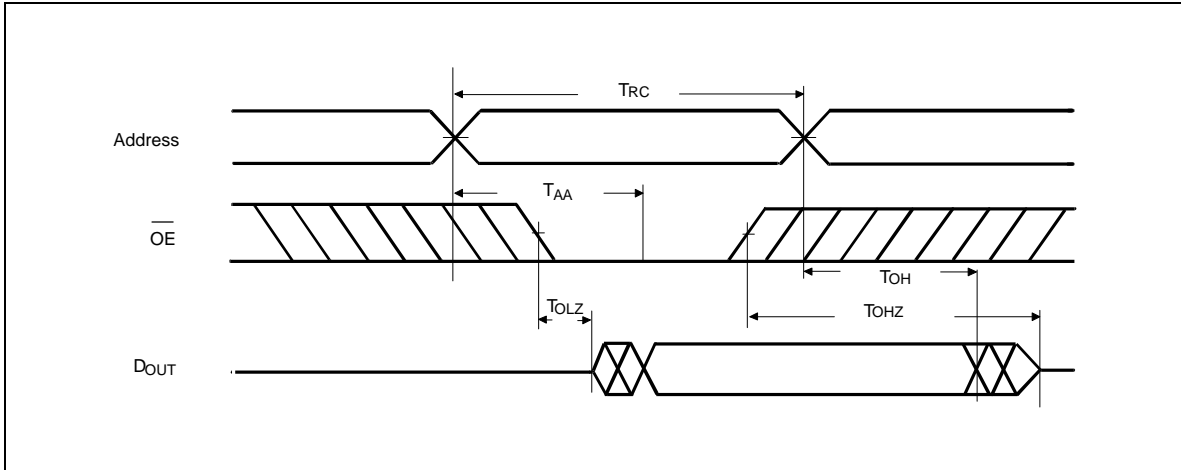
Preliminary W26L04A



Timing Waveforms, continued

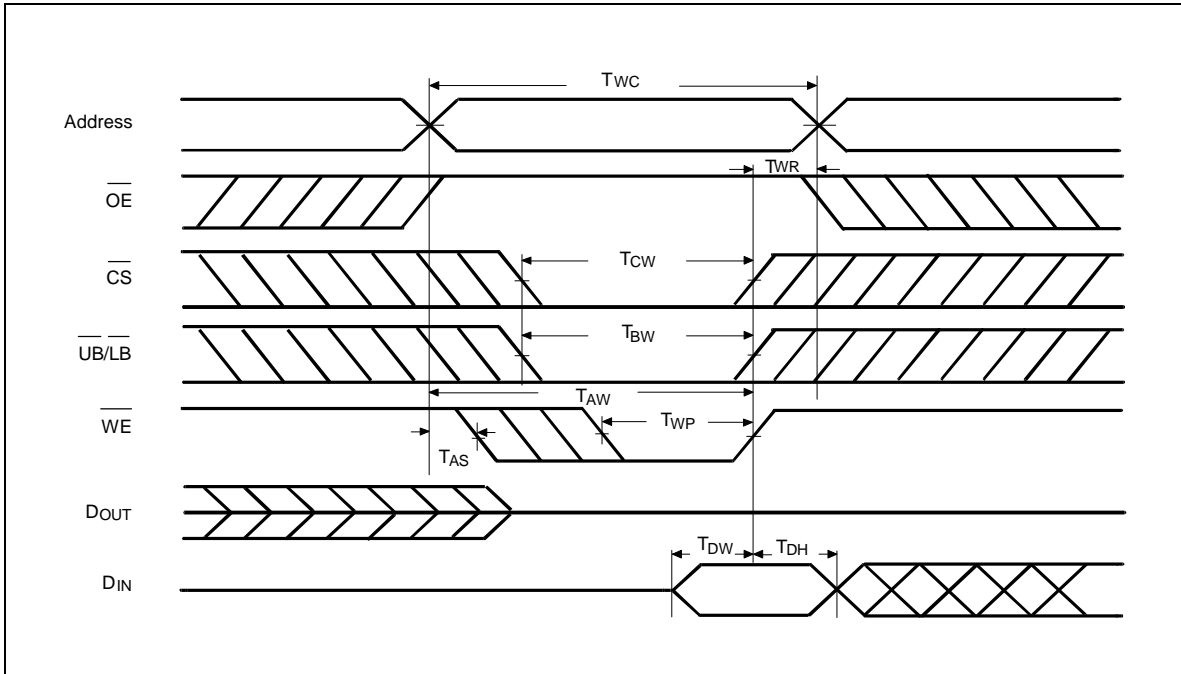
Read Cycle 3

(Output Enable Controlled, $\overline{CS} = \overline{UB} = \overline{LB} = V_{IL}$, $\overline{WE} = V_{IH}$)



Write Cycle 1

(OE Clock)



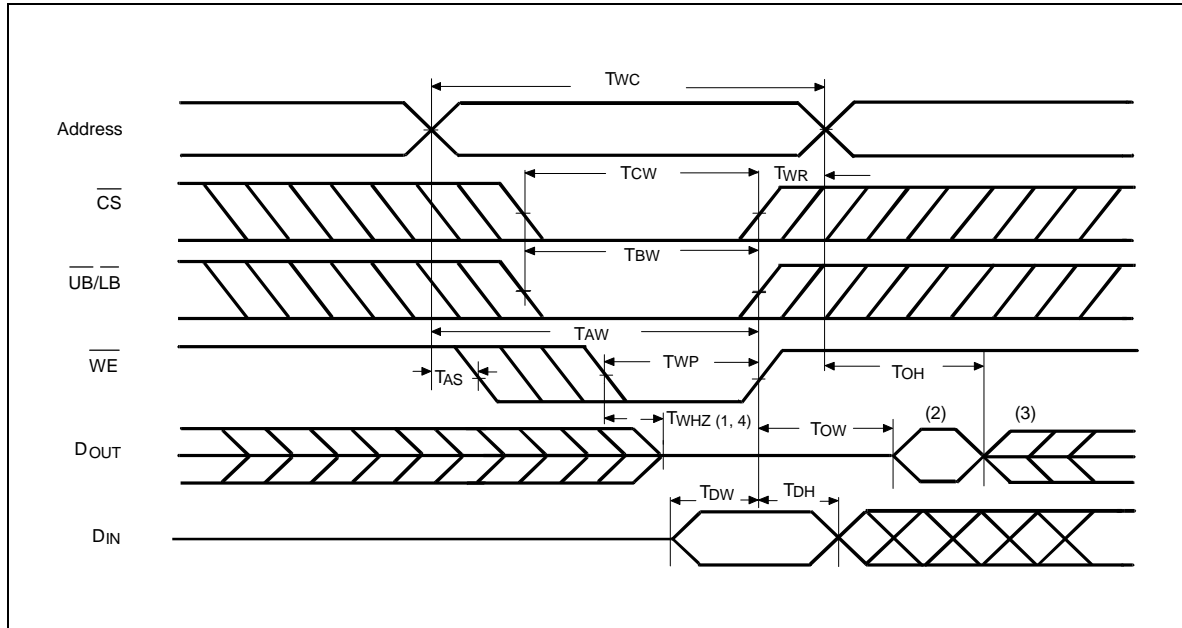
Preliminary W26L04A



Timing Waveforms, continued

Write Cycle 2

($\overline{OE} = V_{IL}$ Fixed)



Notes:

1. During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.
2. The data output from DOUT are the same as the data written to DIN during the write cycle.
3. DOUT provides the read data for the next address.
4. Transition is measured ± 500 mV from steady state with $C_L = 5$ pF. This parameter is guaranteed but not 100% tested.

Preliminary W26L04A



ORDERING INFORMATION

Commercial: 0° C to +70° C

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W26L04AJ-10	10	200	10	44-pin 400 mil SOJ
W26L04AJ-12	12	190	10	44-pin 400 mil SOJ
W26L04AH-10	10	200	10	44-pin TSOP(II)
W26L04AH-12	12	190	10	44-pin TSOP(II)

Industrial: -40° C to +85° C

PART NO.	ACCESS TIME (nS)	OPERATING CURRENT MAX. (mA)	STANDBY CURRENT MAX. (mA)	PACKAGE
W26L04AJ-10I	10	260	10	44-pin 400 mil SOJ
W26L04AJ-12I	12	250	10	44-pin 400 mil SOJ
W26L04AH-10I	10	260	10	44-pin TSOP(II)
W26L04AH-12I	12	250	10	44-pin TSOP(II)

Notes:

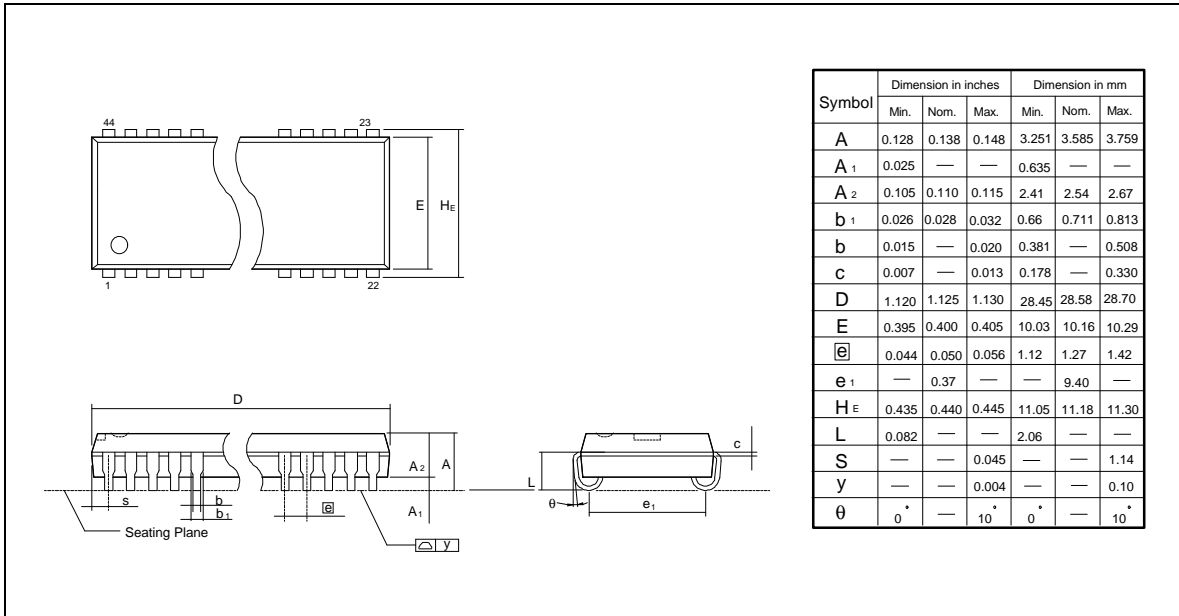
1. Winbond reserves the right to make changes to its products without prior notice.
2. Purchasers are responsible for performing appropriate quality assurance testing on products intended for use in applications where personal injury might occur as a consequence of product failure.

Preliminary W26L04A

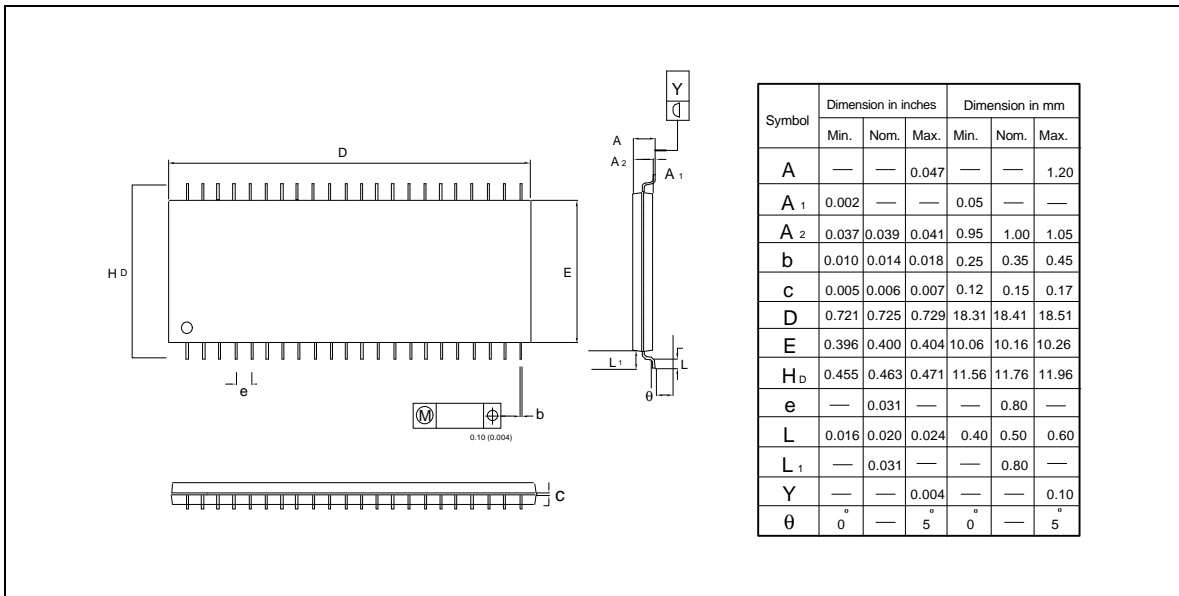


PACKAGE DIMENSIONS

44-pin Small Outline J Band



44-pin Standard Type Two TSOP



Preliminary W26L04A



VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Oct. 1999	-	Initial Issued



Headquarters

No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5796096
<http://www.winbond.com.tw/>
Voice & Fax-on-demand: 886-2-27197006

Taipei Office

11F, No. 115, Sec. 3, Min-Sheng East Rd.,
Taipei, Taiwan
TEL: 886-2-27190505
FAX: 886-2-27197502

Winbond Electronics (H.K.) Ltd.

Rm. 803, World Trade Square, Tower II,
123 Hoi Bun Rd., Kwun Tong,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Winbond Electronics North America Corp.

Winbond Memory Lab.
Winbond Microelectronics Corp.
Winbond Systems Lab.

2727 N. First Street, San Jose,
CA 95134, U.S.A.
TEL: 408-9436666
FAX: 408-5441798

Note: All data and specifications are subject to change without notice.