uPSD34xx

Turbo Plus Series

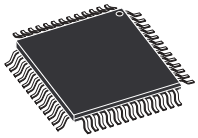
Fast Turbo 8032 MCU with USB and Programmable Logic

DATA BRIEFING

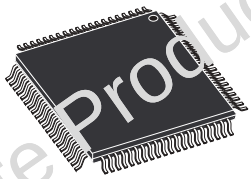
FEATURES SUMMARY

- FAST 8-BIT TURBO 8032 MCU, 40MHz
  - Advanced core, 4-clocks per instruction
  - 10 MIPs peak performance at 40MHz (5V)
  - JTAG Debug and In-System Programming
  - 16-bit internal instruction path fetches double-byte instruction in a single memory cycle
  - Branch Cache & 4 instruction Prefetch Queue
  - Dual XDATA pointers with automatic increment and decrement
  - Compatible with 3rd party 8051 tools
- DUAL FLASH MEMORIES WITH MEMORY MANAGEMENT
  - Place either memory into 8032 program address space or data address space
  - READ-while-WRITE operation for In-Application Programming and EEPROM emulation
  - Single voltage program and erase
  - 100K guaranteed erase cycles, 15-year retention
- CLOCK, RESET, AND POWER SUPPLY MANAGEMENT
  - SRAM is Battery Backup capable
  - Flexible 8-level CPU clock divider register
  - Normal, Idle, and Power Down Modes
  - Power-on and Low Voltage reset supervisor
  - Programmable Watchdog Timer
- PROGRAMMABLE LOGIC, GENERAL PURPOSE
  - 16 macrocells for logic applications (e.g., shifters, state machines, chip-selects, glue-logic to keypads, and LCDs)
- A/D CONVERTER
  - Eight Channels, 10-bit resolution, 6µs

Figure 1. Packages



TQFP52 (T), 52-lead, Thin, Quad, Flat



TQFP80 (U), 80-lead, Thin, Quad, Flat

- COMMUNICATION INTERFACES
  - USB v2.0 Full Speed (12Mbps)
    10 endpoint pairs (In/Out), each endpoint with 64-byte FIFO (supports Control, Intr, and Bulk transfer types)
  - I^2C Master/Slave controller, 833kHz
  - SPI Master controller, 1MHz
  - Two UARTs with independent baud rate
  - IrDA Potocol: up to 115 kbaud
  - Up to 46 I/O, 5V tolerant uPSD34xxV
- TIMERS AND INTERRUPTS
  - Three 8032 standard 16-bit timers
  - Programmable Counter Array (PCA), six 16-bit modules for PWM, CAPCOM, and timers
  - 8/10/16-bit PWM operation
  - 12 Interrupt sources with two external interrupt pins
- OPERATING VOLTAGE SOURCE (±10%)
  - 5V Devices: 5.0V and 3.3V sources
  - 3.3V Devices: 3.3V source

Table 1. Device Summary

Part Number	Max MHz	1st Flash (bytes)	2nd Flash	SRAM	GPIO	8032 Bus	V_{CC}	V_{DD}	Pkg.
uPSD3422E-40T6	40	64K	32K	4K	35	No	3.3V	5.0V	TQFP52
uPSD3422EV-40T6	40	64K	32K	4K	35	No	3.3V	3.3V	TQFP52
uPSD3422E-40U6	40	64K	32K	4K	46	Yes	3.3V	5.0V	TQFP80
uPSD3422EV-40U6	40	64K	32K	4K	46	Yes	3.3V	3.3V	TQFP80
uPSD3433E-40T6	40	128K	32K	8K	35	No	3.3V	5.0V	TQFP52
uPSD3433EV-40T6	40	128K	32K	8K	35	No	3.3V	3.3V	TQFP52
uPSD3433E-40U6	40	128K	32K	8K	46	Yes	3.3V	5.0V	TQFP80
uPSD3433EV-40U6	40	128K	32K	8K	46	Yes	3.3V	3.3V	TQFP80
uPSD3434E-40T6	40	256K	32K	8K	35	No	3.3V	5.0V	TQFP52
uPSD3434EV-40T6	40	256K	32K	8K	35	No	3.3V	3.3V	TQFP52
uPSD3434E-40U6	40	256K	32K	8K	46	Yes	3.3V	5.0V	TQFP80
uPSD3434EV-40U6	40	256K	32K	8K	46	Yes	3.3V	3.3V	TQFP80

Note: Operating temperature is in the Industrial range (–40°C to 85°C).

SUMMARY DESCRIPTION

The *Turbo Plus* uPSD34xx Series combines a powerful 8051-based microcontroller with a flexible memory structure, programmable logic, and a rich peripheral mix to form an ideal embedded controller. At its core is a fast 4-cycle 8032 MCU with a 4-byte instruction prefetch queue (PFQ) and a 4-entry fully associative branching cache (BC). The MCU is connected to a 16-bit internal instruction path to maximize performance, enabling loops of code in smaller localities to execute extremely fast. The 16-bit wide instruction path in the *Turbo Plus* Series allows double-byte instructions to be fetched from memory in a single memory cycle. This keeps the average performance near its peak performance (peak performance for 5V, 40MHz Turbo *Plus* uPSD34xx is 10 MIPS for single-byte instructions, and average performance will be approximately 9 MIPS for mix of single- and multi-byte instructions).

USB 2.0 (full speed, 12Mbps) is included, providing 10 endpoints, each with its own 64-byte FIFO to maintain high data throughput. Endpoint 0 (Control Endpoint) uses two of the 10 endpoints for In and Out directions, the remaining eight endpoints may be allocated in any mix to either type of transfers: Bulk or Interrupt.

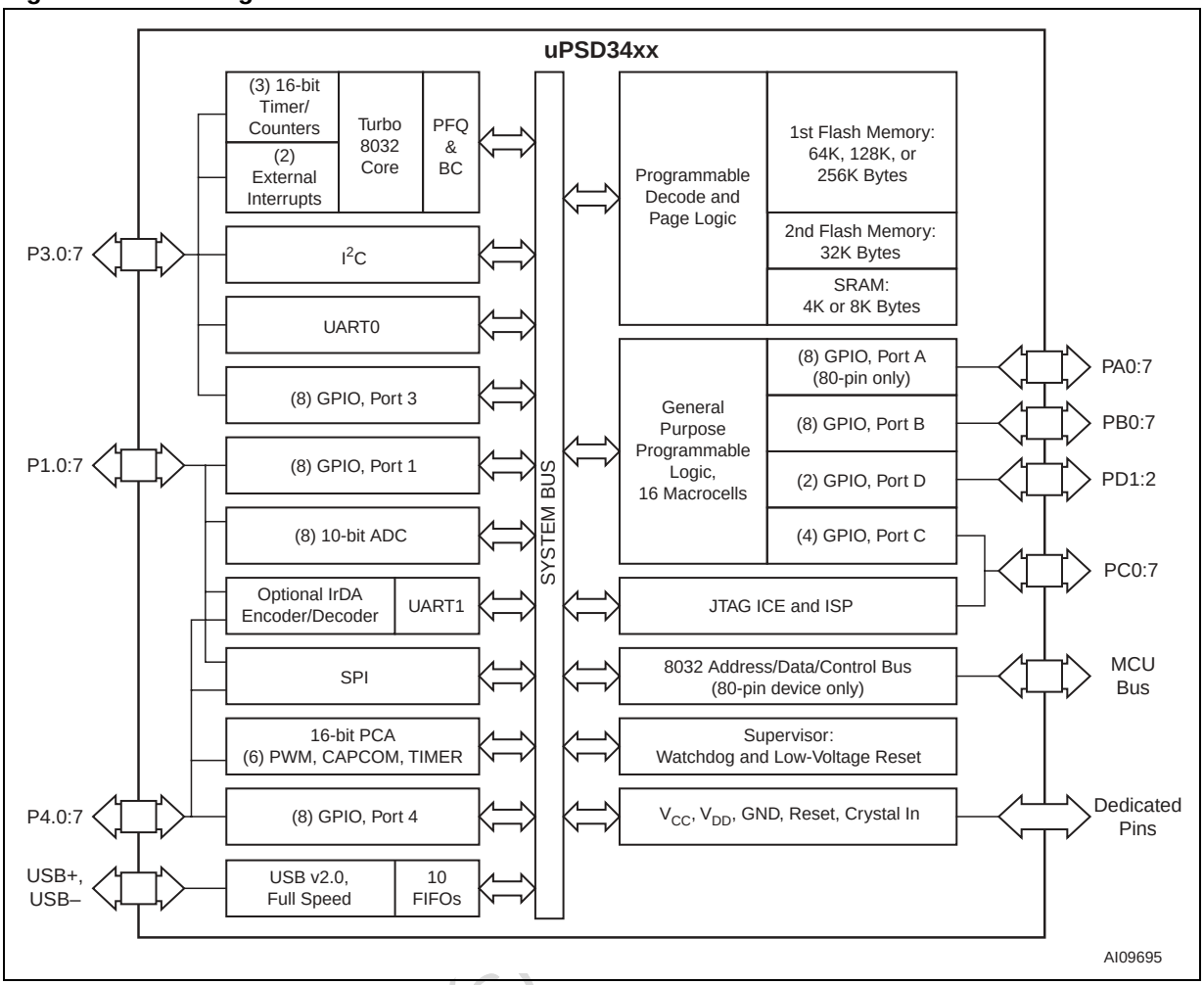
Code development is easily managed without a hardware In-Circuit Emulator by using the serial JTAG debug interface. JTAG is also used for In-System Programming (ISP) in as little as 10 seconds, perfect for manufacturing and lab development. The 8032 core is coupled to Programmable System Device (PSD) architecture to optimize the 8032 memory structure, offering two independent banks of Flash memory that can be placed at virtually any address within 8032 program or data address space, and easily paged beyond 64K bytes using on-chip programmable decode logic.

Dual Flash memory banks provide a robust solution for remote product updates in the field through In-Application Programming (IAP). Dual Flash banks also support EEPROM emulation, eliminating the need for external EEPROM chips.

General purpose programmable logic (PLD) is included to build an endless variety of glue-logic, saving external logic devices. The PLD is configured using the software development tool, PSDsoft Express, available from the web at **www.st.com/psm**, at no charge.

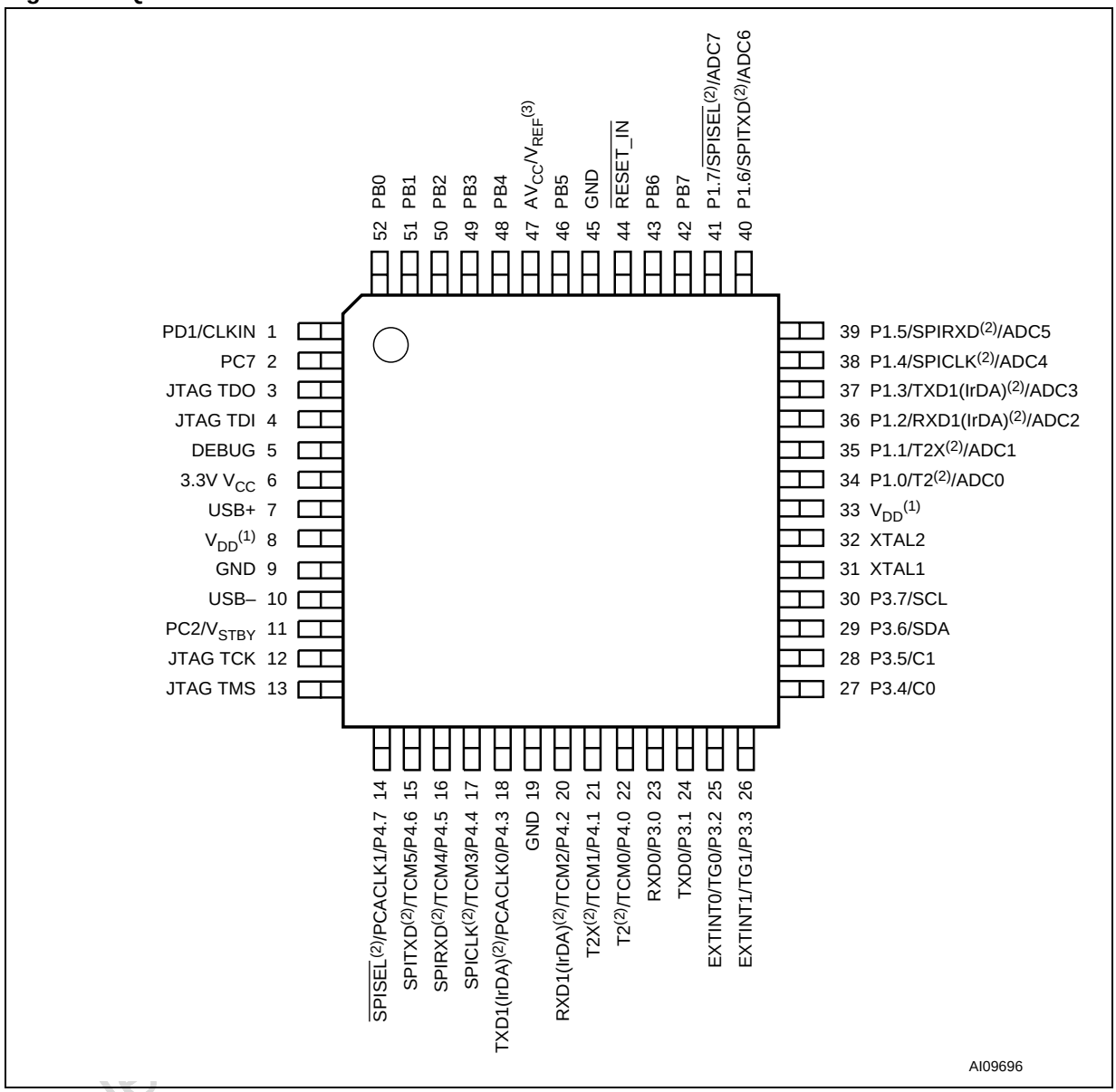
The uPSD34xx also includes supervisor functions such as a programmable watchdog timer and low-voltage reset.

Figure 2. Block Diagram



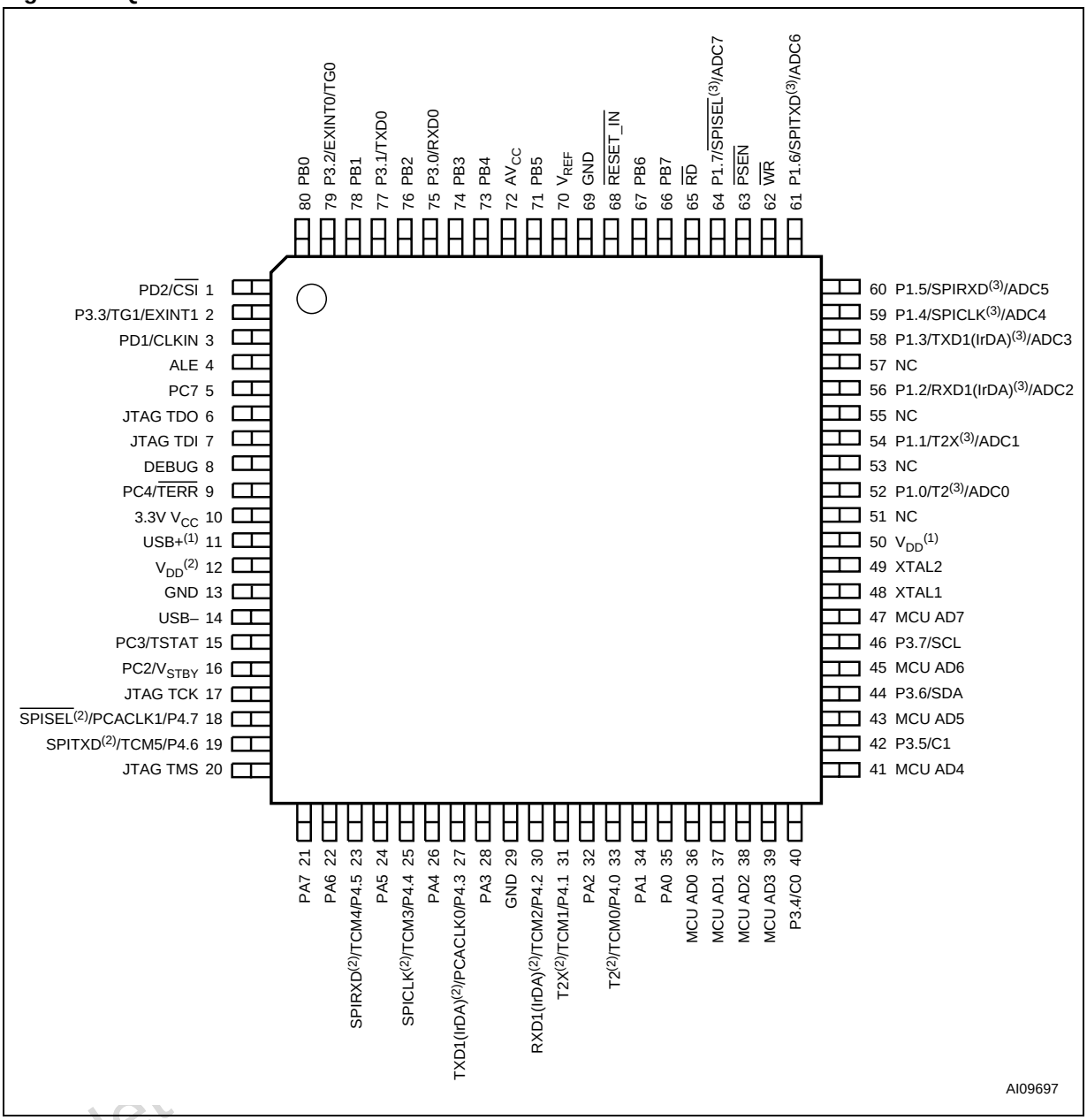
PIN DESCRIPTIONS

Figure 3. TQFP52 Connections



Note: 1. For 5V applications, V_{DD} must be connected to a 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
2. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.
3. AV_{REF} and 3.3V AV_{CC} are shared in the 52-pin package only. ADC channels must use 3.3V as AV_{REF} for the 52-pin package.

Figure 4. TQFP80 Connections



Note: NC = Not Connected

Note: 1. The USB+ pin needs a 1.5kΩ pull-up resistor.
2. For 5V applications, V_{DD} must be connected to a 5.0V source. For 3.3V applications, V_{DD} must be connected to a 3.3V source.
3. These signals can be used on one of two different ports (Port 1 or Port 4) for flexibility. Default is Port1.

Table 2. Major Parameters

Parameter	Test Conditions/Comments	5.0V Value	3.3V Value	Unit
Operating Voltage	–	4.5 to 5.5 (PSD); 3.0 to 3.6 (MCU)	3.0 to 3.6 (PSD and MCU)	V
Operating Temperature	–	–40 to 85	–40 to 85	°C
MCU Frequency	8MHz (min) for I^2C	3 Min, 40 Max	3 Min, 40 Max	MHz
Operating Current, Typical(1) (20% of PLD used; 25°C operation. Bus control signals are blocked from the PLD in Non-Turbo mode.)	40MHz Crystal, Turbo	79	63	mA
	40MHz Crystal, Non-Turbo	71	58	mA
	8MHz Crystal, Turbo	32	24	mA
	8MHz Crystal, Non-Turbo	17.7	14	mA
Idle Current, Typical (20% of PLD used; 25°C operation)	40MHz Crystal divided by 2048 internally. All interfaces are disabled.	19	18	mA
Standby Current, Typical	Power-down Mode needs reset to exit.	140	120	µA
SRAM Backup Current, Typical	If external battery is attached.	0.5	0.5	µA
I/O Sink/Source Current, Ports A, B, C, and D	V_{OL} = 0.45V (max); V_{OH} = 2.4V (min)	I_{OL} = 8 (max); I_{OH} = –2 (min)	I_{OL} = 4 (max); I_{OH} = –1 (min)	mA
I/O Sink/Source Current, Port 4	V_{OL} = 0.6V (max); V_{OH} = 2.4V (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	I_{OL} = 10 (max); I_{OH} = –10 (min)	mA
PLD Macrocells	For registered or combinatorial logic	16	16	–
PLD Inputs	Inputs from pins, feedback, or MCU addresses	69	69	–
PLD Outputs	Output to pins or internal feedback	18	18	–
PLD Propagation Delay, Typical, Turbo Mode	PLD input to output	15	22	ns

Note: 1. Operating current is measured while the uPSD34xx is executing a typical program at 40MHz.

PART NUMBERING

Table 3. Ordering Information Scheme

Example: UPSD 34 3 4 E V – 40 U 6 T

Device Type

uPSD = Microcontroller PSD

Family

34 = Turbo Plus core

SRAM Size

2 = 4Kbyte

3 = 8Kbyte

Main Flash Memory Size

2 = 64Kbyte

3 = 128Kbyte

4 = 256Kbyte

IP Mix

E = IP Mix: USB, I^2C, SPI, UART (2), IrDA, ADC, Supervisor, PCA

Operating Voltage

blank = V_{CC} = 4.5 to 5.5V

V = V_{CC} = 3.0 to 3.6V

Speed

–40 = 40MHz

Package

T = 52-pin TQFP

U = 80-pin TQFP

Temperature Range

6 = –40 to 85°C

Shipping Option

Tape & Reel Packing = T

For other options, or for more information on any aspect of this device, please contact the ST Sales Office nearest you.

REVISION HISTORY

Table 4. Document Revision History

Date	Version	Revision Details
08-Nov-2004	1.0	First Edition
07-Feb-2005	2.0	Updated from v1.0 full datasheet