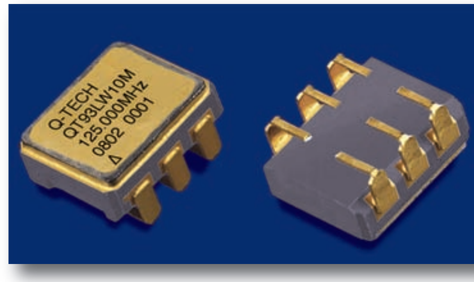
QT93W and QT93P SERIES

HIGH-RELIABILITY LVPECL OR LVDS MINIATURE CLOCK OSCILLATORS
2.5 to 3.3Vdc - 40MHz to 160MHz

Description

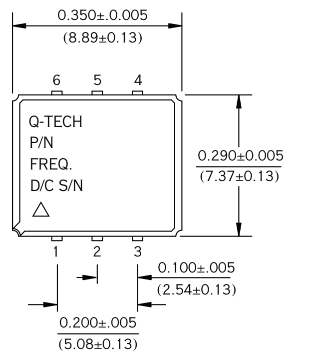
Q-Tech's surface-mount QT93 series oscillators consist of a 2.5Vdc and 3.3Vdc differential PECL or LVDS output oscillator IC and a round AT high-precision quartz crystal built in a rugged surface-mount ceramic miniature package. It was designed to be replaceable and retrofitable into the footprint of a 7 x 5mm COTS LVPECL or LVDS oscillator.



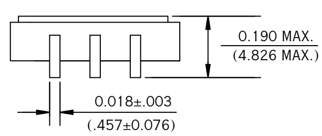
Features

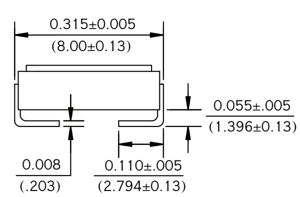
- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- USML Registration # M17677
- Smallest AT round crystal package ever designed
- Broad frequency range from 40MHz to 160MHz
- Able to meet 36000G shock per ITOP 1-2-601
- Rugged 4 point mount design for high shock and vibration
- Differential LVPECL or LVDS output
- Tri-State Output
- Hermetically sealed ceramic SMD package
- 3rd Overtone designs, no sub-harmonics
- Low phase noise, low noise coupling, low emissions
- Custom designs available
- Q-Tech does not use pure lead or pure tin in its products
- RoHS compliant

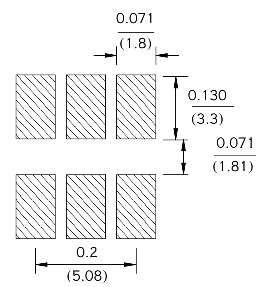
Package Specifications and Outline



Pin No.	Function
1	TRISTATE
2	NC
3	GND
4	OUTPUT
5	COMP. OUTPUT
6	VCC







Dimensions are in inches (mm)

Applications

- SONET/SDH
- Fibre channel
- Gun launched munitions and systems
- Applications required high data transmission throughputs
- Clock generation and distribution
- Audio/Video signal processing
- Broadband access
- Ethernet, Gigabit Ethernet

Package material: 90% AL_2O_3
Lead material: Kovar
Lead finish:
- Gold Plated: 50µ ~ 80µ inches
- Nickel Underplate: 100µ ~ 250µ inches

Electrical Characteristics

Parameters	QT93LW	QT93NW	QT93LP	QT93NP
	(LVDS Output)		(LVPECL Output)	
Output frequency range (Fo)	**40MHz — 160.00MHz (*)**			
Supply voltage (Vcc)	3.3Vdc ± 5%	2.5Vdc ± 5%	3.3Vdc ± 5%	2.5Vdc ± 5%
Frequency stability (ΔF/ΔT)	See option codes			
Operating temperature (Topr)	See option codes			
Storage temperature (Tsto)	-62ºC to + 150ºC			
Operating supply current (Icc)	80mA max. (45mA typ. at 125MHz)	65mA max.	80mA max. (45mA typ. at 100MHz)	
Symmetry (measured at 50% output level)	45/55% max.			
Rise and Fall times (measured between 20% to 80% Vcc)	600ps max.		1.0ns max. (600ps typ.)	
Output Load (Requires termination)	100Ω (Connected between Out and Comp. Out)		50Ω to Vcc -2Vdc (or Thevenin equivalent) (Connected between each Output and Vcc -2Vdc)	
Start-up time (Tstup)	2ms max.			
Output voltage (Voh/Vol)	VOH = 1.45V typ., 1.65V max. VOL = 1.10V typ., 0.90V min.		VOH = 2.215V min.; 2.420V max. VOL = 1.47V min.; 1.745V max.	VOH = 1.415V min.; 1.76V max. VOL = 0.67 min.; 1.195V max.
Enable/Disable Tristate function (see note 1)	Pin 1: Open or VIH ≥ 0.7*Vcc Oscillation VIL ≤ 0.3*Vcc High Z			
Jitter	RMS Phase jitter (integrated 12kHz — 40MHz): 1ps max. Total jitter: 30ps peak-to-peak			

(*) Higher frequencies are available. Please contact Q-Tech for details.

Note 1: There is a built-in OE pull-up resistor which resistance value changes in response to the input level (High or Low) to save power consumption.

Ordering Information

3.3Vdc LVDS

QT93LW — XX — M — 155.520MHz

- 155.520MHz: Output frequency
- M: Screened to MIL-PRF-55310,level B (Left blank if no screening)
- XX:

1	=	±	100ppm	at	0ºC	to	+70ºC
4	=	±	50ppm	at	0ºC	to	+70ºC
5	=	±	25ppm	at	-20ºC	to	+70ºC
6	=	±	50ppm	at	-55ºC	to	+105ºC
9	=	±	50ppm	at	-55ºC	to	+125ºC
10	=	±	100ppm	at	-55ºC	to	+125ºC
11	=	±	50ppm	at	-40ºC	to	+85ºC
12	=	±	100ppm	at	-40ºC	to	+85ºC
14	=	±	20ppm	at	-20ºC	to	+70ºC
15	=	±	25ppm	at	-40ºC	to	+85ºC

2.5Vdc LVDS

QT93NW — XX — M —125.000MHz

- 125.000MHz: Output frequency
- M: Screened to MIL-PRF-55310,level B (Left blank if no screening)
- XX:

1	=	±	100ppm	at	0ºC	to	+70ºC
4	=	±	50ppm	at	0ºC	to	+70ºC
5	=	±	25ppm	at	-20ºC	to	+70ºC
6	=	±	50ppm	at	-55ºC	to	+105ºC
9	=	±	50ppm	at	-55ºC	to	+125ºC
10	=	±	100ppm	at	-55ºC	to	+125ºC
11	=	±	50ppm	at	-40ºC	to	+85ºC
12	=	±	100ppm	at	-40ºC	to	+85ºC
14	=	±	20ppm	at	-20ºC	to	+70ºC
15	=	±	25ppm	at	-40ºC	to	+85ºC

3.3Vdc LVPECL

QT93LP — XX — M — 106.250MHz

- 106.250MHz: Output frequency
- M: Screened to MIL-PRF-55310,level B (Left blank if no screening)
- XX:

1	=	±	100ppm	at	0ºC	to	+70ºC
4	=	±	50ppm	at	0ºC	to	+70ºC
5	=	±	25ppm	at	-20ºC	to	+70ºC
6	=	±	50ppm	at	-55ºC	to	+105ºC
9	=	±	50ppm	at	-55ºC	to	+125ºC
10	=	±	100ppm	at	-55ºC	to	+125ºC
11	=	±	50ppm	at	-40ºC	to	+85ºC
12	=	±	100ppm	at	-40ºC	to	+85ºC
14	=	±	20ppm	at	-20ºC	to	+70ºC
15	=	±	25ppm	at	-40ºC	to	+85ºC

2.5Vdc LVPECL

QT93NP — XX — M — 100.000MHz

- 100.000MHz: Output frequency
- M: Screened to MIL-PRF-55310,level B (Left blank if no screening)
- XX:

1	=	±	100ppm	at	0ºC	to	+70ºC
4	=	±	50ppm	at	0ºC	to	+70ºC
5	=	±	25ppm	at	-20ºC	to	+70ºC
6	=	±	50ppm	at	-55ºC	to	+105ºC
9	=	±	50ppm	at	-55ºC	to	+125ºC
10	=	±	100ppm	at	-55ºC	to	+125ºC
11	=	±	50ppm	at	-40ºC	to	+85ºC
12	=	±	100ppm	at	-40ºC	to	+85ºC
14	=	±	20ppm	at	-20ºC	to	+70ºC
15	=	±	25ppm	at	-40ºC	to	+85ºC

Frequency stability vs. temperature codes may not be available in all frequencies.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Packaging Options

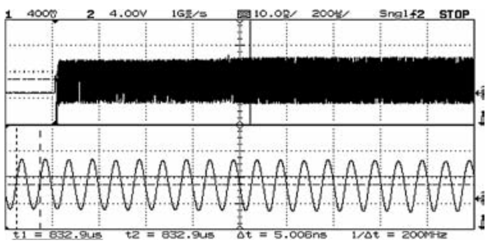
- Standard packaging in anti-static plastic tube (60pcs/tube)
- Tape and Reel (800pcs/reel) is available for an additional charge.

Other Options Available For An Additional Charge

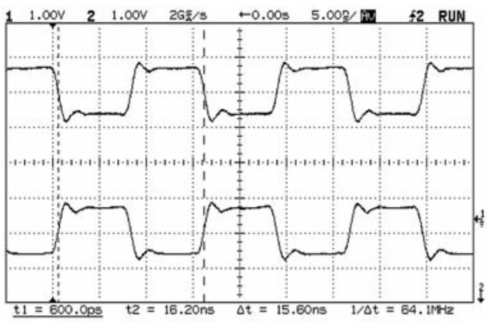
- Solder Dip Sn/Pb 60/40%
- P. I. N. D. test

Specifications subject to change without prior notice.

Output Waveform (Typical)

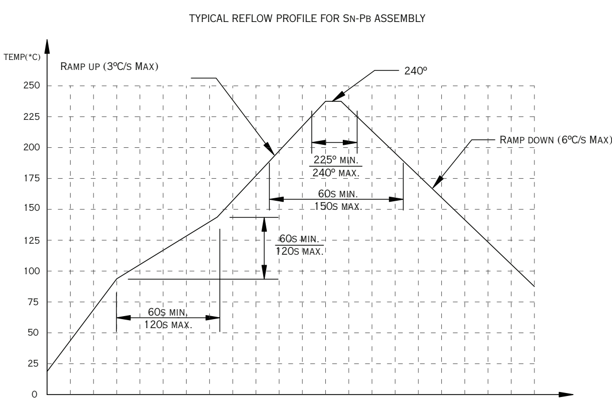


Typical start-up time of an LVPECL 3.3Vdc 200MHz at -55ºC 0.833ms



Typical plot of an LVPECL 3.3Vdc 64MHz terminated with Thevenin equivalent

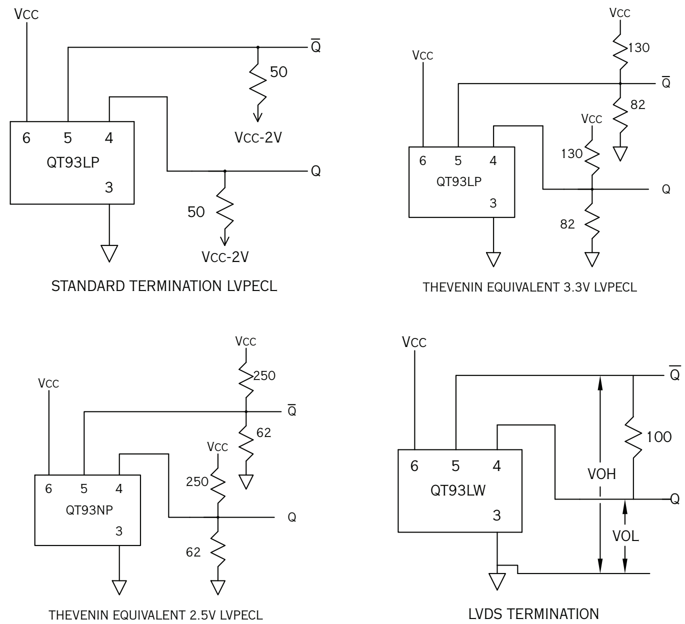
Reflow Profile



Environmental and Mechanical Specifications

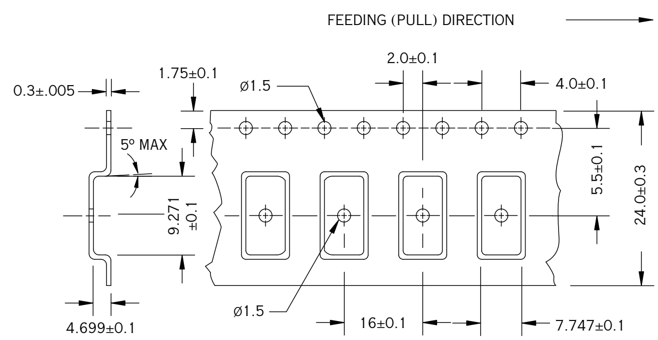
Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal Gross Leak	MIL-STD-883, Method 1014, Cond. C
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208

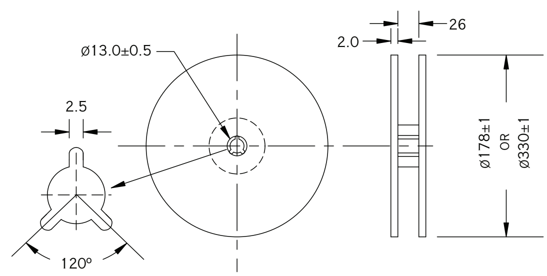
Test Circuit



The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vcc without deteriorating the electrical performance.

Embossed Tape and Reel Information





Dimensions are in mm. Tape is compliant to EIA-481-A.

Reel size (Diameter in mm)	Qty per reel (pcs)
178	1,000

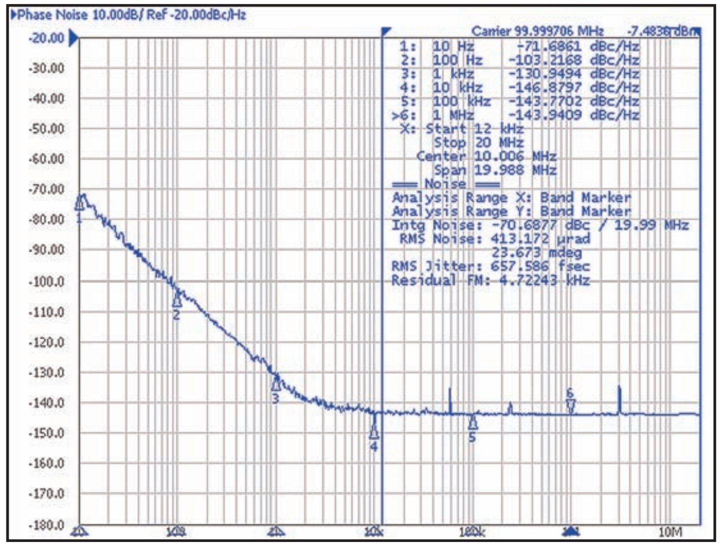
Phase Noise and Phase Jitter Integration

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure 1 shows a typical Phase Noise/Phase jitter of a QT93LW, 3.3Vdc, 100MHz clock at offset frequencies 10Hz to 10MHz, and phase jitter integrated over the bandwidth of 12kHz to 20MHz.



(Figure 1)

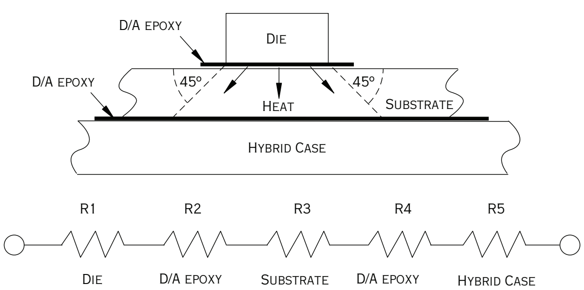
Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 2.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

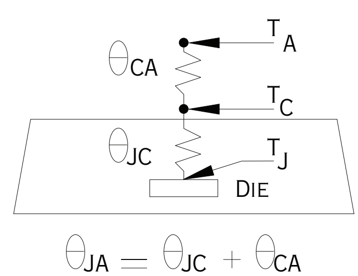
$$RT = R1 + R2 + R3 + R4 + R5$$



(Figure 2)

The total thermal resistance RT (see figure 3) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

- Theta junction to case (Theta JC) for this product is 35°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 135°C/W.



(Figure 3)

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/135 = 1.11W