First-In First-Out (FIFO) 64x4 Memory 15 MHz (Cascadable) With Three-State Outputs

C67L4013D

Features/Benefits

- High-speed 15-MHz shift-in/shift-out rates
- Low power consumption
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation
- Output Enable feature

Ordering Information

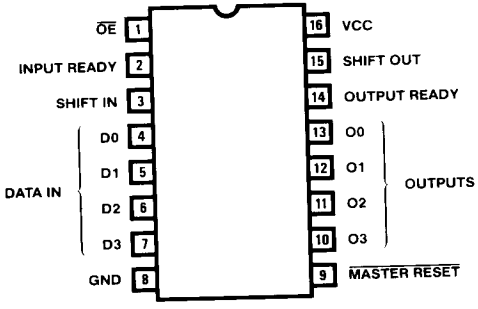
PART NUMBER	PKG	TEMP	O/P	DESCRIPTION
C67L4013D	N, J	Com	3-state	15 MHz FIFO

Description

The C67L4013D is a "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. The C67L4013D has three-state, high-drive (I_{OL} = 24 mA) outputs.

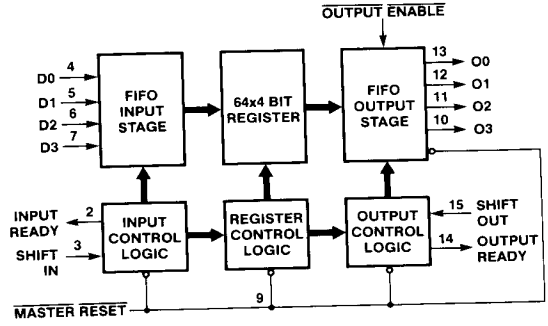
Pin Configuration

C67L4013D



Block Diagram

C67L4013D



Publication #	Rev.	Amendment
10682	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift in rate	1			15	MHz
t_{SIH}	Shift in High time	1	24			ns
t_{SIL}	Shift in Low time	1	15			ns
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold time to SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold time to IR (Input Ready)	4	26			ns
f_{OUT}	Shift out rate	5			15	MHz
t_{SOH}	Shift out High time	5	17			ns
t_{SOL}	Shift out Low time	5	15			ns
t_{MRW}	Master Reset pulse**	10	35			ns
t_{MRS}	Master Reset to SI*	10	35			ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8**	V
V_{IH}	High-level input voltage				2**		V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA		-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level Output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA		0.5	V
		IR, OR		I_{OL} = 8 mA			
V_{OH}	High-level Output voltage	Output, O	V_{CC} = MIN	I_{OH} = -3.0 mA	2.4		V
		IR, OR		I_{OH} = -0.9 mA			
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20	-90	mA
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V		-50	μA
I_{OZH}				V_O = 2.4 V		+50	
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.			110	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		40	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH			26	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		45	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH			50	ns
t_{ODH}†	Output Data Hold (previous word)		12		ns
t_{ODS}	Output Data Shift (next word)			40	ns
t_{PT}	Data throughput	4,8		1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		60	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH*			30	ns
t_{MRIRL}	Master Reset ↓ to Input Ready LOW*			50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			60	ns
t_{IPH}	Input ready pulse HIGH	4	17		ns
t_{OPH}	Output ready pulse HIGH	8	24		ns
t_{ORD}	Output ready ↑ to Data Valid	5		-3	ns
t_{PHZ}	Output Disable Delay, C67L4013D	A		30	ns
t_{PLZ}				30	
t_{PZL}	Output Enable Delay, C67L4013D			30	ns
t_{PZH}				40	

Note: Typicals at 5V V_{CC} and 25° C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

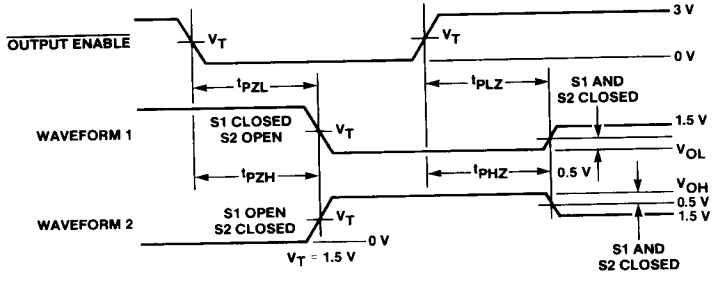
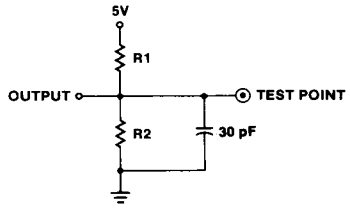


Figure A. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

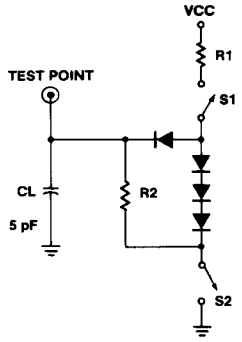
Standard Test Load



I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Three-State Test Load



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Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

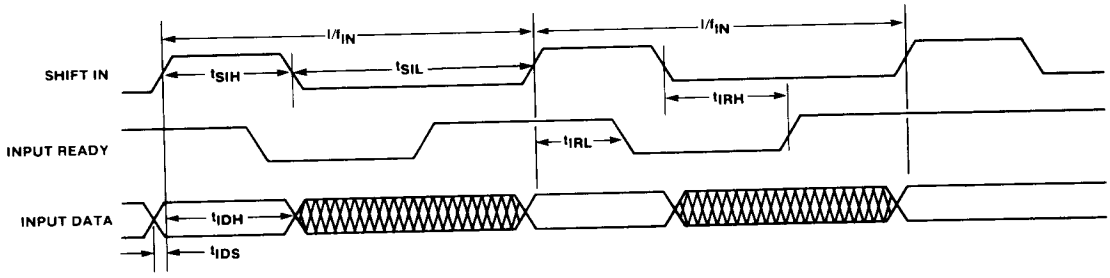

Figure 1. Input Timing

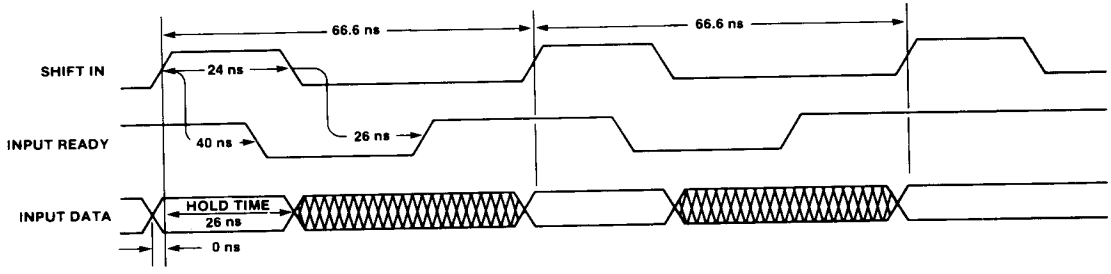

Figure 2. Typical Waveforms for 15 MHz Shift-In Rate

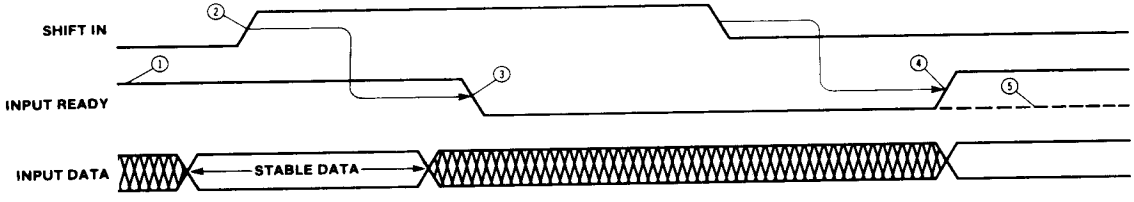

Figure 3. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is avialable and a Shift-In pulse may be applied.

② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.

③ Input Ready goes LOW indicating the first word is full.

④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.

⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

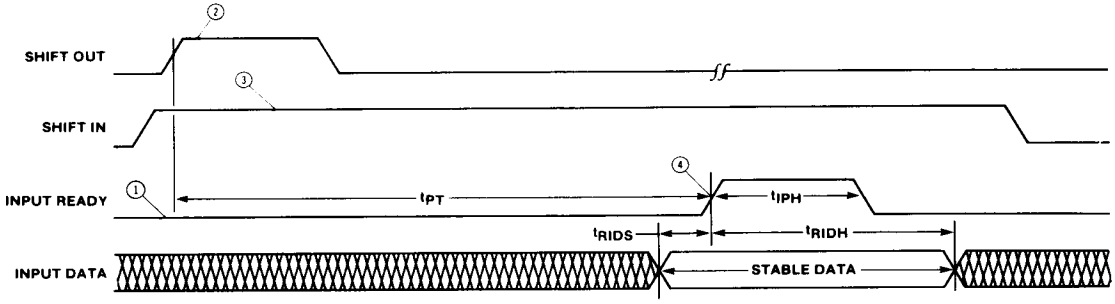

Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulsed is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

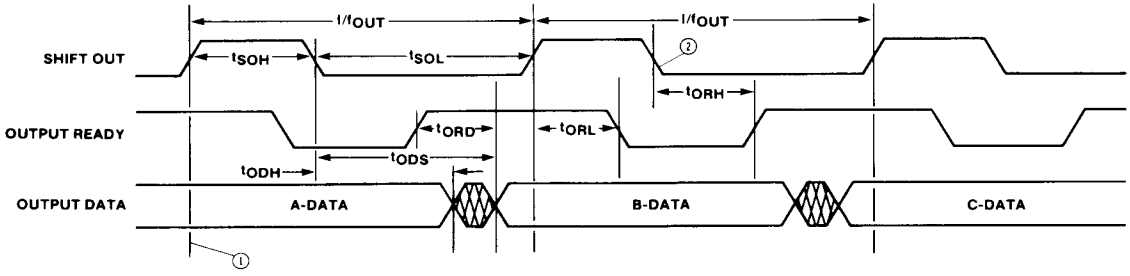

Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

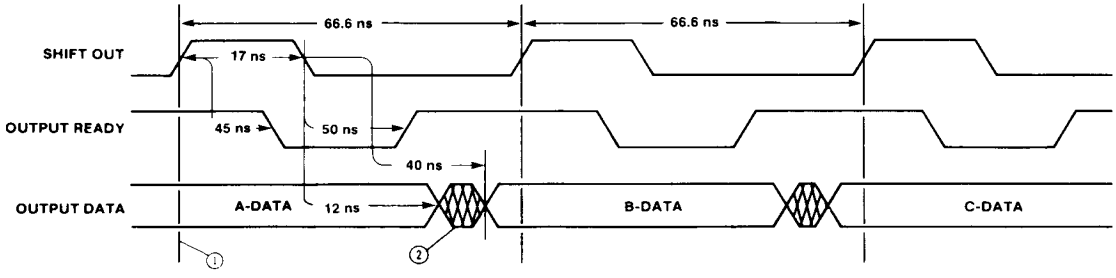

Figure 6. Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

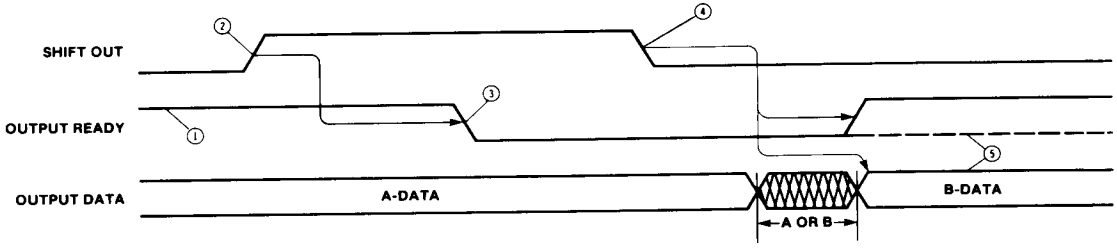

Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

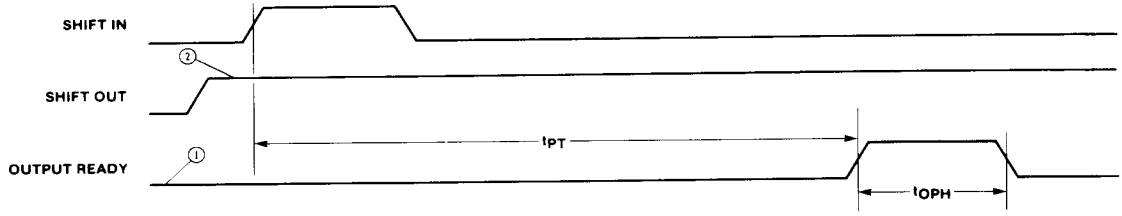

Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

② Shift Out held HIGH.

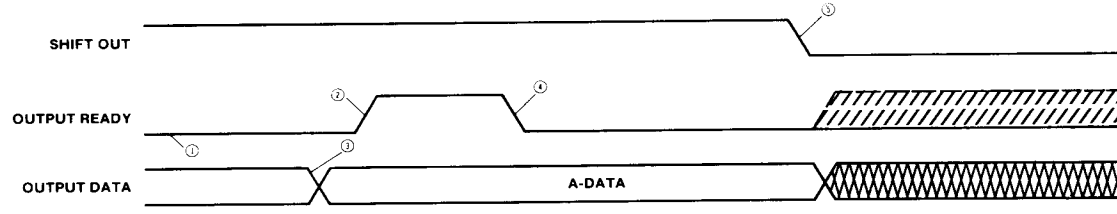

Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

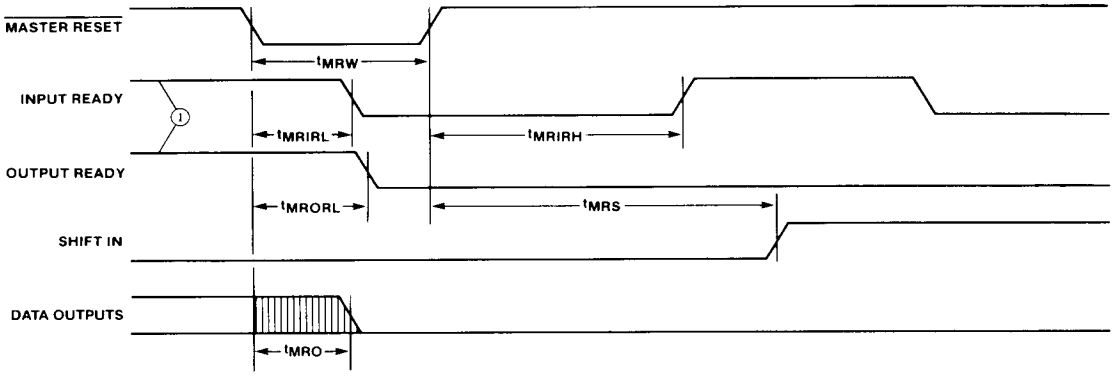

Figure 10. Master Reset Timing

① FIFO initially partially full.