

7.0 x 5.0 x 1.4mm HCMOS/ TTL COMPATIBLE SURFACE MOUNT LOW PROFILE (1.4max) CRYSTAL CLOCK OSCILLATOR



7.0 x 5.0 x 1.4mm

ASV2 SERIES



**RoHS
Compliant**

FEATURES:

- 1.4 mm max. in height
- HCMOS and TTL compatible, 1.8V to 3.3VDC
- Tristate Enable / Disable function
- Reflow capable
- Available optional -40°C to 85°C extended temperature
- Seam sealed package

APPLICATIONS:

- Clock signaling for μ Processors, PC Motherboards & Graphic Cards
- High load output drive capability applications

STANDARD SPECIFICATIONS:

PARAMETERS

| | |
|-------------------------------|---|
| ABRACON P/N | ASV2 Series |
| Frequency Range | 0.012 MHz to 133.000 MHz |
| Operating Temperature | -10° C to + 70° C (see options) |
| Storage Temperature | - 55° C to + 125° C |
| Overall Frequency Stability | \pm 100 ppm max. (see options) |
| Supply Voltage (Vdd) | 3.3 Vdc \pm 10% (see options) |
| Input Current | See Table 1 |
| Symmetry | 40/60 % max.@ 1/2Vdd (see options) |
| Rise time / Fall time (Tr/Tf) | See Table 2 |
| Output Load | 15pF (5TTL) (see options) |
| Output Voltage | VOH = 0.9 * Vdd min. (90% of Vdd) VOL = 0.4 Vdc max. (10% of Vdd) |
| Start-up Time | 8ms max. |
| Tristate Function | "1" (VIH: see table 3) or open: Oscillation "0" (VIL: see table 3): Hi Z |
| Aging at 25°C/year | \pm 5ppm max. |
| Absolute Clock Period Jitter | \pm 40ps max. |
| Disable Current | 10 μ A max. |

TABLE 1

| Frequency | 3.3Vdd | 2.5Vdd | 1.8Vdd |
|------------------------|--------|--------|--------|
| 0.012MHz Fo < 0.048MHz | 5 | 5 | N/A |
| 0.048MHz Fo < 1.5MHz | 5 | 5 | 5 |
| 1.5MHz Fo < 20MHz | 7 | 7 | 5 |
| 20MHz Fo < 50MHz | 20 | 15 | 15 |
| 50MHz Fo < 70MHz | 30 | 20 | 15 |
| 70MHz Fo < 125MHz | 30 | 20 | 20 |
| 125MHz Fo 133MHz | 40 | 30 | N/A |

Unit: (mA max)

TABLE 2

| Frequency | 3.3Vdd | 2.5Vdd | 1.8Vdd |
|----------------------|--------|--------|--------|
| 0.012MHz Fo < 1.0MHz | 200 | 200 | N/A |
| 1.0MHz Fo < 20MHz | 10 | 10 | 10 |
| 20MHz Fo < 50MHz | 6 | 6 | 6 |
| 50MHz Fo < 70MHz | 3 | 3 | 3 |
| 70MHz Fo < 125MHz | 3 | 3 | 3 |
| 125MHz Fo 133MHz | 3 | 3 | N/A |

Tr times are measured between 10% & 90% of Vdd with 15pF load.

TABLE 3

| Vdd | VIH | VIL |
|-----|------|-----|
| 1.8 | 1.26 | 0.5 |
| 2.5 | 1.75 | 0.5 |
| 3.3 | 2 | 0.5 |



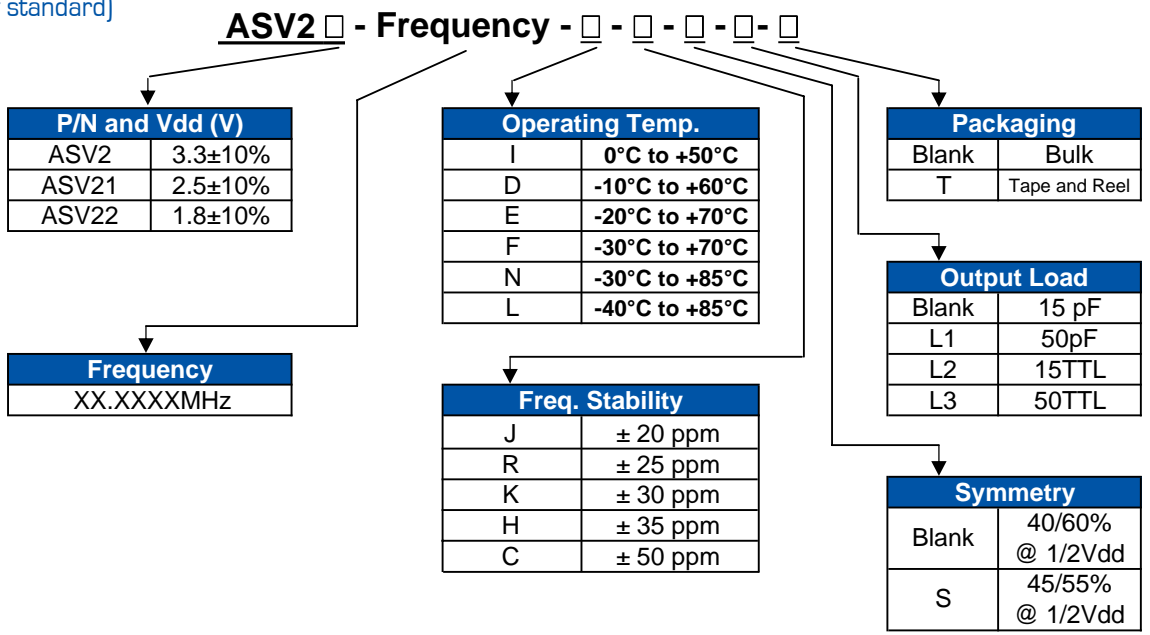


ASV2 SERIES

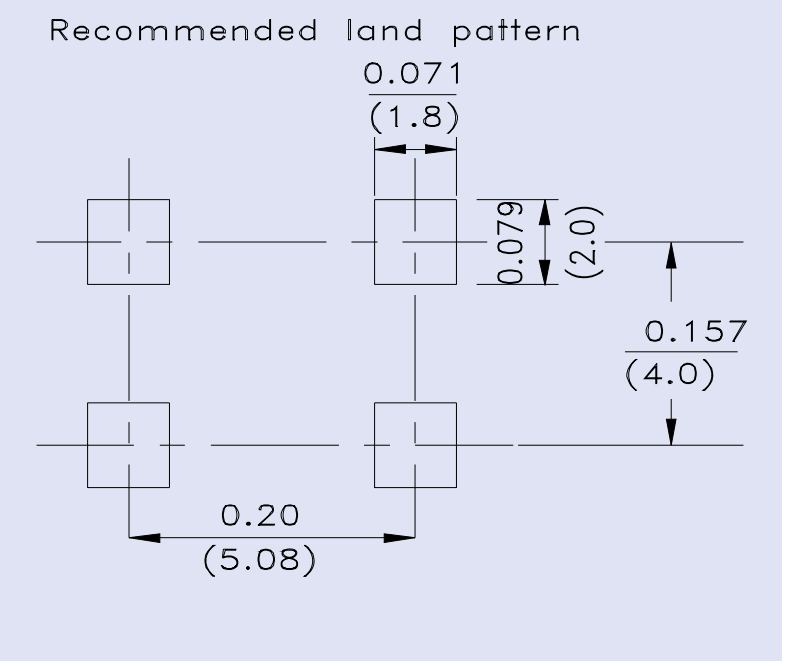
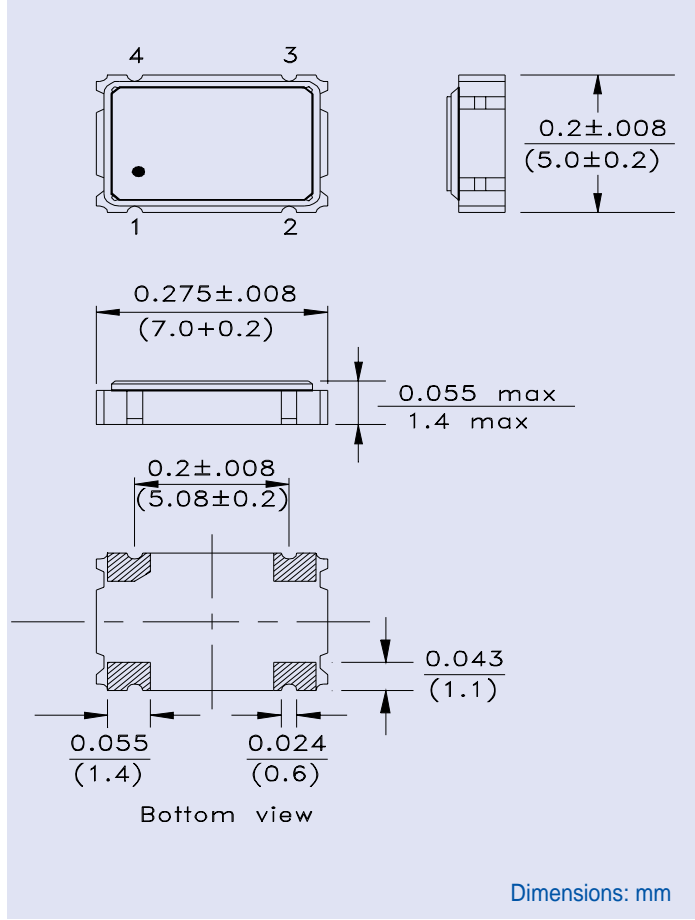


OPTIONS & PART IDENTIFICATION:

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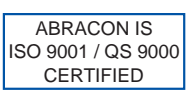


OUTLINE DRAWING:



| PIN | FUNCTION |
|-----|-------------------------|
| 1 | Tristate Enable/Disable |
| 2 | GND/Case |
| 3 | Output |
| 4 | Vdd |

Note: It is recommended to use an approximately 0.01uF bypass capacitor between PIN 2 and 4.



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ASV2

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TAPE & REEL: Tape and reel 1,000pcs/reel

