MC9S12HZ256

Data Sheet

Covers
MC9S12HZ128, MC9S12HZ64, MC9S12HN64
MC3S12HZ256, MC3S12HZ128, MC3S12HZ64,
MC3S12HN64, MC3S12HZ32 & MC3S12HN32

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Microcontrollers

MC9S12HZ256V2
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The following revision history table summarizes changes contained in this document.

Revision History

Date	Revision Level	Description
October 10, 2005	02.01	New Data Sheet
April 20, 2006	02.02	Corrected Table 4-1 Port U and Port V descriptions Added 80QFP to PCB layout guidelines Added derivative differences to appendix D Updated ordering information on appendix E
October 5, 2006	02.03	Added ROM to memory options Updated memory map figures and added tables for RAM mapping options Added ROM derivatives to appendix D Added ROM description to appendices (appendix E)
October 31, 2006	02.04	Added MC3S12HZ64 mask set Updated Table A-5 Thermal Package Characteristics Updated Table A-17 PLL Characteristics

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Chapter 1
MC9S12HZ256 Device Overview

1.1 Introduction

The MC9S12HZ256 microcontroller units (MCU) are 16-bit devices composed of standard on-chip peripherals including a 16-bit central processing unit (HCS12 CPU), up to 256K bytes of Flash EEPROM or ROM, up to 12K bytes of RAM, 2K bytes of EEPROM, two asynchronous serial communications interfaces (SCI), a serial peripheral interface (SPI), an IIC-bus interface (IIC), an 8-channel 16-bit timer (TIM), a 16-channel, 10-bit analog-to-digital converter (ATD), a six-channel pulse width modulator (PWM), and two CAN 2.0 A, B software compatible modules (MSCAN). In addition, they feature a 32x4 liquid crystal display (LCD) controller/driver, a pulse width modulator motor controller (MC) consisting of 16 high current outputs suited to drive up to four stepper motors, and four stepper stall detectors (SSD) to simultaneously calibrate the pointer position of each motor. System resource mapping, clock generation, interrupt control, and external bus interfacing are managed by the HCS12 Core. The MC9S12HZ256 have full 16-bit data paths throughout. The inclusion of a PLL circuit allows power consumption and performance to be adjusted to suit operational requirements. In addition to the I/O ports available in each module, 8 general-purpose I/O pins are available with interrupt and wake-up capability from stop or wait mode.

For information regarding the HCS12 CPU instruction set, please see the *HCS12 CPU Reference Manual*, Freescale document order number S12CPUV2.

1.1.1 Features

- HCS12 core
  - 16-bit HCS12 CPU
    - Upward compatible with M68HC11 instruction set
    - Interrupt stacking and programmer's model identical to M68HC11
    - 16-bit ALU
    - Instruction queue
    - Enhanced indexed addressing
  - MEBI (multiplexed external bus interface)
  - MMC (module mapping control)
  - INT (interrupt control)
  - DBG (debugger and breakpoints)
  - BDM (background debug mode)

- Memory
  - 256K, 128K, 64K, 32K Flash EEPROM or ROM
  - 2K, 1K byte EEPROM
  - 12K, 6K, 4K, 2K byte RAM
- CRG (low current oscillator, PLL, reset, clocks, COP watchdog, real time interrupt, clock monitor)
- Analog-to-digital converter
  - 16 channels, 10-bit resolution
  - External conversion trigger capability
- Two 1-Mbps, CAN 2.0 A, B software compatible modules
  - Five receive and three transmit buffers
  - Flexible identifier filter programmable as 2 x 32 bit, 4 x 16 bit or 8 x 8 bit
  - Four separate interrupt channels for Rx, Tx, error and wake-up
  - Low-pass filter wake-up function
  - Loop-back for self test operation
- Timer
  - 16-bit main counter with 7-bit prescaler
  - 8 programmable input capture or output compare channels
  - Two 8-bit or one 16-bit pulse accumulators
- 6 PWM channels
  - Programmable period and duty cycle
  - 8-bit 6-channel or 16-bit 3-channel
  - Separate control for each pulse width and duty cycle
  - Center-aligned or left-aligned outputs
  - Programmable clock select logic with a wide range of frequencies
  - Fast emergency shutdown input
- Serial interfaces
  - Two asynchronous serial communications interfaces (SCI)
  - Synchronous serial peripheral interface (SPI)
  - Inter-integrated circuit interface (IIC)
- Liquid crystal display (LCD) driver with variable input voltage
  - Configurable for up to 32 frontplanes and 4 backplanes or general-purpose input or output
  - 5 modes of operation allow for different display sizes to meet application requirements
  - Unused frontplane and backplane pins can be used as general-purpose I/O
- PWM motor controller (MC) with 16 high current drivers
  - Each PWM channel switchable between two drivers in an H-bridge configuration
  - Left, right and center aligned outputs
  - Support for sine and cosine drive
  - Dithering
  - Output slew rate control

- Four stepper stall detectors (SSD)
  - Full step control during return to zero
  - Voltage detector and integrator / sigma delta converter circuit
  - 16-bit accumulator register
  - 16-bit modulus down counter
- 112-pin LQFP and 80-pin QFP packages
  - 85 I/O lines with 5-V input and drive capability
  - 5-V A/D converter inputs
  - 8 key wake up interrupts with digital filtering and programmable rising/falling edge trigger
- Operation at 50 MHz equivalent to 25-MHz bus speed
- Development support
  - Single-wire background debug™ mode (BDM)
  - Debugger and on-chip hardware breakpoints

1.1.2 Modes of Operation

User modes

- Normal and emulation operating modes
  - Normal single-chip mode
  - Normal expanded wide mode
  - Normal expanded narrow mode
  - Emulation expanded wide mode
  - Emulation expanded narrow mode
- Special operating mode
  - Special single-chip mode with active background debug mode

Low-power modes

- Stop mode
- Pseudo stop mode
- Wait mode

1.1.3 Block Diagram

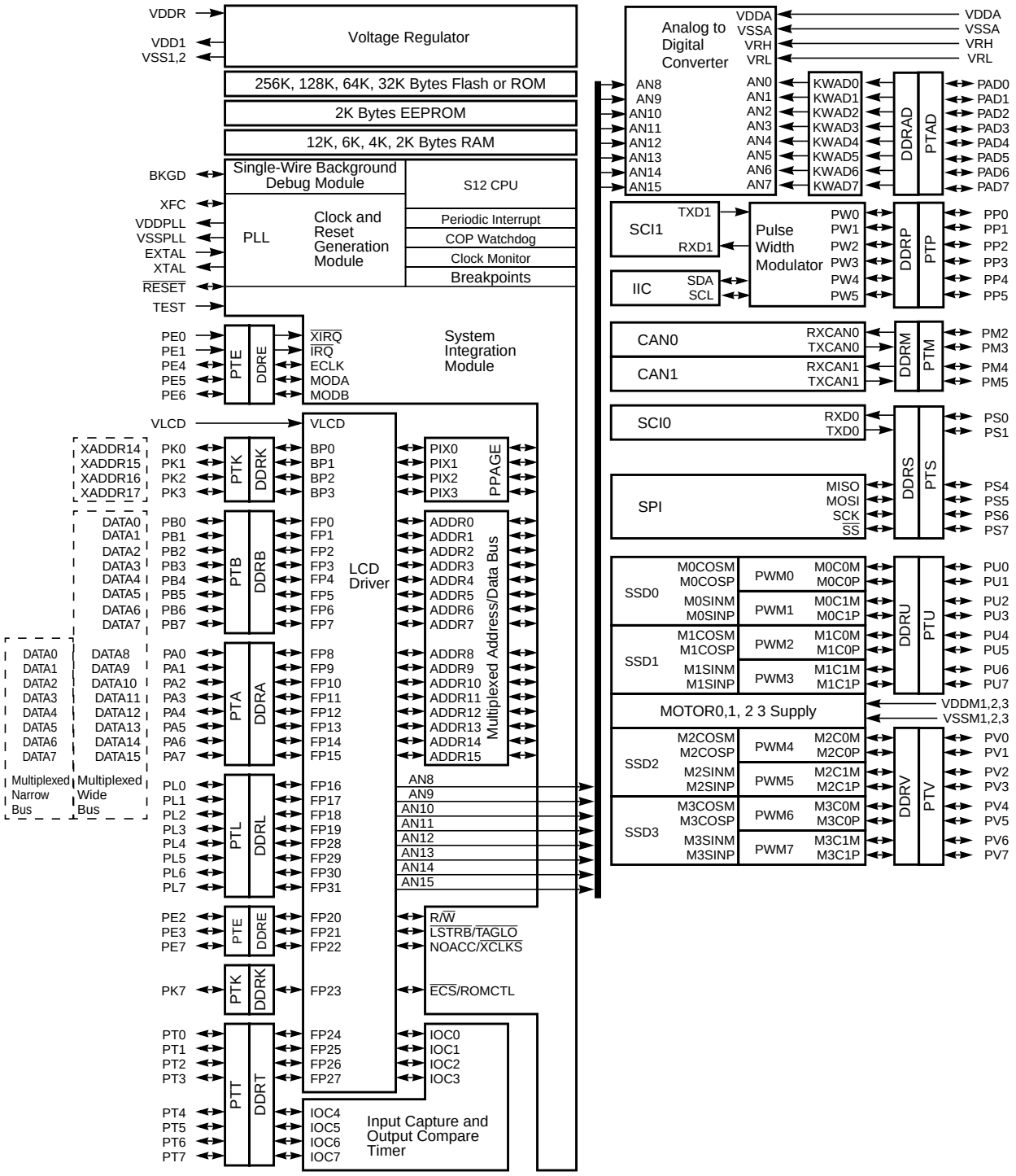


Figure 1-1. MC9S12HZ256 Block Diagram

1.2 Device Memory Map

Table 1-1 shows the device memory map for the MC9S12HZ256 out of reset.

Table 1-1. Device Register Map Overview

Address Offset	Module	Size (Bytes)
0x0000–0x0017	HCS12 Core (Ports A, B, E, Modes, Inits, Test)	24
0x0018–0x0019	Reserved	2
0x001A–0x001B	Device ID register (PARTID)	2
0x001C–0x001F	HCS12 Core (MEMSIZ, IRQ, HPRIO)	4
0x0020–0x0027	Reserved	8
0x0028–0x002F	HCS12 Core (Background Debug Mode)	8
0x0030–0x0033	HCS12 Core (PPAGE, Port K)	4
0x0034–0x003F	Clock and Reset Generator (PLL, RTI, COP)	12
0x0040–0x006F	Standard Timer Module 16-bit 8 channels (TIM)	48
0x0070–0x007F	Reserved	16
0x0080–0x00AF	Analog-to-Digital Converter 10-bit 16 channels (ATD)	48
0x00B0–0x00BF	Reserved	16
0x00C0–0x00C7	Inter Integrated Circuit (IIC)	8
0x00C8–0x00CF	Serial Communications Interface 0 (SCI0)	8
0x00D0–0x00D7	Serial Communications Interface 1 (SCI1)	8
0x00D8–0x00DF	Serial Peripheral Interface (SPI)	8
0x00E0–0x00FF	Pulse Width Modulator 8-bit 6 channels (PWM)	32
0x0100–0x010F	Flash control registers	16
0x0110–0x011B	EEPROM control registers	12
0x011C–0x011F	Reserved	4
0x0120–0x0137	Liquid Crystal Display Driver 32x4 (LCD)	24
0x0140–0x017F	Scalable Controller Area Network 0 (MSCAN0)	64
0x0180–0x01BF	Scalable Controller Area Network 1 (MSCAN1)	64
0x01C0–0x01FF	Motor Control Module (MC)	64
0x0200–0x027F	Port Integration Module (PIM)	128
0x0280–0x0287	Reserved	8
0x0288–0x028F	Stepper Stall Detector 0 (SSD0)	8
0x0290–0x0297	Stepper Stall Detector 1 (SSD1)	8
0x0298–0x029F	Stepper Stall Detector 2 (SSD2)	8
0x02A0–0x02A7	Stepper Stall Detector 3 (SSD3)	8
0x02A8–0x03FF	Reserved	344

Figure 1-2 shows the device memory map for the MC9(3)S12HZ256 out of reset.

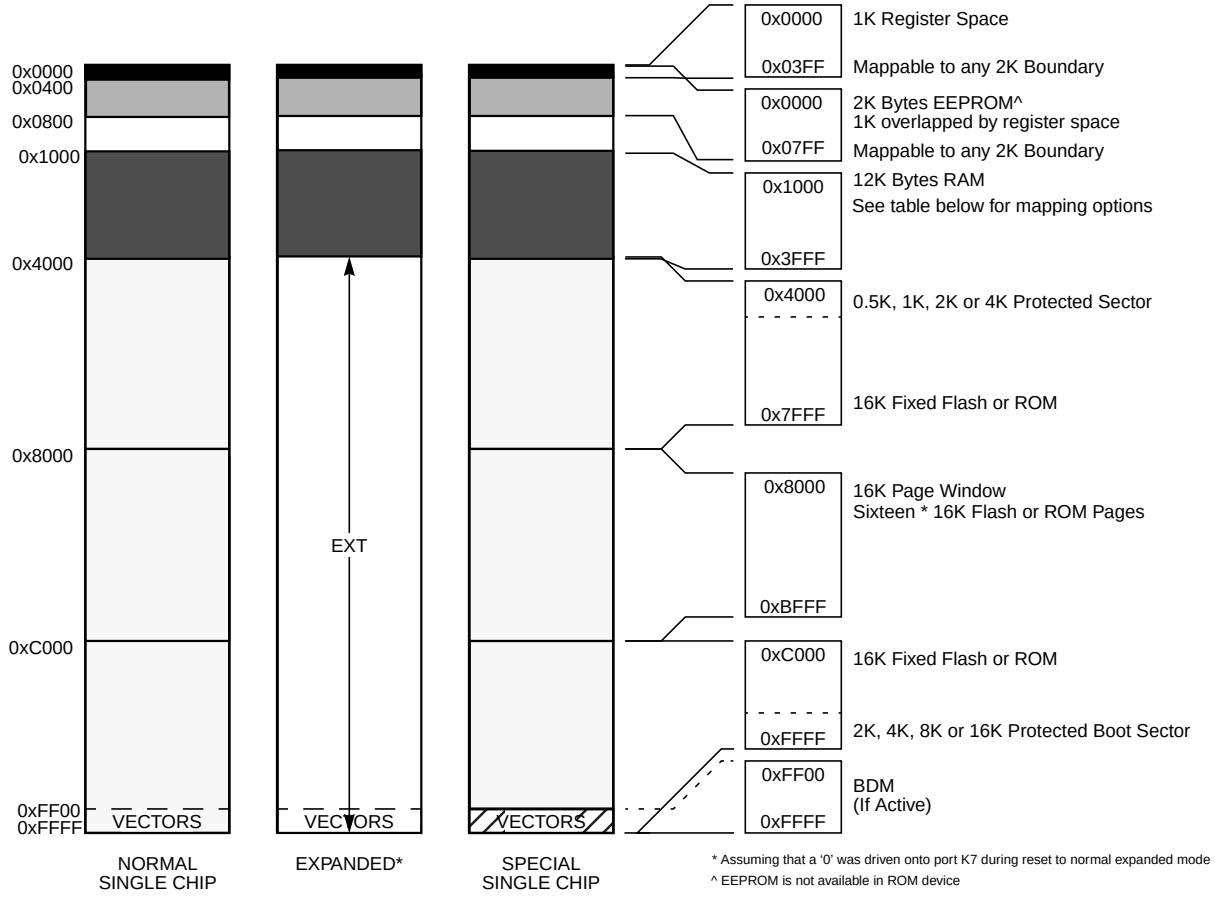


Figure 1-2. MC9(3)S12HZ256 Memory Map

Table 1-2. MC9(3)S12HZ256 RAM mapping options

INITRM	RAM location
0x00	0x0000 - 0x2FFF
0x39	0x1000 - 0x3FFF
0x40	0x4000 - 0x6FFF
0x79	0x5000 - 0x7FFF
0x80	0x8000 - 0xAFFF
0xB9	0x9000 - 0xBFFF
0xC0	0xC000 - 0xEFFF
0xF9	0xD000 - 0xFFFF

Figure 1-3 shows the device memory map for the MC9(3)S12HZ128 out of reset.

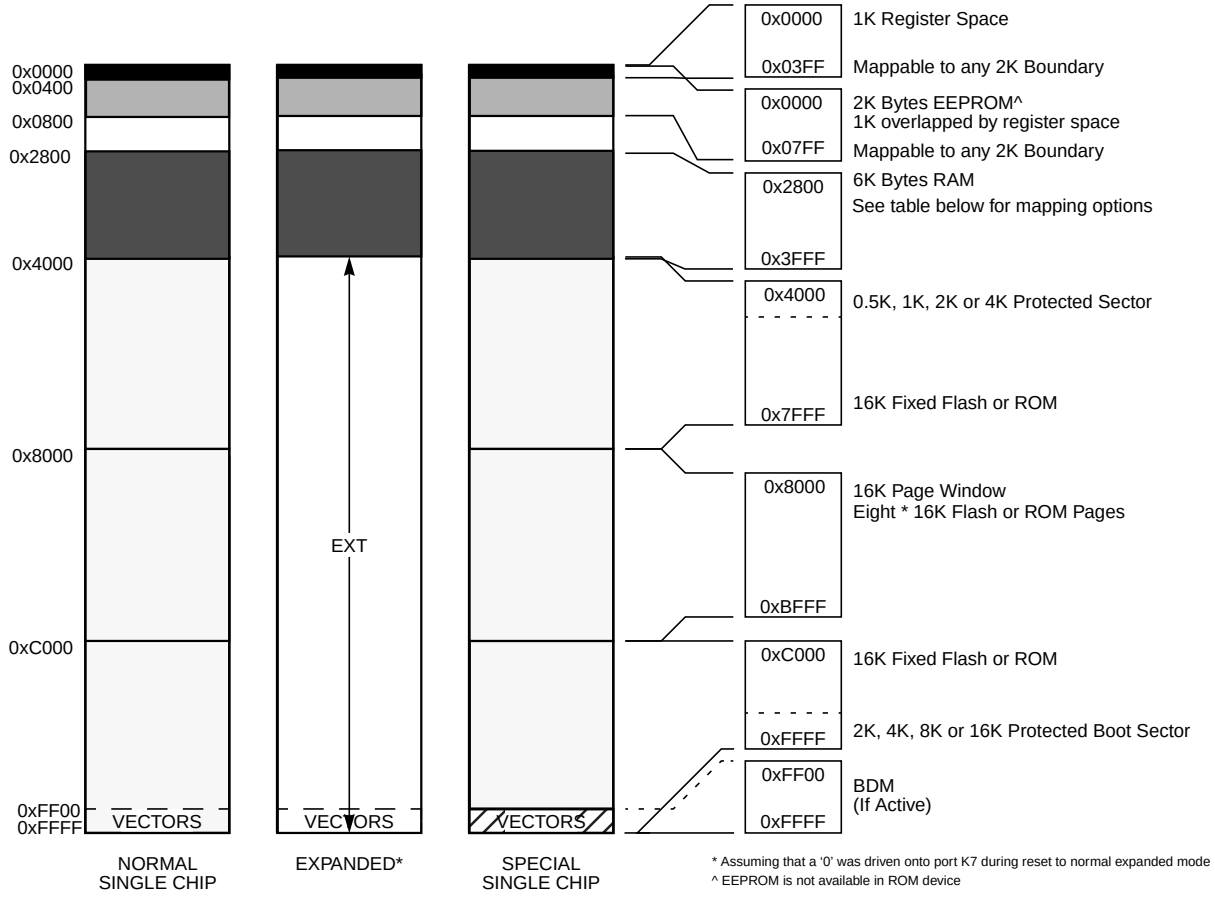


Figure 1-3. MC9(3)S12HZ128 Memory Map

Table 1-3. MC9(3)S12HZ128 RAM mapping options

INITRM[1]	RAM location	Reserved location (no Flash/ROM/EEPROM access)
0x00	0x0000 - 0x17FF	0x1800 - 0x2FFF
0x39	0x2800 - 0x3FFF	0x1000 - 0x27FF
0x40	0x4000 - 0x57FF	0x5800 - 0x6FFF
0x79	0x6800 - 0x7FFF	0x5000 - 0x67FF
0x80	0x8000 - 0x97FF	0x9800 - 0xAFFF
0xB9	0xA800 - 0xBFFF	0x9000 - 0xA7FF
0xC0	0xC000 - 0xD7FF	0xD800 - 0xEFFF
0xF9	0xE800 - 0xFFFF	0xD000 - 0xE7FF

1 User must initialize RAM13 bit to the same value as RAMHAL bit

Figure 1-4 shows the device memory map for the MC9(3)S12HZ64 and MC9(3)S12HN64 out of reset.

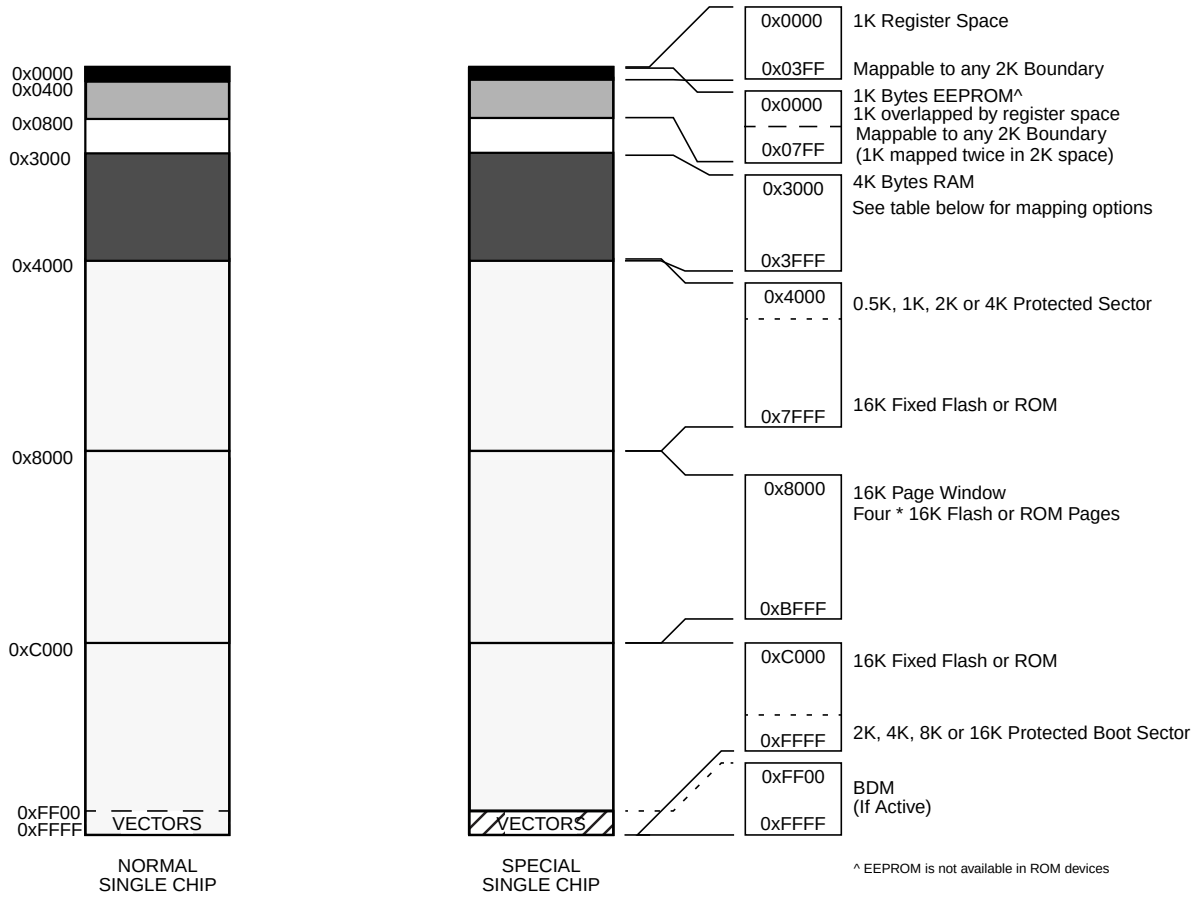


Figure 1-4. MC9(3)S12HZ64 and M9S12(3)HN64 Memory Map

Table 1-4. MC9(3)S12HZ64 and M9S12(3)HN64 RAM mapping options

INITRM[1]	RAM location	Reserved location (no Flash/ROM/EEPROM access)
0x00	0x0000 - 0x0FFF	0x1000 - 0x2FFF
0x39	0x3000 - 0x3FFF	0x1000 - 0x2FFF
0x40	0x4000 - 0x4FFF	0x5000 - 0x6FFF
0x79	0x7000 - 0x7FFF	0x5000 - 0x6FFF
0x80	0x8000 - 0x8FFF	0x9000 - 0xAFFF
0xB9	0xB000 - 0xBFFF	0x9000 - 0xAFFF
0xC0	0xC000 - 0xCFFF	0xD000 - 0xEFFF
0xF9	0xF000 - 0xFFFF	0xD000 - 0xEFFF

1 User must initialize RAM13 and RAM12 bits to the same value as RAMHAL bit

Figure 1-5 shows the device memory map for the MC3S12HZ32 and MC93S12HN32 out of reset.

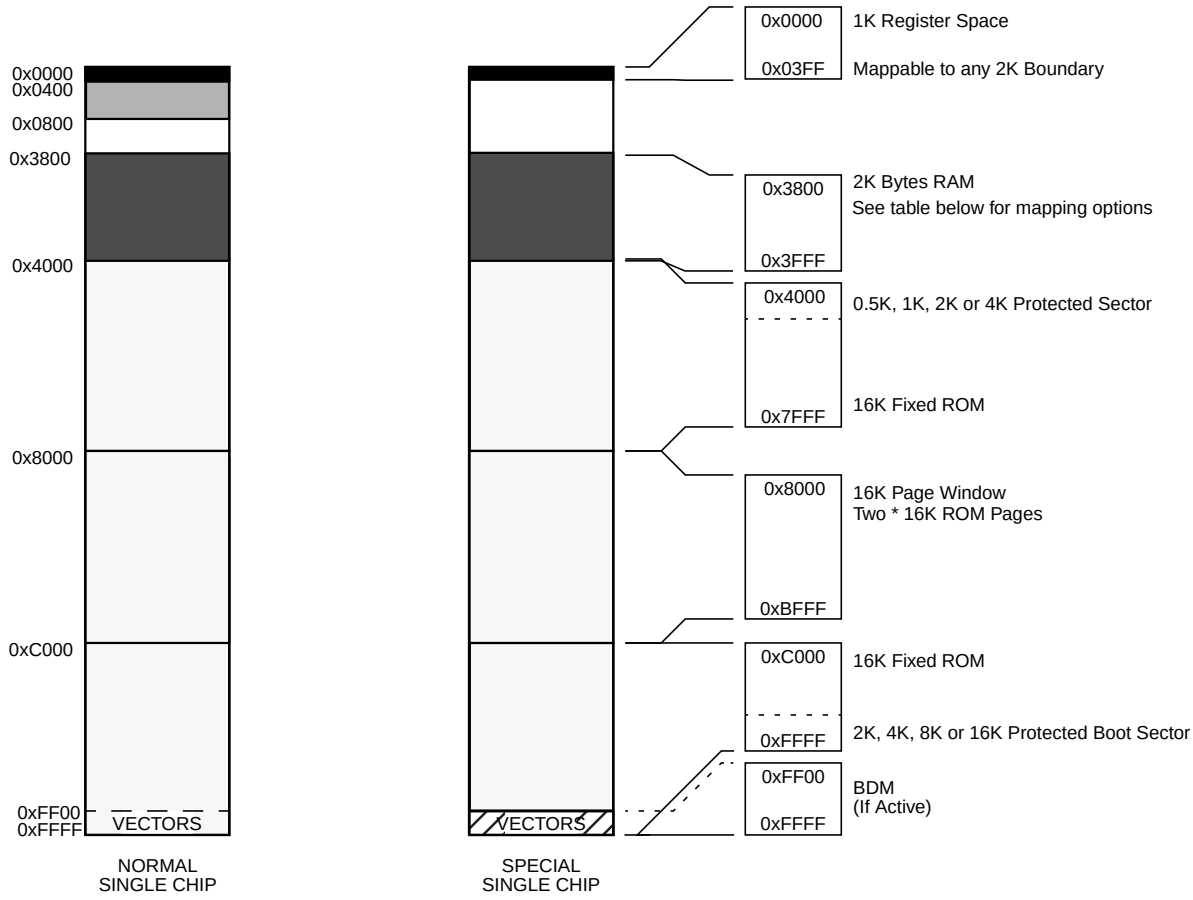


Figure 1-5. MC3S12HZ32 and MC3S12HN32 Memory Map

Table 1-5. MC3S12HZ32 and MC3S12HN32 RAM mapping options

INITRM[1]	RAM location	Reserved location (no ROM access)
0x00	0x0000 - 0x07FF	0x0800 - 0x2FFF
0x39	0x3800 - 0x3FFF	0x1000 - 0x37FF
0x40	0x4000 - 0x47FF	0x4800 - 0x6FFF
0x79	0x7800 - 0x7FFF	0x5000 - 0x77FF
0x80	0x8000 - 0x87FF	0x8800 - 0xAFFF
0xB9	0xB800 - 0xBFFF	0x9000 - 0xB7FF
0xC0	0xC000 - 0xC7FF	0xC800 - 0xEFFF
0xF9	0xF800 - 0xFFFF	0xD000 - 0xF7FF

1 User must initialize RAM13, RAM12 and RAM11 bits to the same value as RAMHAL bit

1.3 Part ID Assignments and Mask Set Numbers

The part ID is located in two 8-bit registers PARTIDH and PARTIDL at addresses 0x001A and 0X001B, respectively. The rado-only value is a unique part ID for each revision of the chip. Table 1-6 shows the assigned part ID and Mask Set numbers.

Table 1-6. Assigned Part ID and Mask Set Numbers

Part Names	Mask Set	Part ID[1]
MC9S12HZ256 MC9S12HZ128 MC9S12HZ64 MC9S12HN64 MC3S12HZ256 MC3S12HZ128	2L16Y/3L16Y	0x1402/0x1403
MC3S12HZ64 MC3S12HN64 MC3S12HZ32 MC3S12HN32	1M36C	0x1501

[1] The coding is as follows:
Bit 15-12: Major family identifier
Bit 11-8: Minor family identifier
Bit 7-4: Major mask set revision including fab transfers
Bit 3-0: Minor non-full mask set revision

The device memory sizes are located in two 8-bit registers MEMSIZ0 and MEMZI1 (addresses 0x001C and 0x001D after reset). Table 1-7 shows the read-only values of these registers. Refer to the HCS12 MMC block description chapter for further details.

Table 1-7. Memory Size Registers

Part Names	MEMSIZ0	MEMSIZ1
MC9S12HZ256 MC9S12HZ128 MC9S12HZ64 MC9S12HN64 MC3S12HZ256 MC3S12HZ128	0x15	0x81
MC3S12HZ64 MC3S12HN64 MC3S12HZ32 MC3S12HN32	0x01	0x80

1.4 Signal Description

This section describes signals that connect off-chip. It includes a pinout diagram, a table of signal properties, and detailed discussion of signals. It is built from the signal description sections of the block description chapters of the individual IP blocks on the device.

1.4.1 Device Pinout

The MC9S12HZ256 are available in a 112-pin quad flat pack (LQFP) and a 80-pin quad flat pack (QFP). Most pins perform two or more functions, as described in 1.5, “Detailed Signal Descriptions”. Figure 1-6, Figure 1-7 and Figure 1-8 show the pin assignments.

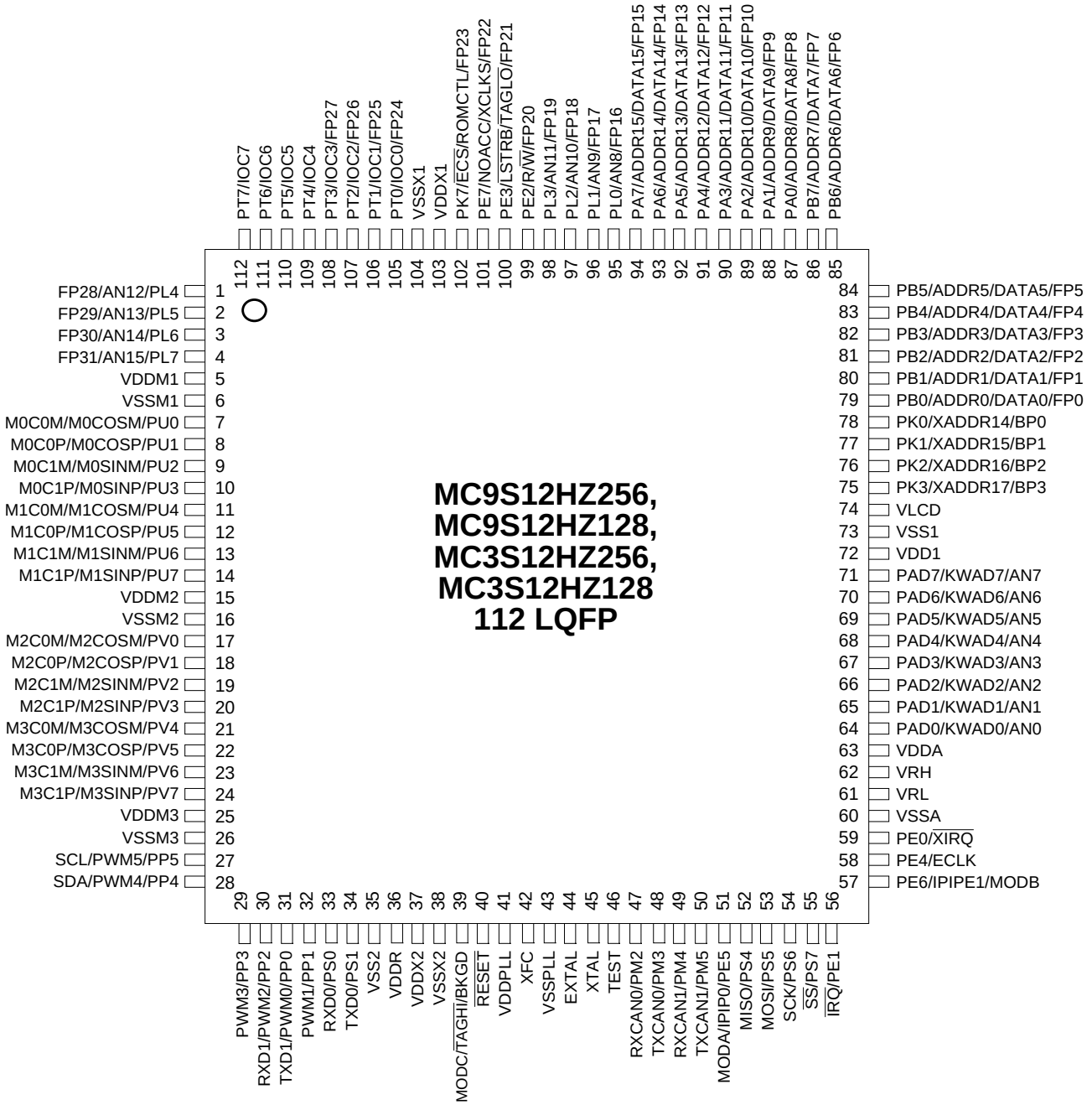


Figure 1-6. 112-Pin LQFP for MC9S12HZ256, MC9S12HZ128, MC3S12HZ256 and MC3S12HZ128

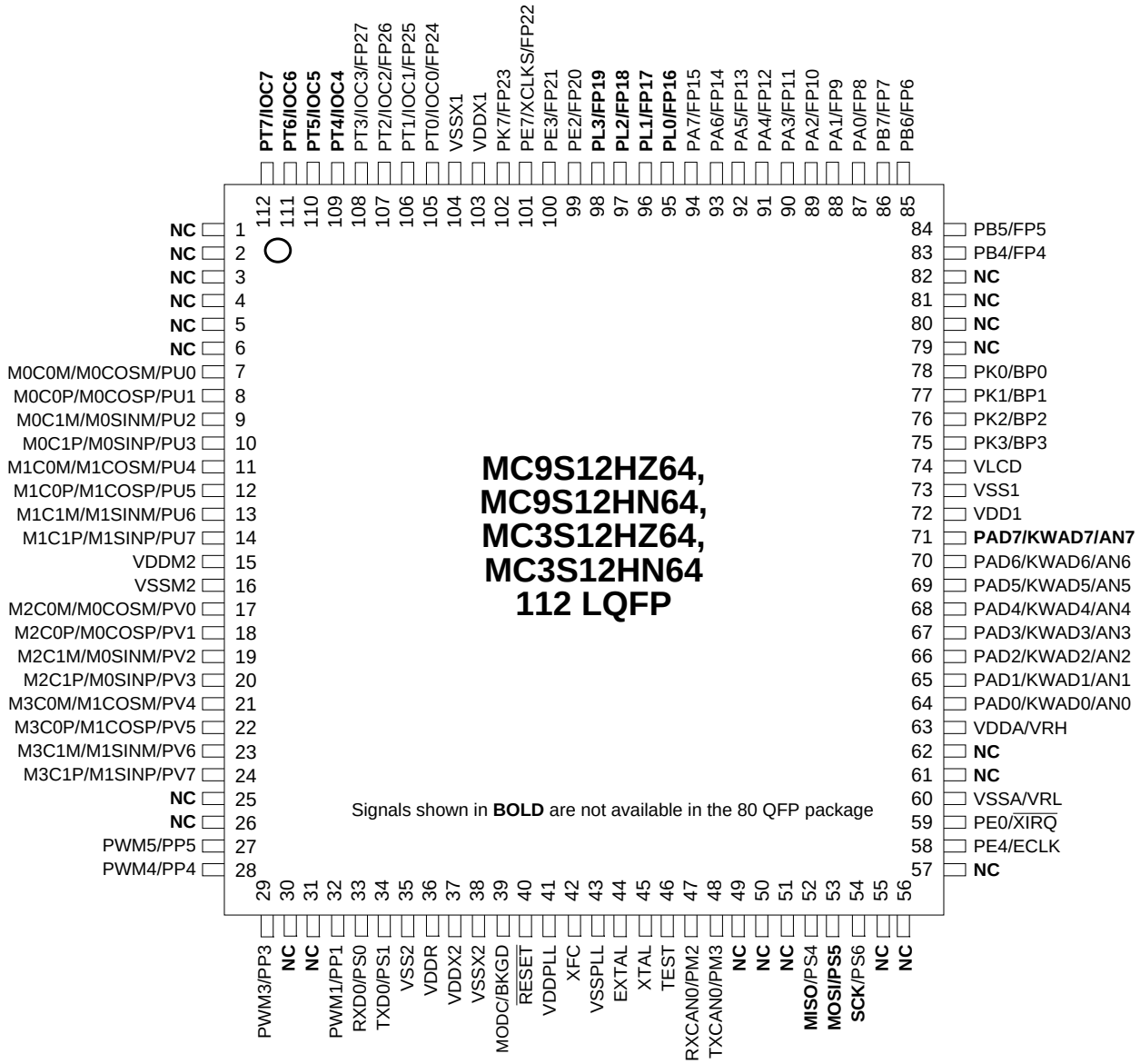


Figure 1-7. 112-Pin LQFP for MC9S12HZ(N)64 and MC3S12HZ(N)64

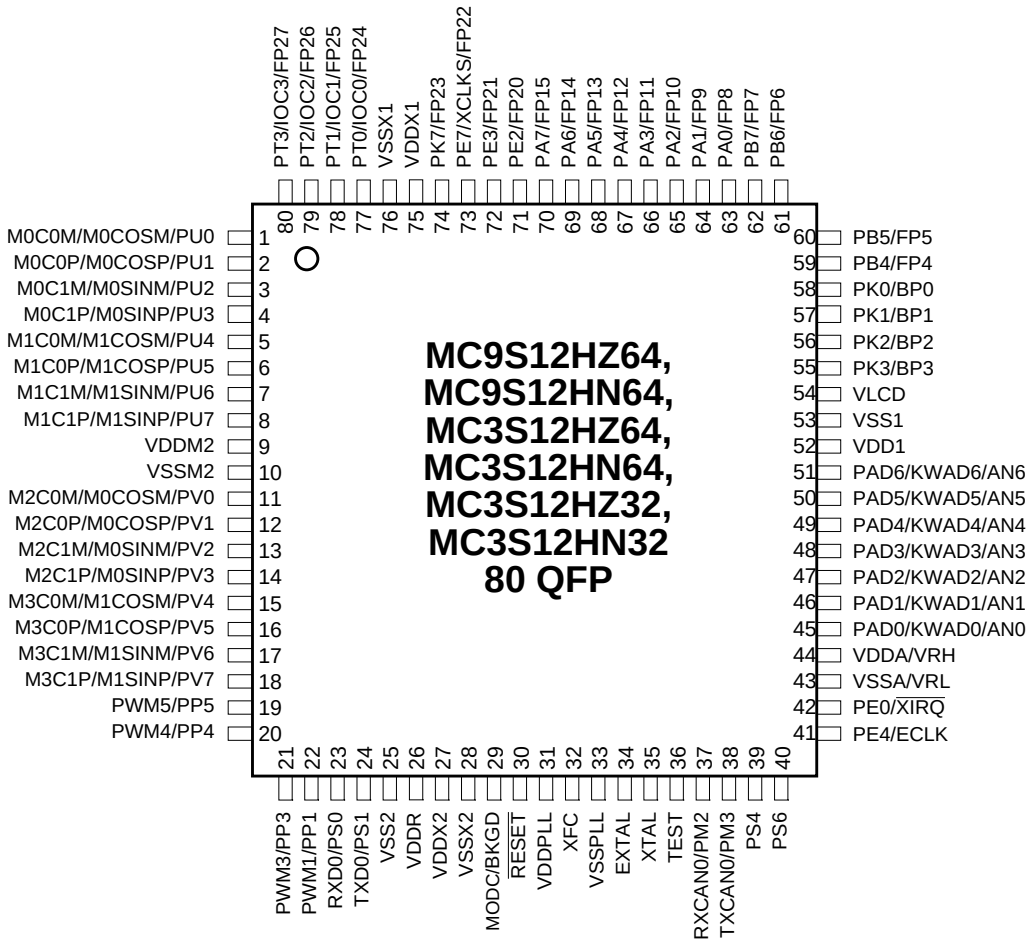


Figure 1-8. 80-Pin QFP for MC9S12HZ(N)64, MC3S12HZ(N)64 and MC3S12HZ(N)32

1.4.2 Signal Properties Summary

Table 1-8 summarizes all pin functions.

Table 1-8. Signal Properties

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Up Resistor		Description
					CTRL	Reset State	
EXTAL	—	—	—	V_{DDPLL}	NA	NA	Oscillator pins
XTAL	—	—	—	V_{DDPLL}	NA	NA	
$\overline{\text{RESET}}$	—	—	—	V_{DDX2}	None	None	External reset pin
TEST	—	—	—	V_{DDX2}	NA	NA	Test input - must be tied to VSS in all applications
XFC	—	—	—	V_{DDPLL}	NA	NA	PLL loop Filter
BKGD	$\overline{\text{TAGHI}}$	MODC	—	V_{DDX2}	Always Up	Up	Background debug, tag high, mode pin
PAD[7:0]	AN[7:0]	KWAD[7:0]	—	V_{DDA}	PERAD/ PPSAD	Disabled	Port AD I/O, Analog inputs (ATD), interrupts
PA[7:0]	FP[15:8]	ADDR[15:8]/ DATA[15:8]	—	V_{DDX1}	PUCR	Down	Port A I/O, multiplexed address/data
PB[7:0]	FP[7:0]	ADDR[7:0]/ DATA[7:0]	—	V_{DDX1}	PUCR	Down	Port B I/O, multiplexed address/data
PE7	FP22	XCLKS	NOACC	V_{DDX1}	PUCR	Down	Port E I/O, access, clock select, LCD driver
PE6	IPIPE1	MODB	—	V_{DDX2}	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, pipe status, mode input
PE5	IPIPE0	MODA	—	V_{DDX2}	While $\overline{\text{RESET}}$ pin is low: Down		Port E I/O, pipe status, mode input
PE4	ECLK	—	—	V_{DDX2}	PUCR	Down	Port E I/O, bus clock output
PE3	FP21	$\overline{\text{LSTRB}}$	$\overline{\text{TAGLO}}$	V_{DDX1}	PUCR	Down	Port E I/O, LCD driver, byte strobe, tag low
PE2	FP20	R/$\overline{\text{W}}$	—	V_{DDX1}	PUCR	Down	Port E I/O, R/$\overline{\text{W}}$ in expanded modes
PE1	$\overline{\text{IRQ}}$	—	—	V_{DDX2}	PUCR	Up	Port E input, maskable interrupt
PE0	$\overline{\text{XIRQ}}$	—	—	V_{DDX2}	PUCR	Up	Port E input, non-maskable interrupt
PK7	FP23	$\overline{\text{ECS}}$	ROMCTL	V_{DDX1}	PUCR	Down	Port K I/O, emulation chip select, ROM on enable
PK[3:0]	BP[3:0]	XADDR[17:14]	—	V_{DDX1}	PUCR	Down	Port K I/O, LCD driver, extended addresses
PL[7:4]	FP[31:28]	AN[15:12]	—	V_{DDA}	PERL/ PPSL	Down	Port L I/O, LCD drivers, analog inputs (ATD)
PL[3:0]	FP[19:16]	AN[11:8]	—	V_{DDX1}	PERL/ PPSL	Down	Port L I/O, LCD drivers, analog inputs (ATD)

Table 1-8. Signal Properties (continued)

Pin Name Function 1	Pin Name Function 2	Pin Name Function 3	Pin Name Function 4	Powered by	Internal Pull Up Resistor		Description
					CTRL	Reset State	
PM5	TXCAN1	—	—	V_{DDX2}	PERM/ PPSM	Disabled	Port M I/O, TX of CAN1
PM4	RXCAN1	—	—	V_{DDX2}			Port M I/O, RX of CAN1
PM3	TXCAN0	—	—	V_{DDX2}			Port M I/O, TX of CAN0
PM2	RXCAN0	—	—	V_{DDX2}			Port M I/O, RX of CAN0
PP5	PWM5	SCL	—	V_{DDX2}	PERP/ PPSP	Disabled	Port P I/O, PWM channel, SCL of IIC
PP4	PWM4	SDA	—	V_{DDX2}			Port P I/O, PWM channel, SDA of IIC
PP3	PWM3	—	—	V_{DDX2}			Port P I/O, PWM channel
PP2	PWM2	RXD1	—	V_{DDX2}			Port P I/O, PWM channel, RXD of SCI1
PP1	PWM1	—	—	V_{DDX2}			Port P I/O, PWM channel
PP0	PWM0	TXD1	—	V_{DDX2}			Port P I/O, PWM channel, TXD of SCI1
PS7	$\overline{SS}$	—	—	V_{DDX2}	PERS/ PPSS	Disabled	Port S I/O, $\overline{SS}$ of SPI
PS6	SCK	—	—	V_{DDX2}			Port S I/O, SCK of SPI
PS5	MOSI	—	—	V_{DDX2}			Port S I/O, MOSI of SPI
PS4	MISO	—	—	V_{DDX2}			Port S I/O, MISO of SPI
PS1	TXD0	—	—	V_{DDX2}			Port S I/O, TXD of SCI0
PS0	RXD0	—	—	V_{DDX2}			Port S I/O, RXD of SCI0
PT[7:4]	IOC[7:4]	—	—	V_{DDX1}	PERT/ PPST	Down	Port T I/O, Timer channels
PT[3:0]	IOC[3:0]	FP[27:24]	—	V_{DDX1}			Port T I/O, Timer channels, LCD driver
PU7	M1C1P	M1SINP	—	$V_{DDM1,2,3}$	PERU/ PPSU	Disabled	Port U I/O, motor1 coil nodes of MC or SSD1
PU6	M1C1M	M1SINM	—	$V_{DDM1,2,3}$			
PU5	M1C0P	M1COSP	—	$V_{DDM1,2,3}$			
PU4	M1C0M	M1COSM	—	$V_{DDM1,2,3}$			
PU3	M0C1P	M0SINP	—	$V_{DDM1,2,3}$			Port U I/O, motor 0 coil nodes of MC or SSD0
PU2	M0C1M	M0SINM	—	$V_{DDM1,2,3}$			
PU1	M0C0P	M0COSP	—	$V_{DDM1,2,3}$			
PU0	M0C0M	M0COSM	—	$V_{DDM1,2,3}$			
PV7	M3C1P	M3SINP	M1SINP	$V_{DDM1,2,3}$	PERV/ PPSV	Disabled	Port V I/O, motor 3 coil nodes of MC or SSD3
PV6	M3C1M	M3SINM	M1SINM	$V_{DDM1,2,3}$			
PV5	M3C0P	M3COSP	M1COSP	$V_{DDM1,2,3}$			
PV4	M3C0M	M3COSM	M1COSM	$V_{DDM1,2,3}$			
PV3	M2C1P	M2SINP	M0SINP	$V_{DDM1,2,3}$			Port V I/O, motor 2 coil nodes of MC or SSD2
PV2	M2C1M	M2SINM	M0SINM	$V_{DDM1,2,3}$			
PV1	M2C0P	M2COSP	M0COSP	$V_{DDM1,2,3}$			
PV0	M2C0M	M2COSM	M0COSM	$V_{DDM1,2,3}$			

Table 1-9. Power and Ground

Mnemonic	Nominal Voltage	Description
V_{LCD}	5.0 V	Voltage reference pin for the LCD driver.
V_{DD1}	2.5 V	Internal power and ground generated by internal regulator. These also allow an external source to supply the core V_{DD}/V_{SS} voltages and bypass the internal voltage regulator.
V_{SS1} V_{SS2}	0V	
V_{DDR}	5.0 V	External power and ground, supply to pin drivers and internal voltage regulator.
V_{SSR}	0 V	
V_{DDX1} V_{DDX2}	5.0 V	External power and ground, supply to pin drivers.
V_{SSX1} V_{SSX2}	0 V	
V_{DDA}	5.0 V	Operating voltage and ground for the analog-to-digital converter and the reference for the internal voltage regulator, allows the supply voltage to the A/D to be bypassed independently.
V_{SSA}	0 V	
V_{RH}	5.0 V	Reference voltage high for the ATD converter.
V_{RL}	0 V	Reference voltage low for the ATD converter.
V_{DDPLL}	2.5 V	Provides operating voltage and ground for the phased-locked Loop. This allows the supply voltage to the PLL to be bypassed independently. Internal power and ground generated by internal regulator.
V_{SSPLL}	0 V	
$V_{DDM1,2,3}$	5.0 V	Provides operating voltage and ground for motor 0, 1, 2 and 3.
$V_{SSM1,2,3}$	0 V	

NOTE

All V_{SS} pins must be connected together in the application. Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on MCU pin load.

1.5 Detailed Signal Descriptions

1.5.1 EXTAL, XTAL — Oscillator Pins

EXTAL and XTAL are the crystal driver and external clock pins. On reset all the device clocks are derived from the EXTAL input frequency. XTAL is the crystal output.

1.5.2 $\overline{\text{RESET}}$ — External Reset Pin

An active low bidirectional control signal, it acts as an input to initialize the MCU to a known start-up state, and an output when an internal MCU function causes a reset.

1.5.3 TEST — Test Pin

This pin is reserved for test.

NOTE

The TEST pin must be tied to V_{SS} in all applications.

1.5.4 XFC — PLL Loop Filter Pin

Dedicated pin used to create the PLL loop filter. Please ask your Freescale representative for the interactive application note to compute PLL loop filter elements. Any current leakage on this pin must be avoided.

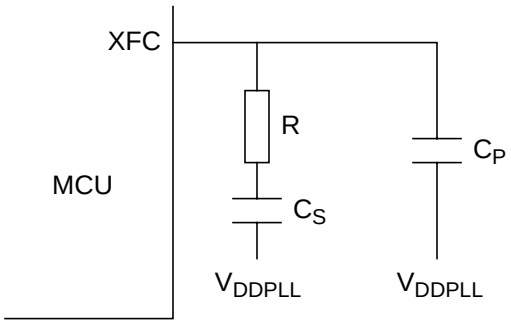


Figure 1-9. PLL Loop Filter Connections

1.5.5 BKGD / $\overline{\text{TAGHI}}$ / MODC — Background Debug, Tag High, and Mode Pin

The BKGD/$\overline{\text{TAGHI}}$/MODC pin is used as a pseudo-open-drain pin for the background debug communication. In MCU expanded modes of operation when instruction tagging is on, an input low on this pin during the falling edge of E-clock tags the high half of the instruction word being read into the instruction queue. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODC bit at the rising edge of $\overline{\text{RESET}}$.

1.5.6 Port Pins

1.5.6.1 PAD[7:0] / AN[7:0] / KWAD[7:0] — Port AD I/O Pins [7:0]

PAD7–PAD0 are general-purpose input or output pins and analog inputs for the analog-to-digital converter. They can be configured to generate an interrupt causing the MCU to exit STOP or WAIT mode.

1.5.6.2 PA[7:0] / FP[15:8] / ADDR[15:8] / DATA[15:8] — Port A I/O Pins

PA7–PA0 are general-purpose input or output pins. They can be configured as frontplane segment driver outputs FP15–FP8 of the LCD. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

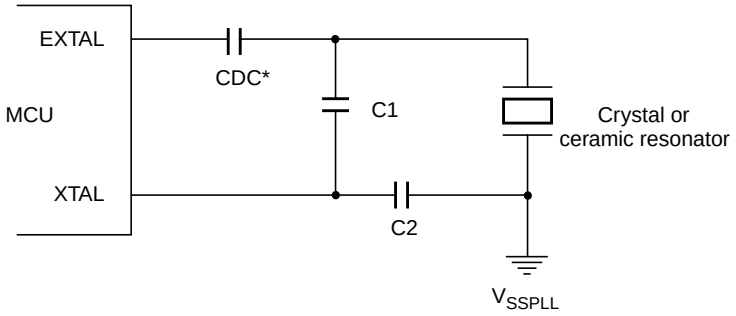
1.5.6.3 PB[7:0] / FP[7:0] / ADDR[7:0] / DATA[7:0] — Port B I/O Pins

PB7–PB0 are general-purpose input or output pins. They can be configured as frontplane segment driver outputs FP7–FP0 of the LCD. In MCU expanded modes of operation, these pins are used for the multiplexed external address and data bus.

1.5.6.4 PE7 / FP22 / XCLKS / NOACC — Port E I/O Pin 7

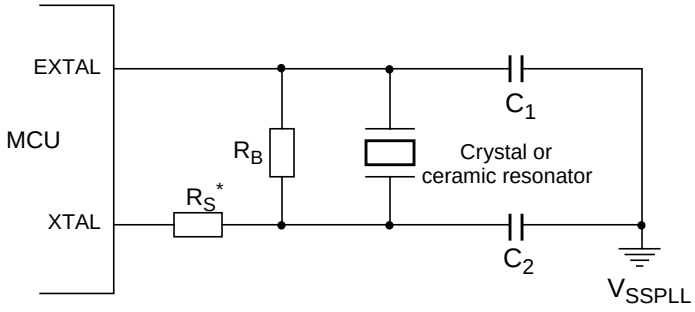
PE7 is a general-purpose input or output pin. It can be configured as frontplane segment driver output FP22 of the LCD module.

The XCLKS is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether Pierce oscillator/external clock circuitry is used. The state of this pin is latched at the rising edge of $\overline{\text{RESET}}$. If the input is a logic high the EXTAL pin is configured for an external clock drive or a Pierce Oscillator. If the input is a logic low a Colpitts oscillator circuit is configured on EXTAL and XTAL. Because this pin is an input with a pull-down device during reset, if the pin remains floating, the default configuration is a Colpitts oscillator circuit on EXTAL and XTAL.



* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal. Please contact the crystal manufacturer for crystal DC.

Figure 1-10. Colpitts Oscillator Connections (PE7 = 0)



* Rs can be zero (shorted) when use with higher frequency crystals. Refer to manufacturer's data.

Figure 1-11. Pierce Oscillator Connections (PE7 = 1)

1.5.6.5 PE6 / MODB / IPIPE1 — Port E I/O Pin 6

PE6 is a general-purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODB bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE1. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

1.5.6.6 PE5 / MODA / IPIPE0 — Port E I/O Pin 5

PE5 is a general-purpose input or output pin. It is used as a MCU operating mode select pin during reset. The state of this pin is latched to the MODA bit at the rising edge of $\overline{\text{RESET}}$. This pin is shared with the instruction queue tracking signal IPIPE0. This pin is an input with a pull-down device which is only active when $\overline{\text{RESET}}$ is low.

1.5.6.7 PE4 / ECLK — Port E I/O Pin 4

PE4 is a general-purpose input or output pin. It can be configured to drive the internal bus clock ECLK. ECLK can be used as a timing reference.

1.5.6.8 PE3 / FP21 / $\overline{\text{LSTRB}}$ / $\overline{\text{TAGLO}}$ — Port E I/O Pin 3

PE3 is a general-purpose input or output pin. It can be configured as frontplane segment driver output FP21 of the LCD module. In MCU expanded modes of operation, $\overline{\text{LSTRB}}$ is used for the low-byte strobe function to indicate the type of bus access and when instruction tagging is on, $\overline{\text{TAGLO}}$ is used to tag the low half of the instruction word being read into the instruction queue.

1.5.6.9 PE2 / FP20 / R/$\overline{W}$ — Port E I/O Pin 2

PE2 is a general-purpose input or output pin. It can be configured as frontplane segment driver output FP20 of the LCD module. In MCU expanded modes of operations, this pin performs the read/write output signal for the external bus. It indicates the direction of data on the external bus.

1.5.6.10 PE1 / $\overline{\text{IRQ}}$ — Port E Input Pin 1

PE1 is a general-purpose input pin and also the maskable interrupt request input that provides a means of applying asynchronous interrupt requests. If IRQ is enabled, this pin can wake up the MCU from stop or wait mode.

1.5.6.11 PE0 / $\overline{\text{XIRQ}}$ — Port E Input Pin 0

PE0 is a general-purpose input pin and also the non-maskable interrupt request input that provides a means of applying asynchronous interrupt requests. This can wake up the MCU from stop or wait mode.

1.5.6.12 PK7 / FP23 / $\overline{\text{ECS}}$ / ROMCTL — Port K I/O Pin 7

PK7 is a general-purpose input or output pin. It can be configured as frontplane segment driver output FP23 of the LCD module.

During MCU expanded modes of operation, this pin is used as the emulation chip select output ($\overline{\text{ECS}}$). During MCU expanded modes of operation, this pin is used to enable the Flash EEPROM memory in the memory map (ROMCTL). At the rising edge of $\overline{\text{RESET}}$, the state of this pin is latched to the ROMON bit.

For all other modes the reset state of the ROMON bit is as follows:

Special single: ROMCTL = 1

Normal single: ROMCTL = 1

Emulation expanded wide: ROMCTL = 0

Emulation expanded narrow: ROMCTL = 0

Special test: ROMCTL = 0

Peripheral test: ROMCTL = 1

1.5.6.13 PK[3:0] / BP[3:0] / XADDR[17:14] — Port K I/O Pins [3:0]

PK3–PK0 are general-purpose input or output pins. They can be configured as backplane segment driver outputs BP3–BP0 of the LCD module. In MCU expanded modes of operation, these pins provide the expanded address XADDR[17:14] for the external bus.

1.5.6.14 PL[7:4] / FP[31:28] / AN[15:12] — Port L I/O Pins [7:4]

PL7–PL4 are general-purpose input or output pins. They can be configured as frontplane segment driver outputs FP31–FP28 of the LCD module or analog inputs for the analog-to-digital converter.

1.5.6.15 PL[3:0] / FP[19:16] / AN[11:8] — Port L I/O Pins [3:0]

PL3–PL0 are general-purpose input or output pins. They can be configured as frontplane segment driver outputs FP19–FP16 of the LCD module or analog inputs for the analog-to-digital converter.

1.5.6.16 PM5 / TXCAN1 — Port M I/O Pin 5

PM5 is a general-purpose input or output pin. It can be configured as the transmit pin TXCAN1 of the scalable controller area network controller 1 (CAN1)

1.5.6.17 PM4 / RXCAN1 — Port M I/O Pin 4

PM4 is a general-purpose input or output pin. It can be configured as the receive pin RXCAN1 of the scalable controller area network controller 1 (CAN1)

1.5.6.18 PM3 / TXCAN0 — Port M I/O Pin 3

PM3 is a general-purpose input or output pin. It can be configured as the transmit pin TXCAN0 of the scalable controller area network controller 0 (CAN0)

1.5.6.19 PM2 / RXCAN0 — Port M I/O Pin 2

PM2 is a general-purpose input or output pin. It can be configured as the receive pin RXCAN0 of the scalable controller area network controller 0 (CAN0)

1.5.6.20 PP5 / PWM5 — Port P I/O Pin 5

PP5 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM5 or the serial clock pin SCL of the inter-IC bus interface (IIC).

1.5.6.21 PP4 / PWM4 — Port P I/O Pin 4

PP4 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM4 or the serial data pin SDA of the inter-IC bus interface (IIC).

1.5.6.22 PP3 / PWM3 — Port P I/O Pin 3

PP3 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM3.

1.5.6.23 PP2 / PWM2 — Port P I/O Pin 2

PP2 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM2 or the receive pin RXD1 of the serial communication interface 1 (SCI1).

1.5.6.24 PP1 / PWM1 — Port P I/O Pin 1

PP1 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM1.

1.5.6.25 PP0 / PWM0 — Port P I/O Pin 0

PP0 is a general-purpose input or output pin. It can be configured as pulse width modulator (PWM) channel output PWM0 or the transmit pin TXD1 of the serial communication interface 1 (SCI1).

1.5.6.26 PS7 / $\overline{SS}$ — Port S I/O Pin 7

PS7 is a general-purpose input or output pin. It can be configured as slave select pin $\overline{SS}$ of the serial peripheral interface (SPI).

1.5.6.27 PS6 / SCK — Port S I/O Pin 6

PS6 is a general-purpose input or output pin. It can be configured as serial clock pin SCK of the serial peripheral interface (SPI).

1.5.6.28 PS5 / MOSI — Port S I/O Pin 5

PS5 is a general-purpose input or output pin. It can be configured as the master output (during master mode) or slave input (during slave mode) pin MOSI of the serial peripheral interface (SPI).

1.5.6.29 PS4 / MISO — Port S I/O Pin 4

PS4 is a general-purpose input or output pin. It can be configured as master input (during master mode) or slave output (during slave mode) pin MISO for the serial peripheral interface (SPI).

1.5.6.30 PS1 / TXD0 — Port S I/O Pin 1

PS1 is a general-purpose input or output pin. It can be configured as transmit pin TXD0 of the serial communication interface 0 (SCI0).

1.5.6.31 PS0 / RXD0 — Port S I/O Pin 0

PS0 is a general-purpose input or output pin. It can be configured as receive pin RXD0 of the serial communication interface 0 (SCI0).

1.5.6.32 PT[7:4] / IOC[7:4] — Port T I/O Pins [7:4]

PT7–PT4 are general-purpose input or output pins. They can be configured as input capture or output compare pins IOC7–IOC4 of the timer (TIM).

1.5.6.33 PT[3:0] / IOC[3:0] / FP[27:24] — Port T I/O Pins [3:0]

PT3–PT0 are general-purpose input or output pins. They can be configured as input capture or output compare pins IOC3–IOC0 of the timer (TIM). They can be configured as frontplane segment driver outputs FP27–FP24 of the LCD module.

1.5.6.34 PU[7:4] / M1C1(SIN)P, M1C1(SIN)M, M1C0(COS)P, M1C0(COS)M — Port U I/O Pins [7:4]

PU7–PU4 are general-purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. These pins interface to the coils of motor 1.

1.5.6.35 PU[3:0] / M0C1(SIN)P, M0C1(SIN)M, M0C0(COS)P, M0C0(COS)M — Port U I/O Pins [3:0]

PU3–PU0 are general-purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. These pins interface to the coils of motor 0.

1.5.6.36 PV[7:4] / M3C1(SIN)P, M3C1(SIN)M, M3C0(COS)P, M3C0(COS)M — Port V I/O Pins [7:4]

PV7–PV4 are general-purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. These pins interface to the coils of motor 3.

1.5.6.37 PV[3:0] / M2C1(SIN)P, M2C1(SIN)M, M2C0(COS)P, M2C0(COS)M — Port V I/O Pins [3:0]

PV3–PV0 are general-purpose input or output pins. They can be configured as high current PWM output pins which can be used for motor drive or to measure the back EMF to calibrate the pointer reset position. These pins interface to the coils of motor 2.

1.5.7 Power Supply Pins

MC9S12HZ256 power and ground pins are described below.

NOTE

All V_{SS} pins must be connected together in the application (See Appendix B, “PCB Layout Guidelines”).

Because fast signal transitions place high, short-duration current demands on the power supply, use bypass capacitors with high-frequency characteristics and place them as close to the MCU as possible. Bypass requirements depend on how heavily the MCU pins are loaded (Table B-1).

1.5.7.1 V_{DDR} — External Power Pin

V_{DDR} is the power supply pin for the internal voltage regulator.

1.5.7.2 V_{DDX1}, V_{DDX2}, V_{SSX1}, V_{SSX2} — External Power and Ground Pins

V_{DDX1}, V_{DDX2}, V_{SSX1} and V_{SSX2} are the power supply and ground pins for input/output drivers.V_{DDX1} and V_{DDX2} as well as V_{SSX1} and V_{SSX2} are not internally connected.

1.5.7.3 V_{DD1}, V_{SS1}, V_{SS2} — Internal Logic Power Pins

V_{DD1}, V_{SS1} and V_{SS2} are the internal logic power and ground pins and related to the voltage regulator output. These pins serve as connection points for filter capacitors. V_{SS1} and V_{SS2} are internally connected.

NOTE

No load allowed except for bypass capacitors.

1.5.7.4 V_{DDA}, V_{SSA} — Power Supply Pins for ATD and VREG

V_{DDA}, V_{SSA} are the power supply and ground pins for the voltage regulator and the analog-to-digital converter.

1.5.7.5 V_{DDM1}, V_{DDM2}, V_{DDM3} — Power Supply Pins for Motor 0 to 3

V_{DDM1}, V_{DDM2} and V_{DDM3} are the supply pins for the ports U and V. V_{DDM1}, V_{DDM2} and V_{DDM3} are internally connected.

1.5.7.6 V_{SSM1}, V_{SSM2}, V_{SSM3} — Ground Pins for Motor 0 to 3

V_{SSM1}, V_{SSM2} and V_{SSM3} are the ground pins for the ports U and V. V_{SSM1}, V_{SSM2} and V_{SSM3} are internally connected.

1.5.7.7 V_{LCD} — Power Supply Reference Pin for LCD driver

V_{LCD} is the voltage reference pin for the LCD driver. Adjusting the voltage on this pin will change the display contrast.

1.5.7.8 V_{RH}, V_{RL} — ATD Reference Voltage Input Pins

V_{RH} and V_{RL} are the voltage reference pins for the analog-to-digital converter.

1.5.7.9 V_{DDPLL}, V_{SSPLL} — Power Supply Pins for PLL

V_{DDPLL} and V_{SSPLL} are the PLL supply pins and serve as connection points for external loop filter components.

NOTE

No load allowed except for bypass capacitors.

1.6 System Clock Description

The clock and reset generator (CRG) provides the internal clock signals for the core and all peripheral modules. Figure 1-12 shows the clock connections from the CRG to all modules.

Consult the CRG block description chapter for details on clock generation.

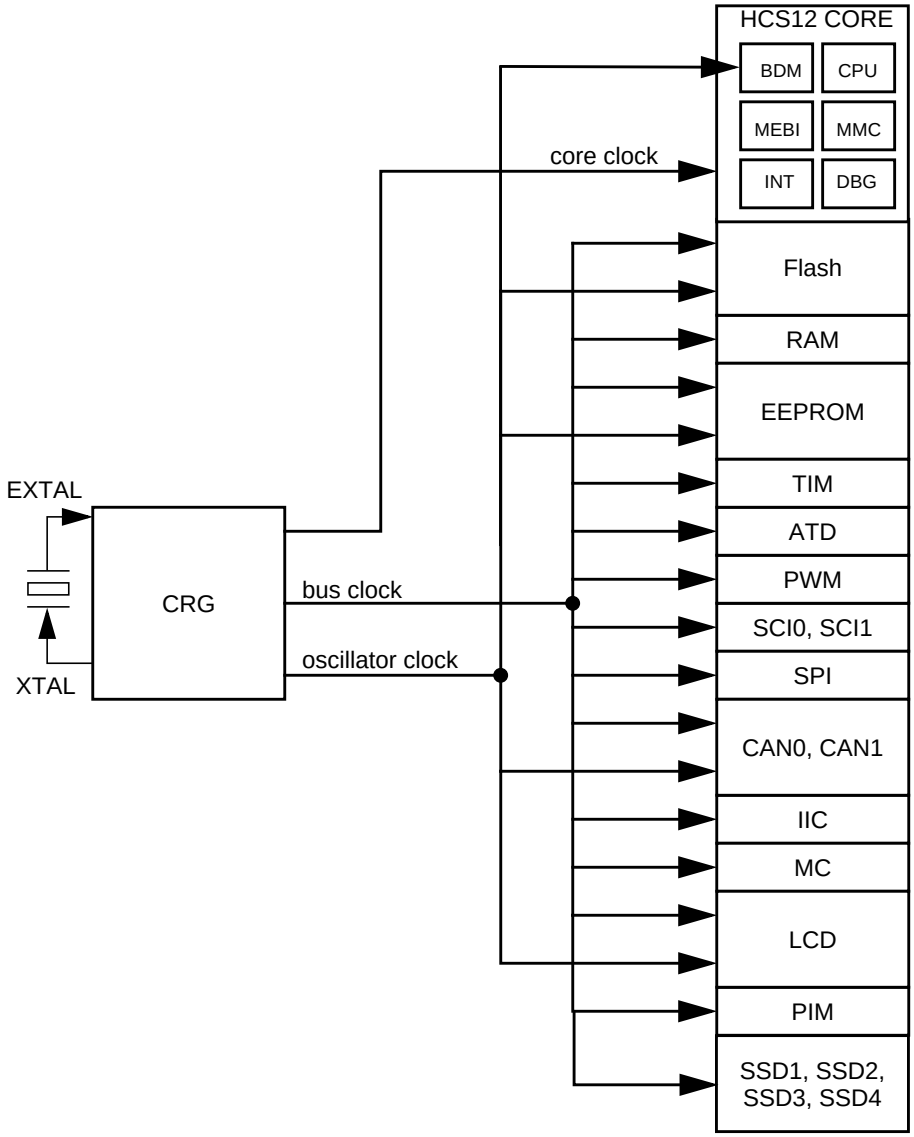


Figure 1-12. Clock Connections

1.7 Modes of Operation

Eight possible modes determine the operating configuration of the MC9S12HZ256. Each mode has an associated default memory map and external bus configuration.

Three low power modes exist for the device.

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (Table 1-10). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 1-10. Mode Selection

MODC	MODB	MODA	Mode Description
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	Emulation Expanded Narrow, BDM allowed
X	1	0	Reserved for factory test
0	1	1	Emulation Expanded Wide, BDM allowed
1	0	0	Normal Single Chip, BDM allowed
1	0	1	Normal Expanded Narrow, BDM allowed
1	1	1	Normal Expanded Wide, BDM allowed

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of port E are not mode dependent. Bit 1 of port E is a general-purpose input or the $\overline{\text{IRQ}}$ interrupt input. $\overline{\text{IRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of port E is a general-purpose input or the $\overline{\text{XIRQ}}$ interrupt input. $\overline{\text{XIRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as pull-down select inputs during reset and high-impedance select inputs after reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

1.7.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

1.7.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of ports A, B, E and K are general-purpose I/O pins initially configured with internal pull-downs enabled, except port E bits 1 and 0 which are available as general-purpose input only pins with internal pull-ups enabled.

The pins associated with port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

1.7.1.2 Normal Expanded Wide Mode

All pins of ports A, B, E and K are general-purpose I/O pins initially configured with internal pull-downs enabled, except port E bits 1 and 0 which are available as general-purpose input only pins with internal pull-ups enabled.

In expanded wide modes, ports A and B are configured as a 16-bit multiplexed address and data bus and port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general-purpose I/O pins. Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure port E pins to act as bus control outputs instead of general-purpose I/O pins.

It is possible to enable the pipe status signals on port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The port E bit 2 pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can remain a general-purpose I/O pin.

The port E bit 3 pin can be reconfigured as the $\overline{\text{LSTRB}}$ bus control signal by writing “1” to the LSTRE bit in PEAR. The default condition of this pin is a general-purpose input because the $\overline{\text{LSTRB}}$ function is not needed in all expanded wide applications.

The port E bit 4 pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. The E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

1.7.1.3 Normal Expanded Narrow Mode

This mode is used for lower cost production systems that use 8-bit wide external EPROMs or RAMs. Such systems take extra bus cycles to access 16-bit locations but this may be preferred over the extra cost of additional external memory devices.

Ports A and B are configured as a 16-bit address bus and port A is multiplexed with data. Internal visibility is not available in this mode because the internal cycles would need to be split into two 8-bit cycles.

Because the PEAR register can only be written one time in this mode, use care to set all bits to the desired states during the single allowed write.

The PE3/$\overline{\text{LSTRB}}$ pin is always a general-purpose I/O pin in normal expanded narrow mode. Although it is possible to write the LSTRE bit in PEAR to “1” in this mode, the state of LSTRE is overridden and port E bit 3 cannot be reconfigured as the $\overline{\text{LSTRB}}$ output.

It is possible to enable the pipe status signals on port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. LSTRB would also be needed to fully understand system activity. Development systems where pipe status signals are monitored would typically use special expanded wide mode or occasionally special expanded narrow mode.

The PE4/ECLK pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

The PE2/R/W pin is initially configured as a general-purpose input with a pull-up but this pin can be reconfigured as the R/$\overline{\text{W}}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded narrow system includes external devices that can be written such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can remain a general-purpose I/O pin.

1.7.1.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or special narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E, R/$\overline{\text{W}}$, and $\overline{\text{LSTRB}}$ are configured as bus control outputs and internal visibility is off (IVIS = 0), E will remain low for the cycle, R/$\overline{\text{W}}$ will remain high, and address, data and the $\overline{\text{LSTRB}}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS = 1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{\text{W}}$ will remain high, data will maintain its previous state, and address and $\overline{\text{LSTRB}}$ pins will be updated with the internal value. During CPU no access cycles when the

BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

1.7.1.5 Emulation Expanded Wide Mode

In expanded wide modes, ports A and B are configured as a 16-bit multiplexed address and data bus and port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general-purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

1.7.1.6 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e., PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if IVIS = 1.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general-purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in special mode are restricted.

1.7.2 Special Operating Modes

1.7.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull-downs enabled; however, writing

to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the port E pins (except PE4/ECLK) are initially configured as general-purpose high-impedance inputs with pull-downs enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK = 0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

1.8 Security

The device will make available a security feature preventing the unauthorized read and write of the memory contents. This feature allows:

- Protection of the contents of FLASH
- Protection of the contents of EEPROM
- Operation in single-chip mode
- Operation from external memory with internal FLASH and EEPROM disabled

The user must be reminded that part of the security must lie with the user's code. An extreme example would be user's code that dumps the contents of the internal program. This code would defeat the purpose of security. At the same time the user may also wish to put a back door in the user's program. An example of this is the user downloads a key through the SCI which allows access to a programming routine that updates parameters stored in EEPROM.

1.8.1 Securing the Microcontroller

After the user has programmed the FLASH and EEPROM (if desired), the part can be secured by programming the security bits located in the FLASH module. These non-volatile bits will keep the part secured through resetting the part and through powering down the part.

The security byte resides in a portion of the Flash array.

Check the Flash block description chapter for more details on the security configuration.

1.8.2 Operation of the Secured Microcontroller

1.8.2.1 Normal Single Chip Mode

This will be the most common usage of the secured part. Everything will appear the same as if the part was not secured with the exception of BDM operation. The BDM operation will be blocked.

1.8.2.2 Executing from External Memory

The user may wish to execute from external space with a secured microcontroller. This is accomplished by resetting directly into expanded mode. The internal FLASH and EEPROM will be disabled. BDM operations will be blocked.

1.8.3 Unsecuring the Microcontroller

In order to unsecure the microcontroller, the internal FLASH and EEPROM must be erased. This can be done through an external program in expanded mode.

After the user has erased the FLASH and EEPROM, the part can be reset into special single chip mode. This invokes a program that verifies the erasure of the internal FLASH and EEPROM. After this program completes, the user can erase and program the FLASH security bits to the unsecured state. This is generally done through the BDM, but the user could also change to expanded mode (by writing the mode bits through the BDM) and jumping to an external program (again through BDM commands). Note that if the part goes through a reset before the security bits are reprogrammed to the unsecure state, the part will be secured again.

1.9 Low Power Modes

Consult the respective block description chapter for information on the module behavior in stop, pseudo stop, and wait mode.

1.10 Resets and Interrupts

Consult the Exception Processing section of the CPU12 Reference Manual for information on resets and interrupts. Both local masking and CCR masking are included as listed in Table 1-11. System resets can be generated through external control of the $\overline{\text{RESET}}$ pin, through the clock and reset generator module CRG or through the low voltage reset (LVR) generator of the voltage regulator module. Refer to the CRG and VREG block description chapters for detailed information on reset generation.

1.10.1 Vectors

Table 1-11 lists interrupt sources and vectors in default order of priority.

Table 1-11. Interrupt Vector Locations

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
0xFFFE, 0xFFFF	External Reset, Power On Reset or Low Voltage Reset (see CRG Flags Register to determine reset source)	None	None	—
0xFFFC, 0xFFFD	Clock Monitor fail reset	None	COPCTL (CME, FCME)	—
0xFFFA, 0xFFFB	COP failure reset	None	COP rate select	—
0xFFF8, 0xFFF9	Unimplemented instruction trap	None	None	—
0xFFF6, 0xFFF7	SWI	None	None	—
0xFFF4, 0xFFF5	XIRQ	X-Bit	None	—

Table 1-11. Interrupt Vector Locations (continued)

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
0xFFF2, 0xFFF3	IRQ	I-Bit	INTCR (IRQEN)	0xF2
0xFFF0, 0xFFF1	Real Time Interrupt	I-Bit	RTICTL (RTIE)	0xF0
0xFFEE, 0xFFEF	Timer channel 0	I-Bit	TIE (C0I)	0xEE
0xFFEC, 0xFFED	Timer channel 1	I-Bit	TIE (C1I)	0xEC
0xFFEA, 0xFFEB	Timer channel 2	I-Bit	TIE (C2I)	0xEA
0xFFE8, 0xFFE9	Timer channel 3	I-Bit	TIE (C3I)	0xE8
0xFFE6, 0xFFE7	Timer channel 4	I-Bit	TIE (C4I)	0xE6
0xFFE4, 0xFFE5	Timer channel 5	I-Bit	TIE (C5I)	0xE4
0xFFE2, 0xFFE3	Timer channel 6	I-Bit	TIE (C6I)	0xE2
0xFFE0, 0xFFE1	Timer channel 7	I-Bit	TIE (C7I)	0xE0
0xFFDE, 0xFFDF	Timer overflow	I-Bit	TSCR2 (TOI)	0xDE
0xFFDC, 0xFFDD	Pulse accumulator A overflow	I-Bit	PACTL (PAOVI)	0xDC
0xFFDA, 0xFFDB	Pulse accumulator input edge	I-Bit	PACTL (PAI)	0xDA
0xFFD8, 0xFFD9	SPI	I-Bit	SPCR1 (SPIE)	0xD8
0xFFD6, 0xFFD7	SCI0	I-Bit	SC0CR2 (TIE, TCIE, RIE, ILIE)	0xD6
0xFFD4, 0xFFD5	SCI1	I-Bit	SC1CR2 (TIE, TCIE, RIE, ILIE)	0xD4
0xFFD2, 0xFFD3	ATD	I-Bit	ATDCTL2 (ASCIE)	0xD2
0xFFD0, 0xFFD1	Reserved	I-Bit	Reserved	0xD0
0xFFCE, 0xFFCF	Reserved	I-Bit	Reserved	0xCE
0xFFCC, 0xFFCD	Reserved	I-Bit	Reserved	0xCC
0xFFCA, 0xFFCB	Reserved	I-Bit	Reserved	0xCA
0xFFC8, 0xFFC9	Port AD	I-Bit	PTADIF (PTADIE)	0xC8
0xFFC6, 0xFFC7	CRG PLL lock	I-Bit	CRGINT (LOCKIE)	0xC6
0xFFC4, 0xFFC5	CRG Self Clock Mode	I-Bit	CRGINT (SCMIE)	0xC4
0xFFC2, 0xFFC3	Reserved	I-Bit	Reserved	0xC2
0xFFC0, 0xFFC1	IIC Bus	I-Bit	IBCR (IBIE)	0xC0
0xFFBE, 0xFFBF	Reserved	I-Bit	Reserved	0xBE
0xFFBC, 0xFFBD	Reserved	I-Bit	Reserved	0xBC
0xFFBA, 0xFFBB	EEPROM	I-Bit	EECTL (CCIE, CBEIE)	0xBA
0xFFB8, 0xFFB9	FLASH	I-Bit	FCTL (CCIE, CBEIE)	0xB8
0xFFB6, 0xFFB7	CAN0 wake-up	I-Bit	CAN0RIER (WUPIE)	0xB6
0xFFB4, 0xFFB5	CAN0 errors	I-Bit	CAN0RIER (CSCIE, OVRIE)	0xB4
0xFFB2, 0xFFB3	CAN0 receive	I-Bit	CAN0RIER (RXFIE)	0xB2
0xFFB0, 0xFFB1	CAN0 transmit	I-Bit	CAN0TIER (TXEIE[2:0])	0xB0
0xFFAE, 0xFFAF	CAN1 wake-up	I-Bit	CAN1RIER (WUPIE)	0xAE
0xFFAC, 0xFFAD	CAN1 errors	I-Bit	CAN1RIER (CSCIE, OVRIE)	0xAC
0xFFAA, 0xFFAB	CAN1 receive	I-Bit	CAN1RIER (RXFIE)	0xAA

Table 1-11. Interrupt Vector Locations (continued)

Vector Address	Interrupt Source	CCR Mask	Local Enable	HPRIO Value to Elevate
0xFFA8, 0xFFA9	CAN1 transmit	I-Bit	CAN1TIER (TXEIE[2:0])	0xA8
0xFFA6, 0xFFA7	Reserved	I-Bit	Reserved	0xA6
0xFFA4, 0xFFA5	Reserved	I-Bit	Reserved	0xA4
0xFFA2, 0xFFA3	Reserved	I-Bit	Reserved	0xA2
0xFFA0, 0xFFA1	SSD0	I-Bit	MDC0CTL (MCZIE, AOVIE)	0xA0
0xFF9E, 0xFF9F	SSD1	I-Bit	MDC1CTL (MCZIE, AOVIE)	0x9E
0xFF9C, 0xFF9D	SSD2	I-Bit	MDC2CTL (MCZIE, AOVIE)	0x9C
0xFF9A, 0xFF9B	SSD3	I-Bit	MDC3CTL (MCZIE, AOVIE)	0x9A
0xFF98, 0xFF99	Reserved	I-Bit	Reserved	0x98
0xFF96, 0xFF97	Motor Control Timer Overflow	I-Bit	MCCTL1 (MCOCIE)	0x96
0xFF94, 0xFF95	Reserved	I-Bit	Reserved	0x94
0xFF92, 0xFF93	Reserved	I-Bit	Reserved	0x92
0xFF90, 0xFF91	Reserved	I-Bit	Reserved	0x90
0xFF8E, 0xFF8F	Reserved	I-Bit	Reserved	0x8E
0xFF8C, 0xFF8D	PWM Emergency Shutdown	I-Bit	PWMSDN(PWMIE)	0x8C
0xFF8A, 0xFF8B	VREG Low Voltage Interrupt	I-Bit	VREGCTRL (LVIE)	0x8A
0xFF80–0xFF89	Reserved	I-Bit	Reserved	0x80–0x88

1.10.2 Resets

Resets are a subset of the interrupts featured in Table 1-12. The different sources capable of generating a system reset are summarized in Table 1-12.

Table 1-12. Reset Summary

Reset	Priority	Source	Vector
Power-on Reset	1	CRG Module	0xFFFE, 0xFFFF
External Reset	1	RESET pin	0xFFFE, 0xFFFF
Low Voltage Reset	1	VREG Module	0xFFFE, 0xFFFF
Clock Monitor Reset	2	CRG Module	0xFFFC, 0xFFFD
COP Watchdog Reset	3	CRG Module	0xFFFA, 0xFFFB

1.10.3 Effects of Reset

When a reset occurs, MCU registers and control bits are changed to known start-up states. Refer to the respective module block description chapters for register reset states. MC mode dependent pin configuration of port A, B and E out of reset.

Refer to the PIM block description chapter for reset configurations of all peripheral module ports.

Refer to Table 1-1 for locations of the memories depending on the operating mode after reset.

The RAM array is not automatically initialized out of reset.

Chapter 2
256 Kbyte Flash Module (FTS256K2V1)

2.1 Introduction

This document describes the FTS256K2 module that includes a 256 Kbyte Flash (nonvolatile) memory. The Flash memory may be read as either bytes, aligned words, or misaligned words. Read access time is one bus cycle for bytes and aligned words, and two bus cycles for misaligned words.

The Flash memory is ideal for program and data storage for single-supply applications allowing for field reprogramming without requiring external voltage sources for program or erase. Program and erase functions are controlled by a command driven interface. The Flash module supports both block erase and sector erase. An erased bit reads 1 and a programmed bit reads 0. The high voltage required to program and erase the Flash memory is generated internally. It is not possible to read from a Flash block while it is being erased or programmed.

CAUTION

A Flash word must be in the erased state before being programmed.
Cumulative programming of bits within a Flash word is not allowed.

2.1.1 Glossary

Banked Register — A memory-mapped register operating on one Flash block which shares the same register address as the equivalent registers for the other Flash blocks. The active register bank is selected by the BKSEL bit in the FCNFG register.

Command Write Sequence — A three-step MCU instruction sequence to execute built-in algorithms (including program and erase) on the Flash memory.

Common Register — A memory-mapped register which operates on all Flash blocks.

2.1.2 Features

- 256 Kbytes of Flash memory comprised of two 128 Kbyte blocks with each block divided into 128 sectors of 1024 bytes
- Automated program and erase algorithm
- Interrupts on Flash command completion, command buffer empty
- Fast sector erase and word program operation
- 2-stage command pipeline for faster multi-word program times
- Sector erase abort feature for critical interrupt response
- Flexible protection scheme to prevent accidental program or erase

- Single power supply for all Flash operations including program and erase
- Security feature to prevent unauthorized access to the Flash memory
- Code integrity check using built-in data compression

2.1.3 Modes of Operation

Program, erase, erase verify, and data compress operations (please refer to Section 2.4.1 for details).

2.1.4 Block Diagram

A block diagram of the Flash module is shown in Figure 2-1.

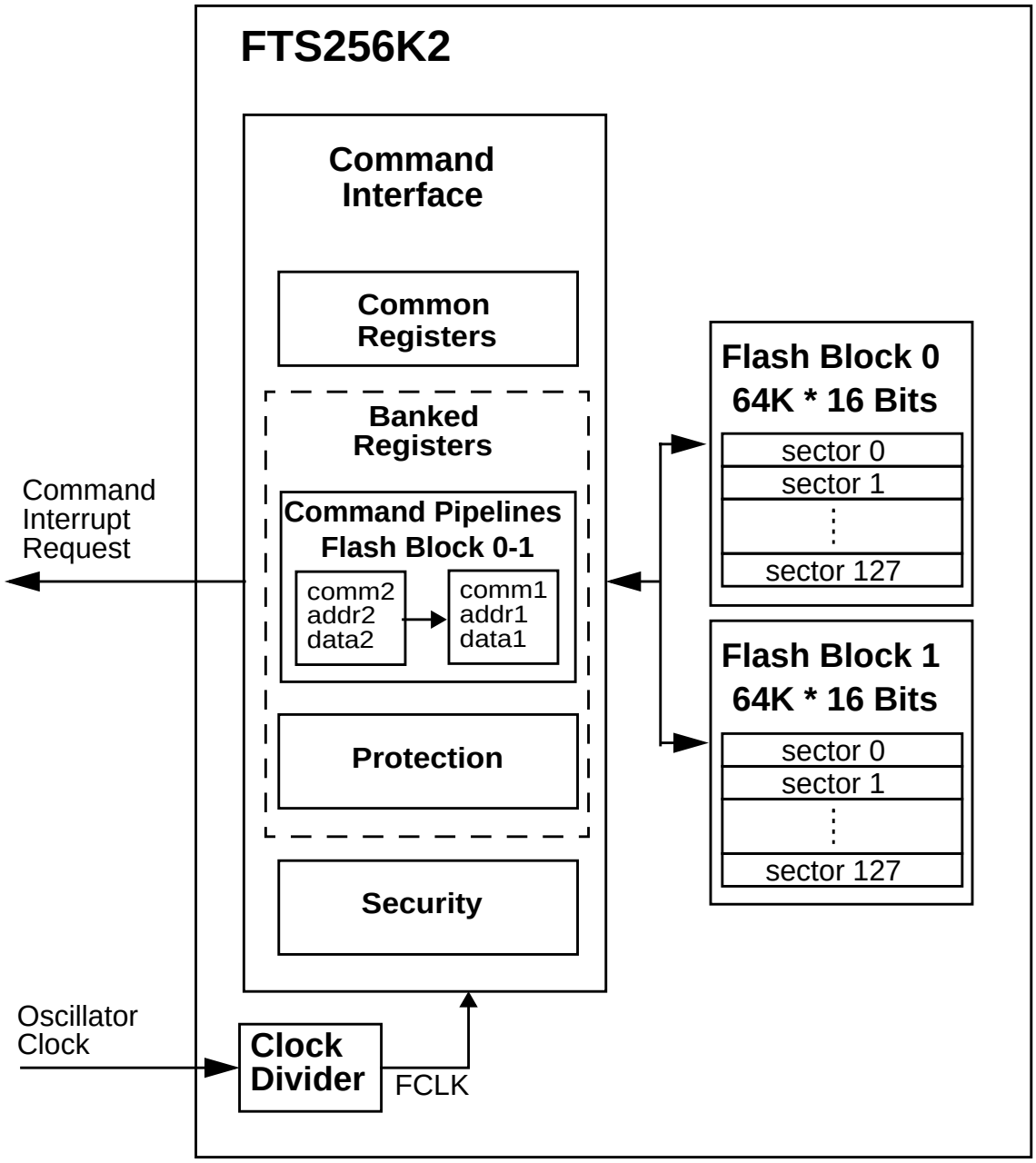


Figure 2-1. FTS256K2 Block Diagram

2.2 External Signal Description

The Flash module contains no signals that connect off-chip.

2.3 Memory Map and Register Definition

This subsection describes the memory map and registers for the Flash module.

2.3.1 Module Memory Map

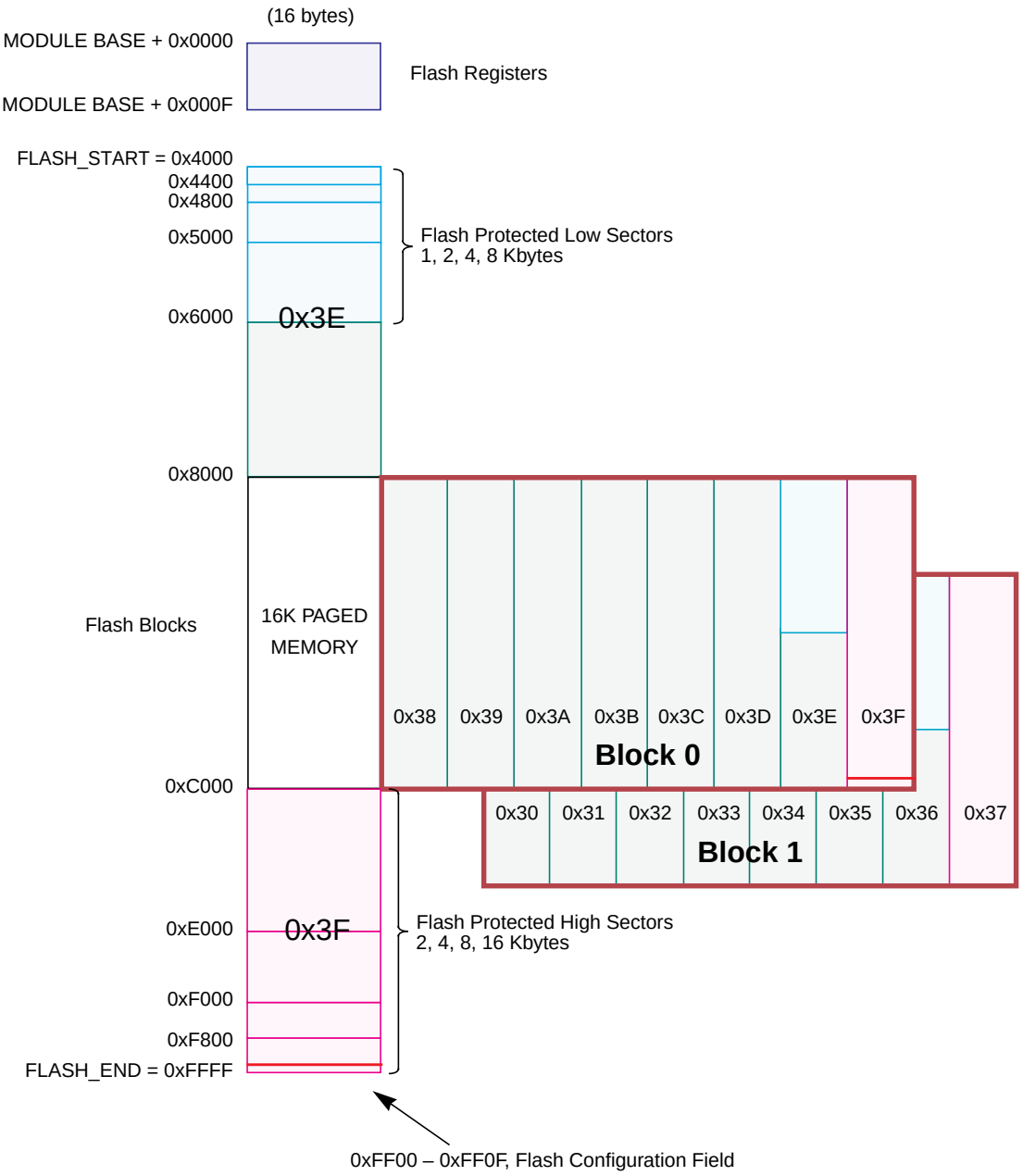
The Flash memory map is shown in Figure 2-2. The HCS12 architecture places the Flash memory addresses between 0x4000 and 0xFFFF which corresponds to three 16-Kbyte pages. The content of the HCS12 core PPAGE register is used to map the logical middle page ranging from address 0x8000 to 0xBFFF to any physical 16 Kbyte page in the Flash memory. By placing 0x3E or 0x3F in the HCS12 Core PPAGE register, the associated 16 Kbyte pages appear twice in the MCU memory map.

The FPROT register, described in Section 2.3.2.5, “Flash Protection Register (FPROT)”, can be set to globally protect a Flash block. However, three separate memory regions, one growing upward from the first address in the next-to-last page in the Flash block (called the lower region), one growing downward from the last address in the last page in the Flash block (called the higher region), and the remaining addresses in the Flash block, can be activated for protection. The Flash locations of these protectable regions are shown in Table 2-2. The higher address region of Flash block 0 is mainly targeted to hold the boot loader code because it covers the vector space. The lower address region of any Flash block can be used for EEPROM emulation in an MCU without an EEPROM module because it can remain unprotected while the remaining addresses are protected from program or erase.

Security information that allows the MCU to restrict access to the Flash module is stored in the Flash configuration field found in Flash block 0, described in Table 2-1.

Table 2-1. Flash Configuration Field

Unpaged Flash Address	Paged Flash Address (PPAGE 0x3F)	Size (Bytes)	Description
0xFF00 – 0xFF07	0xBF00 – 0xBF07	8	Backdoor Comparison Key Refer to Section 2.6.1, “Unsecuring the MCU using Backdoor Key Access”
0xFF08 – 0xFF0B	0xBF08 – 0xBF0B	4	Reserved
0xFF0C	0xBF0C	1	Block 1 Flash Protection Byte Refer to Section 2.3.2.7, “Flash Status Register (FSTAT)”
0xFF0D	0xBF0D	1	Block 0 Flash Protection Byte Refer toSection 2.3.2.7, “Flash Status Register (FSTAT)”
0xFF0E	0xBF0E	1	Flash Nonvolatile Byte Refer to Section 2.3.2.9, “Flash Control Register (FCTL)”
0xFF0F	0xBF0F	1	Flash Security Byte Refer to Section 2.3.2.2, “Flash Security Register (FSEC)”



Note: 0x30–0x3F correspond to the PPAGE register content

Figure 2-2. Flash Memory Map

Table 2-2. Detailed Flash Memory Map

MCU Address Range	PPAGE	Protectable Lower Range	Protectable Higher Range	Flash Block	Block Relative Address[1]
0x4000–0x7FFF	Unpaged (0x3E)	0x4000–0x43FF 0x4000–0x47FF 0x4000–0x4FFF 0x4000–0x5FFF	N.A.	0	0x018000–0x01BFFF
0x8000–0xBFFF	0x30	N.A.	N.A.	1	0x000000–0x003FFF
	0x31	N.A.	N.A.		0x004000–0x007FFF
	0x32	N.A.	N.A.		0x008000–0x00BFFF
	0x33	N.A.	N.A.		0x00C000–0x00FFFF
	0x34	N.A.	N.A.		0x010000–0x013FFF
	0x35	N.A.	N.A.		0x014000–0x017FFF
	0x36	0x8000–0x83FF 0x8000–0x87FF 0x8000–0x8FFF 0x8000–0x9FFF	N.A.		0x018000–0x01BFFF
	0x37	N.A.	0xB800–0xBFFF 0xB000–0xBFFF 0xA000–0xBFFF 0x8000–0xBFFF		0x01C000–0x01FFFF
0x8000–0xBFFF	0x38	N.A.	N.A.	0	0x000000–0x003FFF
	0x39	N.A.	N.A.		0x004000–0x007FFF
	0x3A	N.A.	N.A.		0x008000–0x00BFFF
	0x3B	N.A.	N.A.		0x00C000–0x00FFFF
	0x3C	N.A.	N.A.		0x010000–0x013FFF
	0x3D	N.A.	N.A.		0x014000–0x017FFF
	0x3E	0x8000–0x83FF 0x8000–0x87FF 0x8000–0x8FFF 0x8000–0x9FFF	N.A.		0x018000–0x01BFFF
	0x3F	N.A.	0xB800–0xBFFF 0xB000–0xBFFF 0xA000–0xBFFF 0x8000–0xBFFF		0x01C000–0x01FFFF
0xC000–0xFFFF	Unpaged (0x3F)	N.A.	0xF800–0xFFFF 0xF000–0xFFFF 0xE000–0xFFFF 0xC000–0xFFFF	0	0x01C000–0x01FFFF

[1] Block relative address for each 128 Kbyte Flash block consists of 17 address bits.

The Flash module also contains a set of 16 control and status registers located in address space module base + 0x0000 to module base + 0x000F. In order to accommodate more than one Flash block with a minimum register address space, a set of registers located from module base + 0x0004 to module base + 0x000B are repeated in all banks. The active register bank is selected by the BKSEL bits in the unbanked Flash configuration register (FCNFG). A summary of these registers is given in Table 2-3 while their accessibility in normal and special modes is detailed in Section 2.3.2, “Register Descriptions”.

Table 2-3. Flash Register Map

Module Base +	Register Name	Normal Mode Access
0x0000	Flash Clock Divider Register (FCLKDIV)	R/W
0x0001	Flash Security Register (FSEC)	R
0x0002	Flash Test Mode Register (FTSTMOD)[1]	R
0x0003	Flash Configuration Register (FCNFG)	R/W
0x0004	Flash Protection Register (FPROT)	R/W
0x0005	Flash Status Register (FSTAT)	R/W
0x0006	Flash Command Register (FCMD)	R/W
0x0007	Flash Control Register (FCTL)	R
0x0008	Flash High Address Register (FADDRHI)[1]	R
0x0009	Flash Low Address Register (FADDRLO)[1]	R
0x000A	Flash High Data Register (FDATAHI)	R
0x000B	Flash Low Data Register (FDATALO)	R
0x000C	RESERVED1[1]	R
0x000D	RESERVED2[1]	R
0x000E	RESERVED3[1]	R
0x000F	RESERVED4[1]	R

1 Intended for factory test purposes only.

2.3.2 Register Descriptions

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
FCLKDIV	R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
	W								
FSEC	R	KEYEN		RNV5	RNV4	RNV3	RNV2	SEC	
	W								
FTSTMOD	R	0	0	0	WRALL	0	0	0	0
	W								
FCNFG	R	CBEIE	CCIE	KEYACC	0	0	0	0	BKSEL
	W								
FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS		FPLDIS	FPLS	
	W								
FSTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
	W								
FCMD	R	0	CMDB						
	W								
FCTL	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
	W								
FADDRHI	R	FADDRHI							
	W								
FADDRLO	R	FADDRLO							
	W								
FDATAHI	R	FDATAHI							
	W								
FDATALO	R	FDATALO							
	W								
RESERVED1	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 2-3. FTS256K2 Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
RESERVED2	R	0	0	0	0	0	0	0	0
	W								
RESERVED3	R	0	0	0	0	0	0	0	0
	W								
RESERVED4	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 2-3. FTS256K2 Register Summary (continued)

2.3.2.1 Flash Clock Divider Register (FCLKDIV)

The unbanked FCLKDIV register is used to control timed events in program and erase algorithms.

	7	6	5	4	3	2	1	0
R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-4. Flash Clock Divider Register (FCLKDIV)

All bits in the FCLKDIV register are readable, bits 6-0 are write once and bit 7 is not writable.

Table 2-4. FCLKDIV Field Descriptions

Field	Description
7 FDIVLD	**Clock Divider Loaded.** 0 Register has not been written. 1 Register has been written to since the last reset.
6 PRDIV8	**Enable Prescalar by 8.** 0 The oscillator clock is directly fed into the clock divider. 1 The oscillator clock is divided by 8 before feeding into the clock divider.
5-0 FDIV[5:0]	**Clock Divider Bits** — The combination of PRDIV8 and FDIV[5:0] must divide the oscillator clock down to a frequency of 150 kHz–200 kHz. The maximum divide ratio is 512. Please refer to Section 2.4.1.1, “Writing the FCLKDIV Register” for more information.

2.3.2.2 Flash Security Register (FSEC)

The unbanked FSEC register holds all bits associated with the security of the MCU and Flash module.

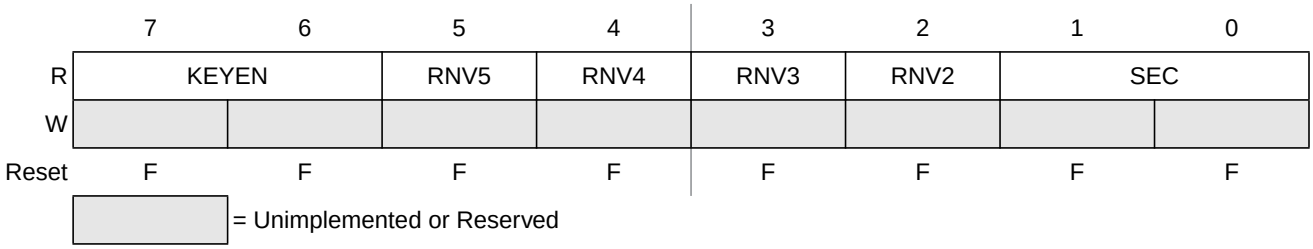


Figure 2-5. Flash Security Register (FSEC)

All bits in the FSEC register are readable but are not writable.

The FSEC register is loaded from the Flash Configuration Field at address $FF0F during the reset sequence, indicated by F in Figure 2-5.

Table 2-5. FSEC Field Descriptions

Field	Description
1-0 KEYEN[1:0]	**Backdoor Key Security Enable Bits** —The KEYEN[1:0] bits define the enabling of backdoor key access to the Flash module as shown in Table 2-6.
5-2 RNV[5:2]	**Reserved Nonvolatile Bits** — The RNV[5:2] bits must remain in the erased 1 state for future enhancements.
1-0 SEC[1:0]	**Flash Security Bits** — The SEC[1:0] bits define the security state of the MCU as shown in Table 2-7. If the Flash module is unsecured using backdoor key access, the SEC bits are forced to 10.

Table 2-6. Flash KEYEN States

KEYEN[1:0]	Status of Backdoor Key Access
00	DISABLED
01[1]	DISABLED
10	**ENABLED**
11	DISABLED

1 Preferred KEYEN state to disable Backdoor Key Access.

Table 2-7. Flash Security States

SEC[1:0]	Status of Security
00	SECURED
01[1]	SECURED
10	**UNSECURED**
11	SECURED

1 Preferred SEC state to set MCU to secured state.

The security function in the Flash module is described in Section 2.6, “Flash Module Security”.

2.3.2.3 Flash Test Mode Register (FTSTMOD)

The unbanked FTSTMOD register is used to control Flash test features.

	7	6	5	4	3	2	1	0
R	0	0	0	WRALL	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-6. Flash Test Mode Register (FTSTMOD)

All bits read 0 and are not writable in normal mode. The WRALL bit is writable only in special mode to simplify mass erase and erase verify operations. When writing to the FTSTMOD register in special mode, all unimplemented/reserved bits must be written to 0.

Table 2-8. FTSTMOD Field Descriptions

Field	Description
4 WRALL	**Write to All Register Banks** — If the WRALL bit is set, all banked registers sharing the same register address will be written simultaneously during a register write. 0 Write only to the bank selected via BKSEL. 1 Write to all register banks.

2.3.2.4 Flash Configuration Register (FCNFG)

The unbanked FCNFG register enables the Flash interrupts and gates the security backdoor writes.

	7	6	5	4	3	2	1	0
R	CBEIE	CCIE	KEYACC	0	0	0	0	BKSEL
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-7. Flash Configuration Register (FCNFG)

CBEIE, CCIE, KEYACC and BKSEL bits are readable and writable while all remaining bits read 0 and are not writable. KEYACC is only writable if KEYEN (see Section 2.3.2.2) is set to the enabled state.

Table 2-9. FCNFG Field Descriptions

Field	Description
7 CBEIE	**Command Buffer Empty Interrupt Enable** — The CBEIE bit enables an interrupt in case of an empty command buffer in the Flash module. 0 Command buffer empty interrupt disabled. 1 An interrupt will be requested whenever the CBEIF flag (see Section 2.3.2.7, “Flash Status Register (FSTAT)”) is set.
6 CCIE	**Command Complete Interrupt Enable** — The CCIE bit enables an interrupt in case all commands have been completed in the Flash module. 0 Command complete interrupt disabled. 1 An interrupt will be requested whenever the CCIF flag (see Section 2.3.2.7, “Flash Status Register (FSTAT)”) is set.
5 KEYACC	**Enable Security Key Writing** 0 Flash writes are interpreted as the start of a command write sequence. 1 Writes to Flash array are interpreted as keys to open the backdoor. Reads of the Flash array return invalid data.
0 BKSEL	**Block Select** — The BKSEL bit indicates which register bank is active. 0 Select register bank associated with Flash block 0. 1 Select register bank associated with Flash block 1.

2.3.2.5 Flash Protection Register (FPROT)

The banked FPROT register defines which Flash sectors are protected against program or erase operations.

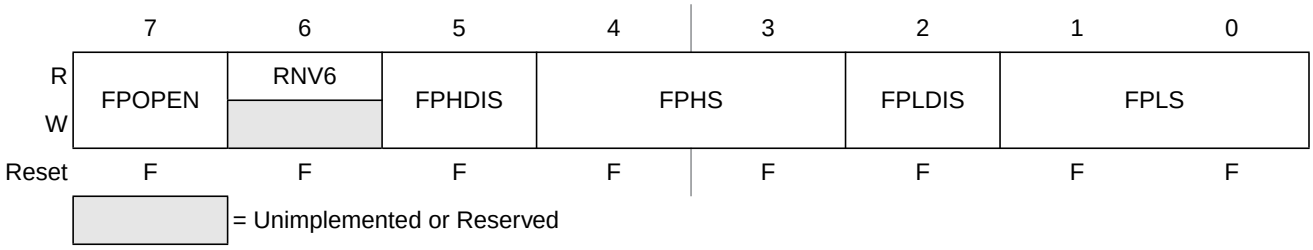


Figure 2-8. Flash Protection Register (FPROT)

All bits in the FPROT register are readable and writable with restrictions except for RNV[6] which is only readable (see Section 2.3.2.6, “Flash Protection Restrictions”).

During reset, the banked FPROT registers are loaded from the Flash Configuration Field at the address shown in Table 2-10. To change the Flash protection that will be loaded during the reset sequence, the upper sector of the Flash memory must be unprotected, then the Flash Protect/Security byte located as described in Table 2-1 must be reprogrammed.

Table 2-10. Reset Loading of FPROT

Flash Address	Protection Byte for
0xFF0D	Flash Block 0
0xFF0C	Flash Block 1

Trying to alter data in any of the protected areas in the Flash block will result in a protection violation error and the PVIOL flag will be set in the FSTAT register. A mass erase of the Flash block is not possible if any of the contained Flash sectors are protected.

Table 2-11. FPROT Field Descriptions

Field	Description
7 FPOPEN	**Protection Function Bit** — The FPOPEN bit determines the protection function for program or erase as shown in Table 2-12. 0 FPHDIS and FPLDIS bits define unprotected address ranges as specified by the corresponding FPHS[1:0] and FPLS[1:0] bits. For an MCU without an EEPROM module, the FPOPEN clear state allows the main part of the Flash block to be protected while a small address range can remain unprotected for EEPROM emulation. 1 FPHDIS and FPLDIS bits enable protection for the address range specified by the corresponding FPHS[1:0] and FPLS[1:0] bits.
6 RNV[6]	**Reserved Nonvolatile Bit** — The RNV[6] bit must remain in the erased state 1 for future enhancements.
5 FPHDIS	**Flash Protection Higher Address Range Disable** — The FPHDIS bit determines whether there is a protected/unprotected area in the higher address space of the Flash block. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
4:3 FPHS[1:0]	**Flash Protection Higher Address Size** — The FPHS[1:0] bits determine the size of the protected/unprotected area as shown in Table 2-13. The FPHS[1:0] bits can only be written to while the FPHDIS bit is set.
2 FPLDIS	**Flash Protection Lower address range Disable** — The FPLDIS bit determines whether there is a protected/unprotected area in the lower address space of the Flash block. 0 Protection/Unprotection enabled 1 Protection/Unprotection disabled
1:0 FPLS[1:0]	**Flash Protection Lower Address Size** — The FPLS[1:0] bits determine the size of the protected/unprotected area as shown in Table 2-14. The FPLS[1:0] bits can only be written to while the FPLDIS bit is set.

Table 2-12. Flash Protection Function

FPOPEN	FPHDIS	FPLDIS	Function[1]
1	1	1	No Protection
1	1	0	Protected Low Range
1	0	1	Protected High Range
1	0	0	Protected High and Low Ranges
0	1	1	Full Block Protected
0	1	0	Unprotected Low Range
0	0	1	Unprotected High Range
0	0	0	Unprotected High and Low Ranges

[1] For range sizes, refer to Table 2-13 and Table 2-14.

Table 2-13. Flash Protection Higher Address Range

FPHS[1:0]	Unpaged Address Range	Paged Address Range	Protected Size
00	0xF800–0xFFFF	0x0037/0x003F: 0xC800–0xCFFF	2 Kbytes
01	0xF000–0xFFFF	0x0037/0x003F: 0xC000–0xCFFF	4 Kbytes
10	0xE000–0xFFFF	0x0037/0x003F: 0xB000–0xCFFF	8 Kbytes
11	0xC000–0xFFFF	0x0037/0x003F: 0x8000–0xCFFF	16 Kbytes

Table 2-14. Flash Protection Lower Address Range

FPLS[1:0]	Unpaged Address Range	Paged Address Range	Protected Size
00	0x4000–0x43FF	0x0036/0x003E: 0x8000–0x83FF	1 Kbyte
01	0x4000–0x47FF	0x0036/0x003E: 0x8000–0x87FF	2 Kbytes
10	0x4000–0x4FFF	0x0036/0x003E: 0x8000–0x8FFF	4 Kbytes
11	0x4000–0x5FFF	0x0036/0x003E: 0x8000–0x9FFF	8 Kbytes

All possible Flash protection scenarios are illustrated in Figure 2-9. Although the protection scheme is loaded from the Flash array after reset, it can be changed by the user. This protection scheme can be used by applications requiring re-programming in single-chip mode while providing as much protection as possible if re-programming is not required.

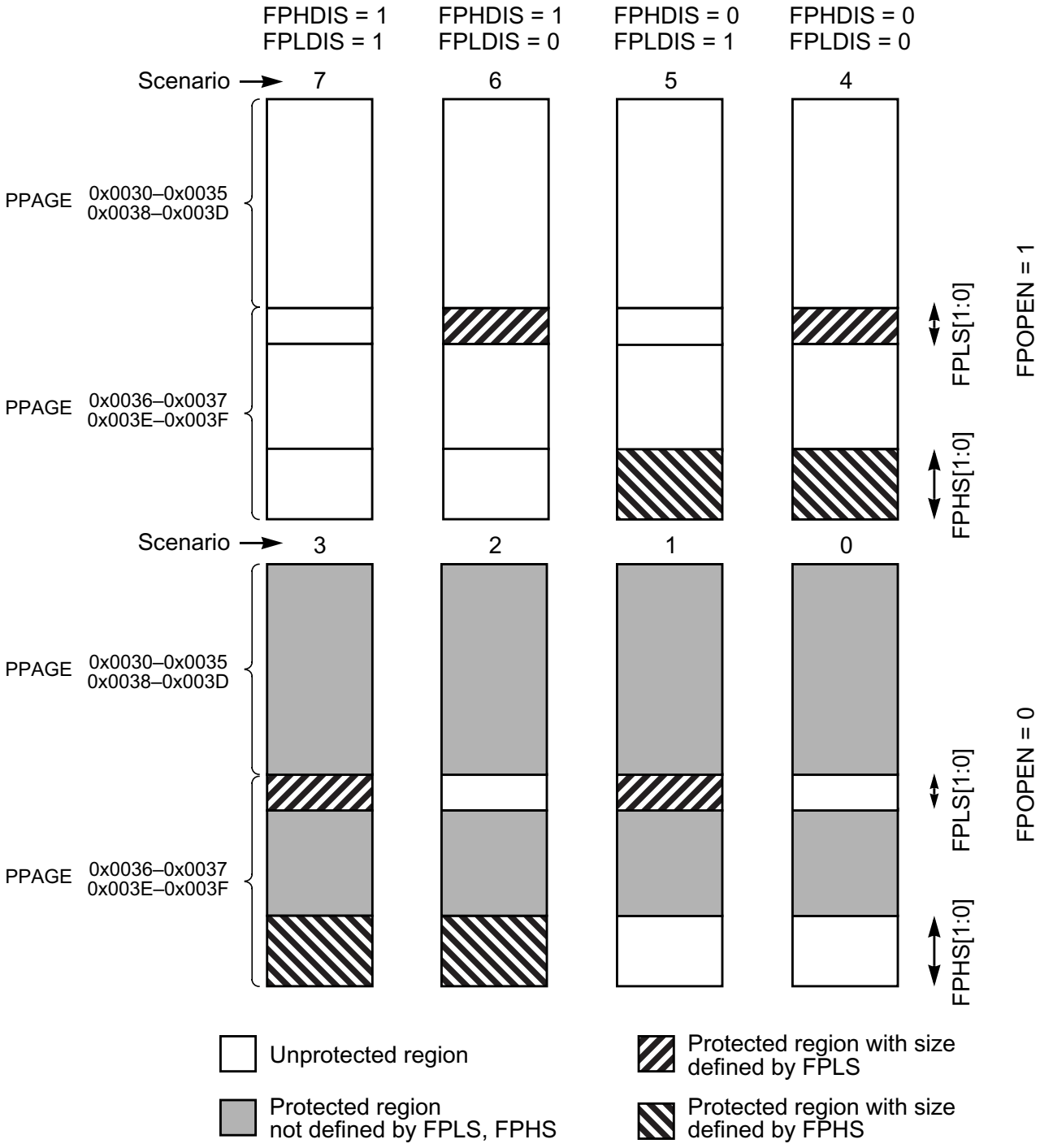


Figure 2-9. Flash Protection Scenarios

2.3.2.6 Flash Protection Restrictions

The general guideline is that Flash protection can only be added and not removed. Table 2-15 specifies all valid transitions between Flash protection scenarios. Any attempt to write an invalid scenario to the FPROT register will be ignored and the FPROT register will remain unchanged. The contents of the

FPROT register reflect the active protection scenario. See the FPHS and FPLS descriptions for additional restrictions.

Table 2-15. Flash Protection Scenario Transitions

From Protection Scenario	To Protection Scenario[1]							
	0	1	2	3	4	5	6	7
0	X	X	X	X				
1		X		X				
2			X	X				
3				X				
4				X	X			
5			X	X	X	X		
6		X		X	X		X	
7	X	X	X	X	X	X	X	X

1 Allowed transitions marked with X.

2.3.2.7 Flash Status Register (FSTAT)

The banked FSTAT register defines the operational status of the module.

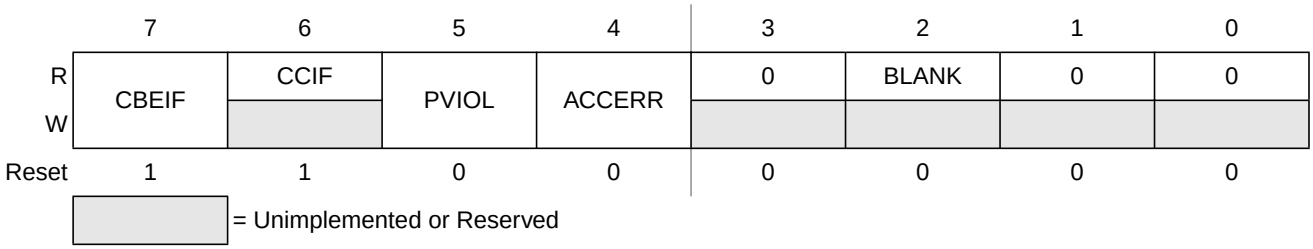


Figure 2-10. Flash Status Register (FSTAT - Normal Mode)

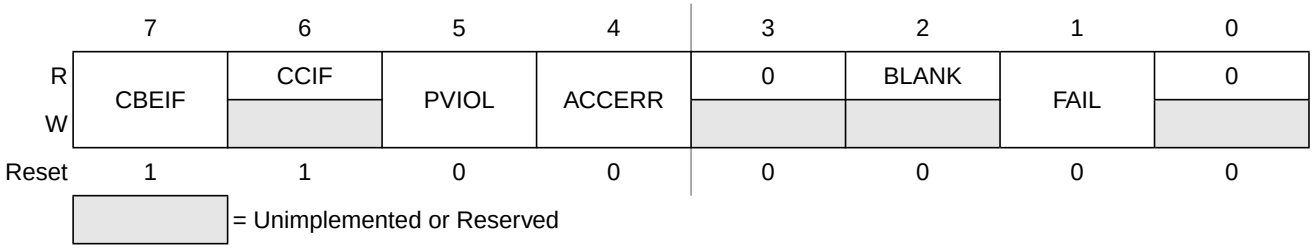


Figure 2-11. Flash Status Register (FSTAT - Special Mode)

CBEIF, PVIOL, and ACCERR are readable and writable, CCIF and BLANK are readable and not writable, remaining bits read 0and are not writable in normal mode. FAIL is readable and writable in special mode. FAIL must be clear when starting a command write sequence.

Table 2-16. FSTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data and command buffers are empty so that a new command write sequence can be started. The CBEIF flag is cleared by writing a 1 to CBEIF. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the Flash address space but before CBEIF is cleared will abort a command write sequence and cause the ACCERR flag to be set. Writing a 0 to CBEIF outside of a command write sequence will not set the ACCERR flag. The CBEIF flag is used together with the CBEIE bit in the FCNFG register to generate an interrupt request (see Figure 2-29). 0 Buffers are full. 1 Buffers are ready to accept a new command.
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is clear and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active commands completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect on CCIF. The CCIF flag is used together with the CCIE bit in the FCNFG register to generate an interrupt request (see Figure 2-29). 0 Command in progress. 1 All commands are completed.
5 PVIOL	**Protection Violation Flag** — The PVIOL flag indicates an attempt was made to program or erase an address in a protected area of the Flash block during a command write sequence. The PVIOL flag is cleared by writing a 1 to PVIOL. Writing a 0 to the PVIOL flag has no effect on PVIOL. While PVIOL is set, it is not possible to launch a command or start a command write sequence. 0 No failure. 1 A protection violation has occurred.
4 ACCERR	**Access Error Flag** — The ACCERR flag indicates an illegal access to the Flash array caused by either a violation of the command write sequence, issuing an illegal command (illegal combination of the CMDBx bits in the FCMD register), launching the sector erase abort command terminating a sector erase operation early or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). The ACCERR flag is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR flag has no effect on ACCERR. While ACCERR is set in any of the banked FTSAT registers, it is not possible to launch a command or start a command write sequence in any of the Flash blocks. If ACCERR is set by an erase verify operation or a data compress operation, any buffered command will not launch. 0 No access error detected. 1 Access error has occurred.
2 BLANK	**Erase Verify Operation Status Flag** — When the CCIF flag is set after completion of an erase verify command, the BLANK flag indicates the result of the erase verify operation. The BLANK flag is cleared by the Flash module when CBEIF is cleared as part of a new valid command write sequence. Writing to the BLANK flag has no effect on BLANK. 0 Flash block verified as not erased. 1 Flash block verified as erased.
1 FAIL	**Flag Indicating a Failed Flash Operation** — The FAIL flag will set if the erase verify operation fails (selected Flash block verified as not erased). The FAIL flag is cleared by writing a 1 to FAIL. Writing a 0 to the FAIL flag has no effect on FAIL. 0 Flash operation completed without error. 1 Flash operation failed.

2.3.2.8 Flash Command Register (FCMD)

The banked FCMD register is the Flash command register.

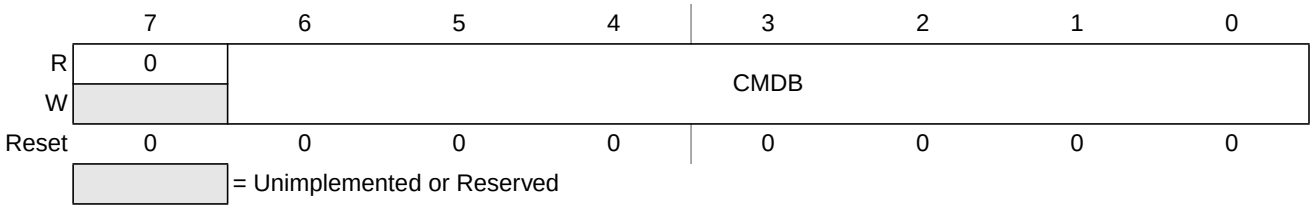


Figure 2-12. Flash Command Register (FCMD - NVM User Mode)

All CMDB bits are readable and writable during a command write sequence while bit 7 reads 0 and is not writable.

Table 2-17. FCMD Field Descriptions

Field	Description
6-0 CMDB[6:0]	**Flash Command** — Valid Flash commands are shown in Table 2-18. Writing any command other than those listed in Table 2-18 sets the ACCERR flag in the FSTAT register.

Table 2-18. Valid Flash Command List

CMDB[6:0]	NVM Command
0x05	Erase Verify
0x06	Data Compress
0x20	Word Program
0x40	Sector Erase
0x41	Mass Erase
0x47	Sector Erase Abort

2.3.2.9 Flash Control Register (FCTL)

The banked FCTL register is the Flash control register.

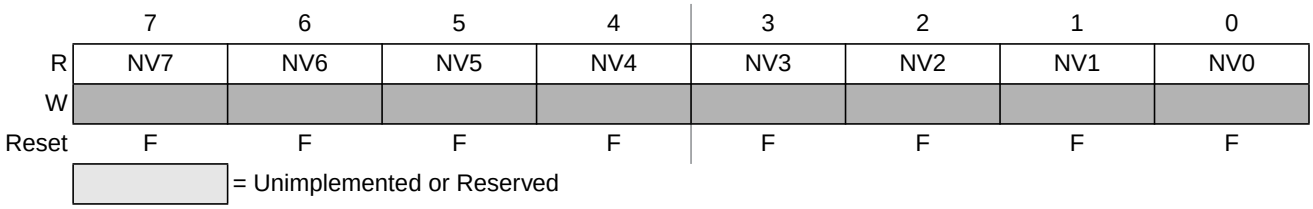


Figure 2-13. Flash Control Register (FCTL)

All bits in the FCTL register are readable but are not writable.

The FCTL register is loaded from the Flash Configuration Field byte at $FF0E during the reset sequence, indicated by F in Figure 2-13.

Table 2-19. FCTL Field Descriptions

Field	Description
7-0 NV[7:0]	**Nonvolatile Bits** — The NV[7:0] bits are available as nonvolatile bits. Refer to the Device User Guide for proper use of the NV bits.

2.3.2.10 Flash Address Registers (FADDR)

The banked FADDRHI and FADDRLO registers are the Flash address registers.

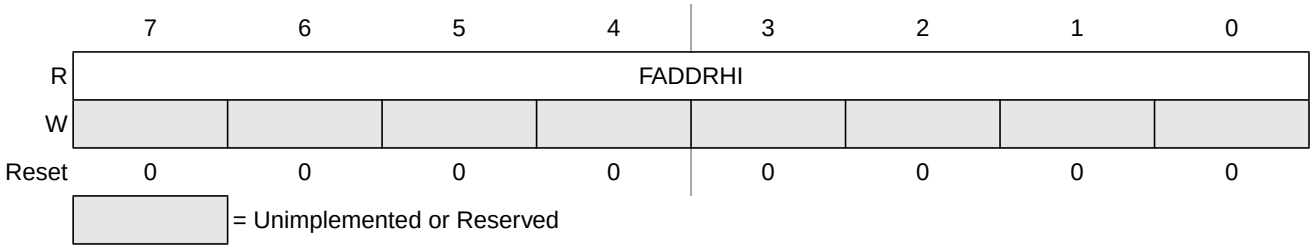


Figure 2-14. Flash Address High Register (FADDRHI)

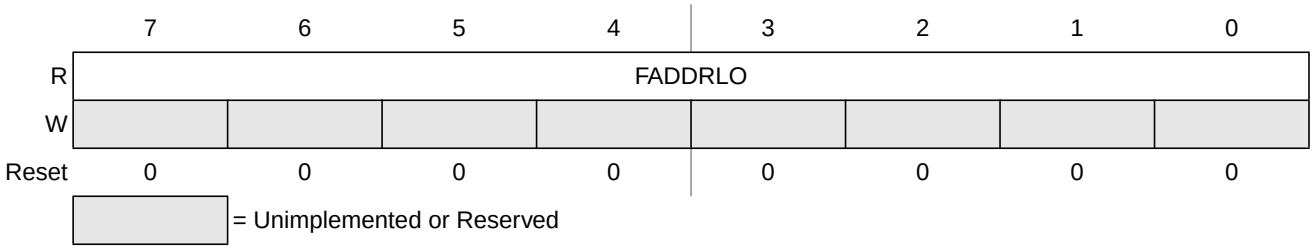


Figure 2-15. Flash Address Low Register (FADDRLO)

All FADDRHI and FADDRLO bits are readable but are not writable. After an array write as part of a command write sequence, the FADDR registers will contain the mapped MCU address written.

2.3.2.11 Flash Data Registers (FDATA)

The banked FDATAHI and FDATALO registers are the Flash data registers.

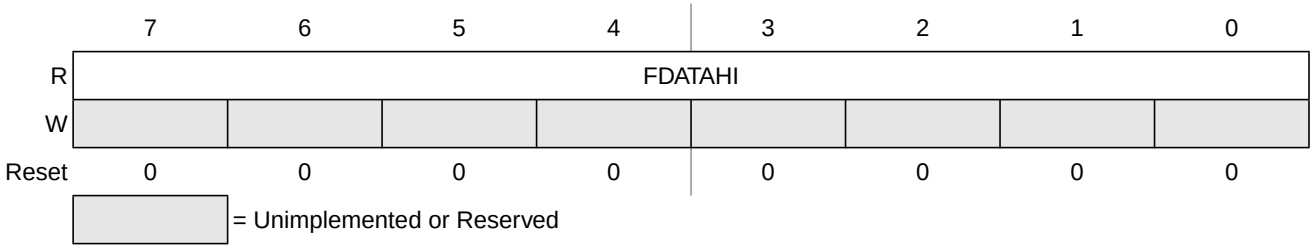


Figure 2-16. Flash Data High Register (FDATAHI)

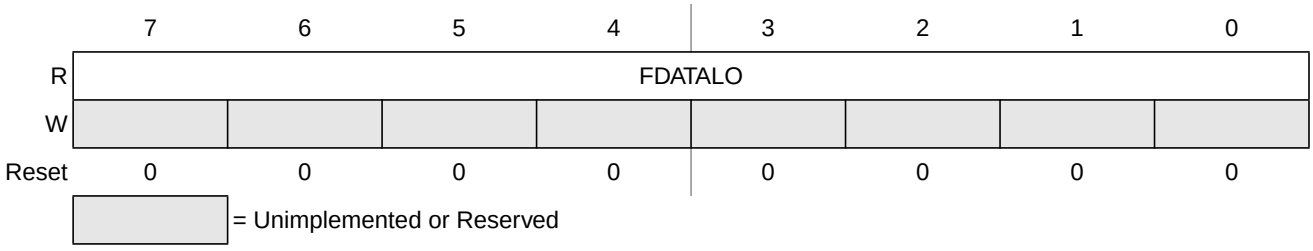


Figure 2-17. Flash Data Low Register (FDATALO)

All FDATAHI and FDATALO bits are readable but are not writable. After an array write as part of a command write sequence, the FDATA registers will contain the data written. At the completion of a data compress operation, the resulting 16-bit signature is stored in the FDATA registers. The data compression signature is readable in the FDATA registers until a new command write sequence is started.

2.3.2.12 RESERVED1

This register is reserved for factory testing and is not accessible.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-18. RESERVED1

All bits read 0 and are not writable.

2.3.2.13 RESERVED2

This register is reserved for factory testing and is not accessible.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-19. RESERVED2

All bits read 0 and are not writable.

2.3.2.14 RESERVED3

This register is reserved for factory testing and is not accessible.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-20. RESERVED3

All bits read 0 and are not writable.

2.3.2.15 RESERVED4

This register is reserved for factory testing and is not accessible.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 2-21. RESERVED4

All bits read 0 and are not writable.

2.4 Functional Description

2.4.1 Flash Command Operations

Write and read operations are both used for the program, erase, erase verify, and data compress algorithms described in this subsection. The program and erase algorithms are time controlled by a state machine whose timebase, FCLK, is derived from the oscillator clock via a programmable divider. The command register as well as the associated address and data registers operate as a buffer and a register (2-stage FIFO) so that a second command along with the necessary data and address can be stored to the buffer while the first command remains in progress. This pipelined operation allows a time optimization when programming more than one word on a specific row in the Flash block as the high voltage generation can be kept active in between two programming commands. The pipelined operation also allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the Flash status register with interrupts generated, if enabled.

The next paragraphs describe:

1. How to write the FCLKDIV register.
2. Command write sequences used to program, erase, and verify the Flash memory.
3. Valid Flash commands.
4. Effects resulting from illegal Flash command write sequences or aborting Flash operations.

2.4.1.1 Writing the FCLKDIV Register

Prior to issuing any program, erase, erase verify, or data compress command, it is first necessary to write the FCLKDIV register to divide the oscillator clock down to within the 150 kHz to 200 kHz range. Because the program and erase timings are also a function of the bus clock, the FCLKDIV determination must take this information into account.

If we define:

- FCLK as the clock of the Flash timing control block,
- Tbus as the period of the bus clock, and

- INT(x) as taking the integer part of x (e.g. INT(4.323)=4).

Then, FCLKDIV register bits PRDIV8 and FDIV[5:0] are to be set as described in Figure 2-22.

For example, if the oscillator clock frequency is 950 kHz and the bus clock frequency is 10 MHz, FCLKDIV bits FDIV[5:0] must be set to 4 (000100) and bit PRDIV8 set to 0. The resulting FCLK frequency is then 190 kHz. As a result, the Flash program and erase algorithm timings are increased over the optimum target by:

$$(200 - 190) / 200 \times 100 \; = \; 5\%$$

CAUTION

Program and erase command execution time will increase proportionally with the period of FCLK. Because of the impact of clock synchronization on the accuracy of the functional timings, programming or erasing the Flash memory cannot be performed if the bus clock runs at less than 1 MHz. Programming or erasing the Flash memory with FCLK < 150 kHz must be avoided. Setting FCLKDIV to a value such that FCLK < 150 kHz can destroy the Flash memory due to overstress. Setting FCLKDIV to a value such that (1/FCLK + Tbus) < 5µs can result in incomplete programming or erasure of the Flash memory cells.

If the FCLKDIV register is written, the FDIVLD bit is set automatically. If the FDIVLD bit is 0, the FCLKDIV register has not been written since the last reset. Flash commands will not be executed if the FCLKDIV register has not been written to.

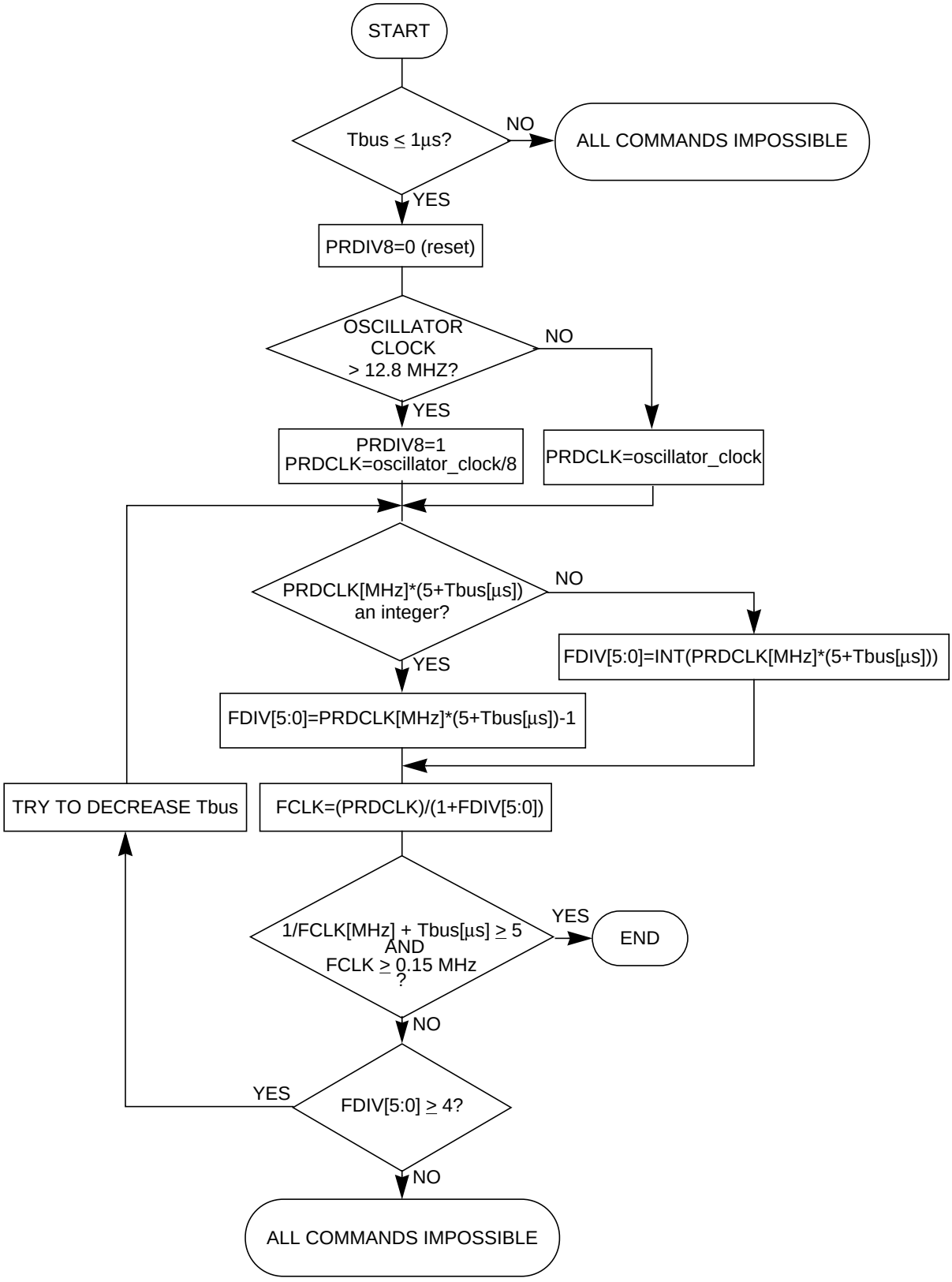


Figure 2-22. Determination Procedure for PRDIV8 and FDIV Bits

2.4.1.2 Command Write Sequence

The Flash command controller is used to supervise the command write sequence to execute program, erase, erase verify, and data compress algorithms.

Before starting a command write sequence, the ACCERR and PVIOL flags in the FSTAT register must be clear (see Section 2.3.2.7, “Flash Status Register (FSTAT)”) and the CBEIF flag must be tested to determine the state of the address, data, and command buffers. If the CBEIF flag is set, indicating the buffers are empty, a new command write sequence can be started. If the CBEIF flag is clear, indicating the buffers are not available, a new command write sequence will overwrite the contents of the address, data, and command buffers.

A command write sequence consists of three steps which must be strictly adhered to with writes to the Flash module not permitted between the steps. However, Flash register and array reads are allowed during a command write sequence. A command write sequence consists of the following steps:

1. Write an aligned data word to a valid Flash array address. The address and data will be stored in the address and data buffers, respectively. If the CBEIF flag is clear when the Flash array write occurs, the contents of the address and data buffers will be overwritten and the CBEIF flag will be set.
2. Write a valid command to the FCMD register.
   a) For the erase verify command (see Section 2.4.1.3.1, “Erase Verify Command”), the contents of the data buffer are ignored and all address bits in the address buffer are ignored.
   b) For the data compress command (see Section 2.4.1.3.2, “Data Compress Command”), the contents of the data buffer represents the number of consecutive words to read for data compression and the contents of the address buffer represents the starting address.
   c) For the program command (see Section 2.4.1.3.3, “Program Command”), the contents of the data buffer will be programmed to the address specified in the address buffer with all address bits valid.
   d) For the sector erase command (see Section 2.4.1.3.4, “Sector Erase Command”), the contents of the data buffer are ignored and address bits [9:0] contained in the address buffer are ignored.
   e) For the mass erase command (see Section 2.4.1.3.5, “Mass Erase Command”), the contents of the data buffer and address buffer are ignored.
   f) For the sector erase abort command (see Section 2.4.1.3.6, “Sector Erase Abort Command”), the contents of the data buffer and address buffer are ignored.
3. Clear the CBEIF flag by writing a 1 to CBEIF to launch the command. When the CBEIF flag is cleared, the CCIF flag is cleared on the same bus cycle by internal hardware indicating that the command was successfully launched. For all command write sequences except data compress and sector erase abort, the CBEIF flag will set four bus cycles after the CCIF flag is cleared indicating that the address, data, and command buffers are ready for a new command write sequence to begin. For data compress and sector erase abort operations, the CBEIF flag will remain clear until the operation completes.

A command write sequence can be aborted prior to clearing the CBEIF flag by writing a 0 to the CBEIF flag and will result in the ACCERR flag being set.

Except for the sector erase abort command, a buffered command will wait for the active operation to be completed before being launched. The sector erase abort command is launched when the CBEIF flag is cleared as part of a sector erase abort command write sequence. After a command is launched, the completion of the command operation is indicated by the setting of the CCIF flag. The CCIF flag only sets when all active and buffered commands have been completed.

2.4.1.3 Valid Flash Commands

Table 2-20 summarizes the valid Flash commands along with the effects of the commands on the Flash block.

Table 2-20. Valid Flash Command Description

FCMDB	NVM Command	Function on Flash Memory
0x05	Erase Verify	Verify all memory bytes in the Flash block are erased. If the Flash block is erased, the BLANK flag in the FSTAT register will set upon command completion.
0x06	Data Compress	Compress data from a selected portion of the Flash block. The resulting signature is stored in the FDATA register.
0x20	Program	Program a word (two bytes) in the Flash block.
0x40	Sector Erase	Erase all memory bytes in a sector of the Flash block.
0x41	Mass Erase	Erase all memory bytes in the Flash block. A mass erase of the full Flash block is only possible when FPLDIS, FPHDIS, and FPOPEN bits in the FPROT register are set prior to launching the command.
0x47	Sector Erase Abort	Abort the sector erase operation. The sector erase operation will terminate according to a set procedure. The Flash sector must not be considered erased if the ACCERR flag is set upon command completion.

CAUTION

A Flash word must be in the erased state before being programmed. Cumulative programming of bits within a Flash word is not allowed.

2.4.1.3.1 Erase Verify Command

The erase verify operation is used to confirm that a Flash block is erased. After launching the erase verify command, the CCIF flag in the FSTAT register will set after the operation has completed unless a second command has been buffered. The number of bus cycles required to execute the erase verify operation is equal to the number of addresses in the Flash block plus 12 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. The result of the erase verify operation is reflected in the state of the BLANK flag in the FSTAT register. If the BLANK flag is set in the FSTAT register, the Flash memory is erased.

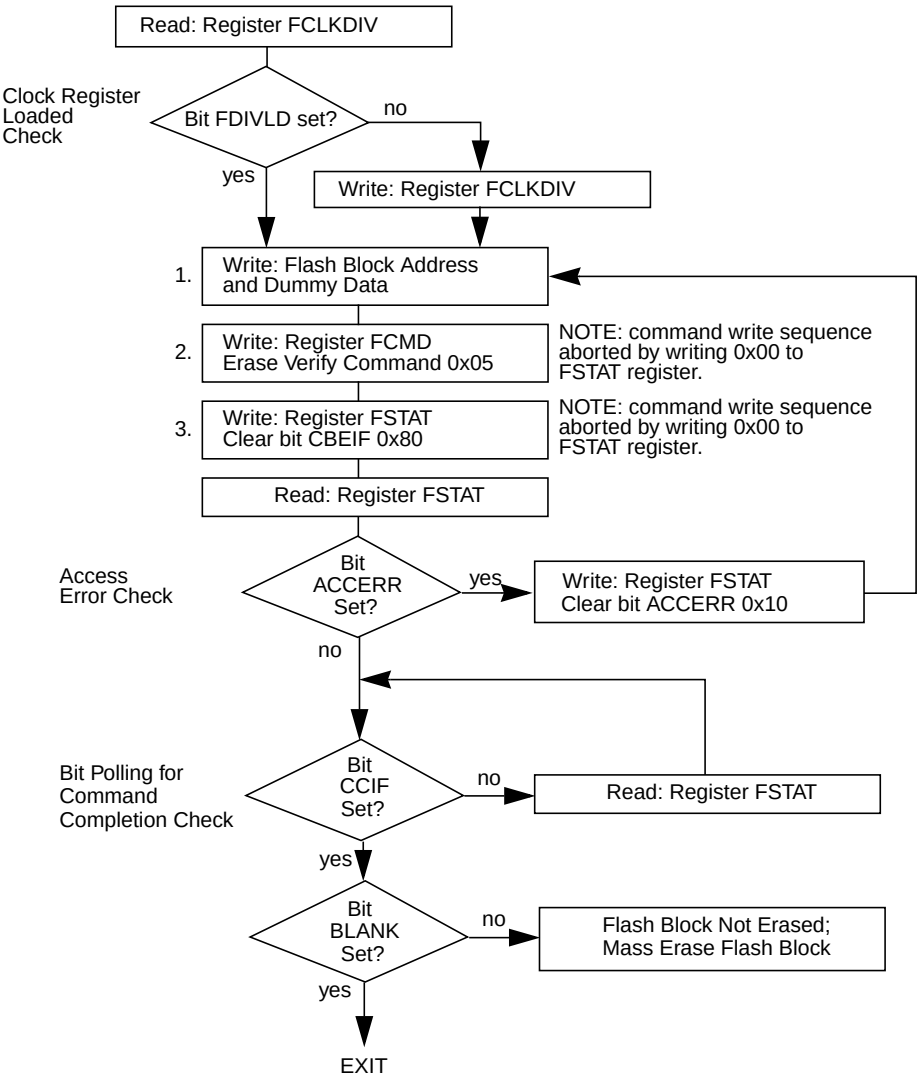


Figure 2-23. Example Erase Verify Command Flow

2.4.1.3.2 Data Compress Command

The data compress command is used to check Flash code integrity by compressing data from a selected portion of the Flash block into a signature analyzer. The starting address for the data compress operation is defined by the address written during the command write sequence. The number of consecutive word addresses compressed is defined by the data written during the command write sequence. If the data value written is 0x0000, 64K addresses or 128 Kbytes will be compressed. After launching the data compress command, the CCIF flag in the FSTAT register will set after the data compress operation has completed. The number of bus cycles required to execute the data compress operation is equal to two times the number of addresses read plus 20 bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set. After the CCIF flag is set, the signature generated by the data compress operation is available in the FDATA register. The signature in the FDATA register can be compared to the expected signature to determine the integrity of the selected data stored in the Flash block. If the last address of the Flash block is reached during the data compress operation, data compression will continue with the starting address of the Flash block.

NOTE

Since the FDATA register (or data buffer) is written to as part of the data compress operation, a command write sequence is not allowed to be buffered behind a data compress command write sequence. The CBEIF flag will not set after launching the data compress command to indicate that a command must not be buffered behind it. If an attempt is made to start a new command write sequence with a data compress operation active, the ACCERR flag in the FSTAT register will be set. A new command write sequence must only be started after reading the signature stored in the FDATA register.

In order to take corrective action, it is recommended that the data compress command be executed on a Flash sector or subset of a Flash sector. If the data compress operation on a Flash sector returns an invalid signature, the Flash sector must be erased using the sector erase command and then reprogrammed using the program command.

The data compress command can be used to verify that a sector or sequential set of sectors are erased.

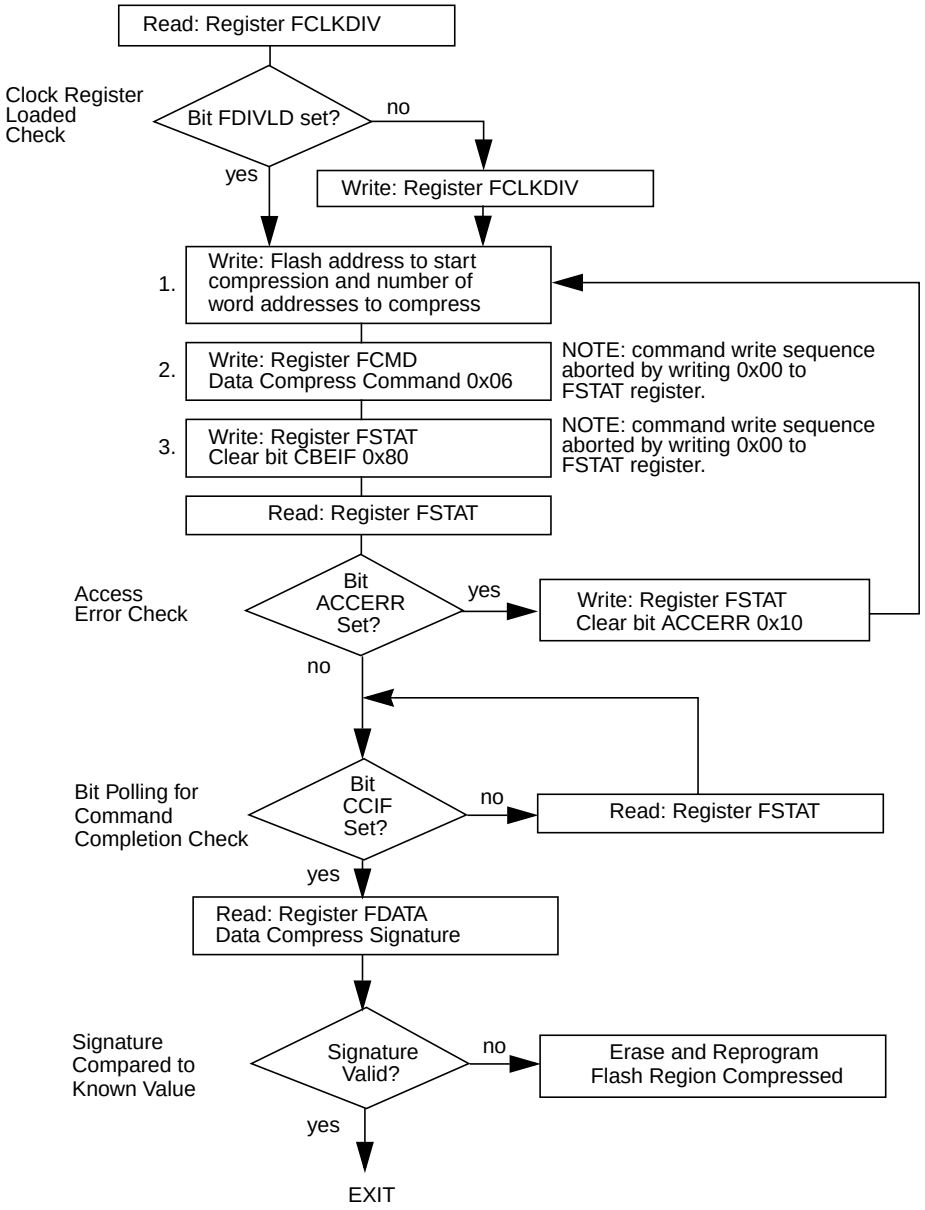


Figure 2-24. Example Data Compress Command Flow

2.4.1.3.3 Program Command

The program command is used to program a previously erased word in the Flash memory using an embedded algorithm. If the word to be programmed is in a protected area of the Flash block, the PVIOL flag in the FSTAT register will set and the program command will not launch. After the program command has successfully launched, the CCIF flag in the FSTAT register will set after the program operation has completed unless a second command has been buffered.

A summary of the launching of a program operation is shown in Figure 2-25.

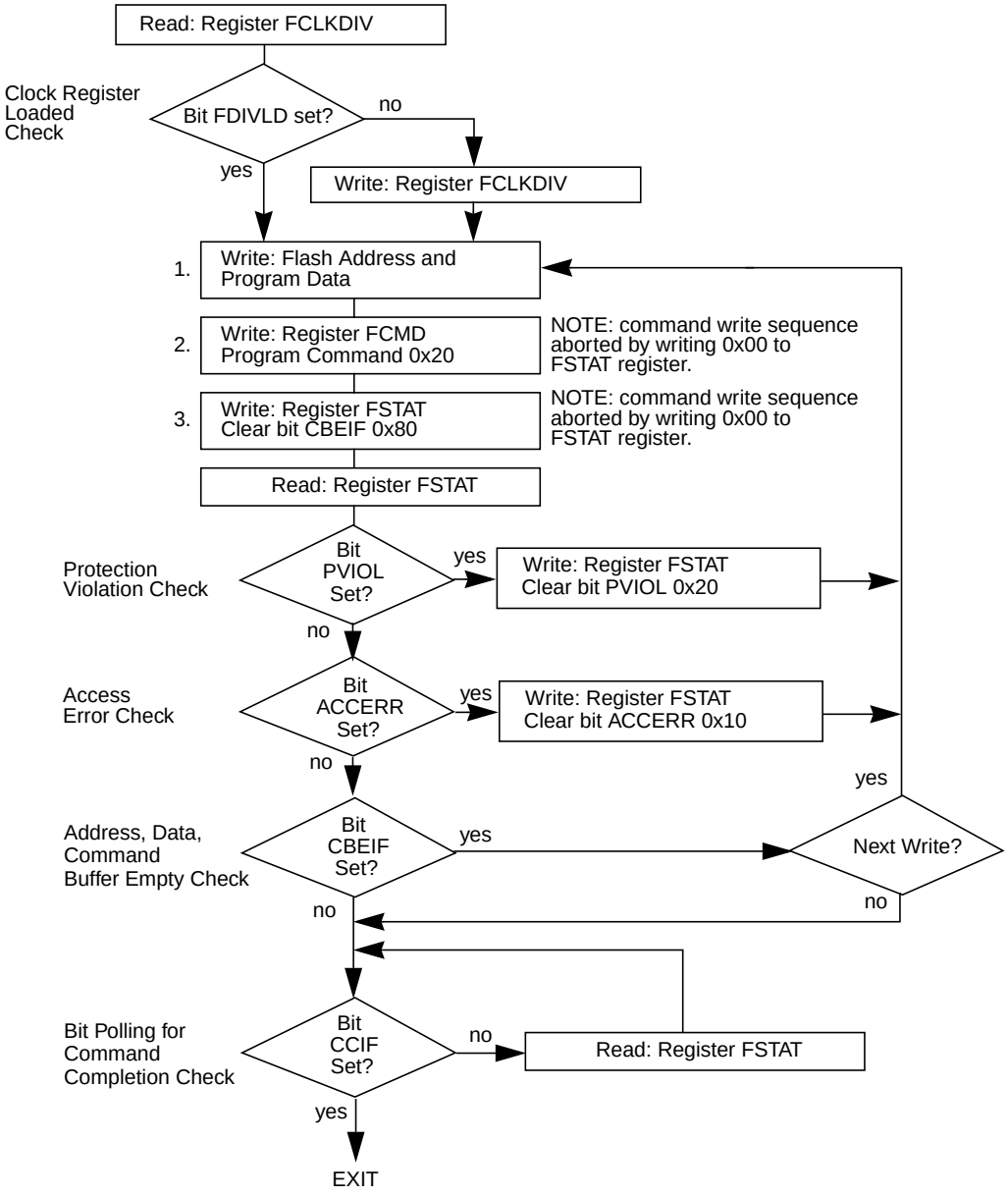


Figure 2-25. Example Program Command Flow

2.4.1.3.4 Sector Erase Command

The sector erase command is used to erase the addressed sector in the Flash memory using an embedded algorithm. If the Flash sector to be erased is in a protected area of the Flash block, the PVIOL flag in the FSTAT register will set and the sector erase command will not launch. After the sector erase command has successfully launched, the CCIF flag in the FSTAT register will set after the sector erase operation has completed unless a second command has been buffered.

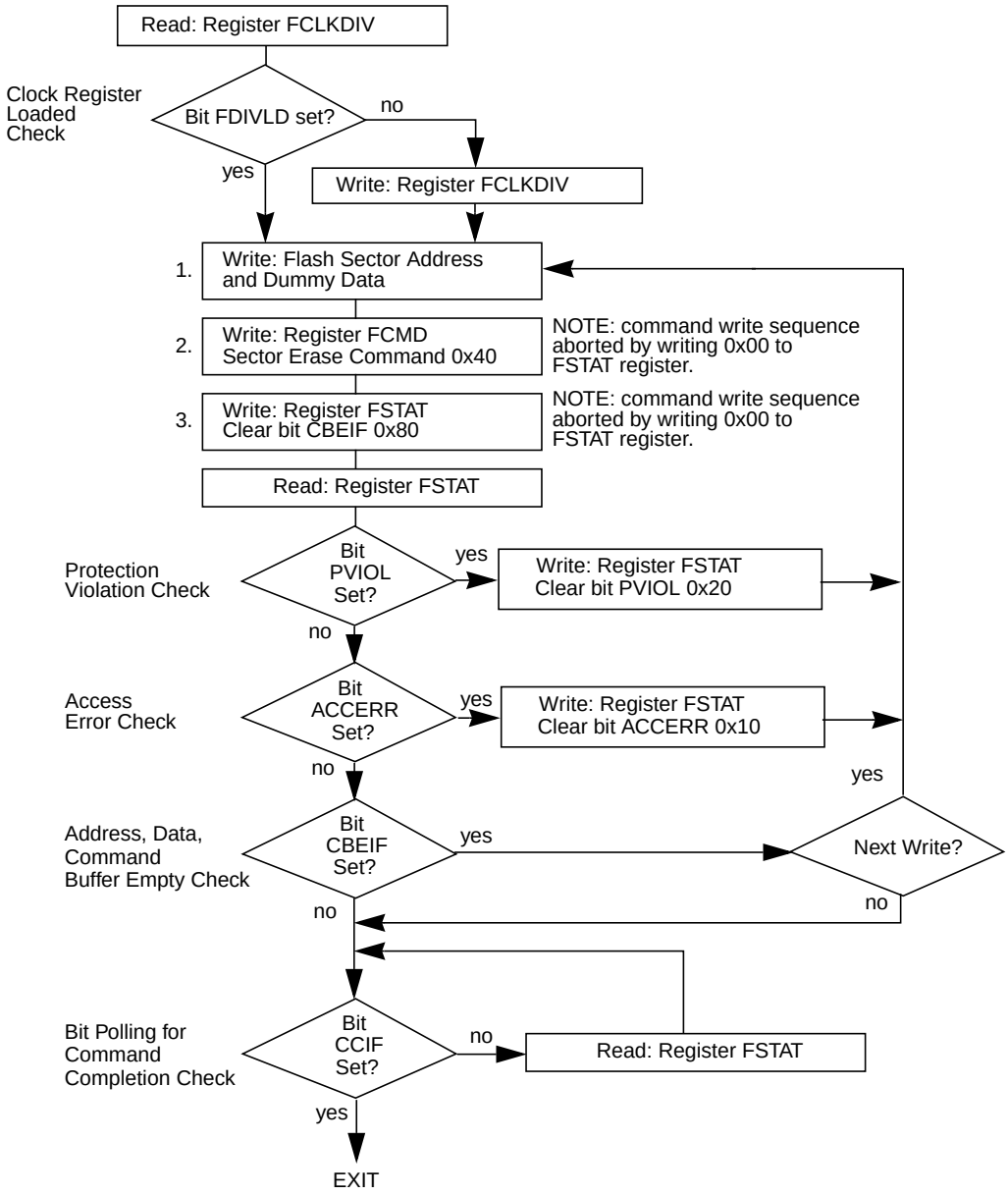


Figure 2-26. Example Sector Erase Command Flow

2.4.1.3.5 Mass Erase Command

The mass erase command is used to erase a Flash memory block using an embedded algorithm. If the Flash block to be erased contains any protected area, the PVIOL flag in the FSTAT register will set and the mass erase command will not launch. After the mass erase command has successfully launched, the CCIF flag in the FSTAT register will set after the mass erase operation has completed unless a second command has been buffered.

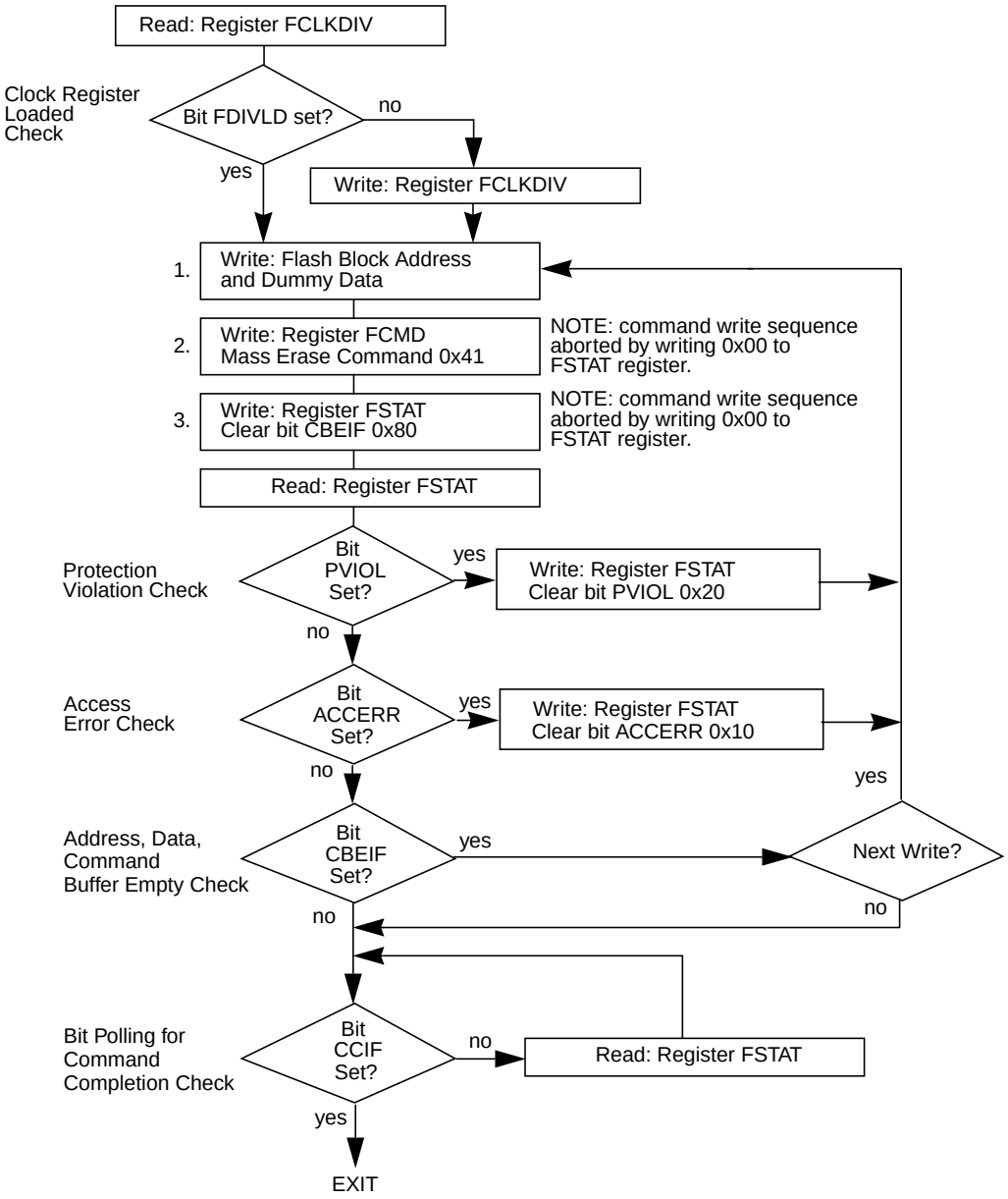


Figure 2-27. Example Mass Erase Command Flow

2.4.1.3.6 Sector Erase Abort Command

The sector erase abort command is used to terminate the sector erase operation so that other sectors in the Flash block are available for read and program operations without waiting for the sector erase operation to complete. If the sector erase abort command is launched resulting in the early termination of an active sector erase operation, the ACCERR flag will set after the operation completes as indicated by the CCIF flag being set. The ACCERR flag sets to inform the user that the sector may not be fully erased and a new sector erase command must be launched before programming any location in that specific sector. If the sector erase abort command is launched but the active sector erase operation completes normally, the ACCERR flag will not set upon completion of the operation as indicated by the CCIF flag being set. Therefore, if the ACCERR flag is not set after the sector erase abort command has completed, the sector being erased when the abort command was launched is fully erased. The maximum number of cycles required to abort a sector erase operation is equal to four FCLK periods (see Section 2.4.1.1, “Writing the FCLKDIV Register”) plus five bus cycles as measured from the time the CBEIF flag is cleared until the CCIF flag is set.

NOTE

Since the ACCERR bit in the FSTAT register may be set at the completion of the sector erase abort operation, a command write sequence is not allowed to be buffered behind a sector erase abort command write sequence. The CBEIF flag will not set after launching the sector erase abort command to indicate that a command must not be buffered behind it. If an attempt is made to start a new command write sequence with a sector erase abort operation active, the ACCERR flag in the FSTAT register will be set. A new command write sequence may be started after clearing the ACCERR flag, if set.

NOTE

The sector erase abort command must be used sparingly because a sector erase operation that is aborted counts as a complete program/erase cycle.

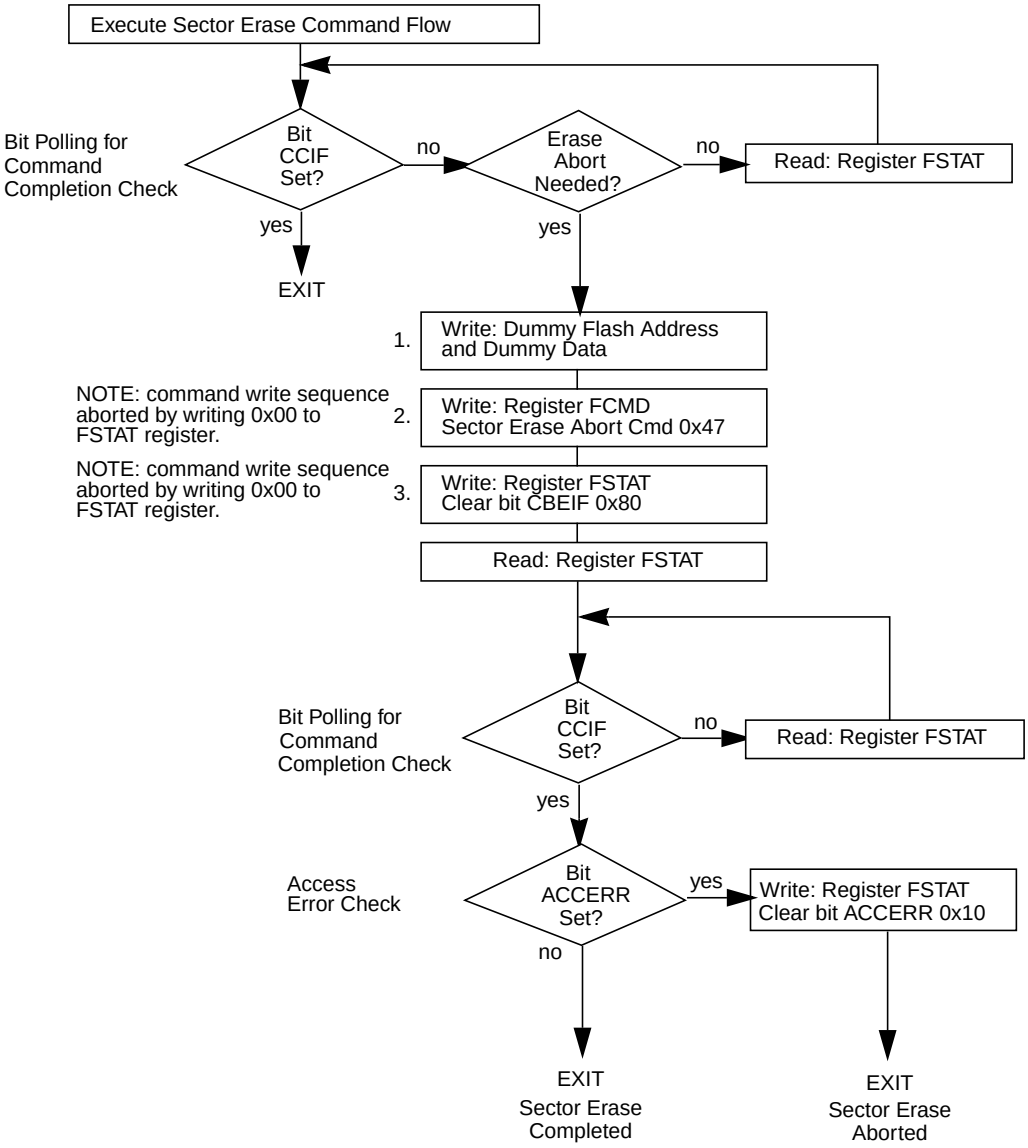


Figure 2-28. Example Sector Erase Abort Command Flow

2.4.1.4 Illegal Flash Operations

The ACCERR flag will be set during the command write sequence if any of the following illegal steps are performed, causing the command write sequence to immediately abort:

1. Writing to a Flash address before initializing the FCLKDIV register.
2. Writing to a Flash address in the range 0x8000–0xBFFF when the PPAGE register does not select a 16 Kbyte page in the Flash block selected by the BKSEL bit in the FCNFG register.
3. Writing to a Flash address in the range 0x4000–0x7FFF or 0xC000–0xFFFF with the BKSEL bit in the FCNFG register not selecting Flash block 0.
4. Writing a byte or misaligned word to a valid Flash address.
5. Starting a command write sequence while a data compress operation is active.
6. Starting a command write sequence while a sector erase abort operation is active.
7. Writing a second word to a Flash address in the same command write sequence.
8. Writing to any Flash register other than FCMD after writing a word to a Flash address.
9. Writing a second command to the FCMD register in the same command write sequence.
10. Writing an invalid command to the FCMD register.
11. When security is enabled, writing a command other than mass erase to the FCMD register when the write originates from a non-secure memory location or from the Background Debug Mode.
12. Writing to any Flash register other than FSTAT (to clear CBEIF) after writing to the FCMD register.
13. Writing a 0 to the CBEIF flag in the FSTAT register to abort a command write sequence.

The ACCERR flag will not be set if any Flash register is read during a valid command write sequence.

The ACCERR flag will also be set if any of the following events occur:

1. Launching the sector erase abort command while a sector erase operation is active which results in the early termination of the sector erase operation (see Section 2.4.1.3.6, “Sector Erase Abort Command”)
2. The MCU enters stop mode and a program or erase operation is in progress. The operation is aborted immediately and any pending command is purged (see Section 2.5.2, “Stop Mode”).

If the Flash memory is read during execution of an algorithm (i.e., CCIF flag in the FSTAT register is low), the read operation will return invalid data and the ACCERR flag will not be set.

If the ACCERR flag is set in the FSTAT register, the user must clear the ACCERR flag before starting another command write sequence (see Section 2.3.2.7, “Flash Status Register (FSTAT)”).

The PVIOL flag will be set after the command is written to the FCMD register during a command write sequence if any of the following illegal operations are attempted, causing the command write sequence to immediately abort:

1. Writing the program command if the address written in the command write sequence was in a protected area of the Flash memory.
2. Writing the sector erase command if the address written in the command write sequence was in a protected area of the Flash memory.
3. Writing the mass erase command while any Flash protection is enabled.

If the PVIOL flag is set in the FSTAT register, the user must clear the PVIOL flag before starting another command write sequence (see Section 2.3.2.7, “Flash Status Register (FSTAT)”).

2.5 Operating Modes

2.5.1 Wait Mode

If a command is active (CCIF = 0) when the MCU enters wait mode, the active command and any buffered command will be completed.

The Flash module can recover the MCU from wait mode if the CBEIF and CCIF interrupts are enabled (Section 2.8, “Interrupts”).

2.5.2 Stop Mode

If a command is active (CCIF = 0) when the MCU enters stop mode, the operation will be aborted and, if the operation is program or erase, the Flash array data being programmed or erased may be corrupted and the CCIF and ACCERR flags will be set. If active, the high voltage circuitry to the Flash memory will immediately be switched off when entering stop mode. Upon exit from stop mode, the CBEIF flag is set and any buffered command will not be launched. The ACCERR flag must be cleared before starting a command write sequence (see Section 2.4.1.2, “Command Write Sequence”).

NOTE

As active commands are immediately aborted when the MCU enters stop mode, it is strongly recommended that the user does not use the STOP instruction during program or erase operations.

2.5.3 Background Debug Mode

In background debug mode (BDM), the FPROT register is writable. If the MCU is unsecured, then all Flash commands listed in Table 2-20 can be executed.

2.6 Flash Module Security

The Flash module provides the necessary security information to the MCU. After each reset, the Flash module determines the security state of the MCU as defined in Section 2.3.2.2, “Flash Security Register (FSEC)”.

The contents of the Flash security byte at 0xFF0F in the Flash configuration field must be changed directly by programming 0xFF0F when the MCU is unsecured and the higher address sector is unprotected. If the Flash security byte remains in a secured state, any reset will cause the MCU to initialize to a secure operating mode.

2.6.1 Unsecuring the MCU using Backdoor Key Access

The MCU may be unsecured by using the backdoor key access feature which requires knowledge of the contents of the backdoor keys (four 16-bit words programmed at addresses 0xFF00–0xFF07). If the KEYEN[1:0] bits are in the enabled state (see Section 2.3.2.2, “Flash Security Register (FSEC)”) and the KEYACC bit is set, a write to a backdoor key address in the Flash memory triggers a comparison between the written data and the backdoor key data stored in the Flash memory. If all four words of data are written to the correct addresses in the correct order and the data matches the backdoor keys stored in the Flash memory, the MCU will be unsecured. The data must be written to the backdoor keys sequentially starting with 0xFF00–0xFF01 and ending with 0xFF06–0xFF07. 0x0000 and 0xFFFF are not permitted as backdoor keys. While the KEYACC bit is set, reads of the Flash memory will return invalid data.

The user code stored in the Flash memory must have a method of receiving the backdoor key from an external stimulus. This external stimulus would typically be through one of the on-chip serial ports.

If the KEYEN[1:0] bits are in the enabled state (see Section 2.3.2.2, “Flash Security Register (FSEC)”), the MCU can be unsecured by the backdoor access sequence described below:

1. Set the KEYACC bit in the Flash configuration register (FCNFG).
2. Write the correct four 16-bit words to Flash addresses 0xFF00–0xFF07 sequentially starting with 0xFF00.
3. Clear the KEYACC bit.
4. If all four 16-bit words match the backdoor keys stored in Flash addresses 0xFF00–0xFF07, the MCU is unsecured and the SEC[1:0] bits in the FSEC register are forced to the unsecure state of 1:0.

The backdoor key access sequence is monitored by an internal security state machine. An illegal operation during the backdoor key access sequence will cause the security state machine to lock, leaving the MCU in the secured state. A reset of the MCU will cause the security state machine to exit the lock state and allow a new backdoor key access sequence to be attempted. The following operations during the backdoor key access sequence will lock the security state machine:

1. If any of the four 16-bit words does not match the backdoor keys programmed in the Flash array.
2. If the four 16-bit words are written in the wrong sequence.
3. If more than four 16-bit words are written.
4. If any of the four 16-bit words written are 0x0000 or 0xFFFF.
5. If the KEYACC bit does not remain set while the four 16-bit words are written.
6. If any two of the four 16-bit words are written on successive MCU clock cycles.

After the backdoor keys have been correctly matched, the MCU will be unsecured. After the MCU is unsecured, the Flash security byte can be programmed to the unsecure state, if desired.

In the unsecure state, the user has full control of the contents of the backdoor keys by programming addresses 0xFF00–0xFF07 in the Flash configuration field.

The security as defined in the Flash security byte (0xFF0F) is not changed by using the backdoor key access sequence to unsecure. The backdoor keys stored in addresses 0xFF00–0xFF07 are unaffected by the backdoor key access sequence. After the next reset of the MCU, the security state of the Flash module

is determined by the Flash security byte (0xFF0F). The backdoor key access sequence has no effect on the program and erase protections defined in the Flash protection register.

It is not possible to unsecure the MCU in special single-chip mode by using the backdoor key access sequence via the background debug mode (BDM).

2.6.2 Unsecuring the Flash Module in Special Single-Chip Mode using BDM

The MCU can be unsecured in special single-chip mode by erasing the Flash module by the following method :

- Reset the MCU into special single-chip mode, delay while the erase test is performed by the BDM secure ROM, send BDM commands to disable protection in the Flash module, and execute a mass erase command write sequence to erase the Flash memory.

After the CCIF flag sets to indicate that the mass operation has completed, reset the MCU into special single-chip mode. The BDM secure ROM will verify that the Flash memory is erased and will assert the UNSEC bit in the BDM status register. This BDM action will cause the MCU to override the Flash security state and the MCU will be unsecured. All BDM commands will be enabled and the Flash security byte may be programmed to the unsecure state by the following method:

- Send BDM commands to execute a word program sequence to program the Flash security byte to the unsecured state and reset the MCU.

2.7 Resets

2.7.1 Flash Reset Sequence

On each reset, the Flash module executes a reset sequence to hold CPU activity while loading the following registers from the Flash memory according to Table 2-1:

- FPROT — Flash Protection Register (see Section 2.3.2.5).
- FCTL — Flash Control Register (see Section 2.3.2.9).
- FSEC — Flash Security Register (see Section 2.3.2.2).

2.7.2 Reset While Flash Command Active

If a reset occurs while any Flash command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector / block being erased is not guaranteed.

2.8 Interrupts

The Flash module can generate an interrupt when all Flash command operations have completed, when the Flash address, data, and command buffers are empty.

Table 2-21. Flash Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Flash address, data and command buffers empty	CBEIF (FSTAT register)	CBEIE (FCNFG register)	I Bit
All Flash commands completed	CCIF (FSTAT register)	CCIE (FCNFG register)	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

2.8.1 Description of Flash Interrupt Operation

The logic used for generating interrupts is shown in Figure 2-29.

The Flash module uses the CBEIF and CCIF flags in combination with the CBIE and CCIE enable bits to generate the Flash command interrupt request.

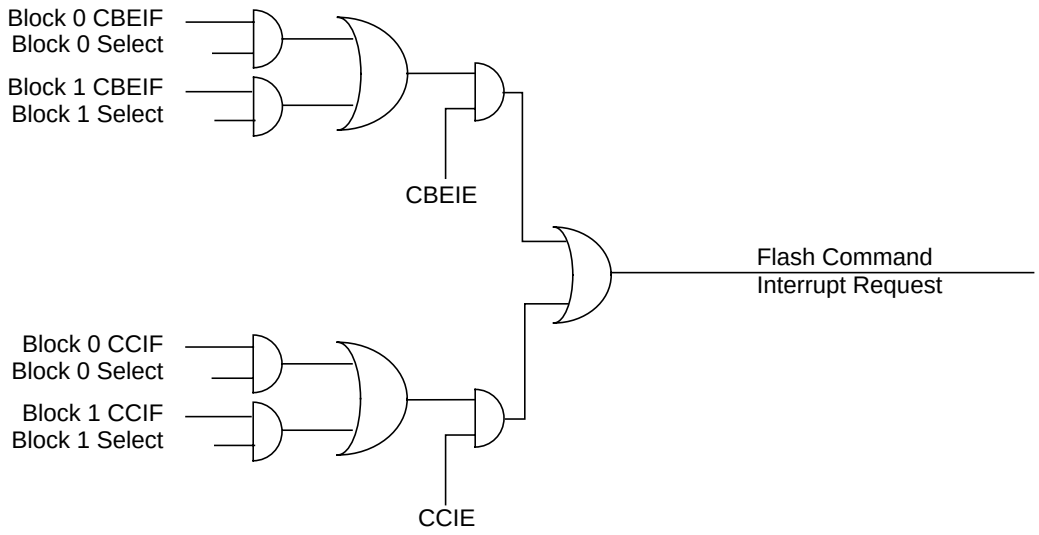


Figure 2-29. Flash Interrupt Implementation

For a detailed description of the register bits, refer to Section 2.3.2.4, “Flash Configuration Register (FCNFG)” and Section 2.3.2.7, “Flash Status Register (FSTAT)”.

Chapter 3
2 Kbyte EEPROM Module (EETS2KV1)

3.1 Introduction

This document describes the EETS2K module which is a 2 Kbyte EEPROM (nonvolatile) memory. The EETS2K block uses a small sector Flash memory to emulate EEPROM functionality. It is an array of electrically erasable and programmable, nonvolatile memory. The EEPROM memory is organized as 1024 rows of 2 bytes (1 word). The EEPROM memory's erase sector size is 2 rows or 2 words (4 bytes).

The EEPROM memory may be read as either bytes, aligned words, or misaligned words. Read access time is one bus cycle for byte and aligned word, and two bus cycles for misaligned words.

Program and erase functions are controlled by a command driven interface. Both sector erase and mass erase of the entire EEPROM memory are supported. An erased bit reads 1 and a programmed bit reads 0. The high voltage required to program and erase is generated internally by on-chip charge pumps.

It is not possible to read from the EEPROM memory while it is being erased or programmed.

The EEPROM memory is ideal for data storage for single-supply applications allowing for field reprogramming without requiring external programming voltage sources.

CAUTION

An EEPROM word must be in the erased state before being programmed. Cumulative programming of bits within a word is not allowed.

3.1.1 Glossary

Command Write Sequence — A three-step MCU instruction sequence to program, erase, or erase verify the EEPROM.

3.1.2 Features

- 2 Kbytes of EEPROM memory
- Minimum erase sector of 4 bytes
- Automated program and erase algorithms
- Interrupts on EEPROM command completion and command buffer empty
- Fast sector erase and word program operation
- 2-stage command pipeline
- Flexible protection scheme for protection against accidental program or erase
- Single power supply program and erase

3.1.3 Modes of Operation

Program and erase operation (please refer to Section 3.4.1 for details).

3.1.4 Block Diagram

Figure 3-1 shows a block diagram of the EETS2K module.

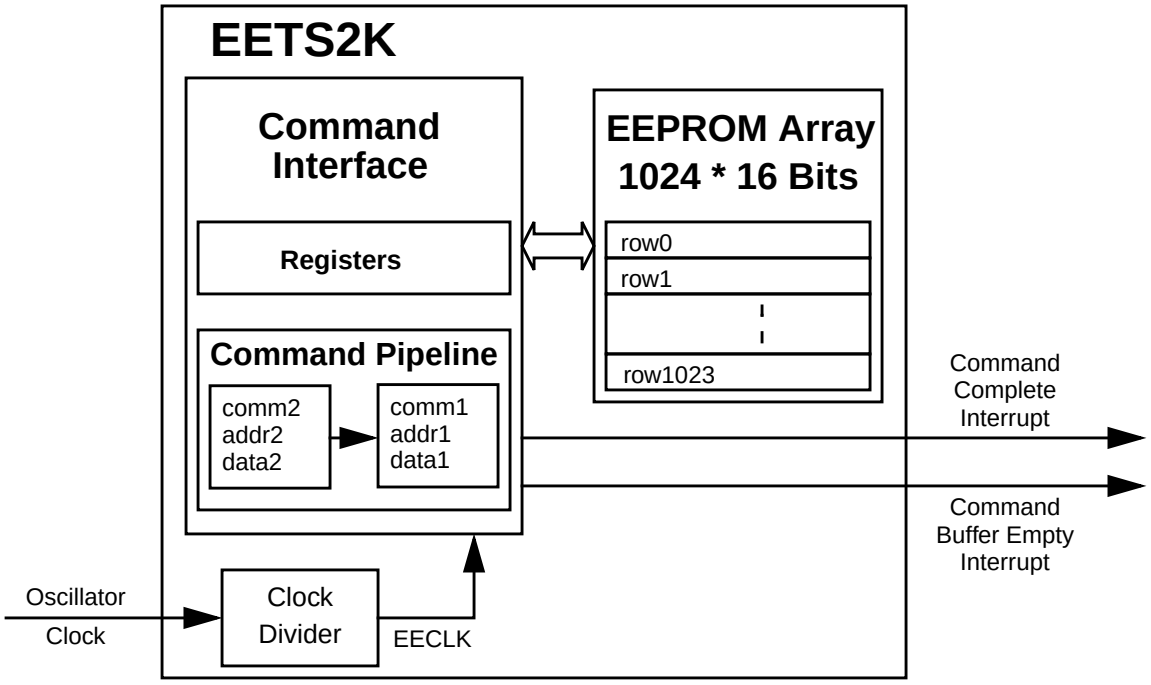


Figure 3-1. EETS2K Block Diagram

3.2 External Signal Description

The EETS2K module contains no signals that connect off chip.

3.3 Memory Map and Register Definition

This section describes the EETS2K memory map and registers.

3.3.1 Module Memory Map

Figure 3-2 shows the EETS2K memory map. Location of the EEPROM array in the MCU memory map is defined in the Device Overview chapter and is reflected in the INITEE register contents defined in the INT block description chapter. Shown within the EEPROM array are: a protection/reserved field and user-defined EEPROM protected sectors. The 16-byte protection/reserved field is located in the EEPROM array from address 0x07F0 to 0x07FF. A description of this protection/reserved field is given in Table 3-1.

Table 3-1. EEPROM Protection/Reserved Field

Address Offset	Size (Bytes)	Description
0x07F0 – 0x07FC	13	Reserved
0x07FD	1	EEPROM protection byte
0x07FE – 0x07FF	2	Reserved

The EEPROM module has hardware interlocks which protect data from accidental corruption. A protected sector is located at the higher address end of the EEPROM array, just below address 0x07FF. The protected sector in the EEPROM array can be sized from 64 bytes to 512 bytes. In addition, the EPOPEN bit in the EPROT register, described in Section 3.3.2.5, “EEPROM Protection Register (EPROT)”, can be set to globally protect the entire EEPROM array.

Chip security is defined at the MCU level.

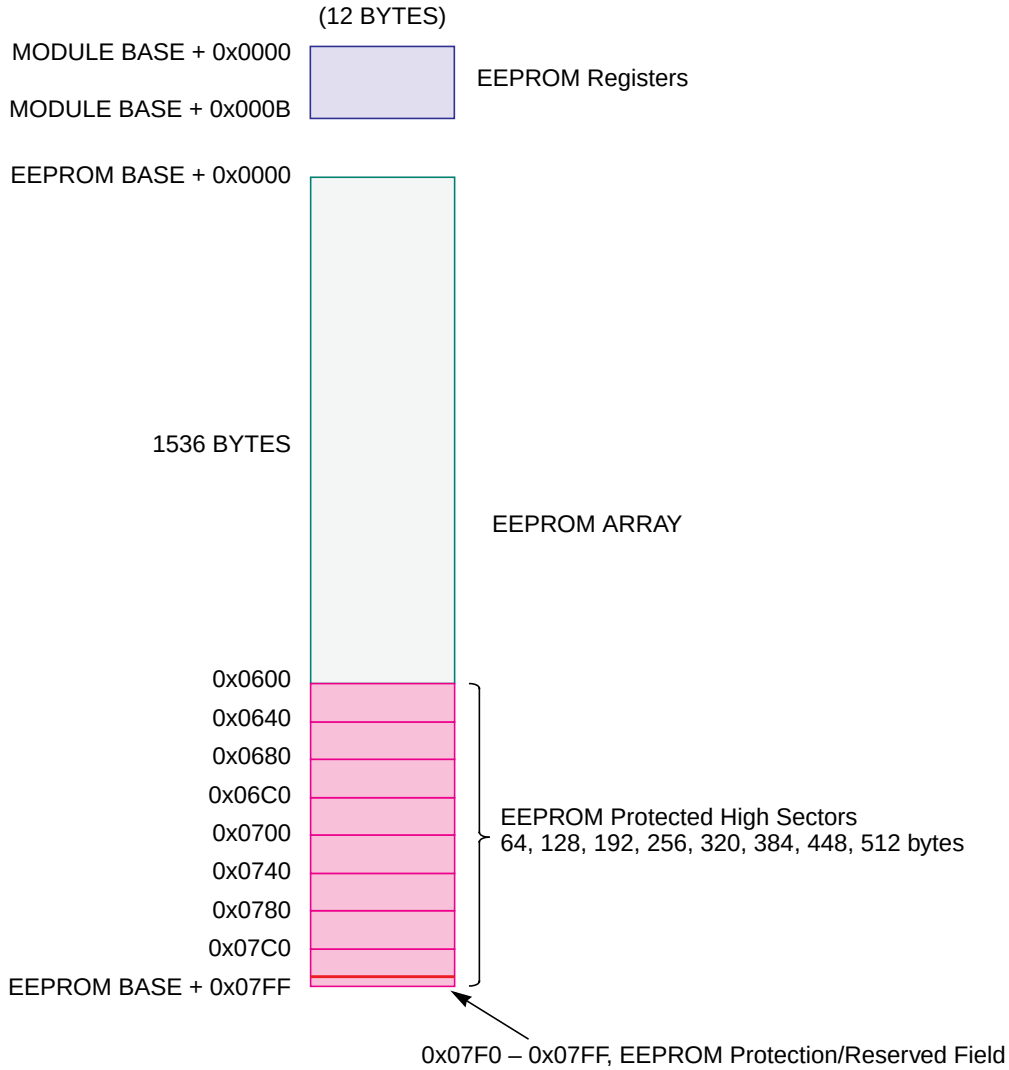


Figure 3-2. EEPROM Memory Map

The EEPROM module also contains a set of 12 control and status registers located in address space module base + 0x0000 to module base + 0x000B.

Table 3-2 gives an overview of all EETS2K registers.

Table 3-2. EEPROM Register Map

Module Base +	Register Name	Normal Mode Access
0x0000	EEPROM Clock Divider Register (ECLKDIV)	R/W
0x0001	RESERVED1[1]	R
0x0002	RESERVED2[1]	R
0x0003	EEPROM Configuration Register (ECNFG)	R/W
0x0004	EEPROM Protection Register (EPROT)	R/W
0x0005	EEPROM Status Register (ESTAT)	R/W
0x0006	EEPROM Command Register (ECMD)	R/W
0x0007	RESERVED3[1]	R
0x0008	EEPROM High Address Register (EADDRHI)	R/W
0x0009	EEPROM Low Address Register (EADDRLO)	R/W
0x000A	EEPROM High Data Register (EDATAHI)	R/W
0x000B	EEPROM Low Data Register (EDATALO)	R/W

1 Intended for factory test purposes only.

3.3.2 Register Descriptions

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
ECLKDIV	R	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
	W								
RESERVED1	R	0	0	0	0	0	0	0	0
	W								
RESERVED2	R	0	0	0	0	0	0	0	0
	W								
ECNFG	R	CBEIE	CCIE	0	0	0	0	0	0
	W								
EPROT	R	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EPO
	W								
ESTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
	W								
ECMD	R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
	W								
RESERVED3	R	0	0	0	0	0	0	0	0
	W								
EADDRHI	R	0	0	0	0	0	0	EABHI	
	W								
EADDRLO	R	EABLO							
	W								
EDATAHI	R	EDHI							
	W								
EDATALO	R	EDLO							
	W								

= Unimplemented or Reserved

Figure 3-3. EETS2K Register Summary

3.3.2.1 EEPROM Clock Divider Register (ECLKDIV)

The ECLKDIV register is used to control timed events in program and erase algorithms.

	7	6	5	4	3	2	1	0
R	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-4. EEPROM Clock Divider Register (ECLKDIV)

All bits in the ECLKDIV register are readable while bits 6-0 are write once and bit 7 is not writable.

Table 3-3. ECLKDIV Field Descriptions

Field	Description
7 EDIVLD	**Clock Divider Loaded** 0 Register has not been written. 1 Register has been written to since the last reset.
6 PRDIV8	**Enable Prescaler by 8** 0 The oscillator clock is directly fed into the ECLKDIV divider. 1 The oscillator clock is divided by 8 before feeding into the clock divider.
5:0 EDIV[5:0]	**Clock Divider Bits** — The combination of PRDIV8 and EDIV[5:0] must divide the oscillator clock down to a frequency of 150 kHz – 200 kHz. The maximum divide ratio is 512. Please refer to Section 3.4.1.1, “Writing the ECLKDIV Register” for more information.

3.3.2.2 RESERVED1

This register is reserved for factory testing and is not accessible to the user.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-5. RESERVED1

All bits read 0 and are not writable.

3.3.2.3 RESERVED2

This register is reserved for factory testing and is not accessible to the user.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-6. RESERVED2

All bits read 0 and are not writable.

3.3.2.4 EEPROM Configuration Register (ECNFG)

The ECNFG register enables the EEPROM interrupts.

	7	6	5	4	3	2	1	0
R	CBEIE	CCIE	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-7. EEPROM Configuration Register (ECNFG)

CBEIE and CCIE bits are readable and writable while bits 5-0 read 0 and are not writable.

Table 3-4. ECNFG Field Descriptions

Field	Description
7 CBEIE	**Command Buffer Empty Interrupt Enable** — The CBEIE bit enables the interrupts in case of an empty command buffer in the EEPROM. 0 Command buffer empty interrupts disabled. 1 An interrupt will be requested whenever the CBEIF flag is set (see Section 3.3.2.6, “EEPROM Status Register (ESTAT)”).
6 CCIE	**Command Complete Interrupt Enable** — The CCIE bit enables the interrupts in case of all commands being completed in the EEPROM. 0 Command complete interrupts disabled. 1 An interrupt will be requested whenever the CCIF flag is set (see Section 3.3.2.6, “EEPROM Status Register (ESTAT)”).

3.3.2.5 EEPROM Protection Register (EPROT)

The EPROT register defines which EEPROM sectors are protected against program or erase.

	7	6	5	4	3	2	1	0
R	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
W								
Reset	F	F	F	F	F	F	F	F

= Unimplemented or Reserved

Figure 3-8. EEPROM Protection Register (EPROT)

The EPROT register is loaded from EEPROM array address 0x07FD during reset, as indicated by the F in Figure 3-8.

All bits in the EPROT register are readable. Bits NV[6:4] are not writable. The EPOPEN and EPDIS bits in the EPROT register can only be written to the protected state (i.e., 0). The EP[2:0] bits can be written anytime until bit EPDIS is cleared. If the EPOPEN bit is cleared, then the state of the EPDIS and EP[2:0] bits is irrelevant.

To change the EEPROM protection that will be loaded on reset, the upper sector of EEPROM must first be unprotected, then the EEPROM protect byte located at address 0x07FD must be written to.

A protected EEPROM sector is disabled by the EPDIS bit while the size of the protected sector is defined by the EP bits in the EPROT register.

Trying to alter any of the protected areas will result in a protect violation error and PVIOL flag will be set in the ESTAT register. A mass erase of a whole EEPROM block is only possible when protection is fully disabled by setting the EPOPEN and EPDIS bits. An attempt to mass erase an EEPROM block while protection is enabled will set the PVIOL flag in the ESTAT register.

Table 3-5. EPROT Field Descriptions

Field	Description
7 EPOPEN	**Opens EEPROM for Program or Erase** 0 The whole EEPROM array is protected. In this case, the EPDIS and EP bits within the protection register are ignored. 1 The EEPROM sectors not protected are enabled for program or erase.
6:4 NV[6:4]	**Nonvolatile Flag Bits** — These three bits are available to the user as nonvolatile flags.
3 EPDIS	**EEPROM Protection Address Range Disable** — The EPDIS bit determines whether there is a protected area in the space of the EEPROM address map. 0 Protection enabled 1 Protection disabled
2:0 EP[2:0]	**EEPROM Protection Address Size** — The EP[2:0] bits determine the size of the protected sector. Refer to Table 3-6.

Table 3-6. EEPROM Address Range Protection

EP[2:0]	Protected Address Range	Protected Size
000	0x07C0-0x07FF	64 bytes
001	0x0780-0x07FF	128 bytes
010	0x0740-0x07FF	192 bytes
011	0x0700-0x07FF	256 bytes
100	0x06C0-0x07FF	320 bytes
101	0x0680-0x07FF	384 bytes
110	0x0640-0x07FF	448 bytes
111	0x0600-0x07FF	512 bytes

3.3.2.6 EEPROM Status Register (ESTAT)

The ESTAT register defines the EEPROM state machine command status and EEPROM array access, protection and erase verify status.

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-9. EEPROM Status Register (ESTAT - Normal Mode)

	7	6	5	4	3	2	1	0
R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	FAIL	DONE
W								
Reset	1	1	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 3-10. EEPROM Status Register (ESTAT - Special Mode)

CBEIF, PVIOL, and ACCERR bits are readable and writable, CCIF and BLANK bits are readable but not writable, remaining bits read 0 and are not writable in normal mode. FAIL is readable and writable in special mode. FAIL must be clear when starting a command write sequence. DONE is readable but not writable in special mode.

Table 3-7. ESTAT Field Descriptions

Field	Description
7 CBEIF	**Command Buffer Empty Interrupt Flag** — The CBEIF flag indicates that the address, data, and command buffers are empty so that a new command sequence can be started. The CBEIF flag is cleared by writing a 1 to CBEIF. Writing a 0 to the CBEIF flag has no effect on CBEIF. Writing a 0 to CBEIF after writing an aligned word to the EEPROM address space but before CBEIF is cleared will abort a command sequence and cause the ACCERR flag in the ESTAT register to be set. Writing a 0 to CBEIF outside of a command sequence will not set the ACCERR flag. The CBEIF flag is used together with the CBEIE bit in the ECNFG register to generate an interrupt request. 0 Buffers are full 1 Buffers are ready to accept a new command
6 CCIF	**Command Complete Interrupt Flag** — The CCIF flag indicates that there are no more commands pending. The CCIF flag is cleared when CBEIF is cleared and sets automatically upon completion of all active and pending commands. The CCIF flag does not set when an active command completes and a pending command is fetched from the command buffer. Writing to the CCIF flag has no effect. The CCIF flag is used together with the CCIE bit in the ECNFG register to generate an interrupt request. 0 Command in progress 1 All commands are completed
5 PVIOL	**Protection Violation** — The PVIOL flag indicates an attempt was made to program or erase an address in a protected EEPROM memory area (Section 3.4.1.4, “Illegal EEPROM Operations”). The PVIOL flag is cleared by writing a 1 to PVIOL. Writing a 0 to the PVIOL flag has no effect on PVIOL. While PVIOL is set, it is not possible to launch another command in the EEPROM. 0 No failure 1 A protection violation has occurred

Table 3-7. ESTAT Field Descriptions (continued)

Field	Description
4 ACCERR	**EEPROM Access Error** — The ACCERR flag indicates an illegal access to the selected EEPROM array (Section 3.4.1.4, “Illegal EEPROM Operations). This can be either a violation of the command sequence, issuing an illegal command (illegal combination of the CMDBx bits in the ECMD register) or the execution of a CPU STOP instruction while a command is executing (CCIF = 0). The ACCERR flag is cleared by writing a 1 to ACCERR. Writing a 0 to the ACCERR flag has no effect on ACCERR. While ACCERR is set, it is not possible to launch another command in the EEPROM. 0 No failure 1 Access error has occurred
2 BLANK	**Array Has Been Verified as Erased** — The BLANK flag indicates that an erase verify command has checked the EEPROM array and found it to be erased. The BLANK flag is cleared by hardware when CBEIF is cleared as part of a new valid command sequence. Writing to the BLANK flag has no effect on BLANK. 0 If an erase verify command has been requested and the CCIF flag is set, then a 0 in BLANK indicates array is not erased 1 EEPROM array verifies as erased
1 FAIL	**Flag Indicating a Failed EEPROM Operation** — The FAIL flag will set if the erase verify operation fails (EEPROM block verified as not erased). The FAIL flag is cleared writing a 1 to FAIL. Writing a 0 to the FAIL flag has no effect on FAIL. 0 EEPROM operation completed without error 1 EEPROM operation failed
0 DONE	**Flag Indicating a Completed EEPROM Operation** 0 EEPROM operation is active (program, erase, erase verify) 1 EEPROM operation not active

3.3.2.7 EEPROM Command Register (ECMD)

The ECMD register defines the EEPROM commands.

	7	6	5	4	3	2	1	0
R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 3-11. EEPROM Command Register (ECMD)

CMDB6, CMDB5, CMDB2, and CMDB0 bits are readable and writable during a command sequence while bits 7, 4, 3, and 1 read 0 and are not writable.

Table 3-8. ECMD Field Descriptions

Field	Description
6, 5, 2, 0 CMDB[6:5] CMDB2 CMDB0	**EEPROM Command** — Valid EEPROM commands are shown in Table 3-9. Any other command written than those mentioned in Table 3-9 sets the ACCERR bit in the ESTAT register.

Table 3-9. Valid EEPROM Command List

Command	Meaning
0x05	Erase verify
0x20	Word program
0x40	Sector erase
0x41	Mass erase
0x60	Sector modify

3.3.2.8 RESERVED3

This register is reserved for factory testing and is not accessible to the user.

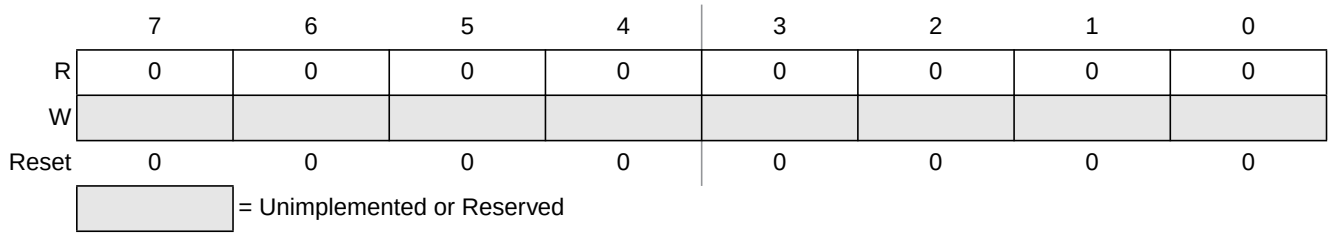


Figure 3-12. RESERVED3

All bits read 0 and are not writable.

3.3.2.9 EEPROM Address Register (EADDR)

EADDRHI and EADDRLO are the EEPROM address registers.

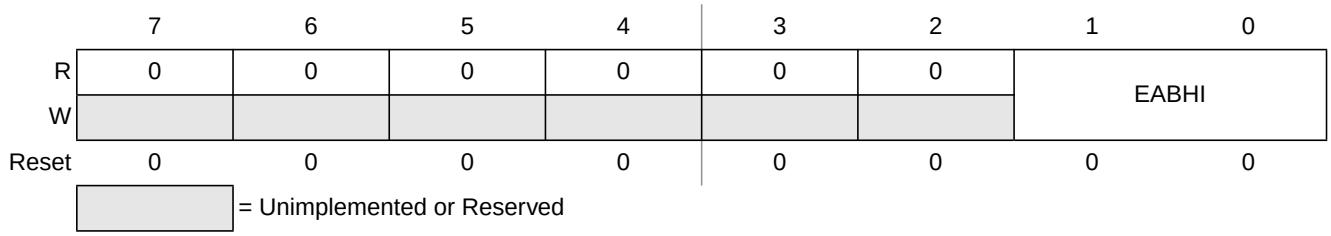


Figure 3-13. EEPROM Address High Register (EADDRHI)

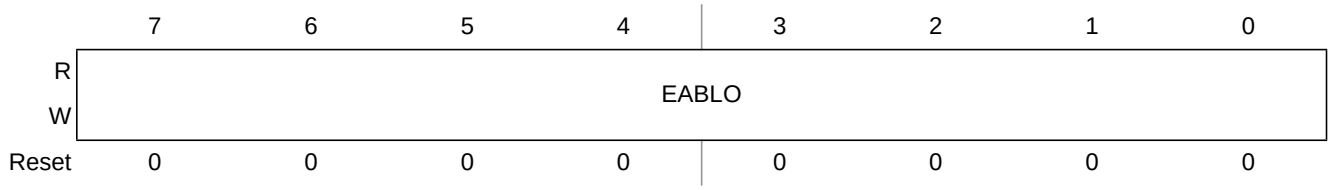


Figure 3-14. EEPROM Address Low Register (EADDRLO)

In normal modes, all EADDRHI and EADDRLO bits read 0 and are not writable.

In special modes, all EADDRHI and EADDRLO bits are readable and writable except EADDRHI[7:2] which are not writable and always read 0.

For sector erase, the MCU address bits AB[1:0] are ignored.

For mass erase, any address within the block is valid to start the command.

3.3.2.10 EEPROM Data Register (EDATA)

EDATAHI and EDATALO are the EEPROM data registers.

	7	6	5	4	3	2	1	0
R W	EDHI							
Reset	0	0	0	0	0	0	0	0

Figure 3-15. EEPROM Data High Register (EDATAHI)

	7	6	5	4	3	2	1	0
R W	EDLO							
Reset	0	0	0	0	0	0	0	0

Figure 3-16. EEPROM Data Low Register (EDATALO)

In normal modes, all EDATAHI and EDATALO bits read 0 and are not writable.

In special modes, all EDATAHI and EDATALO bits are readable and writable.

3.4 Functional Description

3.4.1 Program and Erase Operation

Write and read operations are both used for the program and erase algorithms described in this subsection. These algorithms are controlled by a state machine whose timebase, EECLK, is derived from the oscillator clock via a programmable divider. The command register as well as the associated address and data registers operate as a buffer and a register (2-stage FIFO) so that a new command along with the necessary data and address can be stored to the buffer while the previous command is remains in progress. The pipelined operation allows a simplification of command launching. Buffer empty as well as command completion are signalled by flags in the EEPROM status register. Interrupts for the EEPROM will be generated if enabled.

The next four subsections describe:

- How to write the ECLKDIV register.
- Command write sequences used to program, erase, and verify the EEPROM memory.
- Valid EEPROM commands.
- Errors resulting from illegal EEPROM operations.

3.4.1.1 Writing the ECLKDIV Register

Prior to issuing any program or erase command, it is first necessary to write the ECLKDIV register to divide the oscillator down to within 150 kHz to 200 kHz range. The program and erase timings are also a

function of the bus clock, such that the ECLKDIV determination must take this information into account. If we define:

- EECLK as the clock of the EEPROM timing control block
- Tbus as the period of the bus clock
- INT(x) as taking the integer part of x (e.g., INT(4.323)=4), then ECLKDIV register bits PRDIV8 and EDIV[5:0] are to be set as described in Figure 3-17.

For example, if the oscillator clock is 950 kHz and the bus clock is 10 MHz, ECLKDIV bits EDIV[5:0] must be set to 4 (binary 000100) and bit PRDIV8 set to 0. The resulting EECLK is then 190 kHz. As a result, the EEPROM algorithm timings are increased over optimum target by:

$$(200 - 190) / 200 \times 100 \; = \; 5\%$$

Command execution time will increase proportionally with the period of EECLK.

CAUTION

Because of the impact of clock synchronization on the accuracy of the functional timings, programming or erasing the EEPROM cannot be performed if the bus clock runs at less than 1 MHz. Programming the EEPROM with an oscillator clock < 150 kHz must be avoided. Setting ECLKDIV to a value such that EECLK < 150 kHz can reduce the lifetime of the EEPROM due to overstress. Setting ECLKDIV to a value such that (1/EECLK+Tbus) < 5µs can result in incomplete programming or erasure of the memory array cells.

If the ECLKDIV register is written, the bit EDIVLD is set automatically. If this bit is 0, the register has not been written since the last reset. EEPROM commands will not be executed if this register has not been written to.

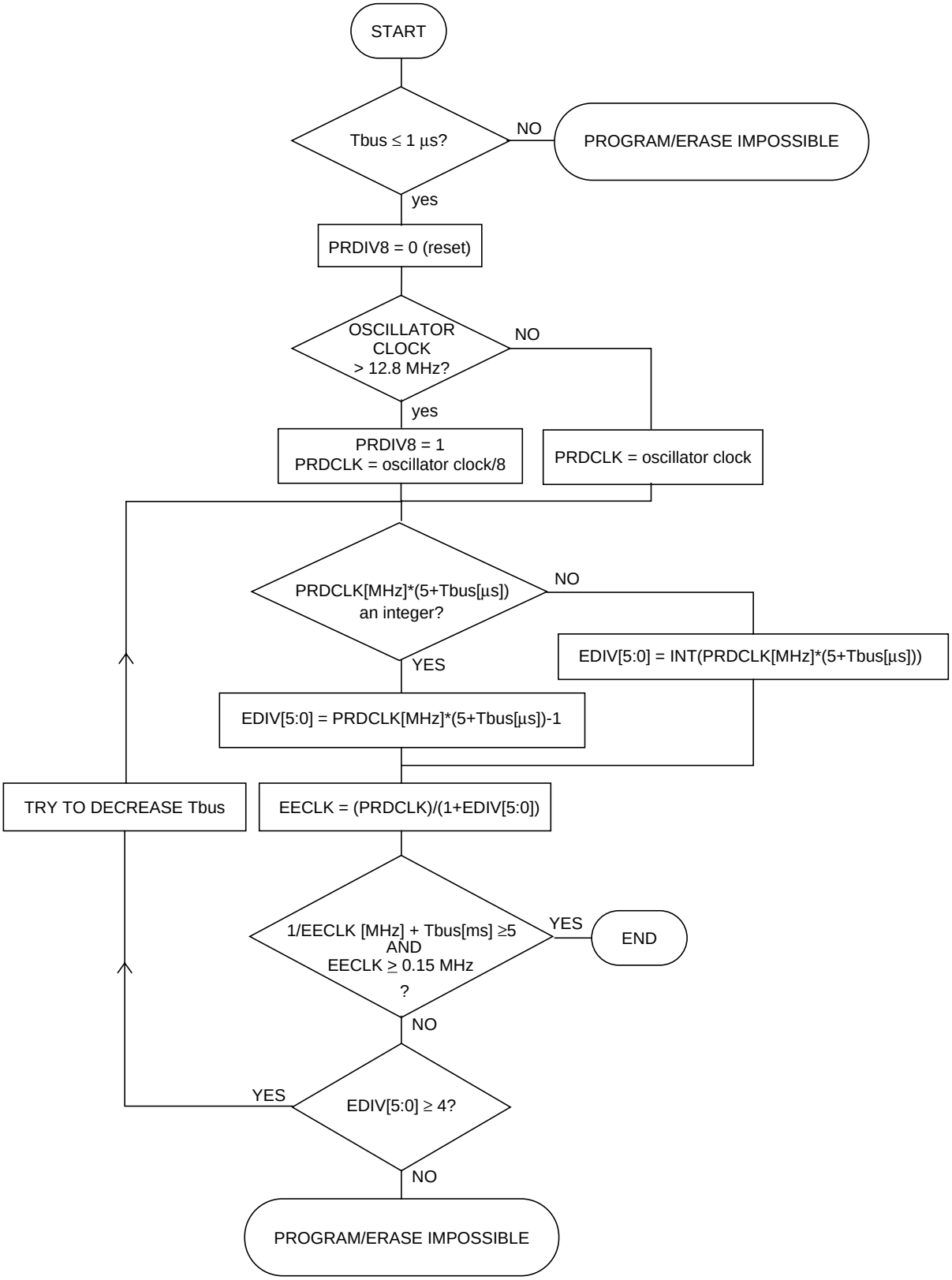


Figure 3-17. PRDIV8 and EDIV Bits Determination Procedure

3.4.1.2 Command Write Sequence

The EEPROM command controller is used to supervise the command write sequence to execute program, erase, mass erase, sector modify, and erase verify operations. Before starting a command write sequence, it is necessary to check that there is no pending access error or protection violation (the ACCERR and PVIOL flags must be cleared in the ESTAT register).

After this initial step, the CBEIF flag must be tested to ensure that the address, data and command buffers are empty. If so, the command sequence can be started. The following 3-step command write sequence must be strictly adhered to and no intermediate access to the EEPROM array is permitted between the 3 steps. It is possible to read any EEPROM register during a command sequence. The command write sequence is as follows:

1. Write an aligned word to be to a valid EEPROM array address. The address and data will be stored in internal buffers.
   - For program and sector modify, all address and data bits are valid.
   - For erase, the value of the data bytes are ignored.
   - For mass erase and erase verify, the address can be anywhere in the available address space of the array.
   - For sector erase, the address bits[1:0] are ignored.
2. Write a valid command, listed in Table 3-10, to the ECMD register.
3. Clear the CBEIF flag by writing a 1 to CBEIF to launch the command. When the CBEIF flag is cleared, the CCIF flag is cleared by hardware indicating that the command was successfully launched. The CBEIF flag will be set again indicating the address, data, and command buffers are ready for a new command write sequence to begin.

The completion of the command is indicated by the CCIF flag setting. The CCIF flag only sets when all active and pending commands have been completed.

The EEPROM command controller will flag errors in command write sequences by means of the ACCERR (access error) and PVIOL (protection violation) flags in the ESTAT register. An erroneous command write sequence will abort and set the appropriate flag. If set, the user must clear the ACCERR or PVIOL flags before commencing another command write sequence. By writing a 0 to the CBEIF flag the command sequence can be aborted after the word write to the EEPROM address space or after writing a command to the ECMD register and before the command is launched. Writing a 0 to the CBEIF flag in this way will set the ACCERR flag.

A summary of the launching of a program operation is shown in Figure 3-18. For other operations, the user writes the appropriate command to the ECMD register.

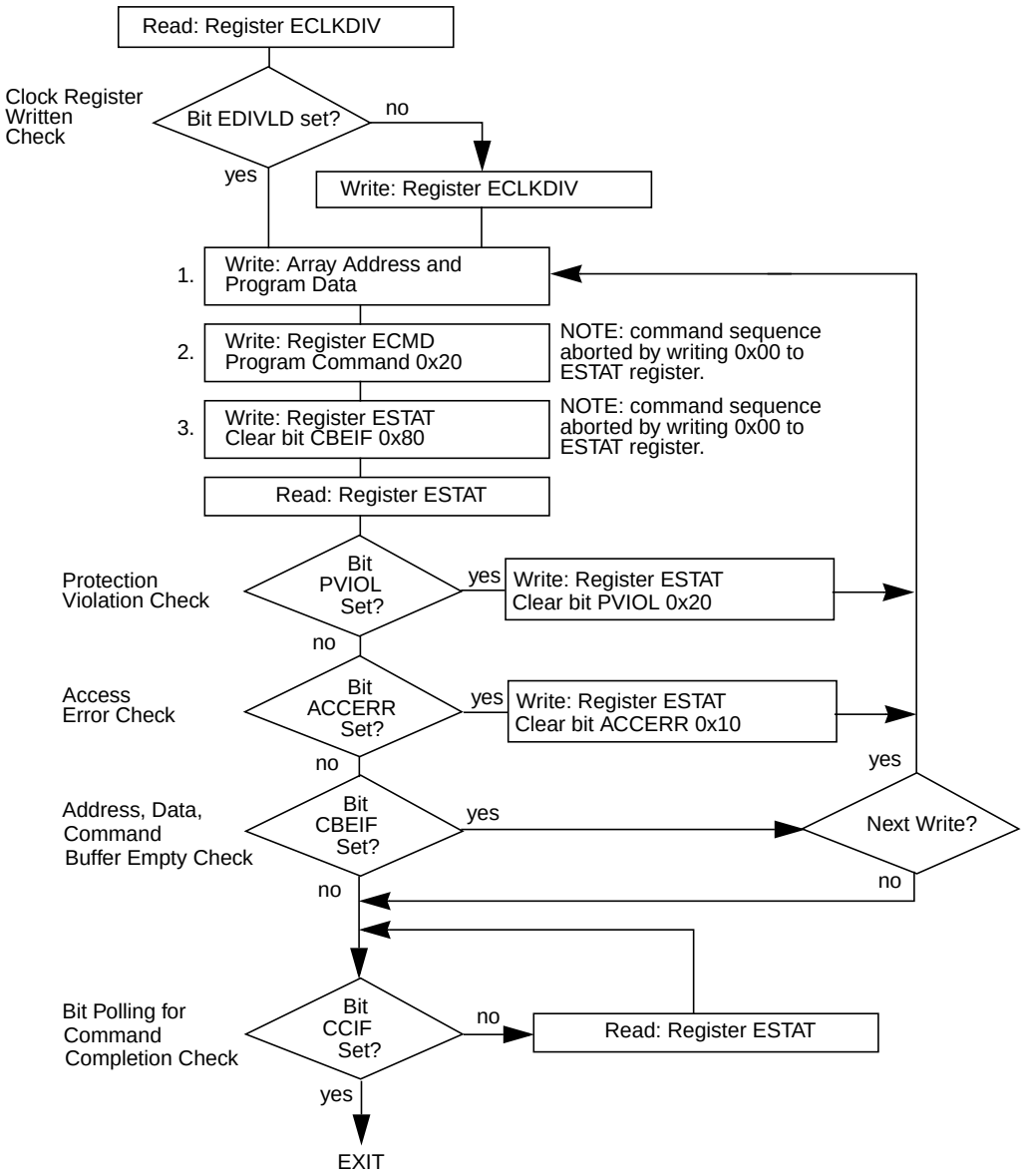


Figure 3-18. Example Program Command Flow

3.4.1.3 Valid EEPROM Commands

Table 3-10 summarizes the valid EEPROM commands. Also shown are the effects of the commands on the EEPROM array.

Table 3-10. Valid EEPROM Commands

ECMD	Meaning	Function on EEPROM Array
0x05	Erase Verify	Verify all memory bytes of the EEPROM array are erased. If the array is erased, the BLANK bit will set in the ESTAT register upon command completion.
0x20	Program	Program a word (two bytes).
0x40	Sector Erase	Erase two words (four bytes) of EEPROM array.
0x41	Mass Erase	Erase all of the EEPROM array. A mass erase of the full array is only possible when EPDIS and EPOPEN are set.
0x60	Sector Modify	Erase two words of EEPROM, re-program one word.

CAUTION

An EEPROM word must be in an erased state before being programmed. Cumulative programming of bits within a word is not allowed.

The sector modify command (0x60) is a two-step command which first erases a sector (2 words) of the EEPROM array and then re-programs one of the words in that sector. The EEPROM sector which is erased by the sector modify command is the sector containing the address of the aligned array write which starts the valid command sequence. That same address is re-programmed with the data which is written. By launching a sector modify command and then pipelining a program command it is possible to completely replace the contents of an EEPROM sector.

3.4.1.4 Illegal EEPROM Operations

The ACCERR flag will be set during the command write sequence if any of the following illegal operations are performed causing the command write sequence to immediately abort:

1. Writing to the EEPROM address space before initializing ECLKDIV.
2. Writing a misaligned word or a byte to the valid EEPROM address space.
3. Writing to the EEPROM address space while CBEIF is not set.
4. Writing a second word to the EEPROM address space before executing a program or erase command on the previously written word.
5. Writing to any EEPROM register other than ECMD after writing a word to the EEPROM address space.
6. Writing a second command to the ECMD register before executing the previously written command.
7. Writing an invalid command to the ECMD register in normal mode.
8. Writing to any EEPROM register other than ESTAT (to clear CBEIF) after writing to the command register (ECMD).

9. The part enters stop mode and a program or erase command is in progress. The command is aborted and any pending command is killed.
10. A 0 is written to the CBEIF bit in the ESTAT register.

The ACCERR flag will not be set if any EEPROM register is read during the command sequence.

If the EEPROM array is read during execution of an algorithm (i.e., CCIF bit in the ESTAT register is low), the read will return non-valid data and the ACCERR flag will not be set.

When an ACCERR flag is set in the ESTAT register, the command state machine is locked. It is not possible to launch another command until the ACCERR flag is cleared.

The PVIOL flag will be set during the command write sequence after the word write to the EEPROM address space and the command sequence will be aborted if any of the following illegal operations are performed.

1. Writing a EEPROM address to program in a protected area of the EEPROM.
2. Writing a EEPROM address to erase in a protected area of the EEPROM.
3. Writing the mass erase command to ECMD while any protection is enabled.

When the PVIOL flag is set in the ESTAT register the command state machine is locked. It is not possible to launch another command until the PVIOL flag is cleared.

3.5 Operating Modes

3.5.1 Wait Mode

If an EEPROM command is active (CCIF = 0) when the MCU enters wait mode, that command and any pending command will be completed.

The EETS2K module can recover the MCU from wait mode if the interrupts are enabled (see Section 3.7, “Interrupts”).

3.5.2 Stop Mode

If a command is active (CCIF = 0) when the MCU enters stop mode, the operation will be aborted and if the operation is program, erase, or sector modify, the data being programmed or erased may be corrupted and the CCIF and ACCERR flags will be set. If active, the high voltage circuitry to the EEPROM array will be switched off when entering stop mode. Upon exit from stop mode, the CBEIF flag is set and any pending command will not be launched. The ACCERR flag must be cleared before starting a new command write sequence.

NOTE

As active commands are immediately aborted when the MCU enters stop mode, it is strongly recommended that the user does not use the STOP instruction during program, erase, or sector modify operations.

3.5.3 Background Debug Mode

In background debug mode (BDM), the EPROT register is writable. If the chip is unsecured then all EEPROM commands listed in Table 3-10 can be executed. If the chip is secured in special single-chip mode, then the only possible command to execute is mass erase.

3.6 Resets

If a reset occurs while any EEPROM command is in progress, that command will be immediately aborted. The state of the word being programmed or the sector / block being erased is not guaranteed.

3.7 Interrupts

The EEPROM module can generate an interrupt when all EEPROM commands are completed or the address, data, and command buffers are empty.

Table 3-11. EEPROM Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
EEPROM address, data and command buffers empty	CBEIF (ESTAT register)	CBEIE	I Bit
All commands are completed on EEPROM	CCIF (ESTAT register)	CCIE	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

For a detailed description of the register bits, refer to Section 3.3.2.4, “EEPROM Configuration Register (ECNFG)” and Section 3.3.2.6, “EEPROM Status Register (ESTAT)”.

Chapter 4
Port Integration Module (PIM9HZ256V2)

4.1 Introduction

The port integration module establishes the interface between the peripheral modules and the I/O pins for for ports AD, L, M, P, T, U and V.

This section covers:

- Port A, B, E, and K and the BKGD pin, which are shared between the core logic (including multiplexed bus interface) and the LCD driver
- Port AD associated with ATD module (channels 7 through 0) and keyboard wake-up interrupts
- Port L connected to the LCD driver and ATD (channels 15 through 8) modules
- Port M connected to 2 CAN modules
- Port P connected to 1 SCI, 1 IIC and PWM modules
- Port S connected to 1 SCI and 1 SPI modules
- Port T connected to the timer module (TIM) and the LCD driver
- Port U and V associated with PWM motor control and stepper stall detect modules

Each I/O pin can be configured by several registers: input/output selection, drive strength reduction, enable and select of pull resistors, wired-or mode selection, interrupt enable, and/or status flags.

NOTE

Ports A, B, E and K, and the BKGD pin are shared between core logic (including multiplexed bus interface) and the LCD driver. Refer to the MEBI block description chapter for details on these ports.

4.1.1 Features

A standard port has the following minimum features:

- Input/output selection
- 5-V output drive with two selectable drive strength (or slew rates)
- 5-V digital and analog input
- Input with selectable pull-up or pull-down device

Optional features:

- Open drain for wired-OR connections
- Interrupt input with glitch filtering

4.1.2 Block Diagram

Figure 4-1 is a block diagram of the PIM9HZ256.

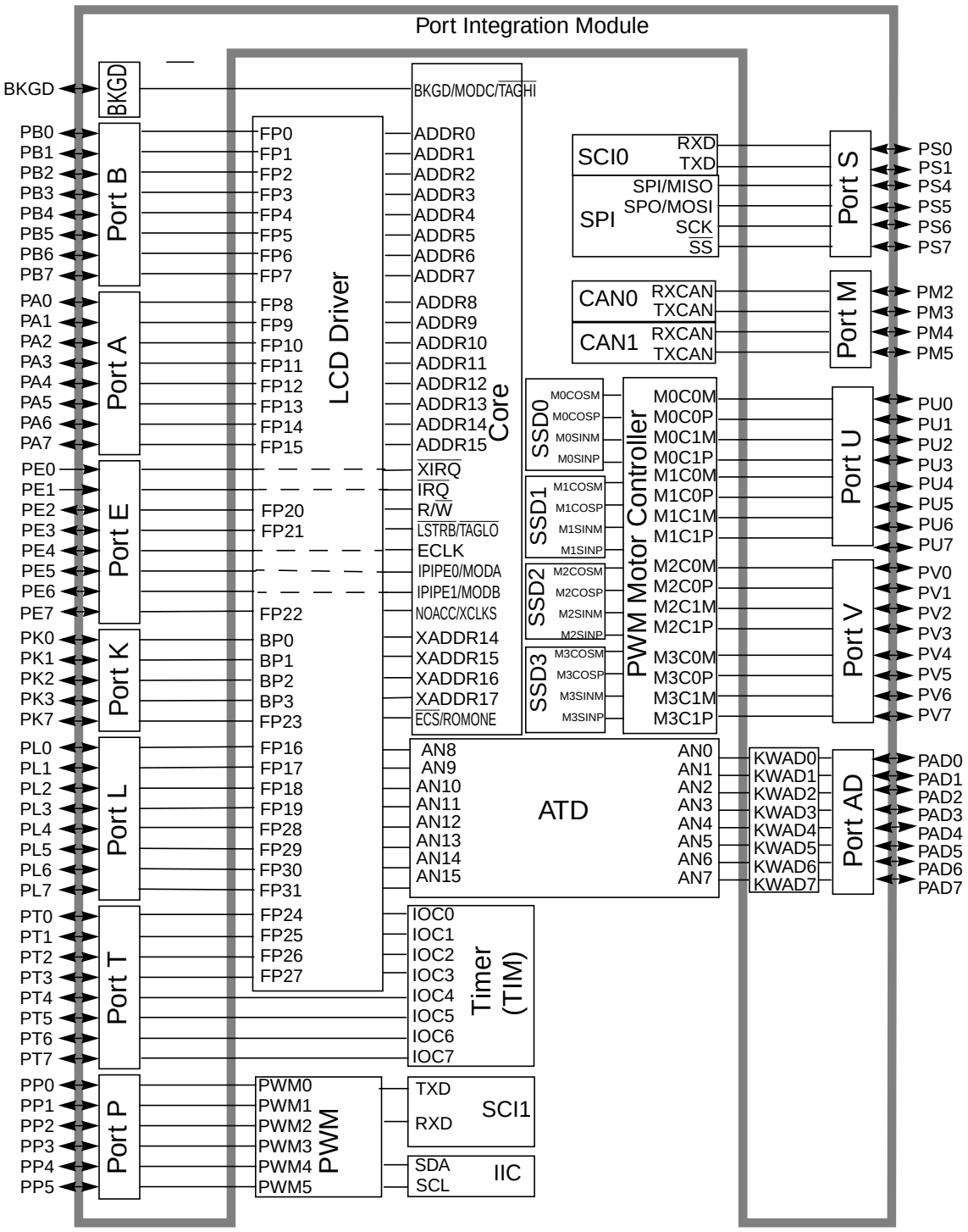


Figure 4-1. PIM9HZ256 Block Diagram

4.2 External Signal Description

This section lists and describes the signals that connect off chip.

Table 4-1 shows all the pins and their functions that are controlled by the PIM9HZ256. The order in which the pin functions are listed represents the functions priority (top – highest priority, bottom – lowest priority).

Table 4-1. Detailed Signal Descriptions (Sheet 1 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
—	BKGD	MODC	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		BKGD	Refer to the BDM block description chapter	
		$\overline{\text{TAGHI}}$	Refer to the MEBI block description chapter	
Port K	PK7	$\overline{\text{ECS}}$/ROMONE	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		FP23	LCD driver interface	
		GPIO	General-purpose I/O	
	PK3	XADDR17	Refer to the MEBI block description chapter	
		BP3	LCD driver interface	
		GPIO	General-purpose I/O	
	PK2	XADDR16	Refer to the MEBI block description chapter	
		BP2	LCD driver interface	
		GPIO	General-purpose I/O	
	PK1	XADDR15	Refer to the MEBI block description chapter	
		BP1	LCD driver interface	
		GPIO	General-purpose I/O	
	PK0	XADDR14	Refer to the MEBI block description chapter	
		BP0	LCD driver interface	
		GPIO	General-purpose I/O	
Port E	PE7	XCLKS	Refer to OSC block description chapter	Refer to the MEBI block description chapter
		NOACC	Refer to the MEBI block description chapter	
		FP22	LCD driver interface	
		GPIO	General-purpose I/O	
	PE6	IPIPE1/MODB	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PE5	IPIPE0/MODA	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PE4	ECLK	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PE3	$\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$	Refer to the MEBI block description chapter	
		FP21	LCD driver interface	
		GPIO	General-purpose I/O	
	PE2	FP20	LCD driver interface	
		R/$\overline{\text{W}}$/GPIO	Refer to the MEBI block description chapter	
	PE1	$\overline{\text{IRQ}}$	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	
	PE0	$\overline{\text{XIRQ}}$	Refer to the MEBI block description chapter	
		GPIO	General-purpose I/O	

Table 4-1. Detailed Signal Descriptions (Sheet 2 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port A	PA7	ADDR15/DATA15	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		FP15	LCD driver interface	
		GPIO	General-purpose I/O	
	PA6	ADDR14/DATA14	Refer to the MEBI block description chapter	
		FP14	LCD driver interface	
		GPIO	General-purpose I/O	
	PA5	ADDR13/DATA13	Refer to the MEBI block description chapter	
		FP13	LCD driver interface	
		GPIO	General-purpose I/O	
	PA4	ADDR12/DATA12	Refer to the MEBI block description chapter	
		FP12	LCD driver interface	
		GPIO	General-purpose I/O	
	PA3	ADDR11/DATA11	Refer to the MEBI block description chapter	
		FP11	LCD driver interface	
		GPIO	General-purpose I/O	
	PA2	ADDR10/DATA10	Refer to the MEBI block description chapter	
		FP10	LCD driver interface	
		GPIO	General-purpose I/O	
	PA1	ADDR9/DATA9	Refer to the MEBI block description chapter	
		FP9	LCD driver interface	
		GPIO	General-purpose I/O	
	PA0	ADDR8/DATA8	Refer to the MEBI block description chapter	
		FP8	LCD driver interface	
		GPIO	General-purpose I/O	
Port B	PB7	ADDR7/DATA7	Refer to the MEBI block description chapter	Refer to the MEBI block description chapter
		FP7	LCD driver interface	
		GPIO	General-purpose I/O	
	PB6	ADDR6/DATA6	Refer to the MEBI block description chapter	
		FP6	LCD driver interface	
		GPIO	General-purpose I/O	
	PB5	ADDR5/DATA5	Refer to the MEBI block description chapter	
		FP5	LCD driver interface	
		GPIO	General-purpose I/O	
	PB4	ADDR4/DATA4	Refer to the MEBI block description chapter	
		FP4	LCD driver interface	
		GPIO	General-purpose I/O	
	PB3	ADDR3/DATA3	Refer to the MEBI block description chapter	
		FP3	LCD driver interface	
		GPIO	General-purpose I/O	
	PB2	ADDR2/DATA2	Refer to the MEBI block description chapter	
		FP2	LCD driver interface	
		GPIO	General-purpose I/O	
	PB1	ADDR1/DATA1	Refer to the MEBI block description chapter	
		FP1	LCD driver interface	
		GPIO	General-purpose I/O	
	PB0	ADDR0/DATA0	Refer to the MEBI block description chapter	
		FP0	LCD driver interface	
		GPIO	General-purpose I/O	

Table 4-1. Detailed Signal Descriptions (Sheet 3 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port AD	PAD7	AN7	Analog-to-digital converter input channel 7	GPIO
		KWAD7	Keyboard wake-up interrupt 7	
		GPIO	General-purpose I/O	
	PAD6	AN6	Analog-to-digital converter input channel 6	
		KWAD6	Keyboard wake-up interrupt 6	
		GPIO	General-purpose I/O	
	PAD5	AN5	Analog-to-digital converter input channel 5	
		KWAD5	Keyboard wake-up interrupt 5	
		GPIO	General-purpose I/O	
	PAD4	AN4	Analog-to-digital converter input channel 4	
		KWAD4	Keyboard wake-up interrupt 4	
		GPIO	General-purpose I/O	
	PAD3	AN3	Analog-to-digital converter input channel 3	
		KWAD3	Keyboard wake-up interrupt 3	
		GPIO	General-purpose I/O	
	PAD2	AN2	Analog-to-digital converter input channel 2	
		KWAD2	Keyboard wake-up interrupt 2	
		GPIO	General-purpose I/O	
	PAD1	AN1	Analog-to-digital converter input channel 1	
		KWAD1	Keyboard wake-up interrupt 1	
		GPIO	General-purpose I/O	
	PAD0	AN0	Analog-to-digital converter input channel 0	
		KWAD0	Keyboard wake-up interrupt 0	
		GPIO	General-purpose I/O	
Port L	PL7	FP31	LCD driver interface	GPIO
		AN15	Analog-to-digital converter input channel 15	
		GPIO	General-purpose I/O	
	PL6	FP30	LCD driver interface	
		AN14	Analog-to-digital converter input channel 14	
		GPIO	General-purpose I/O	
	PL5	FP29	LCD driver interface	
		AN13	Analog-to-digital converter input channel 13	
		GPIO	General-purpose I/O	
	PL4	FP28	LCD driver interface	
		AN12	Analog-to-digital converter input channel 12	
		GPIO	General-purpose I/O	
	PL3	FP19	LCD driver interface	
		AN11	Analog-to-digital converter input channel 11	
		GPIO	General-purpose I/O	
	PL2	FP18	LCD driver interface	
		AN10	Analog-to-digital converter input channel 10	
		GPIO	General-purpose I/O	
	PL1	FP17	LCD driver interface	
		AN9	Analog-to-digital converter input channel 9	
		GPIO	General-purpose I/O	
	PL0	FP16	LCD driver interface	
		AN8	Analog-to-digital converter input channel 8	
		GPIO	General-purpose I/O	

Table 4-1. Detailed Signal Descriptions (Sheet 4 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port M	PM5	TXCAN1	MSCAN1 transmit pin	GPIO
		GPIO	General-purpose I/O	
	PM4	RXCAN1	MSCAN1 receive pin	
		GPIO	General-purpose I/O	
	PM3	TXCAN0	MSCAN0 transmit pin	
		GPIO	General-purpose I/O	
	PM2	RXCAN0	MSCAN0 receive pin	
		GPIO	General-purpose I/O	
Port P	PP5	PWM5	Pulse-width modulator channel 5	GPIO
		SCL	Inter-integrated circuit serial clock line	
		GPIO	General-purpose I/O	
	PP4	PWM4	Pulse-width modulator channel 4	
		SDA	Inter-integrated circuit serial data line	
		GPIO	General-purpose I/O	
	PP3	PWM3	Pulse-width modulator channel 3	
		GPIO	General-purpose I/O	
	PP2	PWM2	Pulse-width modulator channel 2	
		RXD1	Serial communication interface 1 receive pin	
		GPIO	General-purpose I/O	
	PP1	PWM1	Pulse-width modulator channel 1	
		GPIO	General-purpose I/O	
	PP0	PWM0	Pulse-width modulator channel 0	
		TXD1	Serial communication interface 1 transmit pin	
		GPIO	General-purpose I/O	
Port S	PS7	$\overline{SS}$	Serial peripheral interface slave select input/output in master mode, input in slave mode	GPIO
		GPIO	General-purpose I/O	
	PS6	SCK	Serial peripheral interface serial clock pin	
		GPIO	General-purpose I/O	
	PS5	MOSI	Serial peripheral interface master out/slave in pin	
		GPIO	General-purpose I/O	
	PS4	MISO	Serial peripheral interface master in/slave out pin	
		GPIO	General-purpose I/O	
	PS1	TXD0	Serial communication interface 0 transmit pin	
		GPIO	General-purpose I/O	
	PS0	RXD0	Serial communication interface 0 receive pin	
		GPIO	General-purpose I/O	

Table 4-1. Detailed Signal Descriptions (Sheet 5 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port T	PT7	IOC7	Timer channel 7	GPIO
		GPIO	General-purpose I/O	
	PT6	IOC6	Timer channel 6	
		GPIO	General-purpose I/O	
	PT5	IOC5	Timer channel 5	
		GPIO	General-purpose I/O	
	PT4	IOC4	Timer channel 4	
		GPIO	General-purpose I/O	
	PT3	FP27	LCD driver interface	
		IOC3	Timer channel 3	
		GPIO	General-purpose I/O	
	PT2	FP26	LCD driver interface	
		IOC2	Timer channel 2	
		GPIO	General-purpose I/O	
	PT1	FP25	LCD driver interface	
		IOC1	Timer channel 1	
		GPIO	General-purpose I/O	
	PT0	FP24	LCD driver interface	
		IOC0	Timer channel 0	
		GPIO	General-purpose I/O	
Port U	PU7	M1SINP	SSD1 Sine+ Node	GPIO
		M1C1P	PWM motor controller channel 3	
		GPIO	General-purpose I/O	
	PU6	M1SINM	SSD1 Sine- Node	
		M1C1M	PWM motor controller channel 3	
		GPIO	General-purpose I/O	
	PU5	M1COSP	SSD1 Cosine+ Node	
		M1C0P	PWM motor controller channel 2	
		GPIO	General-purpose I/O	
	PU4	M1COSM	SSD1 Cosine- Node	
		M1C0M	PWM motor controller channel 2	
		GPIO	General-purpose I/O	
	PU3	M0SINP	SSD0 Sine+ Node	
		M0C1P	PWM motor controller channel 1	
		GPIO	General-purpose I/O	
	PU2	M0SINM	SSD0 Sine- Node	
		M0C1M	PWM motor controller channel 1	
		GPIO	General-purpose I/O	
	PU1	M0COSP	SSD0 Cosine+ Node	
		M0C0P	PWM motor controller channel 0	
		GPIO	General-purpose I/O	
	PU0	M0COSM	SSD0 Cosine- Node	
		M0C0M	PWM motor controller channel 0	
		GPIO	General-purpose I/O	

Table 4-1. Detailed Signal Descriptions (Sheet 6 of 6)

Port	Pin Name	Pin Function	Description	Pin Function after Reset
Port V	PV7	M3SINP	SSD3 sine+ node	GPIO
		M3C1P	PWM motor controller channel 7	
		GPIO	General-purpose I/O	
	PV6	M3SINM	SSD3 sine- node	
		M3C1M	PWM motor controller channel 7	
		GPIO	General-purpose I/O	
	PV5	M3COSP	SSD3 cosine+ node	
		M3C0P	PWM motor controller channel 6	
		GPIO	General-purpose I/O	
	PV4	M3COSM	SSD3 cosine- node	
		M3C0M	PWM motor controller channel 6	
		GPIO	General-purpose I/O	
	PV3	M2SINP	SSD2 sine+ node	
		M2C1P	PWM motor controller channel 5	
		GPIO	General-purpose I/O	
	PV2	M2SINM	SSD2 sine- node	
		M2C1M	PWM motor controller channel 5	
		GPIO	General-purpose I/O	
	PV1	M2COSP	SSD2 cosine+ node	
		M2C0P	PWM motor controller channel 4	
		GPIO	General-purpose I/O	
	PV0	M2COSM	SSD2 cosine- node	
		M2C0M	PWM motor controller channel 4	
		GPIO	General-purpose I/O	

4.3 Memory Map and Register Definition

This section provides a detailed description of all registers. Table 4-2 is a standard memory map of port integration module.

Table 4-2. PIM9HZ256 Memory Map

Address Offset	Use	Access
0x0000	Port T I/O Register (PTT)	R/W
0x0001	Port T Input Register (PTIT)	R
0x0002	Port T Data Direction Register (DDRT)	R/W
0x0003	Port T Reduced Drive Register (RDRT)	R/W
0x0004	Port T Pull Device Enable Register (PERT)	R/W
0x0005	Port T Polarity Select Register (PPST)	R/W
0x0006 - 0x0007	Reserved	—
0x0008	Port S I/O Register (PTS)	R/W
0x0009	Port S Input Register (PTIS)	R
0x000A	Port S Data Direction Register (DDRS)	R/W
0x000B	Port S Reduced Drive Register (RDRS)	R/W
0x000C	Port S Pull Device Enable Register (PERS)	R/W
0x000D	Port S Polarity Select Register (PPSS)	R/W
0x000E	Port S Wired-OR Mode Register (WOMS)	R/W
0x000F	Reserved	—
0x0010	Port M I/O Register (PTM)	R/W
0x0011	Port M Input Register (PTIM)	R
0x0012	Port M Data Direction Register (DDRM)	R/W
0x0013	Port M Reduced Drive Register (RDRM)	R/W
0x0014	Port M Pull Device Enable Register (PERM)	R/W
0x0015	Port M Polarity Select Register (PPSM)	R/W
0x0016	Port M Wired-OR Mode Register (WOMM)	R/W
0x0017	Reserved	—
0x0018	Port P I/O Register (PTP)	R/W
0x0019	Port P Input Register (PTIP)	R
0x001A	Port P Data Direction Register (DDRP)	R/W
0x001B	Port P Reduced Drive Register (RDRP)	R/W
0x001C	Port P Pull Device Enable Register (PERP)	R/W
0x001D	Port P Polarity Select Register (PPSP)	R/W
0x001E	Port P Wired-OR Mode Register (WOMP)	R/W
0x001F - 0x002F	Reserved	—

Table 4-2. PIM9HZ256 Memory Map (continued)

Address Offset	Use	Access
0x0030	Port L I/O Register (PTL)	R/W
0x0031	Port L Input Register (PTIL)	R
0x0032	Port L Data Direction Register (DDRL)	R/W
0x0033	Port L Reduced Drive Register (RDRL)	R/W
0x0034	Port L Pull Device Enable Register (PERL)	R/W
0x0035	Port L Polarity Select Register (PPSL)	R/W
0x0036 - 0x0037	Reserved	—
0x0038	Port U I/O Register (PTU)	R/W
0x0039	Port U Input Register (PTIU)	R
0x003A	Port U Data Direction Register (DDRU)	R/W
0x003B	Port U Slew Rate Register (SRRU)	R/W
0x003C	Port U Pull Device Enable Register (PERU)	R/W
0x003D	Port U Polarity Select Register (PPSU)	R/W
0x003E - 0x003F	Reserved	—
0x0040	Port V I/O Register (PTV)	R/W
0x0041	Port V Input Register (PTIV)	R
0x0042	Port V Data Direction Register (DDRV)	R/W
0x0043	Port V Slew Rate Register (SRRV)	R/W
0x0044	Port V Pull Device Enable Register (PERV)	R/W
0x0045	Port V Polarity Select Register (PPSV)	R/W
0x0046 - 0x0050	Reserved	—
0x0051	Port AD I/O Register (PTAD)	R/W
0x0052	Reserved	—
0x0053	Port AD Input Register (PTIAD)	R
0x0054	Reserved	—
0x0055	Port AD Data Direction Register (DDRAD)	R/W
0x0056	Reserved	—
0x0057	Port AD Reduced Drive Register (RDRAD)	R/W
0x0058	Reserved	—
0x0059	Port AD Pull Device Enable Register (PERAD)	R/W
0x005A	Reserved	—
0x005B	Port AD Polarity Select Register (PPSAD)	R/W
0x005C	Reserved	—
0x005D	Port AD Interrupt Enable Register (PIEAD)	R/W
0x005E	Reserved	—
0x005F	Port AD Interrupt Flag Register (PIFAD)	R/W
0x0060 - 0x007F	Reserved	—

4.3.1 Port AD

Port AD is associated with the analog-to-digital converter (ATD) and keyboard wake-up (KWU) interrupts. Each pin is assigned to these modules according to the following priority: ATD > KWU > general-purpose I/O.

For the pins of port AD to be used as inputs, the corresponding bits of the ATDDIEN1 register in the ATD module must be set to 1 (digital input buffer is enabled). The ATDDIEN1 register does not affect the port AD pins when they are configured as outputs.

Refer to the ATD block description chapter for information on the ATDDIEN1 register.

During reset, port AD pins are configured as high-impedance analog inputs (digital input buffer is disabled).

4.3.1.1 Port AD I/O Register (PTAD)

	7	6	5	4	3	2	1	0
R W	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
KWU:	KWAD7	KWAD6	KWAD5	KWAD4	KWAD3	KWAD2	KWAD1	KWAD0
ATD:	AN7	AN6	AN55	AN4	AN3	AN2	AN1	AN0
Reset	0	0	0	0	0	0	0	0

Figure 4-2. Port AD I/O Register (PTAD)

Read: Anytime. Write: Anytime.

If the data direction bit of the associated I/O pin (DDRADx) is set to 1 (output), a write to the corresponding I/O Register bit sets the value to be driven to the Port AD pin. If the data direction bit of the associated I/O pin (DDRADx) is set to 0 (input), a write to the corresponding I/O Register bit takes place but has no effect on the Port AD pin.

If the associated data direction bit (DDRADx) is set to 1 (output), a read returns the value of the I/O register bit.

If the associated data direction bit (DDRADx) is set to 0 (input) and the associated ATDDIEN1 bits is set to 0 (digital input buffer is disabled), the associated I/O register bit (PTADx) reads “1”.

If the associated data direction bit (DDRADx) is set to 0 (input) and the associated ATDDIEN1 bits is set to 1 (digital input buffer is enabled), a read returns the value of the pin.

4.3.1.2 Port AD Input Register (PTIAD)

	7	6	5	4	3	2	1	0
R	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
W								
Reset	1	1	1	1	1	1	1	1

= Reserved or Unimplemented

Figure 4-3. Port AD Input Register (PTIAD)

Read: Anytime. Write: Never; writes to these registers have no effect.

If the ATDDIEN1 bit of the associated I/O pin is set to 0 (digital input buffer is disabled), a read returns a 1. If the ATDDIEN1 bit of the associated I/O pin is set to 1 (digital input buffer is enabled), a read returns the status of the associated pin.

4.3.1.3 Port AD Data Direction Register (DDRAD)

	7	6	5	4	3	2	1	0
R W	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-4. Port AD Data Direction Register (DDRAD)

Read: Anytime. Write: Anytime.

This register configures port pins PAD[7:0] as either input or output.

If a data direction bit is 0 (pin configured as input), then a read value on PTADx depends on the associated ATDDIEN1 bit. If the associated ATDDIEN1 bit is set to 1 (digital input buffer is enabled), a read on PTADx returns the value on port AD pin. If the associated ATDDIEN1 bit is set to 0 (digital input buffer is disabled), a read on PTADx returns a 1.

Table 4-3. DDRAD Field Descriptions

Field	Description
7:0 DDRAD[7:0]	**Data Direction Port AD** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.1.4 Port AD Reduced Drive Register (RDRAD)

	7	6	5	4	3	2	1	0
R W	RDRAD7	RDRAD6	RDRAD5	RDRAD4	RDRAD3	RDRAD2	RDRAD1	RDRAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-5. Port AD Reduced Drive Register (RDRAD)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-4. RDRAD Field Descriptions

Field	Description
7:0 RDRAD[7:0]	**Reduced Drive Port AD** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.1.5 Port AD Pull Device Enable Register (PERAD)

	7	6	5	4	3	2	1	0
R W	PERAD7	PERAD6	PERAD5	PERAD4	PERAD3	PERAD2	PERAD1	PERAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-6. Port AD Pull Device Enable Register (PERAD)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-5. PERAD Field Descriptions

Field	Description
7:0 PERAD[7:0]	**Pull Device Enable Port AD** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.1.6 Port AD Polarity Select Register (PPSAD)

	7	6	5	4	3	2	1	0
R W	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-7. Port AD Polarity Select Register (PPSAD)

Read: Anytime. Write: Anytime.

The Port AD Polarity Select Register serves a dual purpose by selecting the polarity of the active interrupt edge as well as selecting a pull-up or pull-down device if enabled (PERADx = 1). The Port AD Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input).

In pull-down mode (PPSADx = 1), a rising edge on a port AD pin sets the corresponding PIFADx bit. In pull-up mode (PPSADx = 0), a falling edge on a port AD pin sets the corresponding PIFADx bit.

Table 4-6. PPSAD Field Descriptions

Field	Description
7:0 PPSAD[7:0]	**Polarity Select Port AD** 0 A pull-up device is connected to the associated port AD pin, and detects falling edge for interrupt generation. 1 A pull-down device is connected to the associated port AD pin, and detects rising edge for interrupt generation.

4.3.1.7 Port AD Interrupt Enable Register (PIEAD)

	7	6	5	4	3	2	1	0
R W	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-8. Port AD Interrupt Enable Register (PIEAD)

Read: Anytime. Write: Anytime.

This register disables or enables on a per pin basis the edge sensitive external interrupt associated with port AD.

Table 4-7. PIEAD Field Descriptions

Field	Description
7:0 PIEAD[7:0]	**Interrupt Enable Port AD** 0 Interrupt is disabled (interrupt flag masked). 1 Interrupt is enabled.

4.3.1.8 Port AD Interrupt Flag Register (PIFAD)

	7	6	5	4	3	2	1	0
R W	PIFAD7	PIFAD6	PIFAD5	PIFAD4	PIFAD3	PIFAD2	PIFAD1	PIFAD0
Reset	0	0	0	0	0	0	0	0

Figure 4-9. Port AD Interrupt Flag Register (PIFAD)

Read: Anytime. Write: Anytime.

Each flag is set by an active edge on the associated input pin. The active edge could be rising or falling based on the state of the corresponding PPSADx bit. To clear each flag, write “1” to the corresponding PIFADx bit. Writing a “0” has no effect.

NOTE

If the ATDDIEN1 bit of the associated pin is set to 0 (digital input buffer is disabled), active edges can not be detected.

Table 4-8. PIFAD Field Descriptions

Field	Description
7:0 PIFAD[7:0]	**Interrupt Flags Port AD** 0 No active edge pending. Writing a “0” has no effect. 1 Active edge on the associated bit has occurred (an interrupt will occur if the associated enable bit is set). Writing a “1” clears the associated flag.

4.3.2 Port L

Port L is associated with the analog-to-digital converter (ATD) and the liquid crystal display (LCD) driver.

If the ATD module is enabled, the AN[15:8] inputs of ATD module are available on port L pins PL[7:0].

If the corresponding LCD frontplane drivers are enabled, the FP[31:29] and FP[19:16] outputs of LCD module are available on port L pins PL[7:0] and the general purpose I/Os are disabled.

For the pins of port L to be used as inputs, the corresponding LCD frontplane drivers must be disabled and the associated ATDDIEN0 register in the ATD module must be set to 1 (digital input buffer is enabled). The ATDDIEN0 register does not affect the port L pins when they are configured as outputs.

Refer to the LCD block description chapter for information on enabling and disabling the LCD and its frontplane drivers. Refer to the ATD block description chapter for information on the ATDDIEN0 register.

During reset, port L pins are configured as inputs with pull down.

4.3.2.1 Port L I/O Register (PTL)

	7	6	5	4	3	2	1	0
R W	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
ATD:	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8
LCD:	1	1	1	1	1	1	1	1
Reset	0	0	0	0	0	0	0	0

Figure 4-10. Port L I/O Register (PTL)

Read: Anytime. Write: Anytime.

If the data direction bit of the associated I/O pin (DDRLx) is set to 1 (output), a write to the corresponding I/O Register bit sets the value to be driven to the Port L pin. If the data direction bit of the associated I/O pin (DDRLx) is set to 0 (input), a write to the corresponding I/O Register bit takes place but has no effect on the Port L pin.

If the associated data direction bit (DDRLx) is set to 1 (output), a read returns the value of the I/O register bit.

If the associated data direction bit (DDRLx) is set to 0 (input) and the associated ATDDIEN0 bits is set to 0 (digital input buffer is disabled), the associated I/O register bit (PTLx) reads “1”.

If the associated data direction bit (DDRLx) is set to 0 (input), the associated ATDDIEN0 bit is set to 1 (digital input buffer is enabled), and the LCD frontplane driver is enabled (and LCD module is enabled), the associated I/O register bit (PTLx) reads “1”.

If the associated data direction bit (DDRLx) is set to 0 (input), the associated ATDDIEN0 bit is set to 1 (digital input buffer is enabled), and the LCD frontplane driver is disabled (or LCD module is disabled), a read returns the value of the pin.

4.3.2.2 Port L Input Register (PTIL)

	7	6	5	4	3	2	1	0
R	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
W								
Reset	1	1	1	1	1	1	1	1

= Reserved or Unimplemented

Figure 4-11. Port L Input Register (PTIL)

Read: Anytime. Write: Never, writes to this register have no effect.

If the LCD frontplane driver of an associated I/O pin is enabled (and LCD module is enabled) or the associated ATDDIEN0 bit is set to 0 (digital input buffer is disabled), a read returns a 1.

If the LCD frontplane driver of an associated I/O pin is disabled (or LCD module is disabled) and the associated ATDDIEN0 bit is set to 1 (digital input buffer is enabled), a read returns the status of the associated pin.

4.3.2.3 Port L Data Direction Register (DDRL)

	7	6	5	4	3	2	1	0
R W	DDRL7	DDRL6	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
Reset	0	0	0	0	0	0	0	0

Figure 4-12. Port L Data Direction Register (DDRL)

Read: Anytime. Write: Anytime.

This register configures port pins PL[7:0] as either input or output.

If a LCD frontplane driver is enabled (and LCD module is enabled), it outputs an analog signal to the corresponding pin and the associated Data Direction Register bit has no effect. If a LCD frontplane driver is disabled (or LCD module is disabled), the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

Table 4-9. DDRL Field Descriptions

Field	Description
7:0 DDRL[7:0]	**Data Direction Port L** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.2.4 Port L Reduced Drive Register (RDRL)

	7	6	5	4	3	2	1	0
R W	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
Reset	0	0	0	0	0	0	0	0

Figure 4-13. Port L Reduced Drive Register (RDRL)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-10. RDRL Field Descriptions

Field	Description
7:0 RDRL[7:0]	**Reduced Drive Port L** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.2.5 Port L Pull Device Enable Register (PERL)

	7	6	5	4	3	2	1	0
R W	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
Reset	1	1	1	1	1	1	1	1

Figure 4-14. Port L Pull Device Enable Register (PERL)

Read:Anytime. Write:Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-11. PERL Field Descriptions

Field	Description
7:0 PERL[7:0]	**Pull Device Enable Port L** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.2.6 Port L Polarity Select Register (PPSL)

	7	6	5	4	3	2	1	0
R W	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
Reset	1	1	1	1	1	1	1	1

Figure 4-15. Port L Polarity Select Register (PPSL)

Read: Anytime. Write: Anytime.

The Port L Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port L Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-12. PPSL Field Descriptions

Field	Description
7:0 PPSL[7:0]	**Pull Select Port L** 0 A pull-up device is connected to the associated port L pin. 1 A pull-down device is connected to the associated port L pin.

4.3.3 Port M

Port M is associated with Freescale's scalable controller area network (CAN1 and CAN0) modules. Each pin is assigned to these modules according to the following priority: CAN1/CAN0 > general-purpose I/O.

When the CAN1 module is enabled, PM[5:4] pins become TXCAN1 (transmitter) and RXCAN1 (receiver) pins for the CAN1 module. When the CAN0 module is enabled, PM[3:2] pins become TXCAN0 (transmitter) and RXCAN0 (receiver) pins for the CAN0 module. Refer to the MSCAN block description chapter for information on enabling and disabling the CAN module.

During reset, port M pins are configured as high-impedance inputs.

4.3.3.1 Port M I/O Register (PTM)

	7	6	5	4	3	2	1	0
R	0	0	PTM5	PTM4	PTM3	PTM2	0	0
W								
CAN0/CAN1:			TXCAN1	RXCAN1	TXCAN0	RXCAN0		
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-16. Port M I/O Register (PTM)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRMx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRMx) is set to 0 (input), a read returns the value of the pin.

4.3.3.2 Port M Input Register (PTIM)

	7	6	5	4	3	2	1	0
R	0	0	PTIM5	PTIM4	PTIM3	PTIM2	0	0
W								
Reset	0	0	u	u	u	u	0	0

= Reserved or Unimplemented u = Unaffected by reset

Figure 4-17. Port M Input Register (PTIM)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

4.3.3.3 Port M Data Direction Register (DDRM)

	7	6	5	4	3	2	1	0
R	0	0	DDRM5	DDRM4	DDRM3	DDRM2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-18. Port M Data Direction Register (DDRM)

Read: Anytime. Write: Anytime.

This register configures port pins PM[5:2] as either input or output.

When a CAN module is enabled, the corresponding transmitter (TXCANx) pin becomes an output, the corresponding receiver (RXCANx) pin becomes an input, and the associated Data Direction Register bits have no effect. If a CAN module is disabled, the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

Table 4-13. DDRM Field Descriptions

Field	Description
5:2 DDRM[5:2]	**Data Direction Port M** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.3.4 Port M Reduced Drive Register (RDRM)

	7	6	5	4	3	2	1	0
R	0	0	RDRM5	RDRM4	RDRM3	RDRM2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-19. Port M Reduced Drive Register (RDRM)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-14. RDRM Field Descriptions

Field	Description
5:2 RDRM[5:2]	**Reduced Drive Port M** 0 Full drive strength at output 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.3.5 Port M Pull Device Enable Register (PERM)

	7	6	5	4	3	2	1	0
R	0	0	PERM5	PERM4	PERM3	PERM2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-20. Port M Pull Device Enable Register (PERM)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input or wired-or output pins. If a pin is configured as push-pull output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-15. PERM Field Descriptions

Field	Description
5:2 PERM[5:2]	**Pull Device Enable Port M** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.3.6 Port M Polarity Select Register (PPSM)

	7	6	5	4	3	2	1	0
R	0	0	PPSM5	PPSM4	PPSM3	PPSM2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-21. Port M Polarity Select Register (PPSM)

Read: Anytime. Write: Anytime.

The Port M Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port M Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

If a CAN module is enabled, a pull-up device can be activated on the receiver pin, and on the transmitter pin if the corresponding wired-OR mode bit is set. Pull-down devices can not be activated on CAN pins.

Table 4-16. PPSM Field Descriptions

Field	Description
5:2 PPSM[5:2]	**Pull Select Port M** 0 A pull-up device is connected to the associated port M pin. 1 A pull-down device is connected to the associated port M pin.

4.3.3.7 Port M Wired-OR Mode Register (WOMM)

	7	6	5	4	3	2	1	0
R	0	0	WOMM5	WOMM4	WOMM3	WOMM2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-22. Port M Wired-OR Mode Register (WOMM)

Read: Anytime. Write: Anytime.

This register selects whether a port M output is configured as push-pull or wired-or. When a Wired-OR Mode Register bit is set to 1, the corresponding output pin is driven active low only (open drain) and a high level is not driven. A Wired-OR Mode Register bit has no effect if the corresponding pin is configured as an input.

These bits apply also to the CAN transmitter and allow a multipoint connection of several serial modules.

Table 4-17. WOMM Field Descriptions

Field	Description
5:2 WOMM[5:2]	**Wired-OR Mode Port M** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

4.3.4 Port P

Port P is associated with the Pulse Width Modulator (PWM), serial communication interface (SCI1) and Inter-IC bus (IIC) modules. Each pin is assigned to these modules according to the following priority: PWM > SCI1/IIC > general-purpose I/O.

When a PWM channel is enabled, the corresponding pin becomes a PWM output with the exception of PP[5] which can be PWM input or output. Refer to the PWM block description chapter for information on enabling and disabling the PWM channels.

When the IIC bus is enabled, the PP[5:4] pins become SCL and SDA respectively as long as the corresponding PWM channels are disabled. Refer to the IIC block description chapter for information on enabling and disabling the IIC bus.

When the SCI1 receiver and transmitter are enabled, the PP[2] and PP[0] pins become RXD1 and TXD1 respectively as long as the corresponding PWM channels are disabled. Refer to the SCI block description chapter for information on enabling and disabling the SCI receiver and transmitter.

During reset, port P pins are configured as high-impedance inputs.

4.3.4.1 Port P I/O Register (PTP)

	7	6	5	4	3	2	1	0
R	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
W								
SCI1/IIC:			SCL	SDA		RXD1		TXD1
PWM:			PWM5	PWM4	PWM3	PWM2	PWM1	PWM0
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-23. Port P I/O Register (PTP)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRPx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRPx) is set to 0 (input), a read returns the value of the pin.

The PWM function takes precedence over the general-purpose I/O function if the associated PWM channel is enabled. The PWM channels 4-0 are outputs if the respective channels are enabled. PWM channel 5 can be an output, or an input if the shutdown feature is enabled.

The IIC function takes precedence over the general-purpose I/O function if the IIC bus is enabled and the corresponding PWM channels remain disabled. The SDA and SCL pins are bidirectional with outputs configured as open-drain.

If enabled, the SCI1 transmitter takes precedence over the general-purpose I/O function, and the corresponding TXD1 pin is configured as an output. If enabled, the SCI1 receiver takes precedence over the general-purpose I/O function, and the corresponding RXD1 pin is configured as an input.

4.3.4.2 Port P Input Register (PTIP)

	7	6	5	4	3	2	1	0
R	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
W								
Reset	0	0	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 4-24. Port P I/O Register (PTP)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

4.3.4.3 Port P Data Direction Register (DDRP)

	7	6	5	4	3	2	1	0
R	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-25. Port P Data Direction Register (DDRP)

Read: Anytime. Write: Anytime.

This register configures port pins PP[5:0] as either input or output.

If a PWM channel is enabled, the corresponding pin is forced to be an output and the associated Data Direction Register bit has no effect. Channel 5 can also force the corresponding pin to be an input if the shutdown feature is enabled.

When the IIC bus is enabled, the PP[5:4] pins become the SCL and SDA bidirectional pins respectively as long as the corresponding PWM channels are disabled. The associated Data Direction Register bits have no effect.

When the SCI1 transmitter is enabled, the PP[0] pin becomes the TXD1 output pin and the associated Data Direction Register bit has no effect. When the SCI1 receiver is enabled, the PP[2] pin becomes the RXD1 input pin and the associated Data Direction Register bit has no effect.

If the PWM, IIC and SCI1 functions are disabled, the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

Table 4-18. DDRP Field Descriptions

Field	Description
5:0 DDRP[5:0]	**Data Direction Port P** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.4.4 Port P Reduced Drive Register (RDRP)

	7	6	5	4	3	2	1	0
R	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-26. Port P Reduced Drive Register (RDRP)

Read:Anytime. Write:Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-19. RDRP Field Descriptions

Field	Description
5:0 RDRP[5:0]	**Reduced Drive Port P** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.4.5 Port P Pull Device Enable Register (PERP)

	7	6	5	4	3	2	1	0
R	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-27. Port P Pull Device Enable Register (PERP)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-20. PERP Field Descriptions

Field	Description
5:0 PERP[5:0]	**Pull Device Enable Port P** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.4.6 Port P Polarity Select Register (PPSP)

	7	6	5	4	3	2	1	0
R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSP0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-28. Port P Polarity Select Register (PPSP)

Read: Anytime. Write: Anytime.

The Port P Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port P Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-21. PPSP Field Descriptions

Field	Description
5:0 PPSP[5:0]	**Polarity Select Port P** 0 A pull-up device is connected to the associated port P pin. 1 A pull-down device is connected to the associated port P pin.

4.3.4.7 Port P Wired-OR Mode Register (WOMP)

	7	6	5	4	3	2	1	0
R	0	0	WOMP5	WOMP4	0	WOMP2	0	WOMPO
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-29. Port P Wired-OR Mode Register (WOMP)

Read: Anytime. Write: Anytime.

This register selects whether a port P output is configured as push-pull or wired-or. When a Wired-OR Mode Register bit is set to 1, the corresponding output pin is driven active low only (open drain) and a high level is not driven. A Wired-OR Mode Register bit has no effect if the corresponding pin is configured as an input.

If the IIC is enabled and the corresponding PWM channels are disabled, the PP[5:4] pins are configured as wired-or and the corresponding Wired-OR Mode Register bits have no effect.

Table 4-22. WOMP Field Descriptions

Field	Description
5:4 WOMP[5:4]	**Wired-OR Mode Port P** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.
2 WOMP2	**Wired-OR Mode Port P** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.
0 WOMP0	**Wired-OR Mode Port P** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

4.3.5 Port S

Port S is associated with the serial peripheral interface (SPI) and serial communication interface (SCI0). Each pin is assigned to these modules according to the following priority: SPI/SCI0 > general-purpose I/O.

When the SPI is enabled, the PS[7:4] pins become $\overline{SS}$, SCK, MOSI, and MISO respectively. Refer to the SPI block description chapter for information on enabling and disabling the SPI.

When the SCI0 receiver and transmitter are enabled, the PS[1:0] pins become TXD0 and RXD0 respectively. Refer to the SCI block description chapter for information on enabling and disabling the SCI receiver and transmitter.

During reset, port S pins are configured as high-impedance inputs.

4.3.5.1 Port S I/O Register (PTS)

	7	6	5	4	3	2	1	0
R	PTS7	PTS6	PTS5	PTS4	0	0	PTS1	PTS0
W								
SPI/SCI:	$\overline{SS}$	SCK	MOSI	MISO			TXD0	RXD0
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-30. Port S I/O Register (PTS)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRSx) is set to 1 (output), a read returns the value of the I/O register bit. If the associated data direction bit (DDRSx) is set to 0 (input), a read returns the value of the pin.

The SPI function takes precedence over the general-purpose I/O function if the SPI is enabled.

If enabled, the SCI0 transmitter takes precedence over the general-purpose I/O function, and the corresponding TXD0 pin is configured as an output. If enabled, the SCI0 receiver takes precedence over the general-purpose I/O function, and the corresponding RXD0 pin is configured as an input.

4.3.5.2 Port S Input Register (PTIS)

	7	6	5	4	3	2	1	0
R	PTIS7	PTIS6	PTIS5	PTIS4	0	0	PTIS1	PTIS0
W								
Reset	u	u	u	u	0	0	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 4-31. Port S Input Register (PTIS)

Read: Anytime. Write: Never, writes to this register have no effect.

This register always reads back the status of the associated pins.

4.3.5.3 Port S Data Direction Register (DDRS)

	7	6	5	4	3	2	1	0
R	DDRS7	DDRS6	DDRS5	DDRS4	0	0	DDRS1	DDRS0
W								
Reset	0	0	0	0	0	0	0	0

= Reserved or Unimplemented

Figure 4-32. Port S Data Direction Register (DDRS)

Read: Anytime. Write: Anytime.

This register configures port pins PS[7:4] and PS[2:0] as either input or output.

When the SPI is enabled, the PS[7:4] pins become the SPI bidirectional pins. The associated Data Direction Register bits have no effect.

When the SCI0 transmitter is enabled, the PS[1] pin becomes the TXD0 output pin and the associated Data Direction Register bit has no effect. When the SCI0 receiver is enabled, the PS[0] pin becomes the RXD0 input pin and the associated Data Direction Register bit has no effect.

If the SPI and SCI0 functions are disabled, the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

Table 4-23. DDRS Field Descriptions

Field	Description
7:4 DDRS[7:4]	**Data Direction Port S** 0 Associated pin is configured as input. 1 Associated pin is configured as output.
1:0 DDRS[1:0]	**Data Direction Port S** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.5.4 Port S Reduced Drive Register (RDRS)

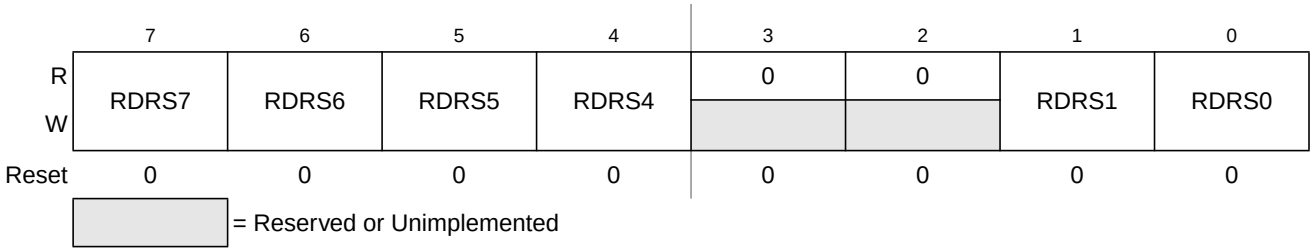


Figure 4-33. Port S Reduced Drive Register (RDRS)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-24. RDRS Field Descriptions

Field	Description
7:4 RDRS[7:4]	**Reduced Drive Port S** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.
1:0 RDRS[1:0]	**Reduced Drive Port S** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.5.5 Port S Pull Device Enable Register (PERS)

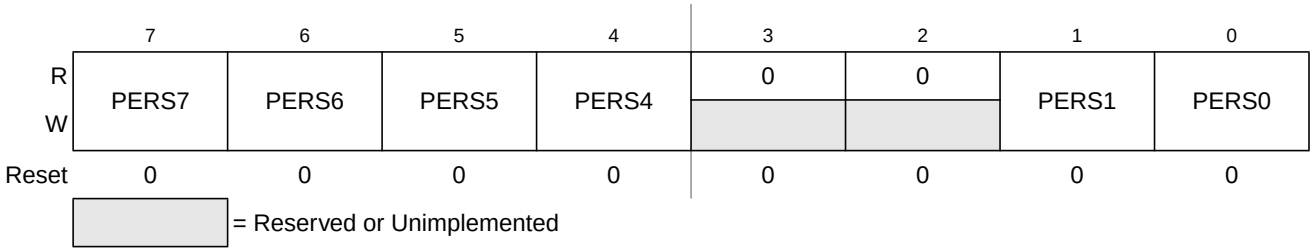


Figure 4-34. Port S Pull Device Enable Register (PERS)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input or wired-or (open drain) output pins. If a pin is configured as push-pull output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-25. PERS Field Descriptions

Field	Description
7:4 PERS[7:4]	**Pull Device Enable Port S** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.
1:0 PERS[1:0]	**Pull Device Enable Port S** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.5.6 Port S Polarity Select Register (PPSS)

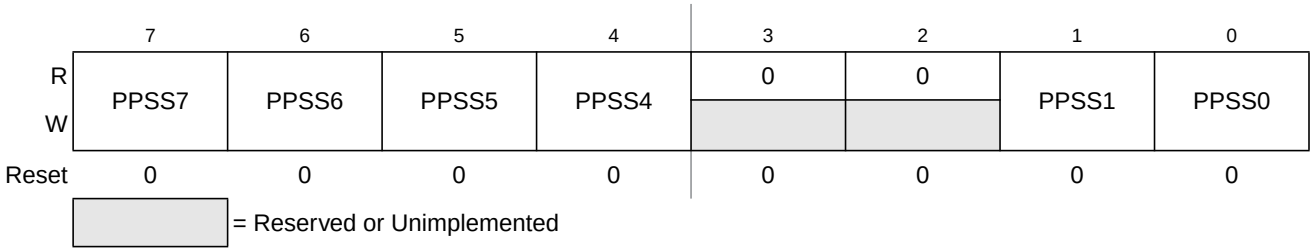


Figure 4-35. Port S Polarity Select Register (PPSS)

Read: Anytime. Write: Anytime.

The Port S Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port S Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-26. PPSS Field Descriptions

Field	Description
7:4 PPSS[7:4]	**Pull Select Port S** 0 A pull-up device is connected to the associated port S pin. 1 A pull-down device is connected to the associated port S pin.
1:0 PPSS[1:0]	**Pull Select Port S** 0 A pull-up device is connected to the associated port S pin. 1 A pull-down device is connected to the associated port S pin.

4.3.5.7 Port S Wired-OR Mode Register (WOMS)

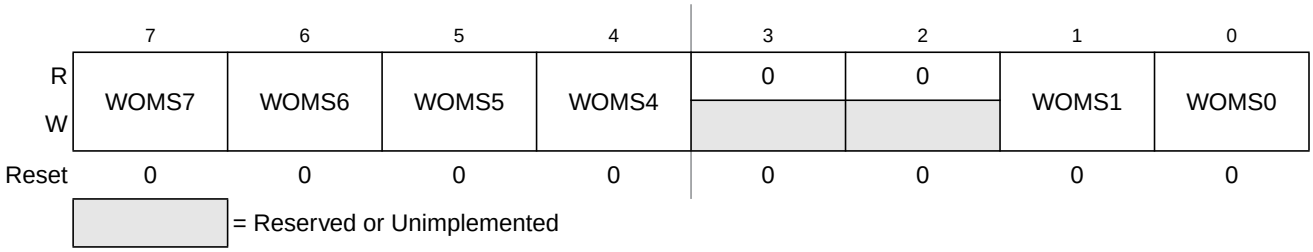


Figure 4-36. Port S Wired-OR Mode Register (WOMS)

Read: Anytime. Write: Anytime.

This register selects whether a port S output is configured as push-pull or wired-or. When a Wired-OR Mode Register bit is set to 1, the corresponding output pin is driven active low only (open drain) and a high level is not driven. A Wired-OR Mode Register bit has no effect if the corresponding pin is configured as an input.

Table 4-27. WOMS Field Descriptions

Field	Description
7:4 WOMS[7:4]	**Wired-OR Mode Port S** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.
1:0 WOMS[1:0]	**Wired-OR Mode Port S** 0 Output buffers operate as push-pull outputs. 1 Output buffers operate as open-drain outputs.

4.3.6 Port T

Port T is associated with the 8-channel timer (TIM) and the liquid crystal display (LCD) driver. Each pin is assigned to these modules according to the following priority:
LCD Driver > timer > general-purpose I/O.

If the corresponding LCD frontplane drivers are enabled (and LCD module is enabled), the FP[27:24] outputs of the LCD module are available on port T pins PT[3:0].

If the corresponding LCD frontplane drivers are disabled (or LCD module is disabled) and the timer is enabled, the timer channels configured for output compare are available on port T pins PT[3:0].

Refer to the LCD block description chapter for information on enabling and disabling the LCD and its frontplane drivers.Refer to the TIM block description chapter for information on enabling and disabling the TIM module.

During reset, port T pins are configured as inputs with pull down.

4.3.6.1 Port T I/O Register (PTT)

	7	6	5	4	3	2	1	0
R W	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
TIM:	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0
LCD:					1	1	1	1
Reset	0	0	0	0	0	0	0	0

Figure 4-37. Port T I/O Register (PTT)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRTx) is set to 1 (output), a read returns the value of the I/O register bit.

If the associated data direction bit (DDRTx) is set to 0 (input) and the LCD frontplane driver is enabled (and LCD module is enabled), the associated I/O register bit (PTTx) reads “1”.

If the associated data direction bit (DDRTx) is set to 0 (input) and the LCD frontplane driver is disabled (or LCD module is disabled), a read returns the value of the pin.

4.3.6.2 Port T Input Register (PTIT)

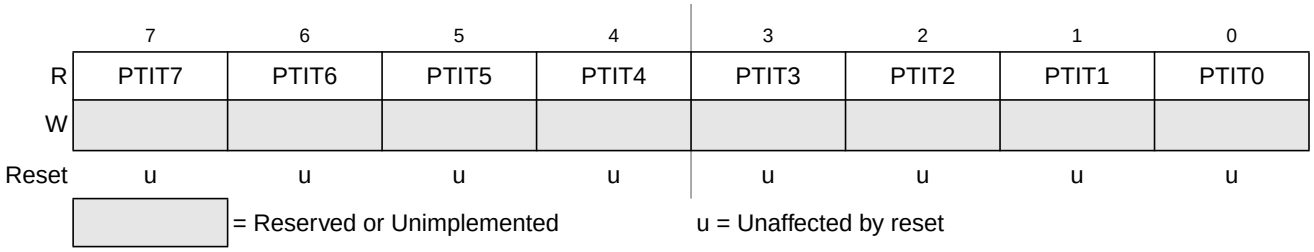


Figure 4-38. Port T Input Register (PTIT)

Read: Anytime. Write: Never, writes to this register have no effect.

If the LCD frontplane driver of an associated I/O pin is enabled (and LCD module is enabled), a read returns a 1.

If the LCD frontplane driver of the associated I/O pin is disabled (or LCD module is disabled), a read returns the status of the associated pin.

4.3.6.3 Port T Data Direction Register (DDRT)

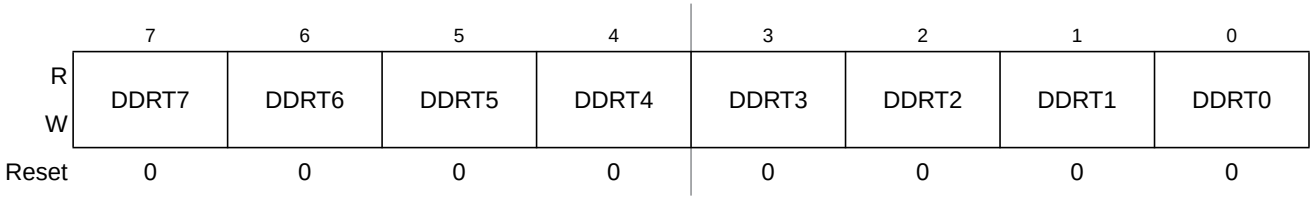


Figure 4-39. Port T Data Direction Register (DDRT)

Read: Anytime. Write: Anytime.

This register configures port pins PT[7:0] as either input or output.

If a LCD frontplane driver is enabled (and LCD module is enabled), it outputs an analog signal to the corresponding pin and the associated Data Direction Register bit has no effect. If a LCD frontplane driver is disabled (or LCD module is disabled), the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

If the TIM module is enabled, each port pin configured for output compare is forced to be an output and the associated Data Direction Register bit has no effect. If the associated timer output compare is disabled, the corresponding Data Direction Register bit reverts to control the I/O direction of the associated pin.

If the TIM module is enabled, each port pin configured as an input capture has the corresponding Data Direction Register bit controlling the I/O direction of the associated pin.

Table 4-28. DDRT Field Descriptions

Field	Description
7:0 DDRT[7:0]	**Data Direction Port T** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.6.4 Port T Reduced Drive Register (RDRT)

	7	6	5	4	3	2	1	0
R W	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
Reset	0	0	0	0	0	0	0	0

Figure 4-40. Port T Reduced Drive Register (RDRT)

Read: Anytime. Write: Anytime.

This register configures the drive strength of configured output pins as either full or reduced. If a pin is configured as input, the corresponding Reduced Drive Register bit has no effect.

Table 4-29. RDRT Field Descriptions

Field	Description
7:0 RDRT[7:0]	**Reduced Drive Port T** 0 Full drive strength at output. 1 Associated pin drives at about 1/3 of the full drive strength.

4.3.6.5 Port T Pull Device Enable Register (PERT)

	7	6	5	4	3	2	1	0
R W	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
Reset	1	1	1	1	1	1	1	1

Figure 4-41. Port T Pull Device Enable Register (PERT)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-30. PERT Field Descriptions

Field	Description
7:0 PERT[7:0]	**Pull Device Enable Port T** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.6.6 Port T Polarity Select Register (PPST)

	7	6	5	4	3	2	1	0
R W	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
Reset	1	1	1	1	1	1	1	1

Figure 4-42. Port T Polarity Select Register (PPST)

Read: Anytime. Write: Anytime.

The Port T Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port T Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-31. PPST Field Descriptions

Field	Description
7:0 PPST[7:0]	**Pull Select Port T** 0 A pull-up device is connected to the associated port T pin. 1 A pull-down device is connected to the associated port T pin.

4.3.7 Port U

Port U is associated with the stepper stall detect (SSD1 and SSD0) and motor controller (MC1 and MC0) modules. Each pin is assigned to these modules according to the following priority: SSD1/SSD0 > MC1/MC0 > general-purpose I/O.

If SSD1 module is enabled, the PU[7:4] pins are controlled by the SSD1 module. If SSD1 module is disabled, the PU[7:4] pins are controlled by the motor control PWM channels 3 and 2 (MC1).

If SSD0 module is enabled, the PU[3:0] pins are controlled by the SSD0 module. If SSD0 module is disabled, the PU[3:0] pins are controlled by the motor control PWM channels 1 and 0 (MC0).

Refer to the SSD and MC block description chapters for information on enabling and disabling the SSD module and the motor control PWM channels respectively.

During reset, port U pins are configured as high-impedance inputs.

4.3.7.1 Port U I/O Register (PTU)

	7	6	5	4	3	2	1	0
R W	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
MC:	M1C1P	M1C1M	M1COP	M1COM	M0C1P	M0C1M	M0C0P	M0C0M
SSD1/ SSD0:	M1SINP	M1SINM	M1COSP	M1COSM	M0SINP	M0SINM	M1COSP	M0COSM
Reset	0	0	0	0	0	0	0	0

Figure 4-43. Port U I/O Register (PTU)

Read: Anytime. Write: Anytime.

If the associated data direction bit (DDRUx) is set to 1 (output), a read returns the value of the I/O register bit.

If the associated data direction bit (DDRUx) is set to 0 (input) and the slew rate is enabled, the associated I/O register bit (PTUx) reads “1”.

If the associated data direction bit (DDRUx) is set to 0 (input) and the slew rate is disabled, a read returns the value of the pin.

4.3.7.2 Port U Input Register (PTIU)

	7	6	5	4	3	2	1	0
R	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
W								
Reset	u	u	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 4-44. Port U Input Register (PTIU)

Read: Anytime. Write: Never, writes to this register have no effect.

If the associated slew rate control is enabled (digital input buffer is disabled), a read returns a “1”. If the associated slew rate control is disabled (digital input buffer is enabled), a read returns the status of the associated pin.

4.3.7.3 Port U Data Direction Register (DDRU)

	7	6	5	4	3	2	1	0
R W	DDRU7	DDRU6	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
Reset	0	0	0	0	0	0	0	0

Figure 4-45. Port U Data Direction Register (DDRU)

Read: Anytime. Write: Anytime.

This register configures port pins PU[7:0] as either input or output.

When enabled, the SSD or MC modules force the I/O state to be an output for each associated pin and the associated Data Direction Register bit has no effect. If the SSD and MC modules are disabled, the corresponding Data Direction Register bits revert to control the I/O direction of the associated pins.

Table 4-32. DDRU Field Descriptions

Field	Description
7:0 DDRU[7:0]	**Data Direction Port U** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.7.4 Port U Slew Rate Register (SRRU)

	7	6	5	4	3	2	1	0
R W	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
Reset	0	0	0	0	0	0	0	0

Figure 4-46. Port U Slew Rate Register (SRRU)

Read: Anytime. Write: Anytime.

This register enables the slew rate control and disables the digital input buffer for port pins PU[7:0].

Table 4-33. SRRU Field Descriptions

Field	Description
7:0 SRRU[7:0]	**Slew Rate Port U** 0 Disables slew rate control and enables digital input buffer. 1 Enables slew rate control and disables digital input buffer.

4.3.7.5 Port U Pull Device Enable Register (PERU)

	7	6	5	4	3	2	1	0
R W	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
Reset	0	0	0	0	0	0	0	0

Figure 4-47. Port U Pull Device Enable Register (PERU)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-34. PERU Field Descriptions

Field	Description
7:0 PERU[7:0]	**Pull Device Enable Port U** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.7.6 Port U Polarity Select Register (PPSU)

	7	6	5	4	3	2	1	0
R W	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
Reset	0	0	0	0	0	0	0	0

Figure 4-48. Port U Polarity Select Register (PPSU)

Read: Anytime. Write: Anytime.

The Port U Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port U Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-35. PPSU Field Descriptions

Field	Description
7:0 PPSU[7:0]	**Pull Select Port U** 0 A pull-up device is connected to the associated port U pin. 1 A pull-down device is connected to the associated port U pin.

4.3.8 Port V

Port V is associated with the stepper stall detect (SSD3 and SSD2) and motor controller (MC3 and MC2) modules. Each pin is assigned to these modules according to the following priority: SSD3/SSD2 > MC3/MC2 > general-purpose I/O.

If SSD3 module is enabled, the PV[7:4] pins are controlled by the SSD3 module. If SSD3 module is disabled, the PV[7:4] pins are controlled by the motor control PWM channels 7 and 6 (MC3).

If SSD2 module is enabled, the PV[3:0] pins are controlled by the SSD2 module. If SSD2 module is disabled, the PV[3:0] pins are controlled by the motor control PWM channels 5 and 4 (MC2).

Refer to the SSD and MC block description chapters for information on enabling and disabling the SSD module and the motor control PWM channels respectively.

During reset, port V pins are configured as high-impedance inputs.

4.3.8.1 Port V I/O Register (PTV)

	7	6	5	4	3	2	1	0
R W	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
MC:	M3C1P	M3C1M	M3C0P	M3C0M	M2C1P	M2C1M	M2C0P	M2C0M
SSD3/ SSD2	M3SINP	M3SINM	M3COSP	M3COSM	M2SINP	M2SINM	M2COSP	M2COSM
Reset	0	0	0	0	0	0	0	0

Figure 4-49. Port V I/O Register (PTV)

Read: Anytime. Write: anytime.

If the associated data direction bit (DDRVx) is set to 1 (output), a read returns the value of the I/O register bit.

If the associated data direction bit (DDRVx) is set to 0 (input) and the slew rate is enabled, the associated I/O register bit (PTVx) reads “1”.

If the associated data direction bit (DDRVx) is set to 0 (input) and the slew rate is disabled, a read returns the value of the pin.

4.3.8.2 Port V Input Register (PTIV)

	7	6	5	4	3	2	1	0
R	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
W								
Reset	u	u	u	u	u	u	u	u

= Reserved or Unimplemented u = Unaffected by reset

Figure 4-50. Port V Input Register (PTIV)

Read: Anytime. Write: Never, writes to this register have no effect.

If the associated slew rate control is enabled (digital input buffer is disabled), a read returns a “1”. If the associated slew rate control is disabled (digital input buffer is enabled), a read returns the status of the associated pin.

4.3.8.3 Port V Data Direction Register (DDRV)

	7	6	5	4	3	2	1	0
R W	DDRV7	DDRV6	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
Reset	0	0	0	0	0	0	0	0

Figure 4-51. Port V Data Direction Register (DDRV)

Read: Anytime. Write: Anytime.

This register configures port pins PV[7:0] as either input or output.

When enabled, the SSD or MC modules force the I/O state to be an output for each associated pin and the associated Data Direction Register bit has no effect. If the SSD and MC modules are disabled, the corresponding Data Direction Register bits revert to control the I/O direction of the associated pins.

Table 4-36. DDRV Field Descriptions

Field	Description
7:0 DDRV[7:0]	**Data Direction Port V** 0 Associated pin is configured as input. 1 Associated pin is configured as output.

4.3.8.4 Port V Slew Rate Register (SRRV)

	7	6	5	4	3	2	1	0
R W	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
Reset	0	0	0	0	0	0	0	0

Figure 4-52. Port V Slew Rate Register (SRRV)

Read: anytime. Write: Anytime.

This register enables the slew rate control and disables the digital input buffer for port pins PV[7:0].

Table 4-37. SRRV Field Descriptions

Field	Description
7:0 SRRV[7:0]	**Slew Rate Port V** 0 Disables slew rate control and enables digital input buffer. 1 Enables slew rate control and disables digital input buffer.

4.3.8.5 Port V Pull Device Enable Register (PERV)

	7	6	5	4	3	2	1	0
R W	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
Reset	0	0	0	0	0	0	0	0

Figure 4-53. Port V Pull Device Enable Register (PERV)

Read: Anytime. Write: Anytime.

This register configures whether a pull-up or a pull-down device is activated on configured input pins. If a pin is configured as output, the corresponding Pull Device Enable Register bit has no effect.

Table 4-38. PERV Field Descriptions

Field	Description
7:0 PERV[7:0]	**Pull Device Enable Port V** 0 Pull-up or pull-down device is disabled. 1 Pull-up or pull-down device is enabled.

4.3.8.6 Port V Polarity Select Register (PPSV)

	7	6	5	4	3	2	1	0
R W	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
Reset	0	0	0	0	0	0	0	0

Figure 4-54. Port V Polarity Select Register (PPSV)

Read: Anytime. Write: Anytime.

The Port V Polarity Select Register selects whether a pull-down or a pull-up device is connected to the pin. The Port V Polarity Select Register is effective only when the corresponding Data Direction Register bit is set to 0 (input) and the corresponding Pull Device Enable Register bit is set to 1.

Table 4-39. PPSV Field Descriptions

Field	Description
7:0 PPSV[7:0]	**Pull Select Port V** 0 A pull-up device is connected to the associated port V pin. 1 A pull-down device is connected to the associated port V pin.

4.4 Functional Description

Each pin associated with ports AD, L, P, S, T, U and V can act as general-purpose I/O. In addition the pin can act as an output from a peripheral module or an input to a peripheral module.

A set of configuration registers is common to all ports. All registers can be written at any time, however a specific configuration might not become active.

> Example: Selecting a pull-up resistor. This resistor does not become active while the port is used as a push-pull output.

4.4.1 I/O Register

The I/O Register holds the value driven out to the pin if the port is used as a general-purpose I/O. Writing to the I/O Register only has an effect on the pin if the port is used as general-purpose output.

When reading the I/O Register, the value of each pin is returned if the corresponding Data Direction Register bit is set to 0 (pin configured as input). If the data direction register bits is set to 1, the content of the I/O Register bit is returned. This is independent of any other configuration (Figure 4-55).

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on the I/O Register when changing the data direction register.

4.4.2 Input Register

The Input Register is a read-only register and generally returns the value of the pin (Figure 4-55). It can be used to detect overload or short circuit conditions.

Due to internal synchronization circuits, it can take up to 2 bus cycles until the correct value is read on the Input Register when changing the Data Direction Register.

4.4.3 Data Direction Register

The Data Direction Register defines whether the pin is used as an input or an output. A Data Direction Register bit set to 0 configures the pin as an input. A Data Direction Register bit set to 0 configures the pin as an output. If a peripheral module controls the pin the contents of the data direction register is ignored (Figure 4-55).

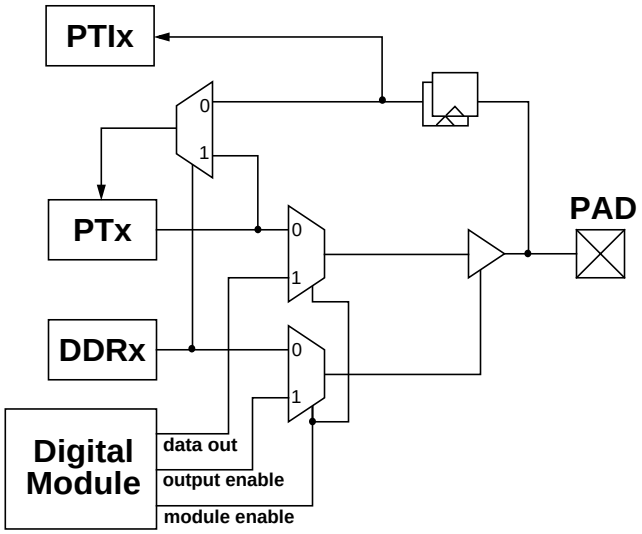


Figure 4-55. Illustration of I/O Pin Functionality

Figure 4-56 shows the state of digital inputs and outputs when an analog module drives the port. When the analog module is enabled all associated digital output ports are disabled and all associated digital input ports read “1”.

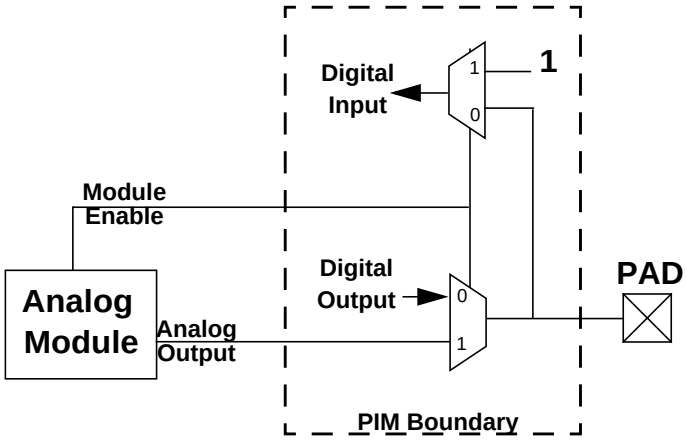


Figure 4-56. Digital Ports and Analog Module

4.4.4 Reduced Drive Register

If the port is used as an output the Reduced Drive Register allows the configuration of the drive strength.

4.4.5 Pull Device Enable Register

The Pull Device Enable Register turns on a pull-up or pull-down device. The pull device becomes active only if the pin is used as an input or as a wired-or output.

4.4.6 Polarity Select Register

The Polarity Select Register selects either a pull-up or pull-down device if enabled. The pull device becomes active only if the pin is used as an input or as a wired-or output.

4.4.7 Pin Configuration Summary

The following table summarizes the effect of various configuration in the Data Direction (DDR), Input/Output (I/O), reduced drive (RDR), Pull Enable (PE), Pull Select (PS) and Interrupt Enable (IE) register bits. The PS configuration bit is used for two purposes:

1. Configure the sensitive interrupt edge (rising or falling), if interrupt is enabled.
2. Select either a pull-up or pull-down device if PE is set to “1”.

Table 4-40. Pin Configuration Summary

DDR	IO	RDR	PE	PS	IE[1]	Function[2]	Pull Device	Interrupt
0	X	X	0	X	0	Input	Disabled	Disabled
0	X	X	1	0	0	Input	Pull Up	Disabled
0	X	X	1	1	0	Input	Pull Down	Disabled
0	X	X	0	0	1	Input	Disabled	Falling Edge
0	X	X	0	1	1	Input	Disabled	Rising Edge
0	X	X	1	0	1	Input	Pull Up	Falling Edge
0	X	X	1	1	1	Input	Pull Down	Rising Edge
1	0	0	X	X	0	Output to 0, Full Drive	Disabled	Disabled
1	1	0	X	X	0	Output to 1, Full Drive	Disabled	Disabled
1	0	1	X	X	0	Output to 0, Reduced Drive	Disabled	Disabled
1	1	1	X	X	0	Output to 1, Reduced Drive	Disabled	Disabled
1	0	0	X	0	1	Output to 0, Full Drive	Disabled	Falling Edge
1	1	0	X	1	1	Output to 1, Full Drive	Disabled	Rising Edge
1	0	1	X	0	1	Output to 0, Reduced Drive	Disabled	Falling Edge
1	1	1	X	1	1	Output to 1, Reduced Drive	Disabled	Rising Edge

1 Applicable only on Port AD.

2 Digital outputs are disabled and digital input logic is forced to “1” when an analog module associated with the port is enabled.

4.5 Resets

The reset values of all registers are given in the register description in Section 4.3, “Memory Map and Register Definition”.

All ports start up as general-purpose inputs on reset.

4.5.1 Reset Initialization

All registers including the data registers get set/reset asynchronously. Table 4-41 summarizes the port properties after reset initialization.

Table 4-41. Port Reset State Summary

Port	Reset States				
	Data Direction	Pull Mode	Red. Drive/ Slew Rate	Wired-OR Mode	Interrupt
A	Refer to section Bus Control and Input/Output	Pull Down	Refer to section Bus Control and Input/Output		
B		Pull Down			
E		Pull Down[1]			
K		Pull Down			
BKGD pin		Pull Down			
T	Input	Pull Down	Disabled	N/A	N/A
S	Input	Hi-z	Disabled	Disabled	N/A
M	Input	Hi-z	Disabled	Disabled	N/A
P	Input	Hi-z	Disabled	N/A	N/A
L	Input	Pull Down	Disabled	N/A	N/A
U	Input	Hi-z	Disabled	N/A	N/A
V	Input	Hi-z	Disabled	N/A	N/A
AD	Input	Hi-z	Disabled	N/A	Disabled

1 PE[1:0] pins have pull-ups instead of pull-downs.

4.6 Interrupts

4.6.1 General

Port AD generates an edge sensitive interrupt if enabled. It offers eight I/O pins with edge triggered interrupt capability in wired-or fashion. The interrupt enable as well as the sensitivity to rising or falling edges can be individually configured on per pin basis. All eight bits/pins share the same interrupt vector. Interrupts can be used with the pins configured as inputs (with the corresponding ATDDIEN1 bit set to 1) or outputs.

An interrupt is generated when a bit in the port interrupt flag register and its corresponding port interrupt enable bit are both set. This external interrupt feature is capable to wake up the CPU when it is in stop or wait mode.

A digital filter on each pin prevents pulses (Figure 4-58) shorter than a specified time from generating an interrupt. The minimum time varies over process conditions, temperature and voltage (Figure 4-57 and Table 4-42).

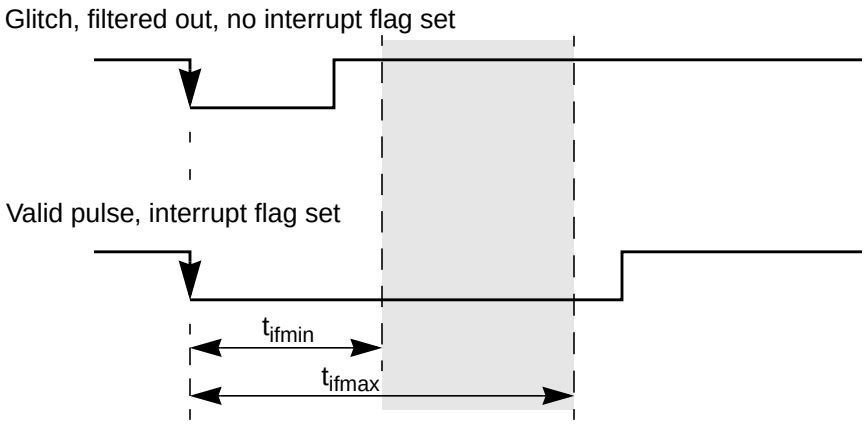


Figure 4-57. Interrupt Glitch Filter on Port AD (PPS = 0)

Table 4-42. Pulse Detection Criteria

Pulse	Mode			
	$\overline{STOP}$		STOP[1]	
		Unit		Unit
Ignored	t_{pulse} <= 3	Bus Clock	t_{pulse} <= 3.2	µs
Uncertain	3 < t_{pulse} < 4	Bus Clock	3.2 < t_{pulse} < 10	µs
Valid	t_{pulse} >= 4	Bus Clock	t_{pulse} >= 10	µs

1 These values include the spread of the oscillator frequency over temperature, voltage and process.

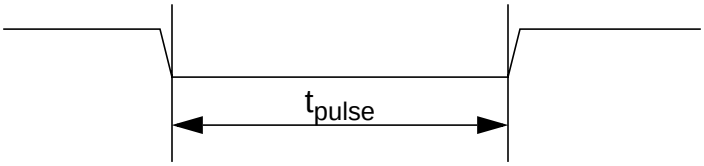


Figure 4-58. Pulse Illustration

A valid edge on an input is detected if 4 consecutive samples of a passive level are followed by 4 consecutive samples of an active level directly or indirectly

The filters are continuously clocked by the bus clock in RUN and WAIT mode. In STOP mode the clock is generated by a single RC oscillator in the port integration module. To maximize current saving the RC oscillator runs only if the following condition is true on any pin:

Sample count <= 4 and port interrupt enabled (PIE=1) and port interrupt flag not set (PIF=0).

4.6.2 Interrupt Sources

Table 4-43. Port Integration Module Interrupt Sources

Interrupt Source	Interrupt Flag	Local Enable	Global (CCR) Mask
Port AD	PIFAD[7:0]	PIEAD[7:0]	I Bit

NOTE

Vector addresses and their relative interrupt priority are determined at the MCU level.

4.6.3 Operation in Stop Mode

All clocks are stopped in STOP mode. The port integration module has asynchronous paths on port AD to generate wake-up interrupts from stop mode. For other sources of external interrupts refer to the respective block description chapters.

Chapter 5
Clocks and Reset Generator (CRGV4)

5.1 Introduction

This specification describes the function of the clocks and reset generator (CRG).

5.1.1 Features

The main features of this block are:

- Phase-locked loop (PLL) frequency multiplier
  - — Reference divider
  - — Automatic bandwidth control mode for low-jitter operation
  - — Automatic frequency lock detector
  - — CPU interrupt on entry or exit from locked condition
  - — Self-clock mode in absence of reference clock
- System clock generator
  - — Clock quality check
  - — Clock switch for either oscillator- or PLL-based system clocks
  - — User selectable disabling of clocks during wait mode for reduced power consumption
- Computer operating properly (COP) watchdog timer with time-out clear window
- System reset generation from the following possible sources:
  - — Power-on reset
  - — Low voltage reset
    Refer to the device overview section for availability of this feature.
  - — COP reset
  - — Loss of clock reset
  - — External pin reset
- Real-time interrupt (RTI)

5.1.2 Modes of Operation

This subsection lists and briefly describes all operating modes supported by the CRG.

- Run mode

  All functional parts of the CRG are running during normal run mode. If RTI or COP functionality is required the individual bits of the associated rate select registers (COPCTL, RTICTL) have to be set to a nonzero value.

- Wait mode

  This mode allows to disable the system and core clocks depending on the configuration of the individual bits in the CLKSEL register.

- Stop mode

  Depending on the setting of the PSTP bit, stop mode can be differentiated between full stop mode (PSTP = 0) and pseudo-stop mode (PSTP = 1).

  — Full stop mode

  The oscillator is disabled and thus all system and core clocks are stopped. The COP and the RTI remain frozen.

  — Pseudo-stop mode

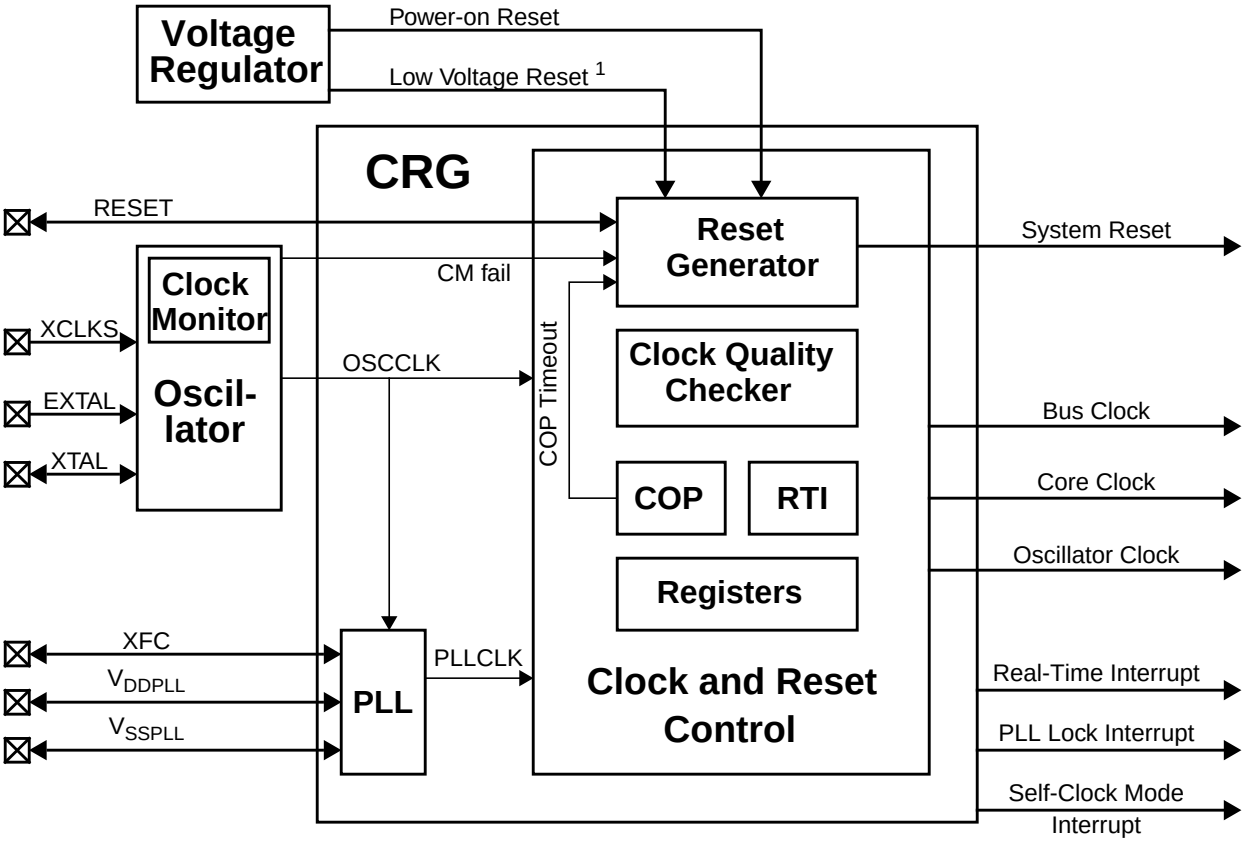
  The oscillator continues to run and most of the system and core clocks are stopped. If the respective enable bits are set the COP and RTI will continue to run, else they remain frozen.

- Self-clock mode

  Self-clock mode will be entered if the clock monitor enable bit (CME) and the self-clock mode enable bit (SCME) are both asserted and the clock monitor in the oscillator block detects a loss of clock. As soon as self-clock mode is entered the CRG starts to perform a clock quality check. Self-clock mode remains active until the clock quality check indicates that the required quality of the incoming clock signal is met (frequency and amplitude). Self-clock mode should be used for safety purposes only. It provides reduced functionality to the MCU in case a loss of clock is causing severe system conditions.

5.1.3 Block Diagram

Figure 5-1 shows a block diagram of the CRG.



1 Refer to the device overview section for availability of the low-voltage reset feature.

Figure 5-1. CRG Block Diagram

5.2 External Signal Description

This section lists and describes the signals that connect off chip.

5.2.1 V_{DDPLL}, V_{SSPLL} — PLL Operating Voltage, PLL Ground

These pins provides operating voltage (V_{DDPLL}) and ground (V_{SSPLL}) for the PLL circuitry. This allows the supply voltage to the PLL to be independently bypassed. Even if PLL usage is not required V_{DDPLL} and V_{SSPLL} must be connected properly.

5.2.2 XFC — PLL Loop Filter Pin

A passive external loop filter must be placed on the XFC pin. The filter is a second-order, low-pass filter to eliminate the VCO input ripple. The value of the external filter network and the reference frequency determines the speed of the corrections and the stability of the PLL. Refer to the device overview chapter for calculation of PLL loop filter (XFC) components. If PLL usage is not required the XFC pin must be tied to V_{DDPLL}.

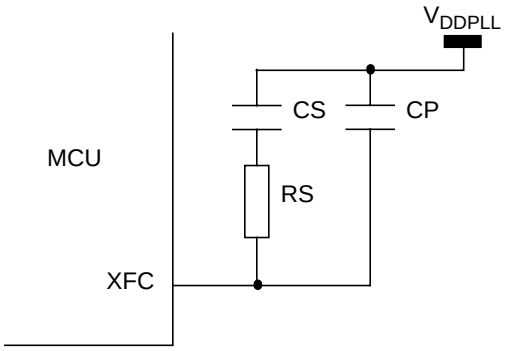


Figure 5-2. PLL Loop Filter Connections

5.2.3 $\overline{\text{RESET}}$ — Reset Pin

$\overline{\text{RESET}}$ is an active low bidirectional reset pin. As an input it initializes the MCU asynchronously to a known start-up state. As an open-drain output it indicates that an system reset (internal to MCU) has been triggered.

5.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the CRG.

5.3.1 Module Memory Map

Table 5-1 gives an overview on all CRG registers.

Table 5-1. CRG Memory Map

Address Offset	Use	Access
0x0000	CRG Synthesizer Register (SYNR)	R/W
0x0001	CRG Reference Divider Register (REFDV)	R/W
0x0002	CRG Test Flags Register (CTFLG)[1]	R/W
0x0003	CRG Flags Register (CRGFLG)	R/W
0x0004	CRG Interrupt Enable Register (CRGINT)	R/W
0x0005	CRG Clock Select Register (CLKSEL)	R/W
0x0006	CRG PLL Control Register (PLLCTL)	R/W
0x0007	CRG RTI Control Register (RTICTL)	R/W
0x0008	CRG COP Control Register (COPCTL)	R/W
0x0009	CRG Force and Bypass Test Register (FORBYP)[2]	R/W
0x000A	CRG Test Control Register (CTCTL)[3]	R/W
0x000B	CRG COP Arm/Timer Reset (ARMCOP)	R/W

1 CTFLG is intended for factory test purposes only.

2 FORBYP is intended for factory test purposes only.

3 CTCTL is intended for factory test purposes only.

NOTE

Register address = base address + address offset, where the base address is defined at the MCU level and the address offset is defined at the module level.

5.3.2 Register Descriptions

This section describes in address order all the CRG registers and their individual bits.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
SYNR	R	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
	W								
REFDV	R	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
	W								
CTFLG	R	0	0	0	0	0	0	0	0
	W								
CRGFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
	W								
CRGINT	R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
	W								
CLKSEL	R	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
	W								
PLLCTL	R	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
	W								
RTICTL	R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
	W								
COPCTL	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
	W								
FORBYP	R	0	0	0	0	0	0	0	0
	W								
CTCTL	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented or Reserved

Figure 5-3. CRG Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
ARMCOP	R	0	0	0	0	0	0	0	0
	W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

= Unimplemented or Reserved

Figure 5-3. CRG Register Summary (continued)

5.3.2.1 CRG Synthesizer Register (SYNR)

The SYNR register controls the multiplication factor of the PLL. If the PLL is on, the count in the loop divider (SYNR) register effectively multiplies up the PLL clock (PLLCLK) from the reference frequency by 2 x (SYNR+1). PLLCLK will not be below the minimum VCO frequency (f_{SCM}).

$$PLLCLK = 2 \times OSCCLK \times \frac{(SYNR + 1)}{(REFDV + 1)}$$

NOTE

If PLL is selected (PLLSEL=1), Bus Clock = PLLCLK / 2
Bus Clock must not exceed the maximum operating system frequency.

	7	6	5	4	3	2	1	0
R	0	0	SYN5	SYNR	SYN3	SYN2	SYN1	SYN0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-4. CRG Synthesizer Register (SYNR)

Read: anytime

Write: anytime except if PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit and the track detector bit.

5.3.2.2 CRG Reference Divider Register (REFDV)

The REFDV register provides a finer granularity for the PLL multiplier steps. The count in the reference divider divides OSCCLK frequency by REFDV + 1.

	7	6	5	4	3	2	1	0
R	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-5. CRG Reference Divider Register (REFDV)

Read: anytime

Write: anytime except when PLLSEL = 1

NOTE

Write to this register initializes the lock detector bit and the track detector bit.

5.3.2.3 Reserved Register (CTFLG)

This register is reserved for factory testing of the CRG module and is not available in normal modes.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-6. CRG Reserved Register (CTFLG)

Read: always reads 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to this register when in special mode can alter the CRG functionality.

5.3.2.4 CRG Flags Register (CRGFLG)

This register provides CRG status bits and flags.

	7	6	5	4	3	2	1	0
R	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
W								
Reset	0	Note 1	Note 2	0	0	0	0	0

1. PORF is set to 1 when a power-on reset occurs. Unaffected by system reset.
2. LVRF is set to 1 when a low-voltage reset occurs. Unaffected by system reset.

= Unimplemented or Reserved

Figure 5-7. CRG Flag Register (CRGFLG)

Read: anytime

Write: refer to each bit for individual write conditions

Table 5-2. CRGFLG Field Descriptions

Field	Description
7 RTIF	**Real-Time Interrupt Flag** — RTIF is set to 1 at the end of the RTI period. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (RTIE = 1), RTIF causes an interrupt request. 0 RTI time-out has not yet occurred. 1 RTI time-out has occurred.
6 PORF	**Power-on Reset Flag** — PORF is set to 1 when a power-on reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Power-on reset has not occurred. 1 Power-on reset has occurred.
5 LVRF	**Low-Voltage Reset Flag** — If low voltage reset feature is not available (see the device overview chapter), LVRF always reads 0. LVRF is set to 1 when a low voltage reset occurs. This flag can only be cleared by writing a 1. Writing a 0 has no effect. 0 Low voltage reset has not occurred. 1 Low voltage reset has occurred.
4 LOCKIF	**PLL Lock Interrupt Flag** — LOCKIF is set to 1 when LOCK status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect.If enabled (LOCKIE = 1), LOCKIF causes an interrupt request. 0 No change in LOCK bit. 1 LOCK bit has changed.
3 LOCK	**Lock Status Bit** — LOCK reflects the current state of PLL lock condition. This bit is cleared in self-clock mode. Writes have no effect. 0 PLL VCO is not within the desired tolerance of the target frequency. 1 PLL VCO is within the desired tolerance of the target frequency.
2 TRACK	**Track Status Bit** — TRACK reflects the current state of PLL track condition. This bit is cleared in self-clock mode. Writes have no effect. 0 Acquisition mode status. 1 Tracking mode status.

Table 5-2. CRGFLG Field Descriptions (continued)

Field	Description
1 SCMIF	**Self-Clock Mode Interrupt Flag** — SCMIF is set to 1 when SCM status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (SCMIE=1), SCMIF causes an interrupt request. 0 No change in SCM bit. 1 SCM bit has changed.
0 SCM	**Self-Clock Mode Status Bit** — SCM reflects the current clocking mode. Writes have no effect. 0 MCU is operating normally with OSCCLK available. 1 MCU is operating in self-clock mode with OSCCLK in an unknown state. All clocks are derived from PLLCLK running at its minimum frequency f_{SCM}.

5.3.2.5 CRG Interrupt Enable Register (CRGINT)

This register enables CRG interrupt requests.

	7	6	5	4	3	2	1	0
R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-8. CRG Interrupt Enable Register (CRGINT)

Read: anytime

Write: anytime

Table 5-3. CRGINT Field Descriptions

Field	Description
7 RTIE	**Real-Time Interrupt Enable Bit** 0 Interrupt requests from RTI are disabled. 1 Interrupt will be requested whenever RTIF is set.
4 LOCKIE	**Lock Interrupt Enable Bit** 0 LOCK interrupt requests are disabled. 1 Interrupt will be requested whenever LOCKIF is set.
1 SCMIE	**Self-Clock Mode Interrupt Enable Bit** 0 SCM interrupt requests are disabled. 1 Interrupt will be requested whenever SCMIF is set.

5.3.2.6 CRG Clock Select Register (CLKSEL)

This register controls CRG clock selection. Refer to Figure 5-17 for details on the effect of each bit.

	7	6	5	4	3	2	1	0
R W	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
Reset	0	0	0	0	0	0	0	0

Figure 5-9. CRG Clock Select Register (CLKSEL)

Read: anytime

Write: refer to each bit for individual write conditions

Table 5-4. CLKSEL Field Descriptions

Field	Description
7 PLLSEL	**PLL Select Bit** — Write anytime. Writing a 1 when LOCK = 0 and AUTO = 1, or TRACK = 0 and AUTO = 0 has no effect. This prevents the selection of an unstable PLLCLK as SYSCLK. PLLSEL bit is cleared when the MCU enters self-clock mode, stop mode or wait mode with PLLWAI bit set. 0 System clocks are derived from OSCCLK (Bus Clock = OSCCLK / 2). 1 System clocks are derived from PLLCLK (Bus Clock = PLLCLK / 2).
6 PSTP	**Pseudo-Stop Bit** — Write: anytime — This bit controls the functionality of the oscillator during stop mode. 0 Oscillator is disabled in stop mode. 1 Oscillator continues to run in stop mode (pseudo-stop). The oscillator amplitude is reduced. Refer to oscillator block description for availability of a reduced oscillator amplitude. **Note:** Pseudo-stop allows for faster stop recovery and reduces the mechanical stress and aging of the resonator in case of frequent stop conditions at the expense of a slightly increased power consumption. **Note:** Lower oscillator amplitude exhibits lower power consumption but could have adverse effects during any electro-magnetic susceptibility (EMS) tests.
5 SYSWAI	**System Clocks Stop in Wait Mode Bit** — Write: anytime 0 In wait mode, the system clocks continue to run. 1 In wait mode, the system clocks stop. **Note:** RTI and COP are not affected by SYSWAI bit.
4 ROAWAI	**Reduced Oscillator Amplitude in Wait Mode Bit** — Write: anytime — Refer to oscillator block description chapter for availability of a reduced oscillator amplitude. If no such feature exists in the oscillator block then setting this bit to 1 will not have any effect on power consumption. 0 Normal oscillator amplitude in wait mode. 1 Reduced oscillator amplitude in wait mode. **Note:** Lower oscillator amplitude exhibits lower power consumption but could have adverse effects during any electro-magnetic susceptibility (EMS) tests.
3 PLLWAI	**PLL Stops in Wait Mode Bit** — Write: anytime — If PLLWAI is set, the CRG will clear the PLLSEL bit before entering wait mode. The PLLON bit remains set during wait mode but the PLL is powered down. Upon exiting wait mode, the PLLSEL bit has to be set manually if PLL clock is required. While the PLLWAI bit is set the AUTO bit is set to 1 in order to allow the PLL to automatically lock on the selected target frequency after exiting wait mode. 0 PLL keeps running in wait mode. 1 PLL stops in wait mode.
2 CWAI	**Core Stops in Wait Mode Bit** — Write: anytime 0 Core clock keeps running in wait mode. 1 Core clock stops in wait mode.

Table 5-4. CLKSEL Field Descriptions (continued)

Field	Description
1 RTIWAI	**RTI Stops in Wait Mode Bit** — Write: anytime 0 RTI keeps running in wait mode. 1 RTI stops and initializes the RTI dividers whenever the part goes into wait mode.
0 COPWAI	**COP Stops in Wait Mode Bit** — Normal modes: Write once —Special modes: Write anytime 0 COP keeps running in wait mode. 1 COP stops and initializes the COP dividers whenever the part goes into wait mode.

5.3.2.7 CRG PLL Control Register (PLLCTL)

This register controls the PLL functionality.

	7	6	5	4	3	2	1	0
R	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
W								
Reset	1	1	1	1	0	0	0	1

= Unimplemented or Reserved

Figure 5-10. CRG PLL Control Register (PLLCTL)

Read: anytime

Write: refer to each bit for individual write conditions

Table 5-5. PLLCTL Field Descriptions

Field	Description
7 CME	**Clock Monitor Enable Bit** — CME enables the clock monitor. Write anytime except when SCM = 1. 0 Clock monitor is disabled. 1 Clock monitor is enabled. Slow or stopped clocks will cause a clock monitor reset sequence or self-clock mode. **Note:** Operating with CME = 0 will not detect any loss of clock. In case of poor clock quality this could cause unpredictable operation of the MCU. **Note:** In Stop Mode (PSTP = 0) the clock monitor is disabled independently of the CME bit setting and any loss of clock will not be detected.
6 PLLON	**Phase Lock Loop On Bit** — PLLON turns on the PLL circuitry. In self-clock mode, the PLL is turned on, but the PLLON bit reads the last latched value. Write anytime except when PLLSEL = 1. 0 PLL is turned off. 1 PLL is turned on. If AUTO bit is set, the PLL will lock automatically.
5 AUTO	**Automatic Bandwidth Control Bit** — AUTO selects either the high bandwidth (acquisition) mode or the low bandwidth (tracking) mode depending on how close to the desired frequency the VCO is running. Write anytime except when PLLWAI=1, because PLLWAI sets the AUTO bit to 1. 0 Automatic mode control is disabled and the PLL is under software control, using ACQ bit. 1 Automatic mode control is enabled and ACQ bit has no effect.
4 ACQ	**Acquisition Bit** — Write anytime. If AUTO=1 this bit has no effect. 0 Low bandwidth filter is selected. 1 High bandwidth filter is selected.

Table 5-5. PLLCTL Field Descriptions (continued)

Field	Description
2 PRE	**RTI Enable during Pseudo-Stop Bit** — PRE enables the RTI during pseudo-stop mode. Write anytime. 0 RTI stops running during pseudo-stop mode. 1 RTI continues running during pseudo-stop mode. **Note:** If the PRE bit is cleared the RTI dividers will go static while pseudo-stop mode is active. The RTI dividers will not initialize like in wait mode with RTIWAI bit set.
1 PCE	**COP Enable during Pseudo-Stop Bit** — PCE enables the COP during pseudo-stop mode. Write anytime. 0 COP stops running during pseudo-stop mode 1 COP continues running during pseudo-stop mode **Note:** If the PCE bit is cleared the COP dividers will go static while pseudo-stop mode is active. The COP dividers will *not* initialize like in wait mode with COPWAI bit set.
0 SCME	**Self-Clock Mode Enable Bit** — Normal modes: Write once —Special modes: Write anytime — SCME can not be cleared while operating in self-clock mode (SCM=1). 0 Detection of crystal clock failure causes clock monitor reset (see Section 5.5.1, “Clock Monitor Reset”). 1 Detection of crystal clock failure forces the MCU in self-clock mode (see Section 5.4.7.2, “Self-Clock Mode”).

5.3.2.8 CRG RTI Control Register (RTICTL)

This register selects the timeout period for the real-time interrupt.

	7	6	5	4	3	2	1	0
R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-11. CRG RTI Control Register (RTICTL)

Read: anytime

Write: anytime

NOTE

A write to this register initializes the RTI counter.

Table 5-6. RTICTL Field Descriptions

Field	Description
6:4 RTR[6:4]	**Real-Time Interrupt Prescale Rate Select Bits** — These bits select the prescale rate for the RTI. See Table 5-7.
3:0 RTR[3:0]	**Real-Time Interrupt Modulus Counter Select Bits** — These bits select the modulus counter target value to provide additional granularity. Table 5-7 shows all possible divide values selectable by the RTICTL register. The source clock for the RTI is OSCCLK.

Table 5-7. RTI Frequency Divide Rates

RTR[3:0]	RTR[6:4] =							
	000 (OFF)	**001 (2^{10})**	**010 (2^{11})**	**011 (2^{12})**	**100 (2^{13})**	**101 (2^{14})**	**110 (2^{15})**	**111 (2^{16})**
0000 (÷1)	OFF*	2^{10}	2^{11}	2^{12}	2^{13}	2^{14}	2^{15}	2^{16}
0001 (÷2)	OFF*	$2x2^{10}$	$2x2^{11}$	$2x2^{12}$	$2x2^{13}$	$2x2^{14}$	$2x2^{15}$	$2x2^{16}$
0010 (÷3)	OFF*	$3x2^{10}$	$3x2^{11}$	$3x2^{12}$	$3x2^{13}$	$3x2^{14}$	$3x2^{15}$	$3x2^{16}$
0011 (÷4)	OFF*	$4x2^{10}$	$4x2^{11}$	$4x2^{12}$	$4x2^{13}$	$4x2^{14}$	$4x2^{15}$	$4x2^{16}$
0100 (÷5)	OFF*	$5x2^{10}$	$5x2^{11}$	$5x2^{12}$	$5x2^{13}$	$5x2^{14}$	$5x2^{15}$	$5x2^{16}$
0101 (÷6)	OFF*	$6x2^{10}$	$6x2^{11}$	$6x2^{12}$	$6x2^{13}$	$6x2^{14}$	$6x2^{15}$	$6x2^{16}$
0110 (÷7)	OFF*	$7x2^{10}$	$7x2^{11}$	$7x2^{12}$	$7x2^{13}$	$7x2^{14}$	$7x2^{15}$	$7x2^{16}$
0111 (÷8)	OFF*	$8x2^{10}$	$8x2^{11}$	$8x2^{12}$	$8x2^{13}$	$8x2^{14}$	$8x2^{15}$	$8x2^{16}$
1000 (÷9)	OFF*	$9x2^{10}$	$9x2^{11}$	$9x2^{12}$	$9x2^{13}$	$9x2^{14}$	$9x2^{15}$	$9x2^{16}$
1001 (÷10)	OFF*	$10x2^{10}$	$10x2^{11}$	$10x2^{12}$	$10x2^{13}$	$10x2^{14}$	$10x2^{15}$	$10x2^{16}$
1010 (÷11)	OFF*	$11x2^{10}$	$11x2^{11}$	$11x2^{12}$	$11x2^{13}$	$11x2^{14}$	$11x2^{15}$	$11x2^{16}$
1011 (÷12)	OFF*	$12x2^{10}$	$12x2^{11}$	$12x2^{12}$	$12x2^{13}$	$12x2^{14}$	$12x2^{15}$	$12x2^{16}$
1100 (÷ 13)	OFF*	$13x2^{10}$	$13x2^{11}$	$13x2^{12}$	$13x2^{13}$	$13x2^{14}$	$13x2^{15}$	$13x2^{16}$
1101 (÷14)	OFF*	$14x2^{10}$	$14x2^{11}$	$14x2^{12}$	$14x2^{13}$	$14x2^{14}$	$14x2^{15}$	$14x2^{16}$
1110 (÷15)	OFF*	$15x2^{10}$	$15x2^{11}$	$15x2^{12}$	$15x2^{13}$	$15x2^{14}$	$15x2^{15}$	$15x2^{16}$
1111 (÷ 16)	OFF*	$16x2^{10}$	$16x2^{11}$	$16x2^{12}$	$16x2^{13}$	$16x2^{14}$	$16x2^{15}$	$16x2^{16}$

* Denotes the default value out of reset.This value should be used to disable the RTI to ensure future backwards compatibility.

5.3.2.9 CRG COP Control Register (COPCTL)

This register controls the COP (computer operating properly) watchdog.

	7	6	5	4	3	2	1	0
R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-12. CRG COP Control Register (COPCTL)

Read: anytime

Write: WCOP, CR2, CR1, CR0: once in user mode, anytime in special mode

Write: RSBCK: once

Table 5-8. COPCTL Field Descriptions

Field	Description
7 WCOP	**Window COP Mode Bit** — When set, a write to the ARMCOP register must occur in the last 25% of the selected period. A write during the first 75% of the selected period will reset the part. As long as all writes occur during this window, 0x0055 can be written as often as desired. As soon as 0x00AA is written after the 0x0055, the time-out logic restarts and the user must wait until the next window before writing to ARMCOP. Table 5-9 shows the exact duration of this window for the seven available COP rates. 0 Normal COP operation 1 Window COP operation
6 RSBCK	COP and RTI Stop in Active BDM Mode Bit 0 Allows the COP and RTI to keep running in active BDM mode. 1 Stops the COP and RTI counters whenever the part is in active BDM mode.
2:0 CR[2:0]	**COP Watchdog Timer Rate Select** — These bits select the COP time-out rate (see Table 5-9). The COP time-out period is OSCCLK period divided by CR[2:0] value. Writing a nonzero value to CR[2:0] enables the COP counter and starts the time-out period. A COP counter time-out causes a system reset. This can be avoided by periodically (before time-out) reinitializing the COP counter via the ARMCOP register.

Table 5-9. COP Watchdog Rates[1]

CR2	CR1	CR0	OSCCLK Cycles to Time Out
0	0	0	COP disabled
0	0	1	2^{14}
0	1	0	2^{16}
0	1	1	2^{18}
1	0	0	2^{20}
1	0	1	2^{22}
1	1	0	2^{23}
1	1	1	2^{24}

1 OSCCLK cycles are referenced from the previous COP time-out reset (writing 0x0055/0x00AA to the ARMCOP register)

5.3.2.10 Reserved Register (FORBYP)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special modes can alter the CRG's functionality.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-13. Reserved Register (FORBYP)

Read: always read 0x0000 except in special modes

Write: only in special modes

5.3.2.11 Reserved Register (CTCTL)

NOTE

This reserved register is designed for factory test purposes only, and is not intended for general user access. Writing to this register when in special test modes can alter the CRG's functionality.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 5-14. Reserved Register (CTCTL)

Read: always read 0x0080 except in special modes

Write: only in special modes

5.3.2.12 CRG COP Timer Arm/Reset Register (ARMCOP)

This register is used to restart the COP time-out period.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 5-15. ARMCOP Register Diagram

Read: always reads 0x0000

Write: anytime

When the COP is disabled (CR[2:0] = “000”) writing to this register has no effect.

When the COP is enabled by setting CR[2:0] nonzero, the following applies:

Writing any value other than 0x0055 or 0x00AA causes a COP reset. To restart the COP time-out period you must write 0x0055 followed by a write of 0x00AA. Other instructions may be executed between these writes but the sequence (0x0055, 0x00AA) must be completed prior to COP end of time-out period to avoid a COP reset. Sequences of 0x0055 writes or sequences of 0x00AA writes are allowed. When the WCOP bit is set, 0x0055 and 0x00AA writes must be done in the last 25% of the selected time-out period; writing any value in the first 75% of the selected period will cause a COP reset.

5.4 Functional Description

This section gives detailed informations on the internal operation of the design.

5.4.1 Phase Locked Loop (PLL)

The PLL is used to run the MCU from a different time base than the incoming OSCCLK. For increased flexibility, OSCCLK can be divided in a range of 1 to 16 to generate the reference frequency. This offers a finer multiplication granularity. The PLL can multiply this reference clock by a multiple of 2, 4, 6,... 126,128 based on the SYNR register.

$$PLLCLK = 2 \times OSCCLK \times \frac{[SYNR + 1]}{[REFDV + 1]}$$

CAUTION

Although it is possible to set the two dividers to command a very high clock frequency, do not exceed the specified bus frequency limit for the MCU.
If (PLLSEL = 1), Bus Clock = PLLCLK / 2

The PLL is a frequency generator that operates in either acquisition mode or tracking mode, depending on the difference between the output frequency and the target frequency. The PLL can change between acquisition and tracking modes either automatically or manually.

The VCO has a minimum operating frequency, which corresponds to the self-clock mode frequency f_{SCM}.

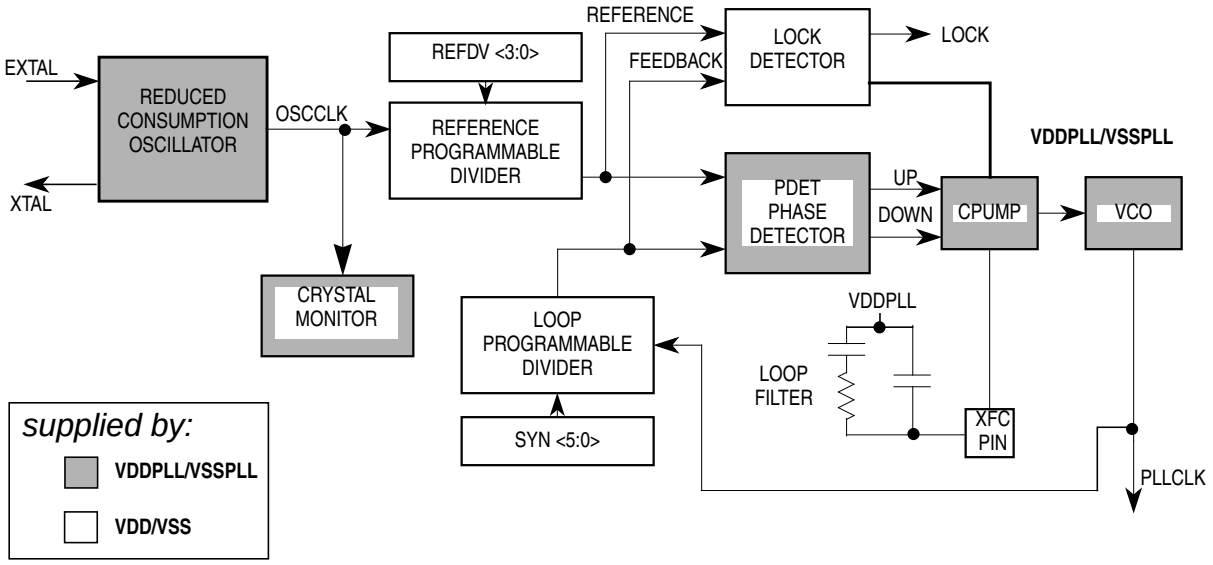


Figure 5-16. PLL Functional Diagram

5.4.1.1 PLL Operation

The oscillator output clock signal (OSCCLK) is fed through the reference programmable divider and is divided in a range of 1 to 16 (REFDV+1) to output the reference clock. The VCO output clock, (PLLCLK) is fed back through the programmable loop divider and is divided in a range of 2 to 128 in increments of [2 x (SYNR +1)] to output the feedback clock. See Figure 5-16.

The phase detector then compares the feedback clock, with the reference clock. Correction pulses are generated based on the phase difference between the two signals. The loop filter then slightly alters the DC voltage on the external filter capacitor connected to XFC pin, based on the width and direction of the correction pulse. The filter can make fast or slow corrections depending on its mode, as described in the next subsection. The values of the external filter network and the reference frequency determine the speed of the corrections and the stability of the PLL.

5.4.1.2 Acquisition and Tracking Modes

The lock detector compares the frequencies of the feedback clock, and the reference clock. Therefore, the speed of the lock detector is directly proportional to the final reference frequency. The circuit determines the mode of the PLL and the lock condition based on this comparison.

The PLL filter can be manually or automatically configured into one of two possible operating modes:

- Acquisition mode

  In acquisition mode, the filter can make large frequency corrections to the VCO. This mode is used at PLL start-up or when the PLL has suffered a severe noise hit and the VCO frequency is far off the desired frequency. When in acquisition mode, the TRACK status bit is cleared in the CRGFLG register.
- Tracking mode

  In tracking mode, the filter makes only small corrections to the frequency of the VCO. PLL jitter is much lower in tracking mode, but the response to noise is also slower. The PLL enters tracking mode when the VCO frequency is nearly correct and the TRACK bit is set in the CRGFLG register.

The PLL can change the bandwidth or operational mode of the loop filter manually or automatically.

In automatic bandwidth control mode (AUTO = 1), the lock detector automatically switches between acquisition and tracking modes. Automatic bandwidth control mode also is used to determine when the PLL clock (PLLCLK) is safe to use as the source for the system and core clocks. If PLL LOCK interrupt requests are enabled, the software can wait for an interrupt request and then check the LOCK bit. If CPU interrupts are disabled, software can poll the LOCK bit continuously (during PLL start-up, usually) or at periodic intervals. In either case, only when the LOCK bit is set, is the PLLCLK clock safe to use as the source for the system and core clocks. If the PLL is selected as the source for the system and core clocks and the LOCK bit is clear, the PLL has suffered a severe noise hit and the software must take appropriate action, depending on the application.

The following conditions apply when the PLL is in automatic bandwidth control mode (AUTO = 1):

- The TRACK bit is a read-only indicator of the mode of the filter.
- The TRACK bit is set when the VCO frequency is within a certain tolerance, Δ_{trk}, and is clear when the VCO frequency is out of a certain tolerance, Δ_{unt}.
- The LOCK bit is a read-only indicator of the locked state of the PLL.
- The LOCK bit is set when the VCO frequency is within a certain tolerance, Δ_{Lock}, and is cleared when the VCO frequency is out of a certain tolerance, Δ_{unl}.
- CPU interrupts can occur if enabled (LOCKIE = 1) when the lock condition changes, toggling the LOCK bit.

The PLL can also operate in manual mode (AUTO = 0). Manual mode is used by systems that do not require an indicator of the lock condition for proper operation. Such systems typically operate well below the maximum system frequency (f_{sys}) and require fast start-up. The following conditions apply when in manual mode:

- ACQ is a writable control bit that controls the mode of the filter. Before turning on the PLL in manual mode, the ACQ bit should be asserted to configure the filter in acquisition mode.
- After turning on the PLL by setting the PLLON bit software must wait a given time (t_{acq}) before entering tracking mode (ACQ = 0).
- After entering tracking mode software must wait a given time (t_{al}) before selecting the PLLCLK as the source for system and core clocks (PLLSEL = 1).

5.4.2 System Clocks Generator

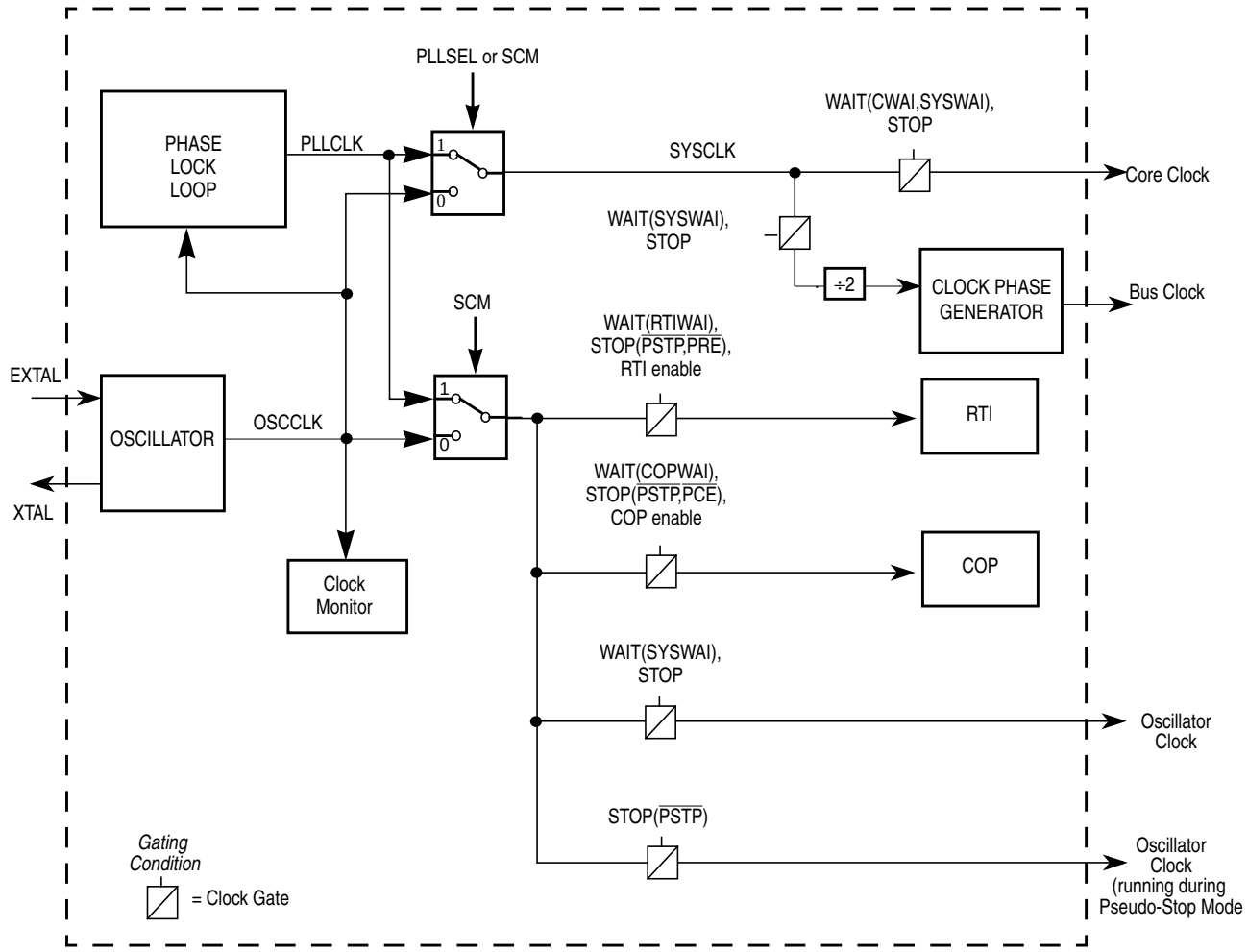


Figure 5-17. System Clocks Generator

The clock generator creates the clocks used in the MCU (see Figure 5-17). The gating condition placed on top of the individual clock gates indicates the dependencies of different modes (stop, wait) and the setting of the respective configuration bits.

The peripheral modules use the bus clock. Some peripheral modules also use the oscillator clock. The memory blocks use the bus clock. If the MCU enters self-clock mode (see Section 5.4.7.2, “Self-Clock Mode”), oscillator clock source is switched to PLLCLK running at its minimum frequency f_{SCM}. The bus clock is used to generate the clock visible at the ECLK pin. The core clock signal is the clock for the CPU. The core clock is twice the bus clock as shown in Figure 5-18. But note that a CPU cycle corresponds to one bus clock.

PLL clock mode is selected with PLLSEL bit in the CLKSEL register. When selected, the PLL output clock drives SYSCLK for the main system including the CPU and peripherals. The PLL cannot be turned off by clearing the PLLON bit, if the PLL clock is selected. When PLLSEL is changed, it takes a maximum

of 4 OSCCLK plus 4 PLLCLK cycles to make the transition. During the transition, all clocks freeze and CPU activity ceases.

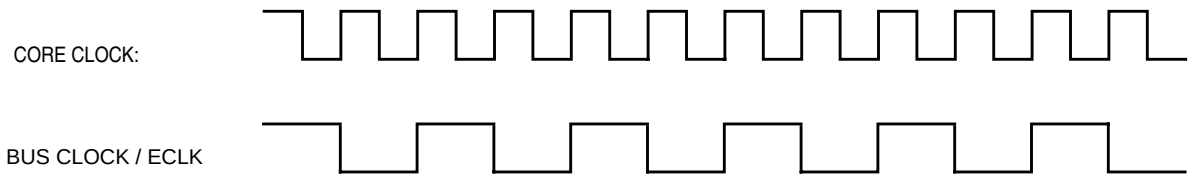


Figure 5-18. Core Clock and Bus Clock Relationship

5.4.3 Clock Monitor (CM)

If no OSCCLK edges are detected within a certain time, the clock monitor within the oscillator block generates a clock monitor fail event. The CRG then asserts self-clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated by the oscillator block.The clock monitor function is enabled/disabled by the CME control bit.

5.4.4 Clock Quality Checker

The clock monitor performs a coarse check on the incoming clock signal. The clock quality checker provides a more accurate check in addition to the clock monitor.

A clock quality check is triggered by any of the following events:

- Power-on reset (POR)
- Low voltage reset (LVR)
- Wake-up from full stop mode (exit full stop)
- Clock monitor fail indication (CM fail)

A time window of 50000 VCO clock cycles[1] is called *check window*.

A number greater equal than 4096 rising OSCCLK edges within a *check window* is called *osc ok*. Note that *osc ok* immediately terminates the current *check window.* See Figure 5-19 as an example.

1. VCO clock cycles are generated by the PLL when running at minimum frequency f_{SCM}.

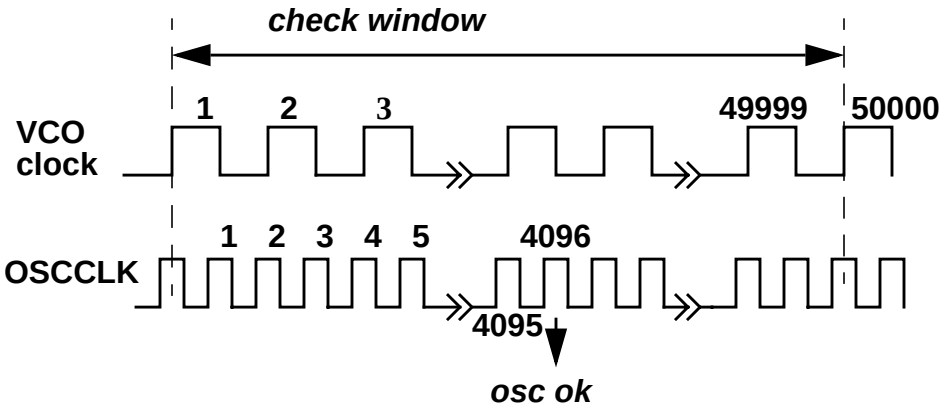


Figure 5-19. Check Window Example

The sequence for clock quality check is shown in Figure 5-20.

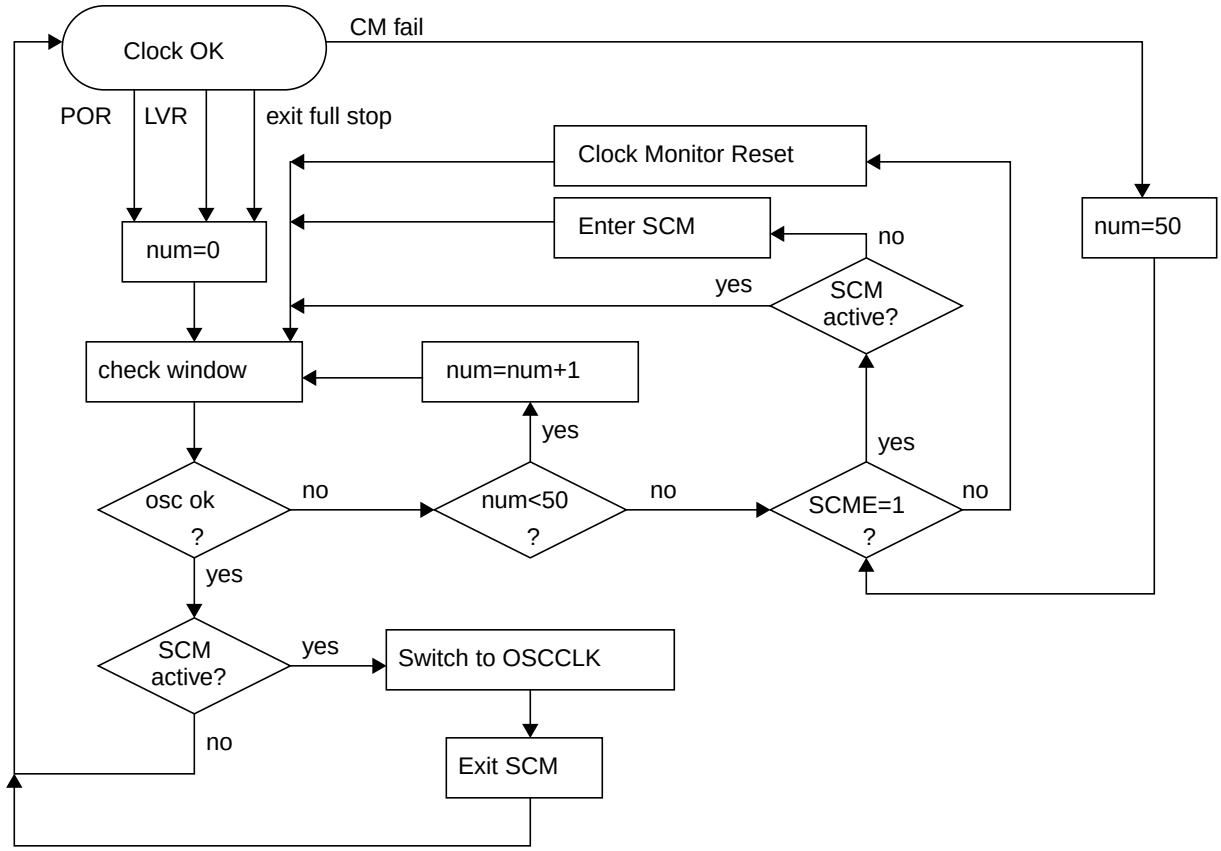


Figure 5-20. Sequence for Clock Quality Check

NOTE

Remember that in parallel to additional actions caused by self-clock mode or clock monitor reset[1] handling the clock quality checker **continues** to check the OSCCLK signal.

1. A Clock Monitor Reset will always set the SCME bit to logical'1'

NOTE

The clock quality checker enables the PLL and the voltage regulator (VREG) anytime a clock check has to be performed. An ongoing clock quality check could also cause a running PLL (f_{SCM}) and an active VREG during pseudo-stop mode or wait mode

5.4.5 Computer Operating Properly Watchdog (COP)

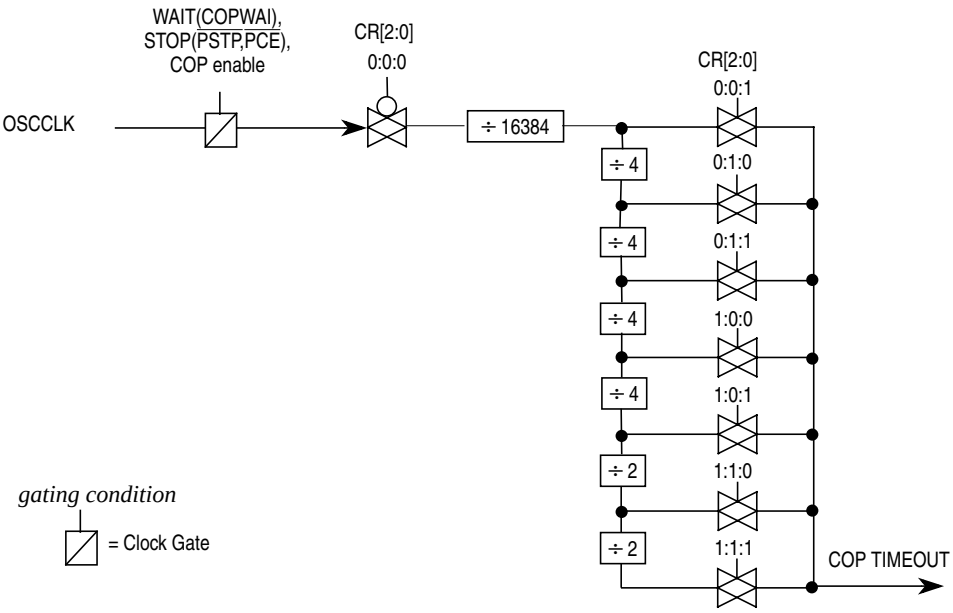


Figure 5-21. Clock Chain for COP

The COP (free running watchdog timer) enables the user to check that a program is running and sequencing properly. The COP is disabled out of reset. When the COP is being used, software is responsible for keeping the COP from timing out. If the COP times out it is an indication that the software is no longer being executed in the intended sequence; thus a system reset is initiated (see Section 5.5.2, “Computer Operating Properly Watchdog (COP) Reset).” The COP runs with a gated OSCCLK (see Section Figure 5-21., “Clock Chain for COP”). Three control bits in the COPCTL register allow selection of seven COP time-out periods.

When COP is enabled, the program must write 0x0055 and 0x00AA (in this order) to the ARMCOP register during the selected time-out period. As soon as this is done, the COP time-out period is restarted. If the program fails to do this and the COP times out, the part will reset. Also, if any value other than 0x0055 or 0x00AA is written, the part is immediately reset.

Windowed COP operation is enabled by setting WCOP in the COPCTL register. In this mode, writes to the ARMCOP register to clear the COP timer must occur in the last 25% of the selected time-out period. A premature write will immediately reset the part.

If PCE bit is set, the COP will continue to run in pseudo-stop mode.

5.4.6 Real-Time Interrupt (RTI)

The RTI can be used to generate a hardware interrupt at a fixed periodic rate. If enabled (by setting RTIE=1), this interrupt will occur at the rate selected by the RTICTL register. The RTI runs with a gated OSCCLK (see Section Figure 5-22., “Clock Chain for RTI”). At the end of the RTI time-out period the RTIF flag is set to 1 and a new RTI time-out period starts immediately.

A write to the RTICTL register restarts the RTI time-out period.

If the PRE bit is set, the RTI will continue to run in pseudo-stop mode.

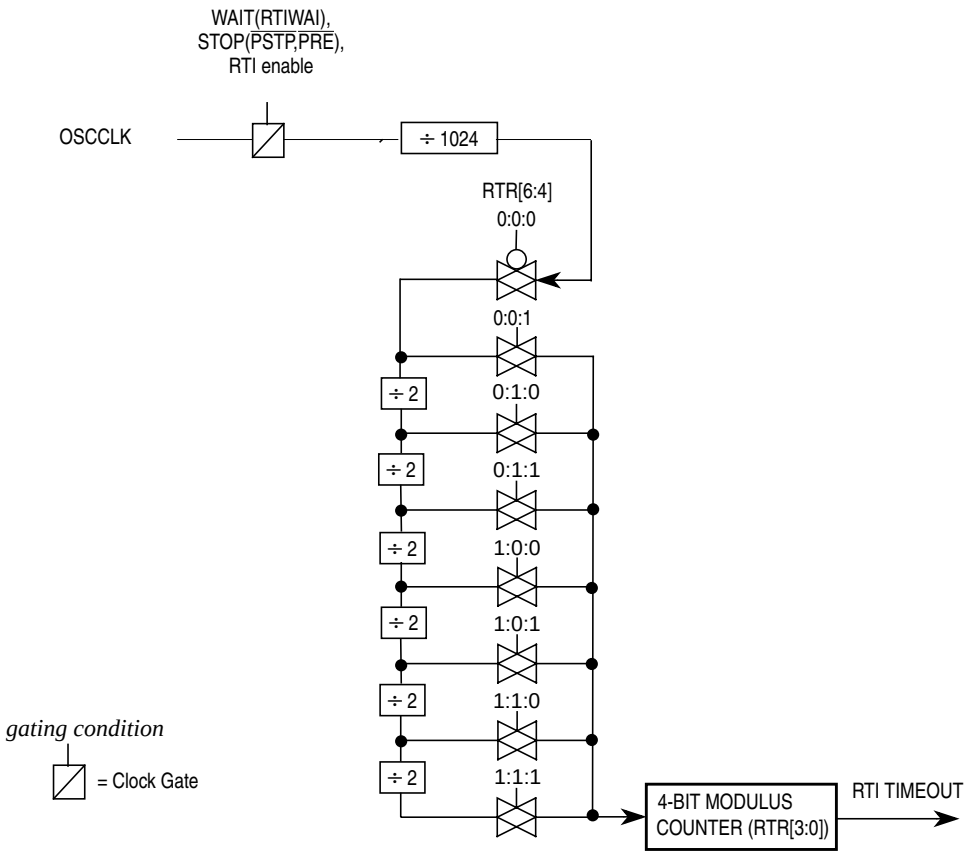


Figure 5-22. Clock Chain for RTI

5.4.7 Modes of Operation

5.4.7.1 Normal Mode

The CRG block behaves as described within this specification in all normal modes.

5.4.7.2 Self-Clock Mode

The VCO has a minimum operating frequency, f_{SCM}. If the external clock frequency is not available due to a failure or due to long crystal start-up time, the bus clock and the core clock are derived from the VCO

running at minimum operating frequency; this mode of operation is called self-clock mode. This requires CME = 1 and SCME = 1. If the MCU was clocked by the PLL clock prior to entering self-clock mode, the PLLSEL bit will be cleared. If the external clock signal has stabilized again, the CRG will automatically select OSCCLK to be the system clock and return to normal mode. See Section 5.4.4, “Clock Quality Checker” for more information on entering and leaving self-clock mode.

NOTE

In order to detect a potential clock loss, the CME bit should be always enabled (CME=1).

If CME bit is disabled and the MCU is configured to run on PLL clock (PLLCLK), a loss of external clock (OSCCLK) will not be detected and will cause the system clock to drift towards the VCO’s minimum frequency f_{SCM}. As soon as the external clock is available again the system clock ramps up to its PLL target frequency. If the MCU is running on external clock any loss of clock will cause the system to go static.

5.4.8 Low-Power Operation in Run Mode

The RTI can be stopped by setting the associated rate select bits to 0.

The COP can be stopped by setting the associated rate select bits to 0.

5.4.9 Low-Power Operation in Wait Mode

The WAI instruction puts the MCU in a low power consumption stand-by mode depending on setting of the individual bits in the CLKSEL register. All individual wait mode configuration bits can be superposed. This provides enhanced granularity in reducing the level of power consumption during wait mode. Table 5-10 lists the individual configuration bits and the parts of the MCU that are affected in wait mode.

Table 5-10. MCU Configuration During Wait Mode

	PLLWAI	CWAI	SYSWAI	RTIWAI	COPWAI	ROAWAI
PLL	stopped	—	—	—	—	—
Core	—	stopped	stopped	—	—	—
System	—	—	stopped	—	—	—
RTI	—	—	—	stopped	—	—
COP	—	—	—	—	stopped	—
Oscillator	—	—	—	—	—	reduced[1]

[1] Refer to oscillator block description for availability of a reduced oscillator amplitude.

After executing the WAI instruction the core requests the CRG to switch MCU into wait mode. The CRG then checks whether the PLLWAI, CWAI and SYSWAI bits are asserted (see Figure 5-23). Depending on the configuration the CRG switches the system and core clocks to OSCCLK by clearing the PLLSEL bit, disables the PLL, disables the core clocks and finally disables the remaining system clocks. As soon as all clocks are switched off wait mode is active.

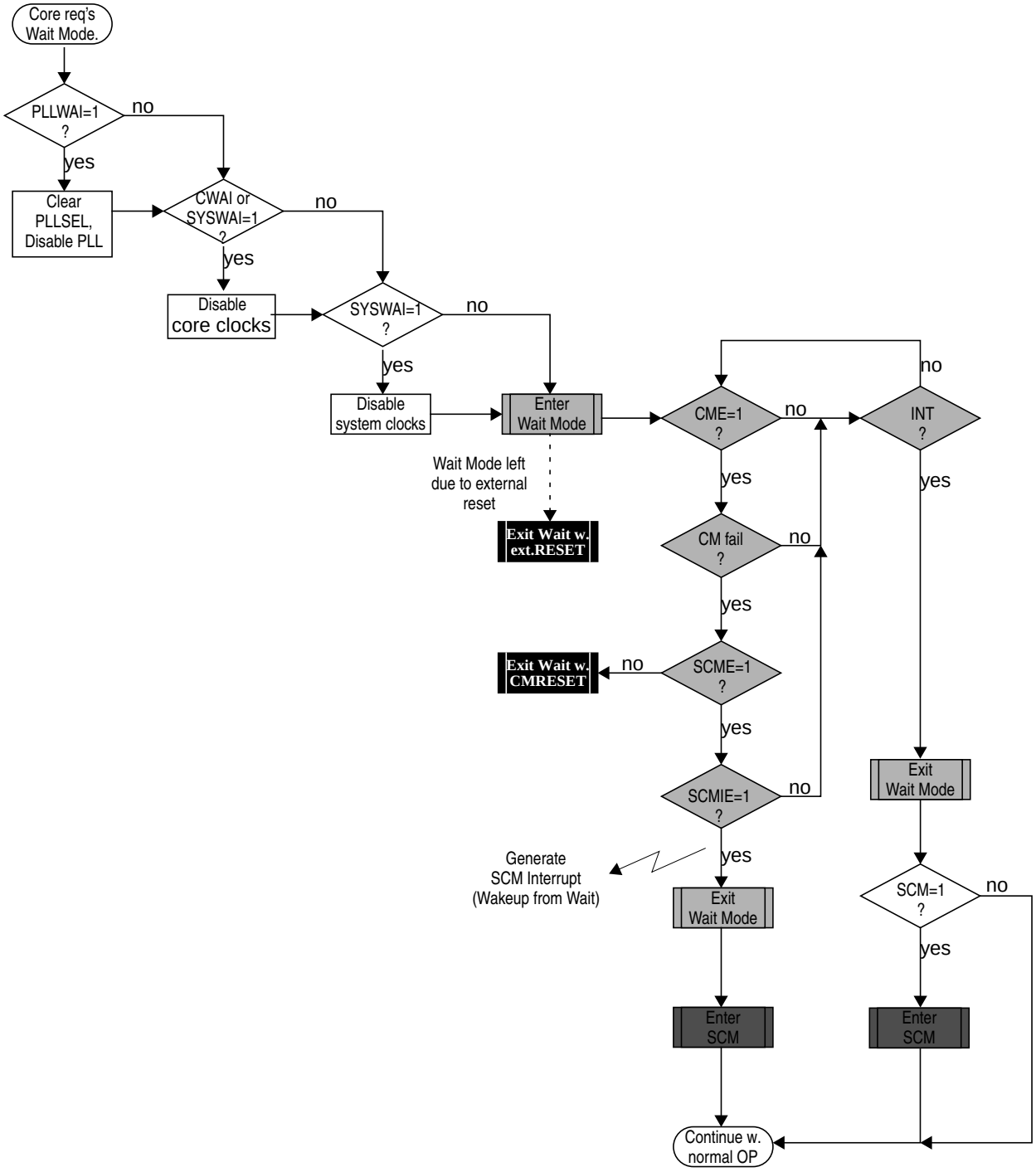


Figure 5-23. Wait Mode Entry/Exit Sequence

There are five different scenarios for the CRG to restart the MCU from wait mode:

- External reset
- Clock monitor reset
- COP reset
- Self-clock mode interrupt
- Real-time interrupt (RTI)

If the MCU gets an external reset during wait mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Wait mode is exited and the MCU is in run mode again.

If the clock monitor is enabled (CME=1) the MCU is able to leave wait mode when loss of oscillator/external clock is detected by a clock monitor fail. If the SCME bit is not asserted the CRG generates a clock monitor fail reset (CMRESET). The CRG's behavior for CMRESET is the same compared to external reset, but another reset vector is fetched after completion of the reset sequence. If the SCME bit is asserted the CRG generates a SCM interrupt if enabled (SCMIE=1). After generating the interrupt the CRG enters self-clock mode and starts the clock quality checker (see Section 5.4.4, "Clock Quality Checker"). Then the MCU continues with normal operation.If the SCM interrupt is blocked by SCMIE = 0, the SCMIF flag will be asserted and clock quality checks will be performed but the MCU will not wake-up from wait mode.

If any other interrupt source (e.g. RTI) triggers exit from wait mode the MCU immediately continues with normal operation. If the PLL has been powered-down during wait mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving wait mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

If wait mode is entered from self-clock mode, the CRG will continue to check the clock quality until clock check is successful. The PLL and voltage regulator (VREG) will remain enabled.

Table 5-11 summarizes the outcome of a clock loss while in wait mode.

Table 5-11. Outcome of Clock Loss in Wait Mode

CME	SCME	SCMIE	CRG Actions
0	X	X	Clock failure --> No action, clock loss not detected.
1	0	X	Clock failure --> CRG performs Clock Monitor Reset immediately
1	1	0	Clock failure --> Scenario 1: OSCCLK **recovers** prior to exiting Wait Mode. – MCU remains in Wait Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag. *Some time later OSCCLK recovers.* – CM no longer indicates a failure, – 4096 OSCCLK cycles later Clock Quality Check indicates clock o.k., – SCM deactivated, – PLL disabled depending on PLLWAI, – VREG remains enabled *(never gets disabled in Wait Mode)*. – MCU remains in Wait Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Wait Mode using OSCCLK as system clock (SYSCLK), – Continue normal operation. *or an External Reset is applied.* – Exit Wait Mode using OSCCLK as system clock, – Start reset sequence. Scenario 2: OSCCLK **does not recover** prior to exiting Wait Mode. – MCU remains in Wait Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag, – Keep performing Clock Quality Checks (could continue infinitely) while in Wait Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform additional Clock Quality Checks until OSCCLK is o.k. again. or an External RESET is applied. – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Start reset sequence, – Continue to perform additional Clock Quality Checks until OSCCLK is o.k.again.

Table 5-11. Outcome of Clock Loss in Wait Mode (continued)

CME	SCME	SCMIE	CRG Actions
1	1	1	Clock failure --> – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – SCMIF set. SCMIF generates Self-Clock Mode wakeup interrupt. – Exit Wait Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform a additional Clock Quality Checks until OSCCLK is o.k. again.

5.4.10 Low-Power Operation in Stop Mode

All clocks are stopped in STOP mode, dependent of the setting of the PCE, PRE and PSTP bit. The oscillator is disabled in STOP mode unless the PSTP bit is set. All counters and dividers remain frozen but do not initialize. If the PRE or PCE bits are set, the RTI or COP continues to run in pseudo-stop mode. In addition to disabling system and core clocks the CRG requests other functional units of the MCU (e.g. voltage-regulator) to enter their individual power-saving modes (if available). This is the main difference between pseudo-stop mode and wait mode.

After executing the STOP instruction the core requests the CRG to switch the MCU into stop mode. If the PLLSEL bit remains set when entering stop mode, the CRG will switch the system and core clocks to OSCCLK by clearing the PLLSEL bit. Then the CRG disables the PLL, disables the core clock and finally disables the remaining system clocks. As soon as all clocks are switched off, stop mode is active.

If pseudo-stop mode (PSTP = 1) is entered from self-clock mode the CRG will continue to check the clock quality until clock check is successful. The PLL and the voltage regulator (VREG) will remain enabled. If full stop mode (PSTP = 0) is entered from self-clock mode an ongoing clock quality check will be stopped. A complete timeout window check will be started when stop mode is exited again.

Wake-up from stop mode also depends on the setting of the PSTP bit.

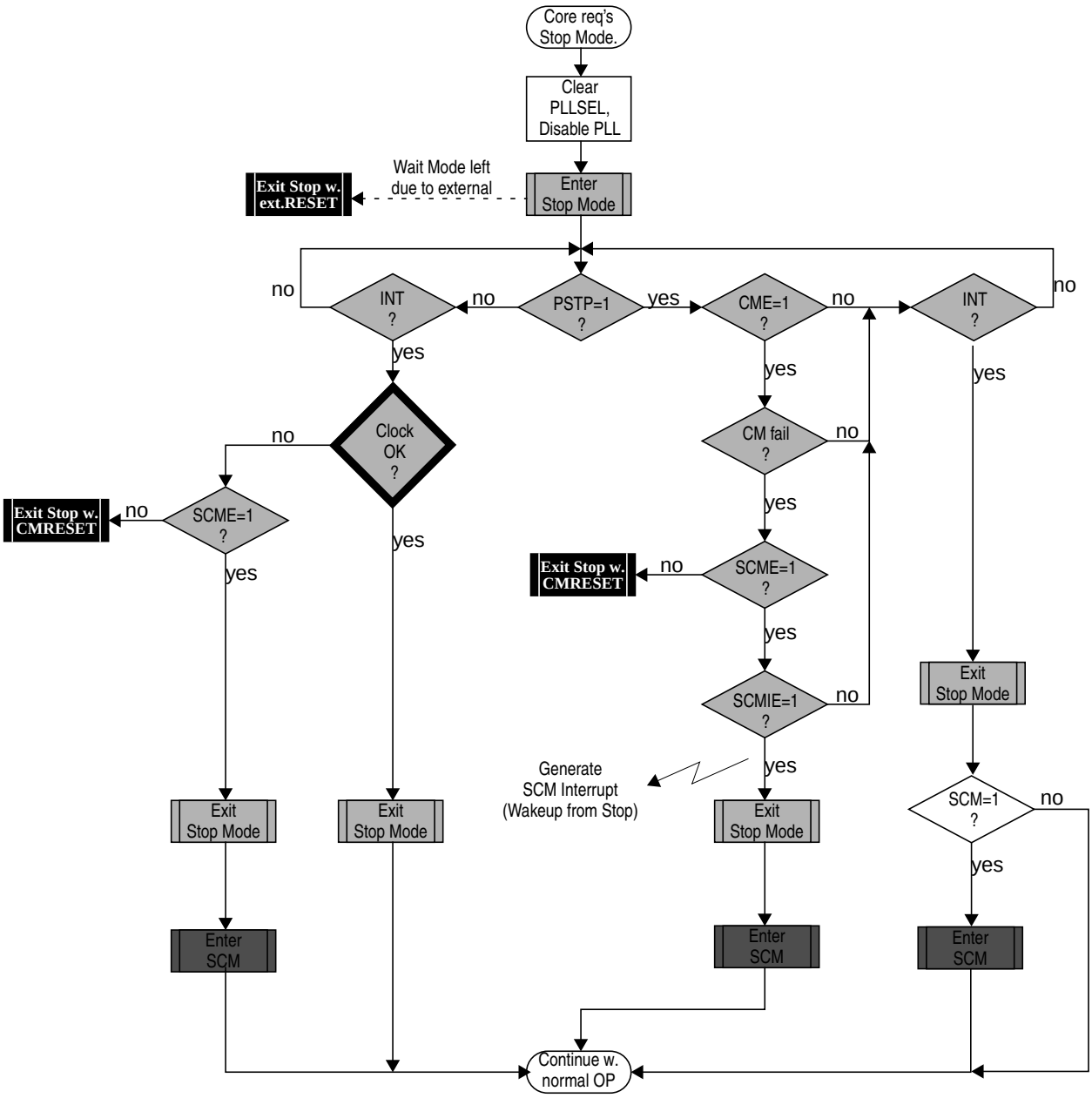


Figure 5-24. Stop Mode Entry/Exit Sequence

5.4.10.1 Wake-Up from Pseudo-Stop (PSTP=1)

Wake-up from pseudo-stop is the same as wake-up from wait mode. There are also three different scenarios for the CRG to restart the MCU from pseudo-stop mode:

- External reset
- Clock monitor fail
- Wake-up interrupt

If the MCU gets an external reset during pseudo-stop mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Pseudo-stop mode is exited and the MCU is in run mode again.

If the clock monitor is enabled (CME = 1) the MCU is able to leave pseudo-stop mode when loss of oscillator/external clock is detected by a clock monitor fail. If the SCME bit is not asserted the CRG generates a clock monitor fail reset (CMRESET). The CRG's behavior for CMRESET is the same compared to external reset, but another reset vector is fetched after completion of the reset sequence. If the SCME bit is asserted the CRG generates a SCM interrupt if enabled (SCMIE=1). After generating the interrupt the CRG enters self-clock mode and starts the clock quality checker (see Section 5.4.4, "Clock Quality Checker"). Then the MCU continues with normal operation. If the SCM interrupt is blocked by SCMIE = 0, the SCMIF flag will be asserted but the CRG will not wake-up from pseudo-stop mode.

If any other interrupt source (e.g. RTI) triggers exit from pseudo-stop mode the MCU immediately continues with normal operation. Because the PLL has been powered-down during stop mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving stop mode. The software must set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

Table 5-12 summarizes the outcome of a clock loss while in pseudo-stop mode.

Table 5-12. Outcome of Clock Loss in Pseudo-Stop Mode

CME	SCME	SCMIE	CRG Actions
0	X	X	Clock failure --> No action, clock loss not detected.
1	0	X	Clock failure --> CRG performs Clock Monitor Reset immediately
1	1	0	Clock Monitor failure --> Scenario 1: OSCCLK **recovers** prior to exiting Pseudo-Stop Mode. – MCU remains in Pseudo-Stop Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag. *Some time later OSCCLK recovers.* – CM no longer indicates a failure, – 4096 OSCCLK cycles later Clock Quality Check indicates clock o.k., – SCM deactivated, – PLL disabled, – VREG disabled. – MCU remains in Pseudo-Stop Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Pseudo-Stop Mode using OSCCLK as system clock (SYSCLK), – Continue normal operation. *or an External Reset is applied.* – Exit Pseudo-Stop Mode using OSCCLK as system clock, – Start reset sequence. Scenario 2: OSCCLK **does not recover** prior to exiting Pseudo-Stop Mode. – MCU remains in Pseudo-Stop Mode, – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – Set SCMIF interrupt flag, – Keep performing Clock Quality Checks (could continue infinitely) while in Pseudo-Stop Mode. *Some time later either a wakeup interrupt occurs (no SCM interrupt)* – Exit Pseudo-Stop Mode in SCM using PLL clock (f_{SCM}) as system clock – Continue to perform additional Clock Quality Checks until OSCCLK is o.k. again. or an External RESET is applied. – Exit Pseudo-Stop Mode in SCM using PLL clock (f_{SCM}) as system clock – Start reset sequence, – Continue to perform additional Clock Quality Checks until OSCCLK is o.k.again.

Table 5-12. Outcome of Clock Loss in Pseudo-Stop Mode (continued)

CME	SCME	SCMIE	CRG Actions
1	1	1	Clock failure --> – VREG enabled, – PLL enabled, – SCM activated, – Start Clock Quality Check, – SCMIF set. SCMIF generates Self-Clock Mode wakeup interrupt. – Exit Pseudo-Stop Mode in SCM using PLL clock (f_{SCM}) as system clock, – Continue to perform a additional Clock Quality Checks until OSCCLK is o.k. again.

5.4.10.2 Wake-up from Full Stop (PSTP=0)

The MCU requires an external interrupt or an external reset in order to wake-up from stop mode.

If the MCU gets an external reset during full stop mode active, the CRG asynchronously restores all configuration bits in the register space to its default settings and will perform a maximum of 50 clock *check_windows* (see Section 5.4.4, “Clock Quality Checker”). After completing the clock quality check the CRG starts the reset generator. After completing the reset sequence processing begins by fetching the normal reset vector. Full stop mode is exited and the MCU is in run mode again.

If the MCU is woken-up by an interrupt, the CRG will also perform a maximum of 50 clock *check_windows* (see Section 5.4.4, “Clock Quality Checker”). If the clock quality check is successful, the CRG will release all system and core clocks and will continue with normal operation. If all clock checks within the timeout-window are failing, the CRG will switch to self-clock mode or generate a clock monitor reset (CMRESET) depending on the setting of the SCME bit.

Because the PLL has been powered-down during stop mode the PLLSEL bit is cleared and the MCU runs on OSCCLK after leaving stop mode. The software must manually set the PLLSEL bit again, in order to switch system and core clocks to the PLLCLK.

NOTE

In full stop mode, the clock monitor is disabled and any loss of clock will not be detected.

5.5 Resets

This section describes how to reset the CRG and how the CRG itself controls the reset of the MCU. It explains all special reset requirements. Because the reset generator for the MCU is part of the CRG, this section also describes all automatic actions that occur during or as a result of individual reset conditions. The reset values of registers and signals are provided in Section 5.3, “Memory Map and Register

Definition." All reset sources are listed in Table 5-13. Refer to the device overview chapter for related vector addresses and priorities.

Table 5-13. Reset Summary

Reset Source	Local Enable
Power-on Reset	None
Low Voltage Reset	None
External Reset	None
Clock Monitor Reset	PLLCTL (CME=1, SCME=0)
COP Watchdog Reset	COPCTL (CR[2:0] nonzero)

The reset sequence is initiated by any of the following events:

- Low level is detected at the $\overline{\text{RESET}}$ pin (external reset).
- Power on is detected.
- Low voltage is detected.
- COP watchdog times out.
- Clock monitor failure is detected and self-clock mode was disabled (SCME = 0).

Upon detection of any reset event, an internal circuit drives the $\overline{\text{RESET}}$ pin low for 128 SYSCLK cycles (see Figure 5-25). Because entry into reset is asynchronous it does not require a running SYSCLK. However, the internal reset circuit of the CRG cannot sequence out of current reset condition without a running SYSCLK. The number of 128 SYSCLK cycles might be increased by n = 3 to 6 additional SYSCLK cycles depending on the internal synchronization latency. After 128+n SYSCLK cycles the $\overline{\text{RESET}}$ pin is released. The reset generator of the CRG waits for additional 64 SYSCLK cycles and then samples the RESET pin to determine the originating source. Table 5-14 shows which vector will be fetched.

Table 5-14. Reset Vector Selection

Sampled $\overline{\text{RESET}}$ Pin (64 Cycles After Release)	Clock Monitor Reset Pending	COP Reset Pending	Vector Fetch
1	0	0	POR / LVR / External Reset
1	1	X	Clock Monitor Reset
1	0	1	COP Reset
0	X	X	POR / LVR / External Reset with rise of $\overline{\text{RESET}}$ pin

NOTE

External circuitry connected to the $\overline{\text{RESET}}$ pin should not include a large capacitance that would interfere with the ability of this signal to rise to a valid logic 1 within 64 SYSCLK cycles after the low drive is released.

The internal reset of the MCU remains asserted while the reset generator completes the 192 SYSCLK long reset sequence. The reset generator circuitry always makes sure the internal reset is deasserted synchronously after completion of the 192 SYSCLK cycles. In case the RESET pin is externally driven low for more than these 192 SYSCLK cycles (external reset), the internal reset remains asserted too.

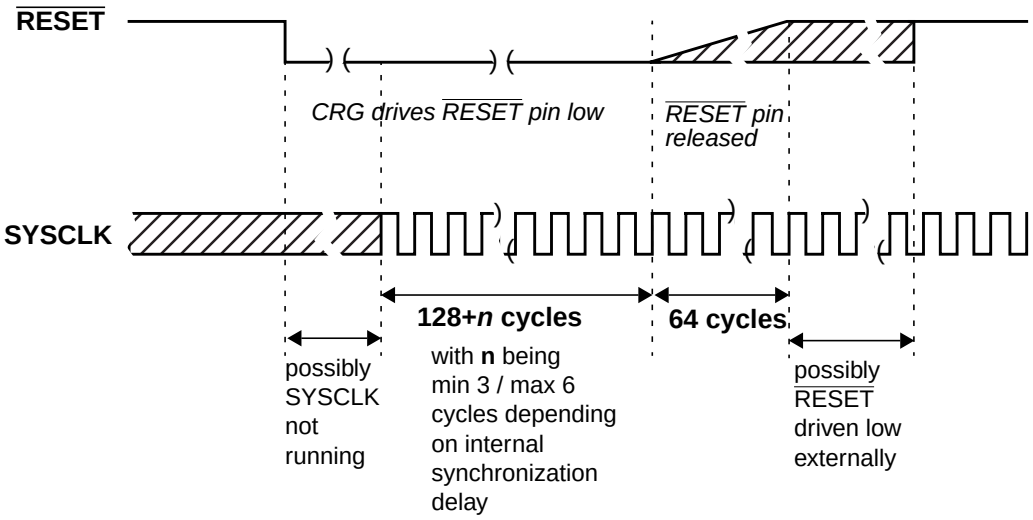


Figure 5-25. RESET Timing

5.5.1 Clock Monitor Reset

The CRG generates a clock monitor reset in case all of the following conditions are true:

- Clock monitor is enabled (CME=1)
- Loss of clock is detected
- Self-clock mode is disabled (SCME=0)

The reset event asynchronously forces the configuration registers to their default settings (see Section 5.3, “Memory Map and Register Definition”). In detail the CME and the SCME are reset to logical ‘1’ (which doesn’t change the state of the CME bit, because it has already been set). As a consequence, the CRG immediately enters self-clock mode and starts its internal reset sequence. In parallel the clock quality check starts. As soon as clock quality check indicates a valid oscillator clock the CRG switches to OSCCLK and leaves self-clock mode. Because the clock quality checker is running in parallel to the reset generator, the CRG may leave self-clock mode while completing the internal reset sequence. When the reset sequence is finished the CRG checks the internally latched state of the clock monitor fail circuit. If a clock monitor fail is indicated processing begins by fetching the clock monitor reset vector.

5.5.2 Computer Operating Properly Watchdog (COP) Reset

When COP is enabled, the CRG expects sequential write of 0x0055 and 0x00AA (in this order) to the ARMCOP register during the selected time-out period. As soon as this is done, the COP time-out period restarts. If the program fails to do this the CRG will generate a reset. Also, if any value other than 0x0055 or 0x00AA is written, the CRG immediately generates a reset. In case windowed COP operation is enabled

writes (0x0055 or 0x00AA) to the ARMCOP register must occur in the last 25% of the selected time-out period. A premature write the CRG will immediately generate a reset.

As soon as the reset sequence is completed the reset generator checks the reset condition. If no clock monitor failure is indicated and the latched state of the COP timeout is true, processing begins by fetching the COP vector.

5.5.3 Power-On Reset, Low Voltage Reset

The on-chip voltage regulator detects when V_{DD} to the MCU has reached a certain level and asserts power-on reset or low voltage reset or both. As soon as a power-on reset or low voltage reset is triggered the CRG performs a quality check on the incoming clock signal. As soon as clock quality check indicates a valid oscillator clock signal the reset sequence starts using the oscillator clock. If after 50 check windows the clock quality check indicated a non-valid oscillator clock the reset sequence starts using self-clock mode.

Figure 5-26 and Figure 5-27 show the power-up sequence for cases when the $\overline{\text{RESET}}$ pin is tied to V_{DD} and when the $\overline{\text{RESET}}$ pin is held low.

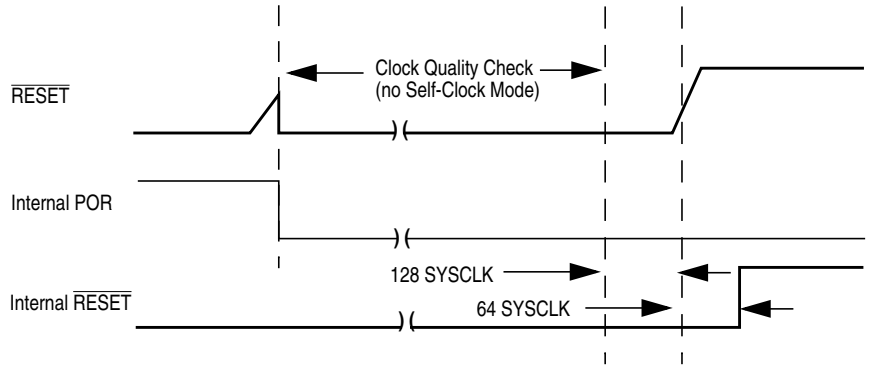


Figure 5-26. $\overline{\text{RESET}}$ Pin Tied to V_{DD} (by a Pull-Up Resistor)

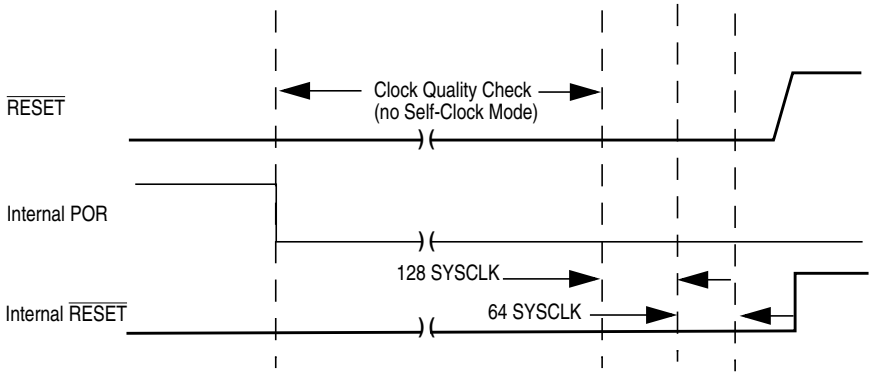


Figure 5-27. $\overline{\text{RESET}}$ Pin Held Low Externally

5.6 Interrupts

The interrupts/reset vectors requested by the CRG are listed in Table 5-15. Refer to the device overview chapter for related vector addresses and priorities.

Table 5-15. CRG Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Real-time interrupt	I bit	CRGINT (RTIE)
LOCK interrupt	I bit	CRGINT (LOCKIE)
SCM interrupt	I bit	CRGINT (SCMIE)

5.6.1 Real-Time Interrupt

The CRG generates a real-time interrupt when the selected interrupt time period elapses. RTI interrupts are locally disabled by setting the RTIE bit to 0. The real-time interrupt flag (RTIF) is set to 1 when a timeout occurs, and is cleared to 0 by writing a 1 to the RTIF bit.

The RTI continues to run during pseudo-stop mode if the PRE bit is set to 1. This feature can be used for periodic wakeup from pseudo-stop if the RTI interrupt is enabled.

5.6.2 PLL Lock Interrupt

The CRG generates a PLL lock interrupt when the LOCK condition of the PLL has changed, either from a locked state to an unlocked state or vice versa. Lock interrupts are locally disabled by setting the LOCKIE bit to 0. The PLL Lock interrupt flag (LOCKIF) is set to1 when the LOCK condition has changed, and is cleared to 0 by writing a 1 to the LOCKIF bit.

5.6.3 Self-Clock Mode Interrupt

The CRG generates a self-clock mode interrupt when the SCM condition of the system has changed, either entered or exited self-clock mode. SCM conditions can only change if the self-clock mode enable bit (SCME) is set to 1. SCM conditions are caused by a failing clock quality check after power-on reset (POR) or low voltage reset (LVR) or recovery from full stop mode (PSTP = 0) or clock monitor failure. For details on the clock quality check refer to Section 5.4.4, “Clock Quality Checker.” If the clock monitor is enabled (CME = 1) a loss of external clock will also cause a SCM condition (SCME = 1).

SCM interrupts are locally disabled by setting the SCMIE bit to 0. The SCM interrupt flag (SCMIF) is set to 1 when the SCM condition has changed, and is cleared to 0 by writing a 1 to the SCMIF bit.

Chapter 6
Oscillator (OSCV2)

6.1 Introduction

The OSC module provides two alternative oscillator concepts:

- A low noise and low power Colpitts oscillator with amplitude limitation control (ALC)
- A robust full swing Pierce oscillator with the possibility to feed in an external square wave

6.1.1 Features

The Colpitts OSC option provides the following features:

- Amplitude limitation control (ALC) loop:
  - Low power consumption and low current induced RF emission
  - Sinusoidal waveform with low RF emission
  - Low crystal stress (an external damping resistor is not required)
  - Normal and low amplitude mode for further reduction of power and emission
- An external biasing resistor is not required

The Pierce OSC option provides the following features:

- Wider high frequency operation range
- No DC voltage applied across the crystal
- Full rail-to-rail (2.5 V nominal) swing oscillation with low EM susceptibility
- Fast start up

Common features:

- Clock monitor (CM)
- Operation from the V_{DDPLL} 2.5 V (nominal) supply rail

6.1.2 Modes of Operation

Two modes of operation exist:

- Amplitude limitation controlled Colpitts oscillator mode suitable for power and emission critical applications
- Full swing Pierce oscillator mode that can also be used to feed in an externally generated square wave suitable for high frequency operation and harsh environments

6.2 External Signal Description

This section lists and describes the signals that connect off chip.

6.2.1 V_{DDPLL} and V_{SSPLL} — PLL Operating Voltage, PLL Ground

These pins provide the operating voltage (V_{DDPLL}) and ground (V_{SSPLL}) for the OSC circuitry. This allows the supply voltage to the OSC to be independently bypassed.

6.2.2 EXTAL and XTAL — Clock/Crystal Source Pins

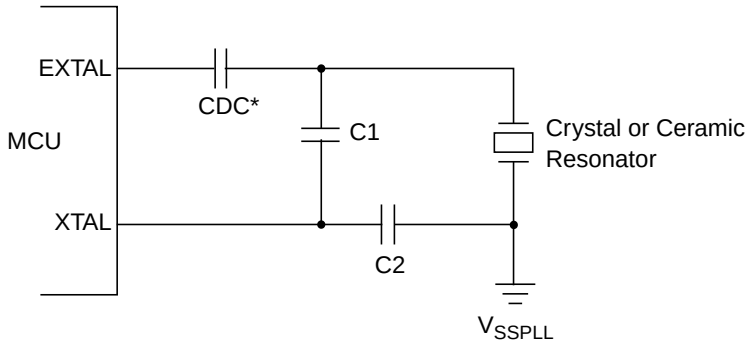
These pins provide the interface for either a crystal or a CMOS compatible clock to control the internal clock generator circuitry. EXTAL is the external clock input or the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. All the MCU internal system clocks are derived from the EXTAL input frequency. In full stop mode (PSTP = 0) the EXTAL pin is pulled down by an internal resistor of typical 200 kΩ.

NOTE

Freescale Semiconductor recommends an evaluation of the application board and chosen resonator or crystal by the resonator or crystal supplier.

The Crystal circuit is changed from standard.

The Colpitts circuit is not suited for overtone resonators and crystals.



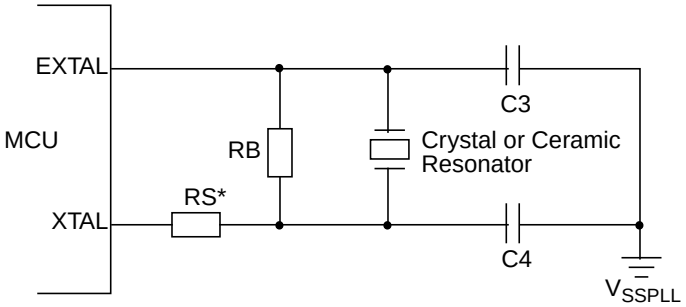
* Due to the nature of a translated ground Colpitts oscillator a DC voltage bias is applied to the crystal.

Please contact the crystal manufacturer for crystal DC bias conditions and recommended capacitor value CDC.

Figure 6-1. Colpitts Oscillator Connections (XCLKS = 0)

NOTE

The Pierce circuit is not suited for overtone resonators and crystals without a careful component selection.



* Rs can be zero (shorted) when used with higher frequency crystals.
Refer to manufacturer's data.

Figure 6-2. Pierce Oscillator Connections (XCLKS = 1)

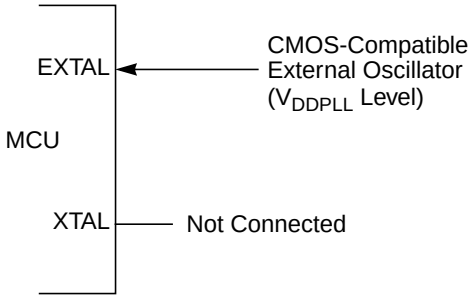


Figure 6-3. External Clock Connections (XCLKS = 1)

6.2.3 XCLKS — Colpitts/Pierce Oscillator Selection Signal

The XCLKS is an input signal which controls whether a crystal in combination with the internal Colpitts (low power) oscillator is used or whether the Pierce oscillator/external clock circuitry is used. The XCLKS signal is sampled during reset with the rising edge of $\overline{\text{RESET}}$. Table 6-1 lists the state coding of the sampled XCLKS signal. Refer to the device overview chapter for polarity of the XCLKS pin.

Table 6-1. Clock Selection Based on XCLKS

XCLKS	Description
0	Colpitts oscillator selected
1	Pierce oscillator/external clock selected

6.3 Memory Map and Register Definition

The CRG contains the registers and associated bits for controlling and monitoring the OSC module.

6.4 Functional Description

The OSC block has two external pins, EXTAL and XTAL. The oscillator input pin, EXTAL, is intended to be connected to either a crystal or an external clock source. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. The XTAL pin is an output signal that provides crystal circuit feedback.

A buffered EXTAL signal, OSCCLK, becomes the internal reference clock. To improve noise immunity, the oscillator is powered by the V_{DDPLL} and V_{SSPLL} power supply pins.

The Pierce oscillator can be used for higher frequencies compared to the low power Colpitts oscillator.

6.4.1 Amplitude Limitation Control (ALC)

The Colpitts oscillator is equipped with a feedback system which does not waste current by generating harmonics. Its configuration is “Colpitts oscillator with translated ground.” The transconductor used is driven by a current source under the control of a peak detector which will measure the amplitude of the AC signal appearing on EXTAL node in order to implement an amplitude limitation control (ALC) loop. The ALC loop is in charge of reducing the quiescent current in the transconductor as a result of an increase in the oscillation amplitude. The oscillation amplitude can be limited to two values. The normal amplitude which is intended for non power saving modes and a small amplitude which is intended for low power operation modes. Please refer to the CRG block description chapter for the control and assignment of the amplitude value to operation modes.

6.4.2 Clock Monitor (CM)

The clock monitor circuit is based on an internal resistor-capacitor (RC) time delay so that it can operate without any MCU clocks. If no OSCCLK edges are detected within this RC time delay, the clock monitor indicates a failure which asserts self clock mode or generates a system reset depending on the state of SCME bit. If the clock monitor is disabled or the presence of clocks is detected no failure is indicated.The clock monitor function is enabled/disabled by the CME control bit, described in the CRG block description chapter.

6.5 Interrupts

OSC contains a clock monitor, which can trigger an interrupt or reset. The control bits and status bits for the clock monitor are described in the CRG block description chapter.

Chapter 7
Analog-to-Digital Converter (ATD10B16CV4)

7.1 Introduction

The ATD10B16C is a 16-channel, 10-bit, multiplexed input successive approximation analog-to-digital converter. Refer to the Electrical Specifications chapter for ATD accuracy.

7.1.1 Features

- 8-/10-bit resolution
- 7 µs, 10-bit single conversion time
- Sample buffer amplifier
- Programmable sample time
- Left/right justified, signed/unsigned result data
- External trigger control
- Conversion completion interrupt generation
- Analog input multiplexer for 16 analog input channels
- Analog/digital input pin multiplexing
- 1 to 16 conversion sequence lengths
- Continuous conversion mode
- Multiple channel scans
- Configurable external trigger functionality on any AD channel or any of four additional trigger inputs. The four additional trigger inputs can be chip external or internal. Refer to device specification for availability and connectivity
- Configurable location for channel wrap around (when converting multiple channels in a sequence)

7.1.2 Modes of Operation

There is software programmable selection between performing **single** or **continuous conversion** on a **single channel** or **multiple channels**.

7.1.3 Block Diagram

Refer to Figure 7-1 for a block diagram of the ATD0B16C block.

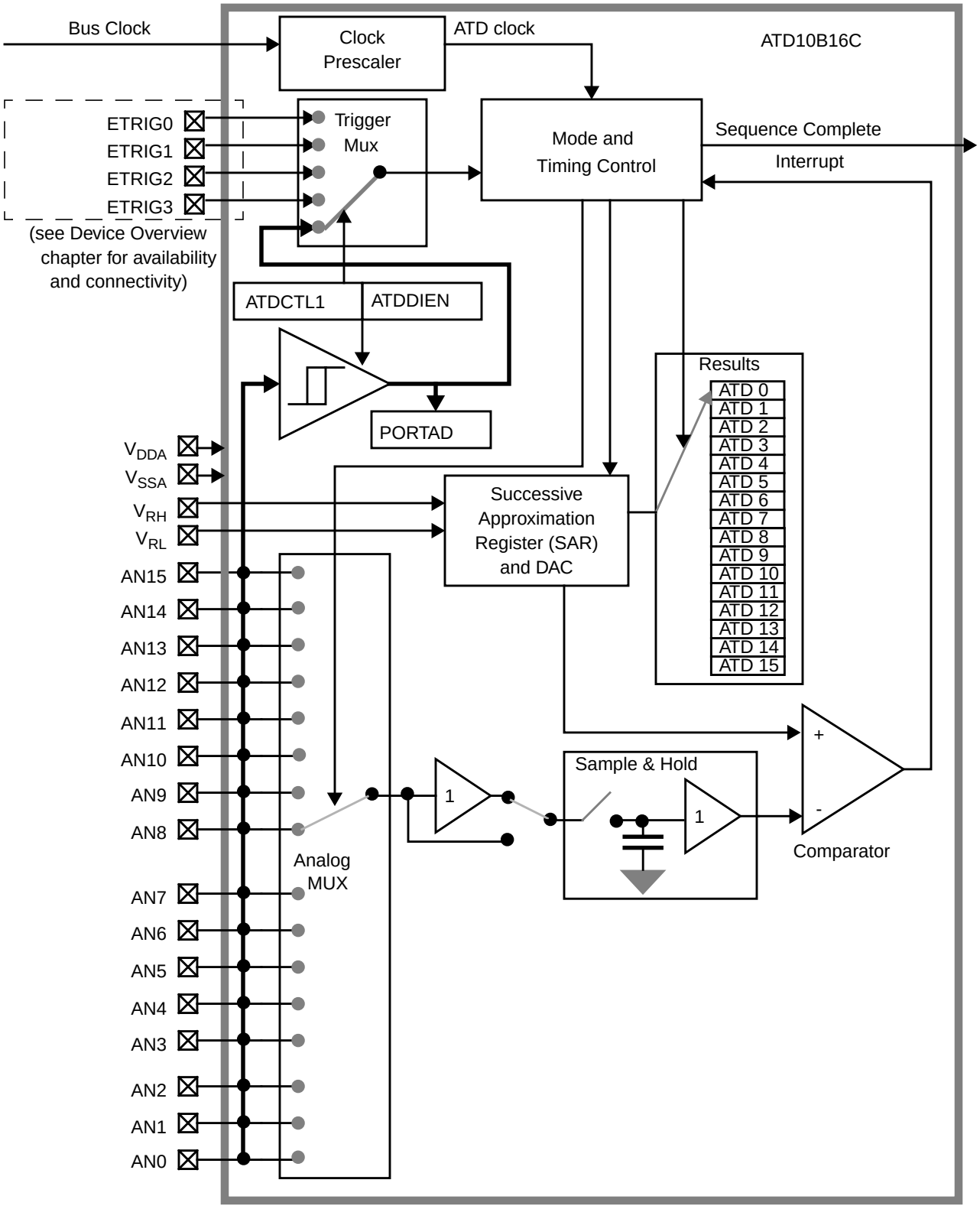


Figure 7-1. ATD10B16C Block Diagram

7.2 External Signal Description

This section lists all inputs to the ATD10B16C block.

7.2.1 AN*x* (*x* = 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0) — Analog Input Channel *x* Pins

This pin serves as the analog input channel *x*. It can also be configured as general-purpose digital input and/or external trigger for the ATD conversion.

7.2.2 ETRIG3, ETRIG2, ETRIG1, ETRIG0 — External Trigger Pins

These inputs can be configured to serve as an external trigger for the ATD conversion.

Refer to the Device Overview chapter for availability and connectivity of these inputs.

7.2.3 V_{RH}, V_{RL} — High Reference Voltage Pin, Low Reference Voltage Pin

V_{RH} is the high reference voltage, V_{RL} is the low reference voltage for ATD conversion.

7.2.4 V_{DDA}, V_{SSA} — Analog Circuitry Power Supply Pins

These pins are the power supplies for the analog circuitry of the ATD10B16C block.

7.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the ATD10B16C.

7.3.1 Module Memory Map

Table 7-1 gives an overview of all ATD10B16C registers

Table 7-1. ATD10B16C Memory Map

Address Offset	Use	Access
0x0000	ATD Control Register 0 (ATDCTL0)	R/W
0x0001	ATD Control Register 1 (ATDCTL1)	R/W
0x0002	ATD Control Register 2 (ATDCTL2)	R/W
0x0003	ATD Control Register 3 (ATDCTL3)	R/W
0x0004	ATD Control Register 4 (ATDCTL4)	R/W
0x0005	ATD Control Register 5 (ATDCTL5)	R/W
0x0006	ATD Status Register 0 (ATDSTAT0)	R/W
0x0007	Unimplemented	
0x0008	ATD Test Register 0 (ATDTEST0)[1]	R
0x0009	ATD Test Register 1 (ATDTEST1)	R/W
0x000A	ATD Status Register 2 (ATDSTAT2)	R
0x000B	ATD Status Register 1 (ATDSTAT1)	R
0x000C	ATD Input Enable Register 0 (ATDDIEN0)	R/W
0x000D	ATD Input Enable Register 1 (ATDDIEN1)	R/W
0x000E	Port Data Register 0 (PORTAD0)	R
0x000F	Port Data Register 1 (PORTAD1)	R
0x0010, 0x0011	ATD Result Register 0 (ATDDR0H, ATDDR0L)	R/W
0x0012, 0x0013	ATD Result Register 1 (ATDDR1H, ATDDR1L)	R/W
0x0014, 0x0015	ATD Result Register 2 (ATDDR2H, ATDDR2L)	R/W
0x0016, 0x0017	ATD Result Register 3 (ATDDR3H, ATDDR3L)	R/W
0x0018, 0x0019	ATD Result Register 4 (ATDDR4H, ATDDR4L)	R/W
0x001A, 0x001B	ATD Result Register 5 (ATDDR5H, ATDDR5L)	R/W
0x001C, 0x001D	ATD Result Register 6 (ATDDR6H, ATDDR6L)	R/W
0x001E, 0x001F	ATD Result Register 7 (ATDDR7H, ATDDR7L)	R/W
0x0020, 0x0021	ATD Result Register 8 (ATDDR8H, ATDDR8L)	R/W
0x0022, 0x0023	ATD Result Register 9 (ATDDR9H, ATDDR9L)	R/W
0x0024, 0x0025	ATD Result Register 10 (ATDDR10H, ATDDR10L)	R/W
0x0026, 0x0027	ATD Result Register 11 (ATDDR11H, ATDDR11L)	R/W
0x0028, 0x0029	ATD Result Register 12 (ATDDR12H, ATDDR12L)	R/W
0x002A, 0x002B	ATD Result Register 13 (ATDDR13H, ATDDR13L)	R/W
0x002C, 0x002D	ATD Result Register 14 (ATDDR14H, ATDDR14L)	R/W
0x002E, 0x002F	ATD Result Register 15 (ATDDR15H, ATDDR15L)	R/W

[1] ATDTEST0 is intended for factory test purposes only.

NOTE

Register Address = Base Address + Address Offset, where the Base Address is defined at the MCU level and the Address Offset is defined at the module level.

7.3.2 Register Descriptions

This section describes in address order all the ATD10B16C registers and their individual bits.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 ATDCTL0	R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
	W								
0x0001 ATDCTL1	R	ETRIGSEL	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
	W								
0x0002 ATDCTL2	R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIGE	ASCIE	ASCIF
	W								
0x0003 ATDCTL3	R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
	W								
0x0004 ATDCTL4	R	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
	W								
0x0005 ATDCTL5	R	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
	W								
0x0006 ATDSTAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
	W								
0x0007 Unimplemented	R								
	W								
0x0008 ATDTEST0	R	Unimplemented							
	W								
0x0009 ATDTEST1	R	Unimplemented							SC
	W								
0x000A ATDSTAT2	R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
	W								
0x000B ATDSTAT1	R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
	W								
0x000C ATDDIEN0	R	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
	W								

= Unimplemented or Reserved u = Unaffected

Figure 7-2. ATD Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000D ATDDIEN1	R	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
	W								
0x000E PORTAD0	R	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
	W								
0x000F PORTAD1	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
	W								
0x0010–0x002F ATDDRxH–ATDDRxL	R	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
	W								
	R	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
	W								

= Unimplemented or Reserved u = Unaffected

Figure 7-2. ATD Register Summary (continued)

7.3.2.1 ATD Control Register 0 (ATDCTL0)

Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 7-3. ATD Control Register 0 (ATDCTL0)

Read: Anytime

Write: Anytime

Table 7-2. ATDCTL0 Field Descriptions

Field	Description
3:0 WRAP[3:0]	**Wrap Around Channel Select Bits** — These bits determine the channel for wrap around when doing multi-channel conversions. The coding is summarized in Table 7-3.

Table 7-3. Multi-Channel Wrap Around Coding

WRAP3	WRAP2	WRAP1	WRAP0	Multiple Channel Conversions (MULT = 1) Wrap Around to AN0 after Converting
0	0	0	0	Reserved
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

7.3.2.2 ATD Control Register 1 (ATDCTL1)

Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R	ETRIGSEL	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 7-4. ATD Control Register 1 (ATDCTL1)

Read: Anytime

Write: Anytime

Table 7-4. ATDCTL1 Field Descriptions

Field	Description
7 ETRIGSEL	**External Trigger Source Select** — This bit selects the external trigger source to be either one of the AD channels or one of the ETRIG[3:0] inputs. See device specification for availability and connectivity of ETRIG[3:0] inputs. If ETRIG[3:0] input option is not available, writing a 1 to ETRISEL only sets the bit but has no effect, that means one of the AD channels (selected by ETRIGCH[3:0]) remains the source for external trigger. The coding is summarized in Table 7-5.
3:0 ETRIGCH[3:0]	**External Trigger Channel Select** — These bits select one of the AD channels or one of the ETRIG[3:0] inputs as source for the external trigger. The coding is summarized in Table 7-5.

Table 7-5. External Trigger Channel Select Coding

ETRIGSEL	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0	External Trigger Source
0	0	0	0	0	AN0
0	0	0	0	1	AN1
0	0	0	1	0	AN2
0	0	0	1	1	AN3
0	0	1	0	0	AN4
0	0	1	0	1	AN5
0	0	1	1	0	AN6
0	0	1	1	1	AN7
0	1	0	0	0	AN8
0	1	0	0	1	AN9
0	1	0	1	0	AN10
0	1	0	1	1	AN11
0	1	1	0	0	AN12
0	1	1	0	1	AN13
0	1	1	1	0	AN14
0	1	1	1	1	AN15
1	0	0	0	0	ETRIG0[1]
1	0	0	0	1	ETRIG1[1]
1	0	0	1	0	ETRIG2[1]
1	0	0	1	1	ETRIG3[1]
1	0	1	X	X	Reserved
1	1	X	X	X	Reserved

[1] Only if ETRIG[3:0] input option is available (see device specification), else ETRISEL is ignored, that means external trigger source remains on one of the AD channels selected by ETRIGCH[3:0]

7.3.2.3 ATD Control Register 2 (ATDCTL2)

This register controls power down, interrupt and external trigger. Writes to this register will abort current conversion sequence but will not start a new sequence.

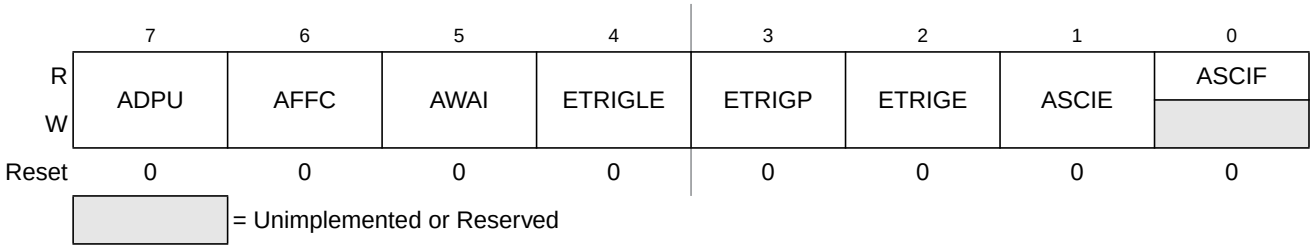


Figure 7-5. ATD Control Register 2 (ATDCTL2)

Read: Anytime

Write: Anytime

Table 7-6. ATDCTL2 Field Descriptions

Field	Description
7 ADPU	**ATD Power Down** — This bit provides on/off control over the ATD10B16C block allowing reduced MCU power consumption. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after ADPU bit is enabled. 0 Power down ATD 1 Normal ATD functionality
6 AFFC	**ATD Fast Flag Clear All** 0 ATD flag clearing operates normally (read the status register ATDSTAT1 before reading the result register to clear the associate CCF flag). 1 Changes all ATD conversion complete flags to a fast clear sequence. Any access to a result register will cause the associate CCF flag to clear automatically.
5 AWAI	**ATD Power Down in Wait Mode** — When entering Wait Mode this bit provides on/off control over the ATD10B16C block allowing reduced MCU power. Because analog electronic is turned off when powered down, the ATD requires a recovery time period after exit from Wait mode. 0 ATD continues to run in Wait mode 1 Halt conversion and power down ATD during Wait mode After exiting Wait mode with an interrupt conversion will resume. But due to the recovery time the result of this conversion should be ignored.
4 ETRIGLE	**External Trigger Level/Edge Control** — This bit controls the sensitivity of the external trigger signal. See Table 7-7 for details.
3 ETRIGP	**External Trigger Polarity** — This bit controls the polarity of the external trigger signal. See Table 7-7 for details.
2 ETRIGE	**External Trigger Mode Enable** — This bit enables the external trigger on one of the AD channels or one of the ETRIG[3:0] inputs as described in Table 7-5. If external trigger source is one of the AD channels, the digital input buffer of this channel is enabled. The external trigger allows to synchronize the start of conversion with external events. 0 Disable external trigger 1 Enable external trigger
1 ASCIE	**ATD Sequence Complete Interrupt Enable** 0 ATD Sequence Complete interrupt requests are disabled. 1 ATD Interrupt will be requested whenever ASCIF = 1 is set.
0 ASCIF	**ATD Sequence Complete Interrupt Flag** — If ASCIE = 1 the ASCIF flag equals the SCF flag (see Section 7.3.2.7, “ATD Status Register 0 (ATDSTAT0)”), else ASCIF reads zero. Writes have no effect. 0 No ATD interrupt occurred 1 ATD sequence complete interrupt pending

Table 7-7. External Trigger Configurations

ETRIGLE	ETRIGP	External Trigger Sensitivity
0	0	Falling Edge
0	1	Ring Edge
1	0	Low Level
1	1	High Level

7.3.2.4 ATD Control Register 3 (ATDCTL3)

This register controls the conversion sequence length, FIFO for results registers and behavior in Freeze Mode. Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-6. ATD Control Register 3 (ATDCTL3)

Read: Anytime

Write: Anytime

Table 7-8. ATDCTL3 Field Descriptions

Field	Description
6 S8C	**Conversion Sequence Length** — This bit controls the number of conversions per sequence. Table 7-9 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 Family.
5 S4C	**Conversion Sequence Length** — This bit controls the number of conversions per sequence. Table 7-9 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 Family.
4 S2C	**Conversion Sequence Length** — This bit controls the number of conversions per sequence. Table 7-9 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 Family.
3 S1C	**Conversion Sequence Length** — This bit controls the number of conversions per sequence. Table 7-9 shows all combinations. At reset, S4C is set to 1 (sequence length is 4). This is to maintain software continuity to HC12 Family.

Table 7-8. ATDCTL3 Field Descriptions (continued)

Field	Description
2 FIFO	**Result Register FIFO Mode** —If this bit is zero (non-FIFO mode), the A/D conversion results map into the result registers based on the conversion sequence; the result of the first conversion appears in the first result register, the second result in the second result register, and so on. If this bit is one (FIFO mode) the conversion counter is not reset at the beginning or ending of a conversion sequence; sequential conversion results are placed in consecutive result registers. In a continuously scanning conversion sequence, the result register counter will wrap around when it reaches the end of the result register file. The conversion counter value (CC3-0 in ATDSTAT0) can be used to determine where in the result register file, the current conversion result will be placed. Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-0) clears the conversion counter even if FIFO=1. So the first result of a new conversion sequence, started by writing to ATDCTL5, will always be place in the first result register (ATDDDR0). Intended usage of FIFO mode is continuos conversion (SCAN=1) or triggered conversion (ETRIG=1). Finally, which result registers hold valid data can be tracked using the conversion complete flags. Fast flag clear mode may or may not be useful in a particular application to track valid data. 0 Conversion results are placed in the corresponding result register up to the selected sequence length. 1 Conversion results are placed in consecutive result registers (wrap around at end).
1:0 FRZ[1:0]	**Background Debug Freeze Enable** — When debugging an application, it is useful in many cases to have the ATD pause when a breakpoint (Freeze Mode) is encountered. These 2 bits determine how the ATD will respond to a breakpoint as shown in Table 7-10. Leakage onto the storage node and comparator reference capacitors may compromise the accuracy of an immediately frozen conversion depending on the length of the freeze period.

Table 7-9. Conversion Sequence Length Coding

S8C	S4C	S2C	S1C	Number of Conversions per Sequence
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Table 7-10. ATD Behavior in Freeze Mode (Breakpoint)

FRZ1	FRZ0	Behavior in Freeze Mode
0	0	Continue conversion
0	1	Reserved
1	0	Finish current conversion, then freeze
1	1	Freeze Immediately

7.3.2.5 ATD Control Register 4 (ATDCTL4)

This register selects the conversion clock frequency, the length of the second phase of the sample time and the resolution of the A/D conversion (i.e., 8-bits or 10-bits). Writes to this register will abort current conversion sequence but will not start a new sequence.

	7	6	5	4	3	2	1	0
R W	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
Reset	0	0	0	0	0	1	0	1

Figure 7-7. ATD Control Register 4 (ATDCTL4)

Read: Anytime

Write: Anytime

Table 7-11. ATDCTL4 Field Descriptions

Field	Description
7 SRES8	**A/D Resolution Select** — This bit selects the resolution of A/D conversion results as either 8 or 10 bits. The A/D converter has an accuracy of 10 bits. However, if low resolution is required, the conversion can be speeded up by selecting 8-bit resolution. 0 10 bit resolution 1 8 bit resolution
6:5 SMP[1:0]	**Sample Time Select** —These two bits select the length of the second phase of the sample time in units of ATD conversion clock cycles. Note that the ATD conversion clock period is itself a function of the prescaler value (bits PRS4-0). The sample time consists of two phases. The first phase is two ATD conversion clock cycles long and transfers the sample quickly (via the buffer amplifier) onto the A/D machine's storage node. The second phase attaches the external analog signal directly to the storage node for final charging and high accuracy. Table 7-12 lists the lengths available for the second sample phase.
4:0 PRS[4:0]	**ATD Clock Prescaler** — These 5 bits are the binary value prescaler value PRS. The ATD conversion clock frequency is calculated as follows: $ATDclock = \frac{[BusClock]}{[PRS+1]} \times 0.5$ **Note:** The maximum ATD conversion clock frequency is half the bus clock. The default (after reset) prescaler value is 5 which results in a default ATD conversion clock frequency that is bus clock divided by 12. Table 7-13 illustrates the divide-by operation and the appropriate range of the bus clock.

Table 7-12. Sample Time Select

SMP1	SMP0	Length of 2nd Phase of Sample Time
0	0	2 A/D conversion clock periods
0	1	4 A/D conversion clock periods
1	0	8 A/D conversion clock periods
1	1	16 A/D conversion clock periods

Table 7-13. Clock Prescaler Values

Prescale Value	Total Divisor Value	Max. Bus Clock[1]	Min. Bus Clock[2]
00000	Divide by 2	4 MHz	1 MHz
00001	Divide by 4	8 MHz	2 MHz
00010	Divide by 6	12 MHz	3 MHz
00011	Divide by 8	16 MHz	4 MHz
00100	Divide by 10	20 MHz	5 MHz
00101	Divide by 12	24 MHz	6 MHz
00110	Divide by 14	28 MHz	7 MHz
00111	Divide by 16	32 MHz	8 MHz
01000	Divide by 18	36 MHz	9 MHz
01001	Divide by 20	40 MHz	10 MHz
01010	Divide by 22	44 MHz	11 MHz
01011	Divide by 24	48 MHz	12 MHz
01100	Divide by 26	52 MHz	13 MHz
01101	Divide by 28	56 MHz	14 MHz
01110	Divide by 30	60 MHz	15 MHz
01111	Divide by 32	64 MHz	16 MHz
10000	Divide by 34	68 MHz	17 MHz
10001	Divide by 36	72 MHz	18 MHz
10010	Divide by 38	76 MHz	19 MHz
10011	Divide by 40	80 MHz	20 MHz
10100	Divide by 42	84 MHz	21 MHz
10101	Divide by 44	88 MHz	22 MHz
10110	Divide by 46	92 MHz	23 MHz
10111	Divide by 48	96 MHz	24 MHz
11000	Divide by 50	100 MHz	25 MHz
11001	Divide by 52	104 MHz	26 MHz
11010	Divide by 54	108 MHz	27 MHz
11011	Divide by 56	112 MHz	28 MHz
11100	Divide by 58	116 MHz	29 MHz
11101	Divide by 60	120 MHz	30 MHz
11110	Divide by 62	124 MHz	31 MHz
11111	Divide by 64	128 MHz	32 MHz

1 Maximum ATD conversion clock frequency is 2 MHz. The maximum allowed bus clock frequency is shown in this column.

2 Minimum ATD conversion clock frequency is 500 kHz. The minimum allowed bus clock frequency is shown in this column.

7.3.2.6 ATD Control Register 5 (ATDCTL5)

This register selects the type of conversion sequence and the analog input channels sampled. Writes to this register will abort current conversion sequence and start a new conversion sequence. If external trigger is enabled (ETRIGE = 1) an initial write to ATDCTL5 is required to allow starting of a conversion sequence which will then occur on each trigger event. Start of conversion means the beginning of the sampling phase.

	7	6	5	4	3	2	1	0
R W	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
Reset	0	0	0	0	0	0	0	0

Figure 7-8. ATD Control Register 5 (ATDCTL5)

Read: Anytime

Write: Anytime

Table 7-14. ATDCTL5 Field Descriptions

Field	Description
7 DJM	**Result Register Data Justification** — This bit controls justification of conversion data in the result registers. See Section 7.3.2.16, “ATD Conversion Result Registers (ATDDRx)” for details. 0 Left justified data in the result registers. 1 Right justified data in the result registers.
6 DSGN	**Result Register Data Signed or Unsigned Representation** — This bit selects between signed and unsigned conversion data representation in the result registers. Signed data is represented as 2’s complement. Signed data is not available in right justification. See <st-bold>7.3.2.16 ATD Conversion Result Registers (ATDDRx) for details. 0 Unsigned data representation in the result registers. 1 Signed data representation in the result registers. Table 7-15 summarizes the result data formats available and how they are set up using the control bits. Table 7-16 illustrates the difference between the signed and unsigned, left justified output codes for an input signal range between 0 and 5.12 Volts.
5 SCAN	**Continuous Conversion Sequence Mode** — This bit selects whether conversion sequences are performed continuously or only once. If external trigger is enabled (ETRIGE=1) setting this bit has no effect, that means each trigger event starts a single conversion sequence. 0 Single conversion sequence 1 Continuous conversion sequences (scan mode)
4 MULT	**Multi-Channel Sample Mode** — When MULT is 0, the ATD sequence controller samples only from the specified analog input channel for an entire conversion sequence. The analog channel is selected by channel selection code (control bits CD/CC/CB/CA located in ATDCTL5). When MULT is 1, the ATD sequence controller samples across channels. The number of channels sampled is determined by the sequence length value (S8C, S4C, S2C, S1C). The first analog channel examined is determined by channel selection code (CC, CB, CA control bits); subsequent channels sampled in the sequence are determined by incrementing the channel selection code or wrapping around to AN0 (channel 0. 0 Sample only one channel 1 Sample across several channels

Table 7-14. ATDCTL5 Field Descriptions (continued)

Field	Description
3:0 C[D:A}	**Analog Input Channel Select Code** — These bits select the analog input channel(s) whose signals are sampled and converted to digital codes. Table 7-17 lists the coding used to select the various analog input channels. In the case of single channel conversions (MULT = 0), this selection code specified the channel to be examined. In the case of multiple channel conversions (MULT = 1), this selection code represents the first channel to be examined in the conversion sequence. Subsequent channels are determined by incrementing the channel selection code or wrapping around to AN0 (after converting the channel defined by the Wrap Around Channel Select Bits WRAP[3:0] in ATDCTL0). In case starting with a channel number higher than the one defined by WRAP[3:0] the first wrap around will be AN15 to AN0.

Table 7-15. Available Result Data Formats.

SRES8	DJM	DSGN	Result Data Formats Description and Bus Bit Mapping
1	0	0	8-bit / left justified / unsigned — bits 15:8
1	0	1	8-bit / left justified / signed — bits 15:8
1	1	X	8-bit / right justified / unsigned — bits 7:0
0	0	0	10-bit / left justified / unsigned — bits 15:6
0	0	1	10-bit / left justified / signed -— bits 15:6
0	1	X	10-bit / right justified / unsigned — bits 9:0

Table 7-16. Left Justified, Signed and Unsigned ATD Output Codes.

Input Signal V_{RL} = 0 Volts V_{RH} = 5.12 Volts	Signed 8-Bit Codes	Unsigned 8-Bit Codes	Signed 10-Bit Codes	Unsigned 10-Bit Codes
5.120 Volts	7F	FF	7FC0	FFC0
5.100	7F	FF	7F00	FF00
5.080	7E	FE	7E00	FE00
2.580	01	81	0100	8100
2.560	00	80	0000	8000
2.540	FF	7F	FF00	7F00
0.020	81	01	8100	0100
0.000	80	00	8000	0000

Table 7-17. Analog Input Channel Select Coding

CD	CC	CB	CA	Analog Input Channel
0	0	0	0	AN0
0	0	0	1	AN1
0	0	1	0	AN2
0	0	1	1	AN3
0	1	0	0	AN4
0	1	0	1	AN5
0	1	1	0	AN6
0	1	1	1	AN7
1	0	0	0	AN8
1	0	0	1	AN9
1	0	1	0	AN10
1	0	1	1	AN11
1	1	0	0	AN12
1	1	0	1	AN13
1	1	1	0	AN14
1	1	1	1	AN15

7.3.2.7 ATD Status Register 0 (ATDSTAT0)

This read-only register contains the Sequence Complete Flag, overrun flags for external trigger and FIFO mode, and the conversion counter.

	7	6	5	4	3	2	1	0
R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-9. ATD Status Register 0 (ATDSTAT0)

Read: Anytime

Write: Anytime (No effect on CC[3:0])

Table 7-18. ATDSTAT0 Field Descriptions

Field	Description
7 SCF	**Sequence Complete Flag** — This flag is set upon completion of a conversion sequence. If conversion sequences are continuously performed (SCAN = 1), the flag is set after each one is completed. This flag is cleared when one of the following occurs: • Write “1” to SCF • Write to ATDCTL5 (a new conversion sequence is started) • If AFFC = 1 and read of a result register 0 Conversion sequence not completed 1 Conversion sequence has completed
5 ETORF	**External Trigger Overrun Flag** —While in edge trigger mode (ETRIGLE = 0), if additional active edges are detected while a conversion sequence is in process the overrun flag is set. This flag is cleared when one of the following occurs: • Write “1” to ETORF • Write to ATDCTL0,1,2,3,4 (a conversion sequence is aborted) • Write to ATDCTL5 (a new conversion sequence is started) 0 No External trigger over run error has occurred 1 External trigger over run error has occurred

Table 7-18. ATDSTAT0 Field Descriptions (continued)

Field	Description
4 FIFOR	**FIFO Over Run Flag** — This bit indicates that a result register has been written to before its associated conversion complete flag (CCF) has been cleared. This flag is most useful when using the FIFO mode because the flag potentially indicates that result registers are out of sync with the input channels. However, it is also practical for non-FIFO modes, and indicates that a result register has been over written before it has been read (i.e., the old data has been lost). This flag is cleared when one of the following occurs: • Write “1” to FIFOR • Start a new conversion sequence (write to ATDCTL5 or external trigger) 0 No over run has occurred 1 Overrun condition exists (result register has been written while associated CCFx flag remained set)
3:0 CC[3:0}	**Conversion Counter** — These 4 read-only bits are the binary value of the conversion counter. The conversion counter points to the result register that will receive the result of the current conversion. For example, CC3 = 0, CC2 = 1, CC1 = 1, CC0 = 0 indicates that the result of the current conversion will be in ATD Result Register 6. If in non-FIFO mode (FIFO = 0) the conversion counter is initialized to zero at the begin and end of the conversion sequence. If in FIFO mode (FIFO = 1) the register counter is not initialized. The conversion counters wraps around when its maximum value is reached. Aborting a conversion or starting a new conversion by write to an ATDCTL register (ATDCTL5-0) clears the conversion counter even if FIFO=1.

7.3.2.8 Reserved Register 0 (ATDTEST0)

	7	6	5	4	3	2	1	0
R	u	u	u	u	u	u	u	u
W								
Reset	1	0	0	0	0	0	0	0

= Unimplemented or Reserved u = Unaffected

Figure 7-10. Reserved Register 0 (ATDTEST0)

Read: Anytime, returns unpredictable values

Write: Anytime in special modes, unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter functionality.

7.3.2.9 ATD Test Register 1 (ATDTEST1)

This register contains the SC bit used to enable special channel conversions.

	7	6	5	4	3	2	1	0
R	u	u	u	u	u	u	u	SC
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved u = Unaffected

Figure 7-11. Reserved Register 1 (ATDTEST1)

Read: Anytime, returns unpredictable values for bit 7 and bit 6

Write: Anytime

NOTE

Writing to this register when in special modes can alter functionality.

Table 7-19. ATDTEST1 Field Descriptions

Field	Description
0 SC	**Special Channel Conversion Bit** — If this bit is set, then special channel conversion can be selected using CC, CB, and CA of ATDCTL5. Table 7-20 lists the coding. 0 Special channel conversions disabled 1 Special channel conversions enabled

Table 7-20. Special Channel Select Coding

SC	CD	CC	CB	CA	Analog Input Channel
1	0	0	X	X	Reserved
1	0	1	0	0	V_{RH}
1	0	1	0	1	V_{RL}
1	0	1	1	0	$(V_{RH}+V_{RL}) / 2$
1	0	1	1	1	Reserved
1	1	X	X	X	Reserved

7.3.2.10 ATD Status Register 2 (ATDSTAT2)

This read-only register contains the Conversion Complete Flags CCF15 to CCF8.

	7	6	5	4	3	2	1	0
R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-12. ATD Status Register 2 (ATDSTAT2)

Read: Anytime

Write: Anytime, no effect

Table 7-21. ATDSTAT2 Field Descriptions

Field	Description
7:0 CCF[15:8]	**Conversion Complete Flag Bits** — A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF8 is set when the ninth conversion in a sequence is complete and the result is available in result register ATDDR8; CCF9 is set when the tenth conversion in a sequence is complete and the result is available in ATDDR9, and so forth. A flag CCFx (x = 15, 14, 13, 12, 11, 10, 9, 8) is cleared when one of the following occurs: • Write to ATDCTL5 (a new conversion sequence is started) • If AFFC = 0 and read of ATDSTAT2 followed by read of result register ATDDRx • If AFFC = 1 and read of result register ATDDRx In case of a concurrent set and clear on CCFx: The clearing by method A) will overwrite the set. The clearing by methods B) or C) will be overwritten by the set. 0 Conversion number x not completed 1 Conversion number x has completed, result ready in ATDDRx

7.3.2.11 ATD Status Register 1 (ATDSTAT1)

This read-only register contains the Conversion Complete Flags CCF7 to CCF0

	7	6	5	4	3	2	1	0
R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-13. ATD Status Register 1 (ATDSTAT1)

Read: Anytime

Write: Anytime, no effect

Table 7-22. ATDSTAT1 Field Descriptions

Field	Description
7:0 CCF[7:0]	**Conversion Complete Flag Bits** — A conversion complete flag is set at the end of each conversion in a conversion sequence. The flags are associated with the conversion position in a sequence (and also the result register number). Therefore, CCF0 is set when the first conversion in a sequence is complete and the result is available in result register ATDDR0; CCF1 is set when the second conversion in a sequence is complete and the result is available in ATDDR1, and so forth. A CCF flag is cleared when one of the following occurs: • Write to ATDCTL5 (a new conversion sequence is started) • If AFFC = 0 and read of ATDSTAT1 followed by read of result register ATDDRx • If AFFC = 1 and read of result register ATDDRx In case of a concurrent set and clear on CCFx: The clearing by method A) will overwrite the set. The clearing by methods B) or C) will be overwritten by the set. Conversion number x not completed Conversion number x has completed, result ready in ATDDRx

7.3.2.12 ATD Input Enable Register 0 (ATDDIEN0)

	7	6	5	4	3	2	1	0
R W	IEN15	IEN14	IEN13	IEN12	IEN11	IEN10	IEN9	IEN8
Reset	0	0	0	0	0	0	0	0

Figure 7-14. ATD Input Enable Register 0 (ATDDIEN0)

Read: Anytime

Write: anytime

Table 7-23. ATDDIEN0 Field Descriptions

Field	Description
7:0 IEN[15:8]	**ATD Digital Input Enable on Channel Bits** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

7.3.2.13 ATD Input Enable Register 1 (ATDDIEN1)

	7	6	5	4	3	2	1	0
R W	IEN7	IEN6	IEN5	IEN4	IEN3	IEN2	IEN1	IEN0
Reset	0	0	0	0	0	0	0	0

Figure 7-15. ATD Input Enable Register 1 (ATDDIEN1)

Read: Anytime

Write: Anytime

Table 7-24. ATDDIEN1 Field Descriptions

Field	Description
7:0 IEN[7:0]	**ATD Digital Input Enable on Channel Bits** — This bit controls the digital input buffer from the analog input pin (ANx) to PTADx data register. 0 Disable digital input buffer to PTADx 1 Enable digital input buffer to PTADx. **Note:** Setting this bit will enable the corresponding digital input buffer continuously. If this bit is set while simultaneously using it as an analog port, there is potentially increased power consumption because the digital input buffer maybe in the linear region.

7.3.2.14 Port Data Register 0 (PORTAD0)

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN[15:8].

	7	6	5	4	3	2	1	0
R	PTAD15	PTAD14	PTAD13	PTAD12	PTAD11	PTAD10	PTAD9	PTAD8
W								
Reset	1	1	1	1	1	1	1	1
Pin Function	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8

= Unimplemented or Reserved

Figure 7-16. Port Data Register 0 (PORTAD0)

Read: Anytime

Write: Anytime, no effect

The A/D input channels may be used for general-purpose digital input.

Table 7-25. PORTAD0 Field Descriptions

Field	Description
7:0 PTAD[15:8]	**A/D Channel x (ANx) Digital Input Bits**— If the digital input buffer on the ANx pin is enabled (IENx = 1) or channel x is enabled as external trigger (ETRIGE = 1, ETRIGCH[3-0] = x, ETRIGSEL = 0) read returns the logic level on ANx pin (signal potentials not meeting V_{IL} or V_{IH} specifications will have an indeterminate value)). If the digital input buffers are disabled (IENx = 0) and channel x is not enabled as external trigger, read returns a “1”. Reset sets all PORTAD0 bits to “1”.

7.3.2.15 Port Data Register 1 (PORTAD1)

The data port associated with the ATD is input-only. The port pins are shared with the analog A/D inputs AN7-0.

	7	6	5	4	3	2	1	0
R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
W								
Reset	1	1	1	1	1	1	1	1
Pin Function	AN 7	AN6	AN5	AN4	AN3	AN2	AN1	AN0

= Unimplemented or Reserved

Figure 7-17. Port Data Register 1 (PORTAD1)

Read: Anytime

Write: Anytime, no effect

The A/D input channels may be used for general-purpose digital input.

Table 7-26. PORTAD1 Field Descriptions

Field	Description
7:0 PTAD[7:8]	**A/D Channel x (ANx) Digital Input Bits** — If the digital input buffer on the ANx pin is enabled (IENx=1) or channel x is enabled as external trigger (ETRIGE = 1, ETRIGCH[3-0] = x, ETRIGSEL = 0) read returns the logic level on ANx pin (signal potentials not meeting V_{IL} or V_{IH} specifications will have an indeterminate value)). If the digital input buffers are disabled (IENx = 0) and channel x is not enabled as external trigger, read returns a “1”. Reset sets all PORTAD1 bits to “1”.

7.3.2.16 ATD Conversion Result Registers (ATDDRx)

The A/D conversion results are stored in 16 read-only result registers. The result data is formatted in the result registers bases on two criteria. First there is left and right justification; this selection is made using the DJM control bit in ATDCTL5. Second there is signed and unsigned data; this selection is made using the DSGN control bit in ATDCTL5. Signed data is stored in 2's complement format and only exists in left justified format. Signed data selected for right justified format is ignored.

Read: Anytime

Write: Anytime in special mode, unimplemented in normal modes

7.3.2.16.1 Left Justified Result Data

	7	6	5	4	3	2	1	0
R (10-BIT) R (8-BIT)	BIT 9 MSB BIT 7 MSB	BIT 8 BIT 6	BIT 7 BIT 5	BIT 6 BIT 4	BIT 5 BIT 3	BIT 4 BIT 2	BIT 3 BIT 1	BIT 2 BIT 0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-18. Left Justified, ATD Conversion Result Register x, High Byte (ATDDRxH)

	7	6	5	4	3	2	1	0
R (10-BIT) R (8-BIT)	BIT 1 u	BIT 0 u	0 0	0 0	0 0	0 0	0 0	0 0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved u = Unaffected

Figure 7-19. Left Justified, ATD Conversion Result Register x, Low Byte (ATDDRxL)

7.3.2.16.2 Right Justified Result Data

	7	6	5	4	3	2	1	0
R (10-BIT)	0	0	0	0	0	0	BIT 9 MSB	BIT 8
R (8-BIT)	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-20. Right Justified, ATD Conversion Result Register x, High Byte (ATDDRxH)

	7	6	5	4	3	2	1	0
R (10-BIT)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
R (8-BIT)	BIT 7 MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 7-21. Right Justified, ATD Conversion Result Register x, Low Byte (ATDDRxL)

7.4 Functional Description

The ATD10B16C is structured in an analog and a digital sub-block.

7.4.1 Analog Sub-block

The analog sub-block contains all analog electronics required to perform a single conversion. Separate power supplies V_{DDA} and V_{SSA} allow to isolate noise of other MCU circuitry from the analog sub-block.

7.4.1.1 Sample and Hold Machine

The sample and hold (S/H) machine accepts analog signals from the external world and stores them as capacitor charge on a storage node.

The sample process uses a two stage approach. During the first stage, the sample amplifier is used to quickly charge the storage node.The second stage connects the input directly to the storage node to complete the sample for high accuracy.

When not sampling, the sample and hold machine disables its own clocks. The analog electronics continue drawing their quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

The input analog signals are unipolar and must fall within the potential range of V_{SSA} to VDDA.

7.4.1.2 Analog Input Multiplexer

The analog input multiplexer connects one of the 16 external analog input channels to the sample and hold machine.

7.4.1.3 Sample Buffer Amplifier

The sample amplifier is used to buffer the input analog signal so that the storage node can be quickly charged to the sample potential.

7.4.1.4 Analog-to-Digital (A/D) Machine

The A/D machine performs analog to digital conversions. The resolution is program selectable at either 8 or 10 bits. The A/D machine uses a successive approximation architecture. It functions by comparing the stored analog sample potential with a series of digitally generated analog potentials. By following a binary search algorithm, the A/D machine locates the approximating potential that is nearest to the sampled potential.

When not converting the A/D machine disables its own clocks. The analog electronics continue drawing quiescent current. The power down (ADPU) bit must be set to disable both the digital clocks and the analog power consumption.

Only analog input signals within the potential range of V_{RL} to V_{RH} (A/D reference potentials) will result in a non-railed digital output codes.

7.4.2 Digital Sub-Block

This subsection explains some of the digital features in more detail. See register descriptions for all details.

7.4.2.1 External Trigger Input

The external trigger feature allows the user to synchronize ATD conversions to the external environment events rather than relying on software to signal the ATD module when ATD conversions are to take place. The external trigger signal (out of reset ATD channel 15, configurable in ATDCTL1) is programmable to be edge or level sensitive with polarity control. Table 7-27 gives a brief description of the different combinations of control bits and their effect on the external trigger function.

Table 7-27. External Trigger Control Bits

ETRIGLE	ETRIGP	ETRIGE	SCAN	Description
X	X	0	0	Ignores external trigger. Performs one conversion sequence and stops.
X	X	0	1	Ignores external trigger. Performs continuous conversion sequences.
0	0	1	X	Falling edge triggered. Performs one conversion sequence per trigger.
0	1	1	X	Rising edge triggered. Performs one conversion sequence per trigger.
1	0	1	X	Trigger active low. Performs continuous conversions while trigger is active.
1	1	1	X	Trigger active high. Performs continuous conversions while trigger is active.

During a conversion, if additional active edges are detected the overrun error flag ETORF is set.

In either level or edge triggered modes, the first conversion begins when the trigger is received. In both cases, the maximum latency time is one bus clock cycle plus any skew or delay introduced by the trigger circuitry.

After ETRIGE is enabled, conversions cannot be started by a write to ATDCTL5, but rather must be triggered externally.

If the level mode is active and the external trigger both de-asserts and re-asserts itself during a conversion sequence, this does not constitute an overrun. Therefore, the flag is not set. If the trigger remains asserted in level mode while a sequence is completing, another sequence will be triggered immediately.

7.4.2.2 General-Purpose Digital Input Port Operation

The input channel pins can be multiplexed between analog and digital data. As analog inputs, they are multiplexed and sampled to supply signals to the A/D converter. As digital inputs, they supply external input data that can be accessed through the digital port registers (PORTAD0 & PORTAD1) (input-only).

The analog/digital multiplex operation is performed in the input pads. The input pad is always connected to the analog inputs of the ATD10B16C. The input pad signal is buffered to the digital port registers. This buffer can be turned on or off with the ATDDIEN0 & ATDDIEN1 register. This is important so that the buffer does not draw excess current when analog potentials are presented at its input.

7.4.3 Operation in Low Power Modes

The ATD10B16C can be configured for lower MCU power consumption in three different ways:

- **Stop Mode**
  Stop Mode: This halts A/D conversion. Exit from Stop mode will resume A/D conversion, But due to the recovery time the result of this conversion should be ignored.

  Entering stop mode causes all clocks to halt and thus the system is placed in a minimum power standby mode. This halts any conversion sequence in progress. During recovery from stop mode, there must be a minimum delay for the stop recovery time t_{SR} before initiating a new ATD conversion sequence.
- **Wait Mode**
  Wait Mode with AWAI = 1: This halts A/D conversion. Exit from Wait mode will resume A/D conversion, but due to the recovery time the result of this conversion should be ignored.

  Entering wait mode, the ATD conversion either continues or halts for low power depending on the logical value of the AWAIT bit.
- **Freeze Mode**
  Writing ADPU = 0 (Note that all ATD registers remain accessible.): This aborts any A/D conversion in progress.

  In freeze mode, the ATD10B16C will behave according to the logical values of the FRZ1 and FRZ0 bits. This is useful for debugging and emulation.

NOTE

The reset value for the ADPU bit is zero. Therefore, when this module is reset, it is reset into the power down state.

7.5 Resets

At reset the ATD10B16C is in a power down state. The reset state of each individual bit is listed within Section 7.3, “Memory Map and Register Definition,” which details the registers and their bit fields.

7.6 Interrupts

The interrupt requested by the ATD10B16C is listed in Table 7-28. Refer to MCU specification for related vector address and priority.

Table 7-28. ATD Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Sequence Complete Interrupt	I bit	ASCIE in ATDCTL2

See Section 7.3.2, “Register Descriptions,” for further details.

Chapter 8
Liquid Crystal Display (LCD32F4BV1)

8.1 Introduction

The LCD32F4B driver module has 32 frontplane drivers and 4 backplane drivers so that a maximum of 128 LCD segments are controllable. Each segment is controlled by a corresponding bit in the LCD RAM. Four multiplex modes (1/1, 1/2, 1/3, 1/4 duty), and three bias (1/1, 1/2, 1/3) methods are available. The V_0 voltage is the lowest level of the output waveform and V_3 becomes the highest level. All frontplane and backplane pins can be multiplexed with other port functions.

The LCD32F4B driver system consists of five major sub-modules:

- Timing and Control – consists of registers and control logic for frame clock generation, bias voltage level select, frame duty select, backplane select, and frontplane select/enable to produce the required frame frequency and voltage waveforms.
- LCD RAM – contains the data to be displayed on the LCD. Data can be read from or written to the display RAM at any time.
- Frontplane Drivers – consists of 32 frontplane drivers.
- Backplane Drivers – consists of 4 backplane drivers.
- Voltage Generator – Based on voltage applied to VLCD, it generates the voltage levels for the timing and control logic to produce the frontplane and backplane waveforms.

8.1.1 Features

The LCD32F4B includes these distinctive features:

- Supports five LCD operation modes
- 32 frontplane drivers
- 4 backplane drivers
  - — Each frontplane has an enable bit respectively
- Programmable frame clock generator
- Programmable bias voltage level selector
- On-chip generation of 4 different output voltage levels

8.1.2 Modes of Operation

The LCD32F4B module supports five operation modes with different numbers of backplanes and different biasing levels. During pseudo stop mode and wait mode the LCD operation can be suspended under

software control. Depending on the state of internal bits, the LCD can operate normally or the LCD clock generation can be turned off and the LCD32F4B module enters a power conservation state.

This is a high level description only, detailed descriptions of operating modes are contained in Section 8.4.2, “Operation in Wait Mode”, Section 8.4.3, “Operation in Pseudo Stop Mode”, and Section 8.4.4, “Operation in Stop Mode”.

8.1.3 Block Diagram

Figure 8-1 is a block diagram of the LCD32F4B module.

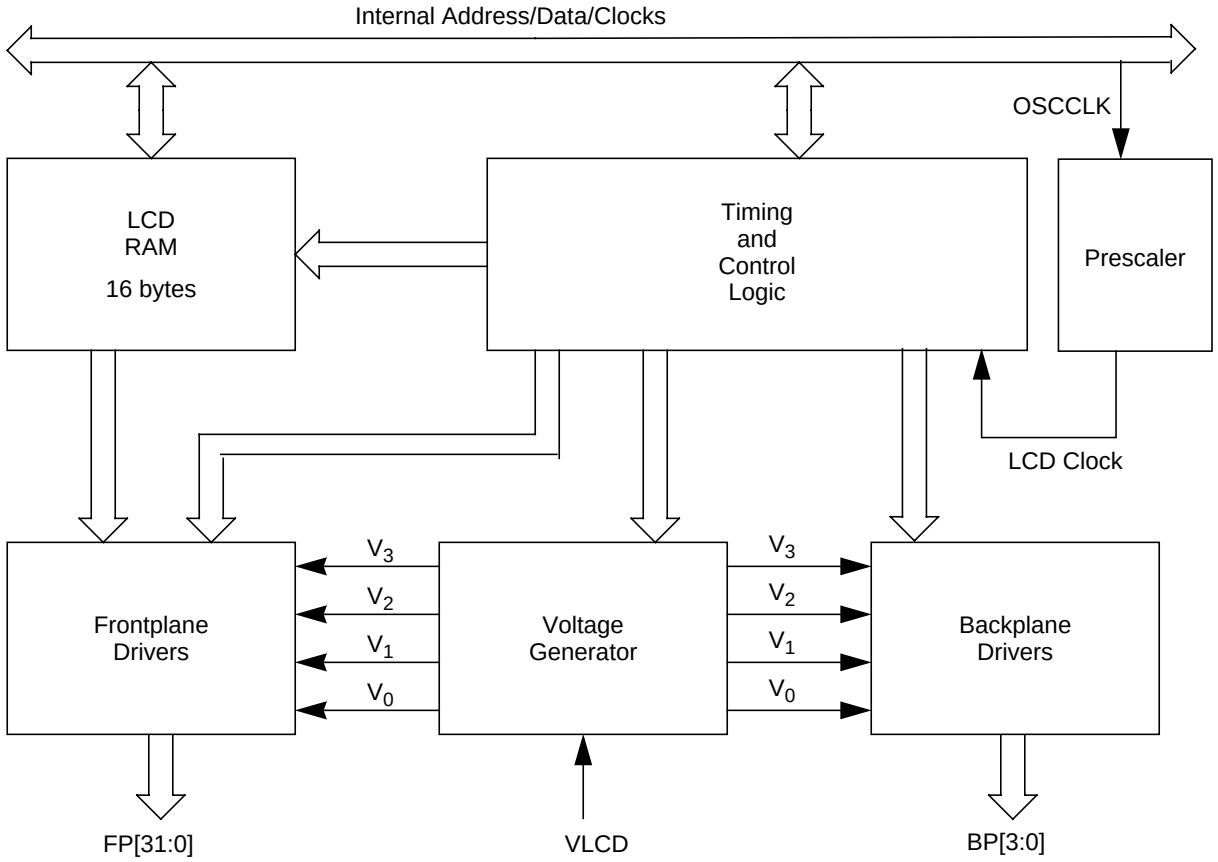


Figure 8-1. LCD32F4B Block Diagram

8.2 External Signal Description

The LCD32F4B module has a total of 37 external pins.

Table 8-1. Signal Properties

Name	Port	Function	Reset State
4 backplane waveforms	BP[3:0]	Backplane waveform signals that connect directly to the pads	High impedance
32 frontplane waveforms	FP[31:0]	Frontplane waveform signals that connect directly to the pads	High impedance
LCD voltage	VLCD	LCD supply voltage	—

8.2.1 BP[3:0] — Analog Backplane Pins

This output signal vector represents the analog backplane waveforms of the LCD32F4B module and is connected directly to the corresponding pads.

8.2.2 FP[31:0] — Analog Frontplane Pins

This output signal vector represents the analog frontplane waveforms of the LCD32F4B module and is connected directly to the corresponding pads.

8.2.3 VLCD — LCD Supply Voltage Pin

Positive supply voltage for the LCD waveform generation.

8.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

8.3.1 Module Memory Map

The memory map for the LCD32F4B module is given in Table 8-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the LCD32F4B module and the address offset for each register.

Table 8-2. LCD32F4B Memory Map

Address Offset	Use	Access
0x0000	LCD Control Register 0 (LCDCR0)	Read/Write
0x0001	LCD Control Register 1 (LCDCR1)	Read/Write
0x0002	LCD Frontplane Enable Register 0 (FPENR0)	Read/Write
0x0003	LCD Frontplane Enable Register 1 (FPENR1)	Read/Write
0x0004	LCD Frontplane Enable Register 2 (FPENR2)	Read/Write
0x0005	LCD Frontplane Enable Register 3 (FPENR3)	Read/Write
0x0006	Unimplemented	
0x0007	Unimplemented	
0x0008	LCDRAM (Location 0)	Read/Write
0x0009	LCDRAM (Location 1)	Read/Write
0x000A	LCDRAM (Location 2)	Read/Write
0x000B	LCDRAM (Location 3)	Read/Write
0x000C	LCDRAM (Location 4)	Read/Write
0x000D	LCDRAM (Location 5)	Read/Write
0x000E	LCDRAM (Location 6)	Read/Write
0x000F	LCDRAM (Location 7)	Read/Write
0x0010	LCDRAM (Location 8)	Read/Write
0x0011	LCDRAM (Location 9)	Read/Write
0x0012	LCDRAM (Location 10)	Read/Write
0x0013	LCDRAM (Location 11)	Read/Write
0x0014	LCDRAM (Location 12)	Read/Write
0x0015	LCDRAM (Location 13)	Read/Write
0x0016	LCDRAM (Location 14)	Read/Write
0x0017	LCDRAM (Location 15)	Read/Write

8.3.2 Register Descriptions

This section consists of register descriptions. Each description includes a standard register diagram. Details of register bit and field function follow the register diagrams, in bit order.

8.3.2.1 LCD Control Register 0 (LCDCR0)

	7	6	5	4	3	2	1	0
R	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 8-2. LCD Control Register 0 (LCDCR0)

Read: anytime

Write: LCDEN anytime. To avoid segment flicker the clock prescaler bits, the bias select bit and the duty select bits must not be changed when the LCD is enabled.

Table 8-3. LCDCR0 Field Descriptions

Field	Description
7 LCDEN	**LCD32F4B Driver System Enable** — The LCDEN bit starts the LCD waveform generator. 0 All frontplane and backplane pins are disabled. In addition, the LCD32F4B system is disabled and all LCD waveform generation clocks are stopped. 1 LCD driver system is enabled. All FP[31:0] pins with FP[31:0]EN set, will output an LCD driver waveform The BP[3:0] pins will output an LCD32F4B driver waveform based on the settings of DUTY0 and DUTY1.
5:3 LCLK[2:0]	**LCD Clock Prescaler** — The LCD clock prescaler bits determine the OSCCLK divider value to produce the LCD clock frequency. For detailed description of the correlation between LCD clock prescaler bits and the divider value please refer to Table 8-7.
2 BIAS	**BIAS Voltage Level Select** — This bit selects the bias voltage levels during various LCD operating modes, as shown in Table 8-8.
1:0 DUTY[1:0]	**LCD Duty Select** — The DUTY1 and DUTY0 bits select the duty (multiplex mode) of the LCD32F4B driver system, as shown in Table 8-8.

8.3.2.2 LCD Control Register 1 (LCDCR1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	LCDSWAI	LCDRPSTP
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 8-3. LCD Control Register 1 (LCDCR1)

Read: anytime

Write: anytime

Table 8-4. LCDCR1 Field Descriptions

Field	Description
1 LCDSWAI	**LCD Stop in Wait Mode** — This bit controls the LCD operation while in wait mode. 0 LCD operates normally in wait mode. 1 Stop LCD32F4B driver system when in wait mode.
0 LCDRPSTP	**LCD Run in Pseudo Stop Mode** — This bit controls the LCD operation while in pseudo stop mode. 0 Stop LCD32F4B driver system when in pseudo stop mode. 1 LCD operates normally in pseudo stop mode.

8.3.2.3 LCD Frontplane Enable Register 0–3 (FPENR0–FPENR3)

	7	6	5	4	3	2	1	0
R W	FP7EN	FP6EN	FP5EN	FP4EN	FP3EN	FP2EN	FP1EN	FP0EN
Reset	0	0	0	0	0	0	0	0

Figure 8-4. LCD Frontplane Enable Register 0 (FPENR0)

	7	6	5	4	3	2	1	0
R W	FP15EN	FP14EN	FP13EN	FP12EN	FP11EN	FP10EN	FP9EN	FP8EN
Reset	0	0	0	0	0	0	0	0

Figure 8-5. LCD Frontplane Enable Register 1 (FPENR1)

	7	6	5	4	3	2	1	0
R W	FP23EN	FP22EN	FP21EN	FP20EN	FP19EN	FP18EN	FP17EN	FP16EN
Reset	0	0	0	0	0	0	0	0

Figure 8-6. LCD Frontplane Enable Register 2 (FPENR2)

	7	6	5	4	3	2	1	0
R W	FP31EN	FP30EN	FP29EN	FP28EN	FP27EN	FP26EN	FP25EN	FP24EN
Reset	0	0	0	0	0	0	0	0

Figure 8-7. LCD Frontplane Enable Register 3 (FPENR3)

These bits enable the frontplane output waveform on the corresponding frontplane pin when LCDEN = 1.

Read: anytime

Write: anytime

Table 8-5. FPENR0–FPENR3 Field Descriptions

Field	Description
31:0 FP[31:0]EN	**Frontplane Output Enable** — The FP[31:0]EN bit enables the frontplane driver outputs. If LCDEN = 0, these bits have no effect on the state of the I/O pins. It is recommended to set FP[31:0]EN bits before LCDEN is set. 0 Frontplane driver output disabled on FP[31:0]. 1 Frontplane driver output enabled on FP[31:0].

8.3.2.4 LCD RAM (LCDRAM)

The LCD RAM consists of 16 bytes. After reset the LCD RAM contents will be indeterminate (I), as indicated by Figure 8-8.

		7	6	5	4	3	2	1	0
LCDRAM	R W	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
	Reset	I	I	I	I	I	I	I	I

I = Value is indeterminate

Figure 8-8. LCD RAM (LCDRAM)

LCDRAM	R W	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP19BP3	FP19BP2	FP19BP1	FP19BP0	FP18BP3	FP18BP2	FP18BP1	FP18BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP21BP3	FP21BP2	FP21BP1	FP21BP0	FP20BP3	FP20BP2	FP20BP1	FP20BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP23BP3	FP23BP2	FP23BP1	FP23BP0	FP22BP3	FP22BP2	FP22BP1	FP22BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP25BP3	FP25BP2	FP25BP1	FP25BP0	FP24BP3	FP24BP2	FP24BP1	FP24BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP27BP3	FP27BP2	FP27BP1	FP27BP0	FP26BP3	FP26BP2	FP26BP1	FP26BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP29BP3	FP29BP2	FP29BP1	FP29BP0	FP28BP3	FP28BP2	FP28BP1	FP28BP0
	Reset	I	I	I	I	I	I	I	I
LCDRAM	R W	FP31BP3	FP31BP2	FP31BP1	FP31BP0	FP30BP3	FP30BP2	FP30BP1	FP30BP0
	Reset	I	I	I	I	I	I	I	I

I = Value is indeterminate

Figure 8-8. LCD RAM (LCDRAM) (continued)

Read: anytime

Write: anytime

Table 8-6. LCD RAM Field Descriptions

Field	Description
31:0 3:0 FP[31:0] BP[3:0]	**LCD Segment ON** — The FP[31:0]BP[3:0] bit displays (turns on) the LCD segment connected between FP[31:0] and BP[3:0]. 0 LCD segment OFF 1 LCD segment ON

8.4 Functional Description

This section provides a complete functional description of the LCD32F4B block, detailing the operation of the design from the end user perspective in a number of subsections.

8.4.1 LCD Driver Description

8.4.1.1 Frontplane, Backplane, and LCD System During Reset

During a reset the following conditions exist:

- The LCD32F4B system is configured in the default mode, 1/4 duty and 1/3 bias, that means all backplanes are used.
- All frontplane enable bits, FP[31:0]EN are cleared and the ON/OFF control for the display, the LCDEN bit is cleared, thereby forcing all frontplane and backplane driver outputs to the high impedance state. The MCU pin state during reset is defined by the port integration module (PIM).

8.4.1.2 LCD Clock and Frame Frequency

The frequency of the oscillator clock (OSCCLK) and divider determine the LCD clock frequency. The divider is set by the LCD clock prescaler bits, LCLK[2:0], in the LCD control register 0 (LCDCR0). Table 8-7 shows the LCD clock and frame frequency for some multiplexed mode at OSCCLK = 16 MHz, 8 MHz, 4 MHz, 2 MHz, 1 MHz, and 0.5 MHz.

Table 8-7. LCD Clock and Frame Frequency

Oscillator Frequency in MHz	LCD Clock Prescaler			Divider	LCD Clock Frequency [Hz]	Frame Frequency [Hz]			
	LCLK2	LCLK1	LCLK0			1/1 Duty	1/2 Duty	1/3 Duty	1/4 Duty
OSCCLK = 0.5	0 0	0 0	0 1	1024 2048	488 244	488 244	244 122	163 81	122 61
OSCCLK = 1.0	0 0	0 1	1 0	2048 4096	488 244	488 244	244 122	163 81	122 61
OSCCLK = 2.0	0 0	1 1	0 1	4096 8192	488 244	488 244	244 122	163 81	122 61
OSCCLK = 4.0	0 1	1 0	1 0	8192 16384	488 244	488 244	244 122	163 81	122 61
OSCCLK = 8.0	1 1	0 0	0 1	16384 32768	488 244	488 244	244 122	163 81	122 61
OSCCLK = 16.0	1 1	1 1	0 1	65536 131072	244 122	244 122	122 61	81 40	61 31

For other combinations of OSCCLK and divider not shown in Table 8-7, the following formula may be used to calculate the LCD frame frequency for each multiplex mode:

$$\text{LCD Frame Frequency (Hz)} = \left[\frac{\text{OSCCLK (Hz)}}{\text{Divider}}\right] \cdot \text{Duty}$$

The possible divider values are shown in Table 8-7.

8.4.1.3 LCD RAM

For a segment on the LCD to be displayed, data must be written to the LCD RAM which is shown in Section 8.3, “Memory Map and Register Definition”. The 128 bits in the LCD RAM correspond to the 128 segments that are driven by the frontplane and backplane drivers. Writing a 1 to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment ON when the LCDEN bit is set and the corresponding FP[31:0]EN bit is set. Writing a 0 to a given location will result in the corresponding display segment being driven with a differential RMS voltage necessary to turn the segment OFF. The LCD RAM is a dual port RAM that interfaces with the internal address and data buses of the MCU. It is possible to read from LCD RAM locations for scrolling purposes. When LCDEN = 0, the LCD RAM can be used as on-chip RAM. Writing or reading of the LCDEN bit does not change the contents of the LCD RAM. After a reset, the LCD RAM contents will be indeterminate.

8.4.1.4 LCD Driver System Enable and Frontplane Enable Sequencing

If LCDEN = 0 (LCD32F4B driver system disabled) and the frontplane enable bit, FP[31:0]EN, is set, the frontplane driver waveform will not appear on the output until LCDEN is set. If LCDEN = 1 (LCD32F4B driver system enabled), the frontplane driver waveform will appear on the output as soon as the corresponding frontplane enable bit, FP[31:0]EN, in the registers FPENR0–FPENR3 is set.

8.4.1.5 LCD Bias and Modes of Operation

The LCD32F4B driver has five modes of operation:

- 1/1 duty (1 backplane), 1/1 bias (2 voltage levels)
- 1/2 duty (2 backplanes), 1/2 bias (3 voltage levels)
- 1/2 duty (2 backplanes), 1/3 bias (4 voltage levels)
- 1/3 duty (3 backplanes), 1/3 bias (4 voltage levels)
- 1/4 duty (4 backplanes), 1/3 bias (4 voltage levels)

The voltage levels required for the different operating modes are generated internally based on VLCD. Changing VLCD alters the differential RMS voltage across the segments in the ON and OFF states, thereby setting the display contrast.

The backplane waveforms are continuous and repetitive every frame. They are fixed within each operating mode and are not affected by the data in the LCD RAM.

The frontplane waveforms generated are dependent on the state (ON or OFF) of the LCD segments as defined in the LCD RAM. The LCD32F4B driver hardware uses the data in the LCD RAM to construct the frontplane waveform to create a differential RMS voltage necessary to turn the segment ON or OFF.

The LCD duty is decided by the DUTY1 and DUTY0 bits in the LCD control register 0 (LCDCR0). The number of bias voltage levels is determined by the BIAS bit in LCDCR0. Table 8-8 summarizes the multiplex modes (duties) and the bias voltage levels that can be selected for each multiplex mode (duty). The backplane pins have their corresponding backplane waveform output BP[3:0] in high impedance state when in the OFF state as indicated in Table 8-8. In the OFF state the corresponding pins BP[3:0]can be used for other functionality, for example as general purpose I/O ports.

Table 8-8. LCD Duty and Bias

Duty	LCDCR0 Register		Backplanes				Bias (BIAS = 0)			Bias (BIAS = 1)		
	DUTY1	DUTY0	BP3	BP2	BP1	BP0	1/1	1/2	1/3	1/1	1/2	1/3
1/1	0	1	OFF	OFF	OFF	BP0	YES	NA	NA	YES	NA	NA
1/2	1	0	OFF	OFF	BP1	BP0	NA	YES	NA	NA	NA	YES
1/3	1	1	OFF	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES
1/4	0	0	BP3	BP2	BP1	BP0	NA	NA	YES	NA	NA	YES

8.4.2 Operation in Wait Mode

The LCD32F4B driver system operation during wait mode is controlled by the LCD stop in wait (LCDSWAI) bit in the LCD control register 1 (LCDCR1). If LCDSWAI is reset, the LCD32F4B driver system continues to operate during wait mode. If LCDSWAI is set, the LCD32F4B driver system is turned off during wait mode. In this case, the LCD waveform generation clocks are stopped and the LCD32F4B drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering wait mode. The contents of the LCD RAM and the LCD registers retain the values they had prior to entering wait mode.

8.4.3 Operation in Pseudo Stop Mode

The LCD32F4B driver system operation during pseudo stop mode is controlled by the LCD run in pseudo stop (LCDRPSTP) bit in the LCD control register 1 (LCDCR1). If LCDRPSTP is reset, the LCD32F4B driver system is turned off during pseudo stop mode. In this case, the LCD waveform generation clocks are stopped and the LCD32F4B drivers pull down to VSSX those frontplane and backplane pins that were enabled before entering pseudo stop mode. If LCDRPSTP is set, the LCD32F4B driver system continues to operate during pseudo stop mode. The contents of the LCD RAM and the LCD registers retain the values they had prior to entering pseudo stop mode.

8.4.4 Operation in Stop Mode

All LCD32F4B driver system clocks are stopped, the LCD32F4B driver system pulls down to VSSX those frontplane and backplane pins that were enabled before entering stop mode. Also, during stop mode, the contents of the LCD RAM and the LCD registers retain the values they had prior to entering stop mode. As a result, after exiting from stop mode, the LCD32F4B driver system clocks will run (if LCDEN = 1) and the frontplane and backplane pins retain the functionality they had prior to entering stop mode.

8.4.5 LCD Waveform Examples

Figure 8-9 through Figure 8-13 show the timing examples of the LCD output waveforms for the available modes of operation.

8.4.5.1 1/1 Duty Multiplexed with 1/1 Bias Mode

Duty = 1/1:DUTY1 = 0, DUTY0 = 1

Bias = 1/1:BIAS = 0 or BIAS = 1

$V_0 = V_1 = VSSX$, $V_2 = V_3 = VLCD$

- BP1, BP2, and BP3 are not used, a maximum of 32 segments are displayed.

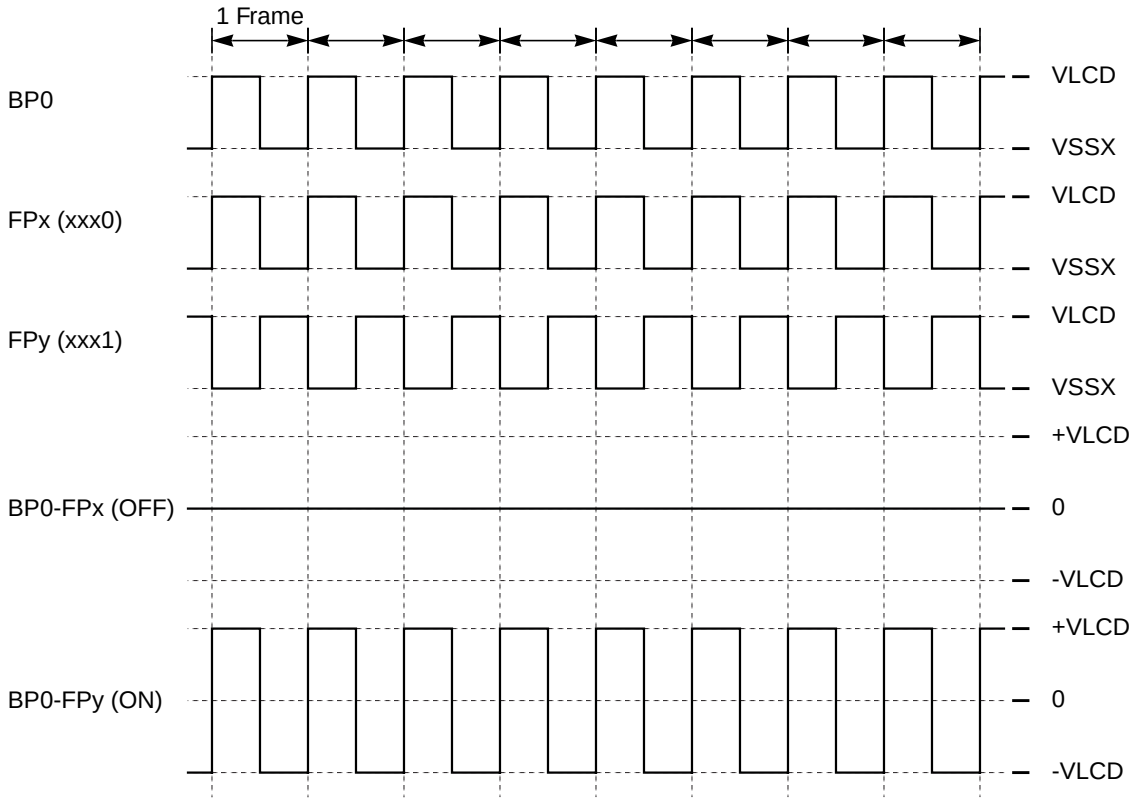


Figure 8-9. 1/1 Duty and 1/1 Bias

8.4.5.2 1/2 Duty Multiplexed with 1/2 Bias Mode

Duty = 1/2:DUTY1 = 1, DUTY0 = 0

Bias = 1/2:BIAS = 0

V_0 = VSSX, V_1 = V_2 = VLCD * 1/2, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.

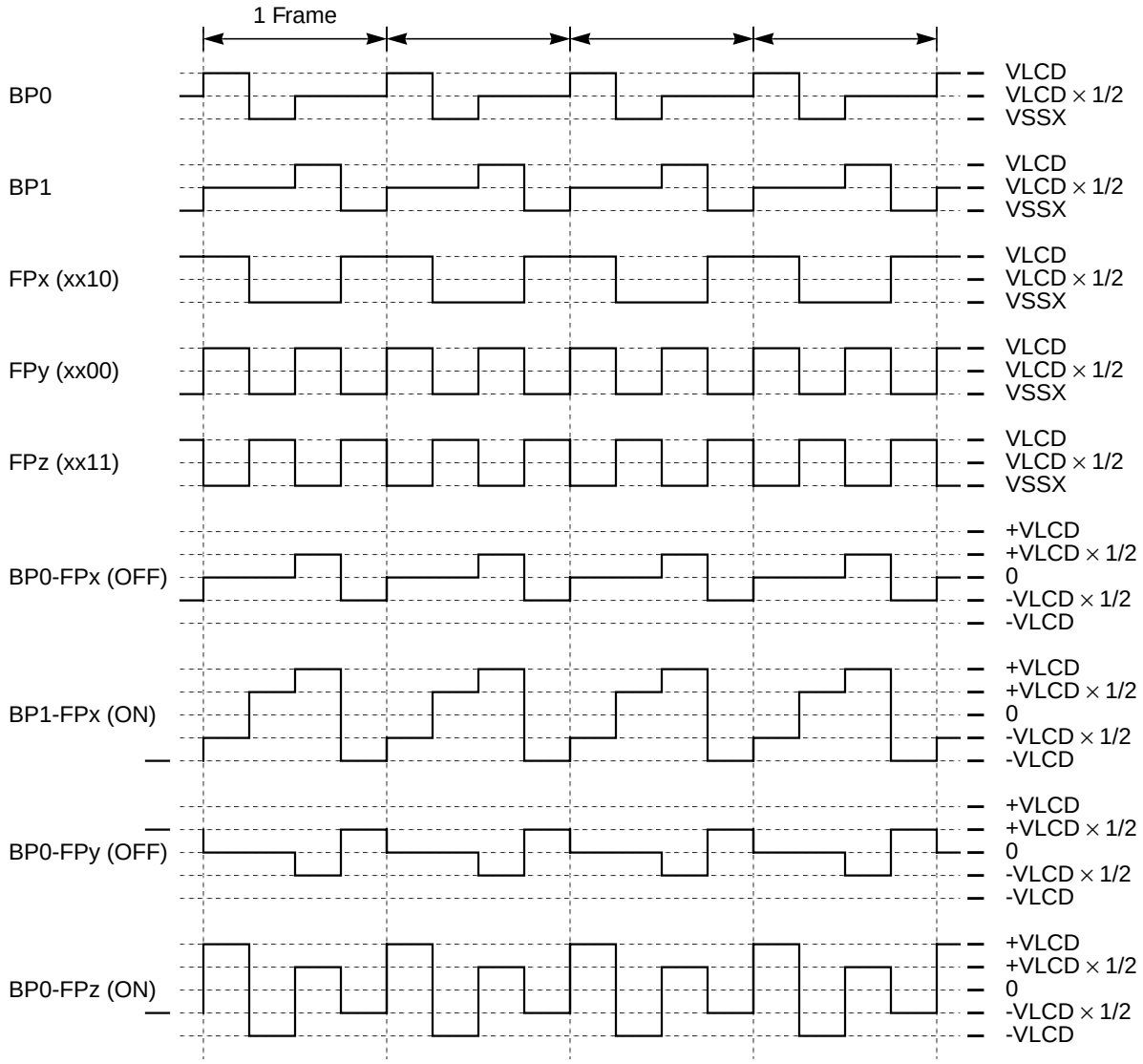


Figure 8-10. 1/2 Duty and 1/2 Bias

8.4.5.3 1/2 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/2:DUTY1 = 1, DUTY0 = 0

Bias = 1/3:BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP2 and BP3 are not used, a maximum of 64 segments are displayed.

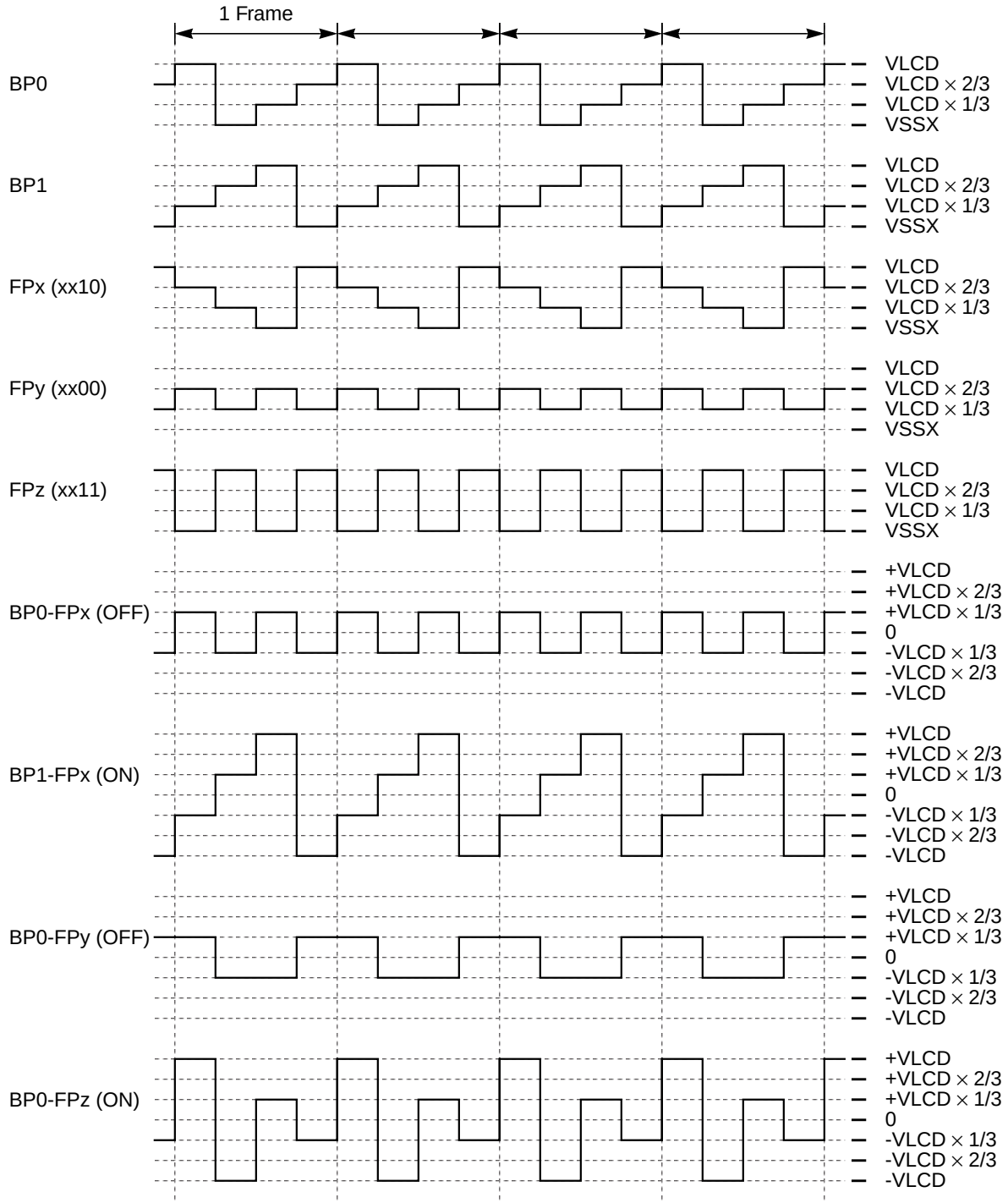


Figure 8-11. 1/2 Duty and 1/3 Bias

8.4.5.4 1/3 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/3:DUTY1 = 1, DUTY0 = 1

Bias = 1/3:BIAS = 0 or BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- BP3 is not used, a maximum of 96 segments are displayed.

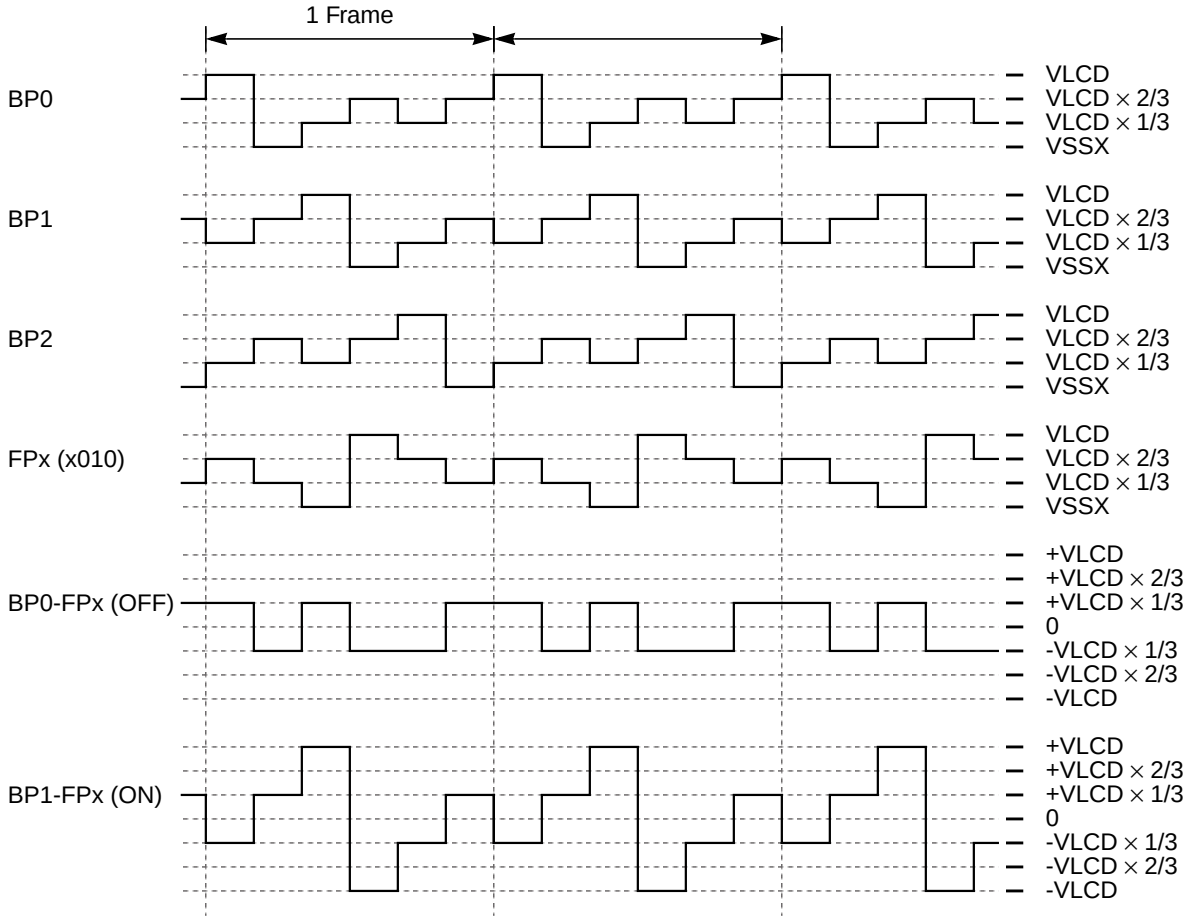


Figure 8-12. 1/3 Duty and 1/3 Bias

8.4.5.5 1/4 Duty Multiplexed with 1/3 Bias Mode

Duty = 1/4:DUTY1 = 0, DUTY0 = 0

Bias = 1/3:BIAS = 0 or BIAS = 1

V_0 = VSSX, V_1 = VLCD * 1/3, V_2 = VLCD * 2/3, V_3 = VLCD

- A maximum of 128 segments are displayed.

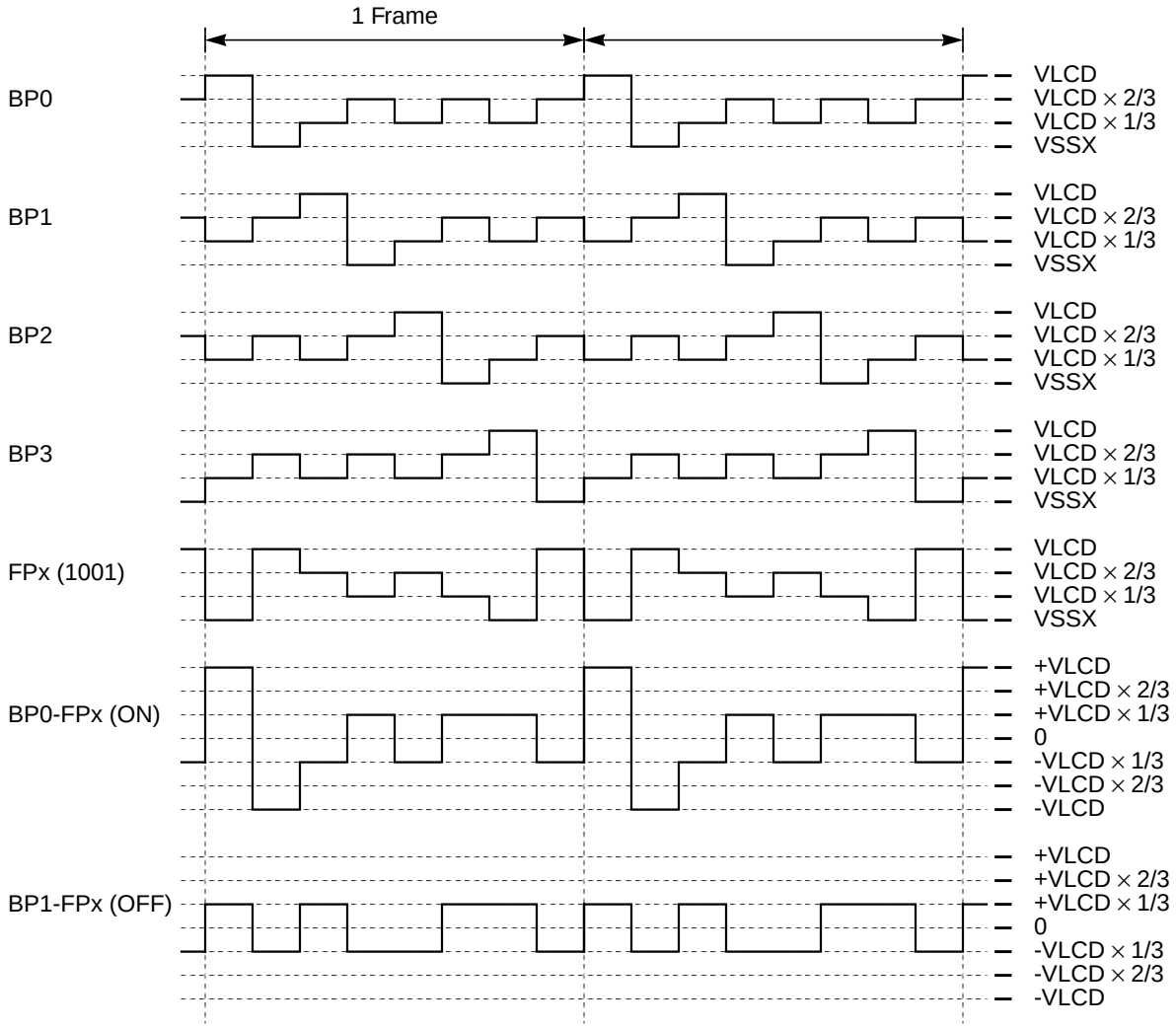


Figure 8-13. 1/4 Duty and 1/3 Bias

8.5 Resets

The reset values of registers and signals are described in Section 8.3, “Memory Map and Register Definition”. The behavior of the LCD32F4B system during reset is described in Section 8.4.1, “LCD Driver Description”.

8.6 Interrupts

This module does not generate any interrupts.

Chapter 9
Motor Controller (MC10B8CV1)

9.1 Introduction

The block MC10B8C is a PWM motor controller suitable to drive instruments in a cluster configuration or any other loads requiring a PWM signal. The motor controller has eight PWM channels associated with two pins each (16 pins in total).

9.1.1 Features

The MC10B8C includes the following features:

- 10/11-bit PWM counter
- 11-bit resolution with selectable PWM dithering function
- 7-bit resolution mode (fast mode): duty cycle can be changed by accessing only 1 byte/output
- Left, right, or center aligned PWM
- Output slew rate control
- This module is suited for, but not limited to, driving small stepper and air core motors used in instrumentation applications. This module can be used for other motor control or PWM applications that match the frequency, resolution, and output drive capabilities of the module.

9.1.2 Modes of Operation

9.1.2.1 Functional Modes

9.1.2.1.1 PWM Resolution

The motor controller can be configured to either 11- or 7-bits resolution mode by clearing or setting the FAST bit. This bit influences all PWM channels. For details, please refer to Section 9.3.2.5, “Motor Controller Duty Cycle Registers”.

9.1.2.1.2 Dither Function

Dither function can be selected or deselected by setting or clearing the DITH bit. This bit influences all PWM channels. For details, please refer to Section 9.4.1.3.5, “Dither Bit (DITH)”.

9.1.2.2 PWM Channel Configuration Modes

The eight PWM channels can operate in three functional modes. Those modes are, with some restrictions, selectable for each channel independently.

9.1.2.2.1 Dual Full H-Bridge Mode

This mode is suitable to drive a stepper motor or a 360^{o} air gauge instrument. For details, please refer to Section 9.4.1.1.1, “Dual Full H-Bridge Mode (MCOM = 11)”. In this mode two adjacent PWM channels are combined, and two PWM channels drive four pins.

9.1.2.2.2 Full H-Bridge Mode

This mode is suitable to drive any load requiring a PWM signal in a H-bridge configuration using two pins. For details please refer to Section 9.4.1.1.2, “Full H-Bridge Mode (MCOM = 10)”.

9.1.2.2.3 Half H-Bridge Mode

This mode is suitable to drive a 90^{o} instrument driven by one pin. For details, please refer to Section 9.4.1.1.3, “Half H-Bridge Mode (MCOM = 00 or 01)”.

9.1.2.3 PWM Alignment Modes

Each PWM channel can operate independently in three different alignment modes. For details, please refer to Section 9.4.1.3.1, “PWM Alignment Modes”.

9.1.2.4 Low-Power Modes

The behavior of the motor controller in low-power modes is programmable. For details, please refer to Section 9.4.5, “Operation in Wait Mode” and Section 9.4.6, “Operation in Stop and Pseudo-Stop Modes”.

9.1.3 Block Diagram

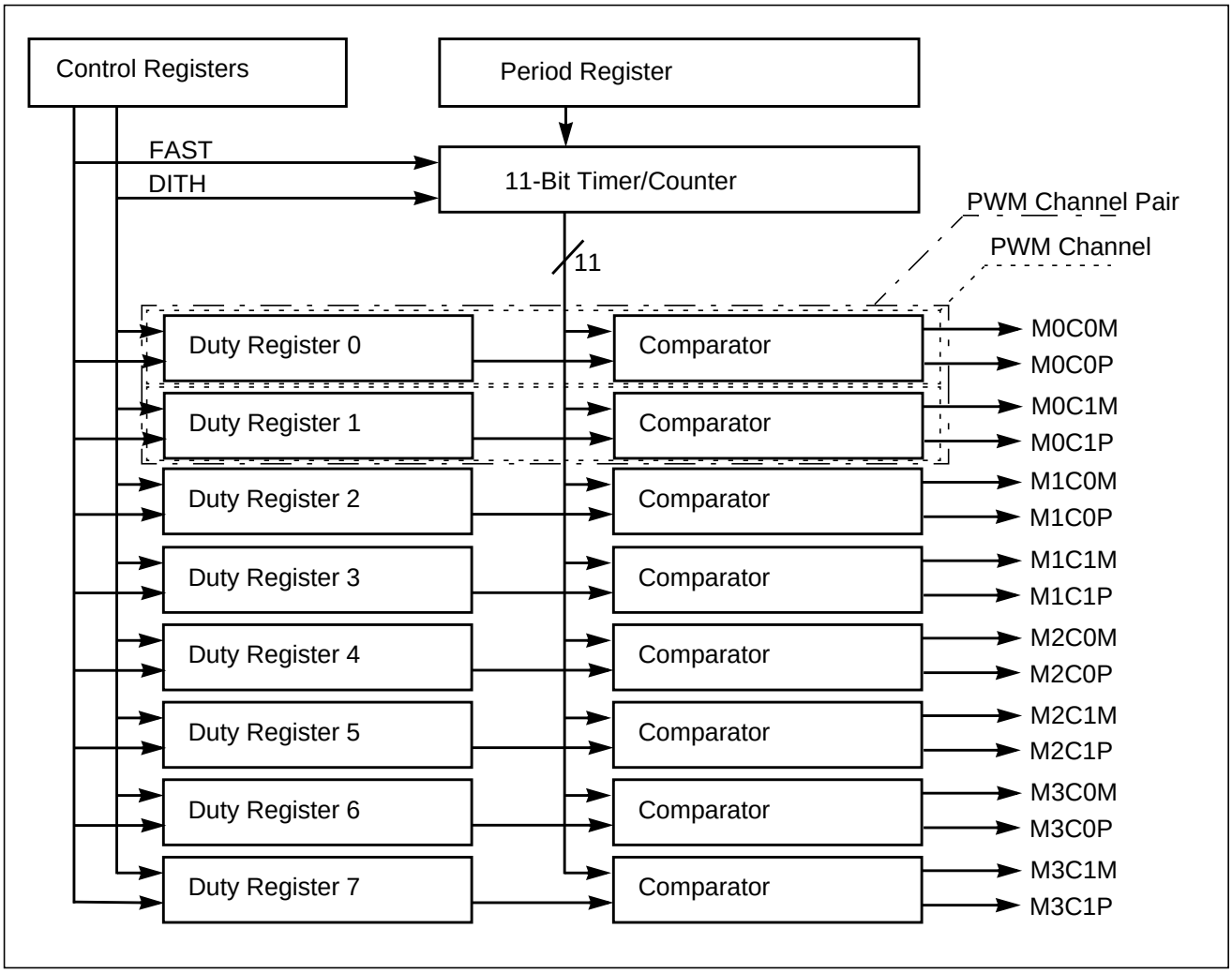


Figure 9-1. MC10B8C Block Diagram

9.2 External Signal Description

The motor controller is associated with 16 pins. Table 9-1 lists the relationship between the PWM channels and signal pins as well as PWM channel pair (motor number), coils, and nodes they are supposed to drive if all channels are set to dual full H-bridge configuration.

Table 9-1. PWM Channel and Pin Assignment

Pin Name	PWM Channel	PWM Channel Pair[1]	Coil	Node
M0C0M	0	0	0	Minus
M0C0P				Plus
M0C1M	1		1	Minus
M0C1P				Plus
M1C0M	2	1	0	Minus
M1C0P				Plus
M1C1M	3		1	Minus
M1C1P				Plus
M2C0M	4	2	0	Minus
M2C0P				Plus
M2C1M	5		1	Minus
M2C1P				Plus
M3C0M	6	3	0	Minus
M3C0P				Plus
M3C1M	7		1	Minus
M3C1P				Plus

[1] A PWM Channel Pair always consists of PWM channel x and PWM channel x+1 (x = 2·n). The term “PWM Channel Pair” is equivalent to the term “Motor”. E.g. Channel Pair 0 is equivalent to Motor 0

9.2.1 M0C0M/M0C0P/M0C1M/M0C1P — PWM Output Pins for Motor 0

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 0. PWM output on M0C0M results in a positive current flow through coil 0 when M0C0P is driven to a logic high state. PWM output on M0C1M results in a positive current flow through coil 1 when M0C1P is driven to a logic high state.

9.2.2 M1C0M/M1C0P/M1C1M/M1C1P — PWM Output Pins for Motor 1

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 1. PWM output on M1C0M results in a positive current flow through coil 0 when M1C0P is driven to a logic high state. PWM output on M1C1M results in a positive current flow through coil 1 when M1C1P is driven to a logic high state.

9.2.3 M2C0M/M2C0P/M2C1M/M2C1P — PWM Output Pins for Motor 2

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 2. PWM output on M2C0M results in a positive current flow through coil 0 when M2C0P is driven

to a logic high state. PWM output on M2C1M results in a positive current flow through coil 1 when M2C1P is driven to a logic high state.

9.2.4 M3C0M/M3C0P/M3C1M/M3C1P — PWM Output Pins for Motor 3

High current PWM output pins that can be used for motor drive. These pins interface to the coils of motor 3. PWM output on M3C0M results in a positive current flow through coil 0 when M3C0P is driven to a logic high state. PWM output on M3C1M results in a positive current flow through coil 1 when M3C1P is driven to a logic high state.

9.3 Memory Map and Register Definition

This section provides a detailed description of all registers of the 10-bit 8-channel motor controller module.

9.3.1 Module Memory Map

Figure 9-2 shows the memory map of the 10-bit 8-channel motor controller module.

Figure 9-2. MC10B8C Memory Map

Offset	Register	Access
0x0000	Motor Controller Control Register 0 (MCCTL0)	RW
0x0001	Motor Controller Control Register 1 (MCCTL1)	RW
0x0002	Motor Controller Period Register (High Byte)	RW
0x0003	Motor Controller Period Register (Low Byte)	RW
0x0004	Reserved[1]	—
0x0005	Reserved	—
0x0006	Reserved	—
0x0007	Reserved	—
0x0008	Reserved	—
0x0009	Reserved	—
0x000A	Reserved	—
0x000B	Reserved	—
0x000C	Reserved	—
0x000D	Reserved	—
0x000E	Reserved	—
0x000F	Reserved	—
0x0010	Motor Controller Channel Control Register 0 (MCCC0)	RW
0x0011	Motor Controller Channel Control Register 1 (MCCC1)	RW
0x0012	Motor Controller Channel Control Register 2 (MCCC2)	RW
0x0013	Motor Controller Channel Control Register 3 (MCCC3)	RW
0x0014	Motor Controller Channel Control Register 4 (MCCC4)	RW
0x0015	Motor Controller Channel Control Register 5 (MCCC5)	RW

Figure 9-2. MC10B8C Memory Map (continued)

Offset	Register	Access
0x0016	Motor Controller Channel Control Register 6 (MCCC6)	RW
0x0017	Motor Controller Channel Control Register 7 (MCCC7)	RW
0x0018	Reserved	—
0x0019	Reserved	—
0x001A	Reserved	—
0x001B	Reserved	—
0x001C	Reserved	—
0x001D	Reserved	—
0x001E	Reserved	—
0x001F	Reserved	—
0x0020	Motor Controller Duty Cycle Register 0 (MCDC0) — High Byte	RW
0x0021	Motor Controller Duty Cycle Register 0 (MCDC0) — Low Byte	RW
0x0022	Motor Controller Duty Cycle Register 1 (MCDC1) — High Byte	RW
0x0023	Motor Controller Duty Cycle Register 1 (MCDC1) — Low Byte	RW
0x0024	Motor Controller Duty Cycle Register 2 (MCDC2) — High Byte	RW
0x0025	Motor Controller Duty Cycle Register 2 (MCDC2) — Low Byte	RW
0x0026	Motor Controller Duty Cycle Register 3 (MCDC3) — High Byte	RW
0x0027	Motor Controller Duty Cycle Register 3 (MCDC3) — Low Byte	RW
0x0028	Motor Controller Duty Cycle Register 4 (MCDC4) — High Byte	RW
0x0029	Motor Controller Duty Cycle Register 4 (MCDC4) — Low Byte	RW
0x002A	Motor Controller Duty Cycle Register 5 (MCDC5) — High Byte	RW
0x002B	Motor Controller Duty Cycle Register 5 (MCDC5) — Low Byte	RW
0x002C	Motor Controller Duty Cycle Register 6 (MCDC6) — High Byte	RW
0x002D	Motor Controller Duty Cycle Register 6 (MCDC6) — Low Byte	RW
0x002E	Motor Controller Duty Cycle Register 7 (MCDC7) — High Byte	RW
0x002F	Motor Controller Duty Cycle Register 7 (MCDC7) — Low Byte	RW
0x0030	Reserved	—
0x0031	Reserved	—
0x0032	Reserved	—
0x0033	Reserved	—
0x0034	Reserved	—
0x0035	Reserved	—
0x0036	Reserved	—
0x0037	Reserved	—
0x0038	Reserved	—
0x0039	Reserved	—
0x003A	Reserved	—
0x003B	Reserved	—
0x003C	Reserved	—
0x003D	Reserved	—

Figure 9-2. MC10B8C Memory Map (continued)

Offset	Register	Access
0x003E	Reserved	—
0x003F	Reserved	—

1 Write accesses to “Reserved” addresses have no effect. Read accesses to “Reserved” addresses provide **invalid** data (0x0000).

9.3.2 Register Descriptions

9.3.2.1 Motor Controller Control Register 0

This register controls the operating mode of the motor controller module.

	7	6	5	4	3	2	1	0
R	0	MCPRE[1:0]		MCSWAI	FAST	DITH	0	MCTOIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-3. Motor Controller Control Register 0 (MCCTL0)

Table 9-2. MCCTL0 Field Descriptions

Field	Description
6:5 MCPRE[1:0]	**Motor Controller Prescaler Select** — MCPRE1 and MCPRE0 determine the prescaler value that sets the motor controller timer counter clock frequency (f_{TC}). The clock source for the prescaler is the peripheral bus clock (f_{BUS}) as shown in Figure 9-22. Writes to MCPRE1 or MCPRE0 will not affect the timer counter clock frequency f_{TC} until the start of the next PWM period. Table 9-3 shows the prescaler values that result from the possible combinations of MCPRE1 and MCPRE0
4 MCSWAI	**Motor Controller Module Stop in Wait Mode** 0 Entering wait mode has no effect on the motor controller module and the associated port pins maintain the functionality they had prior to entering wait mode both during wait mode and after exiting wait mode. 1 Entering wait mode will stop the clock of the module and debias the analog circuitry. The module will release the pins.
3 FAST	**Motor Controller PWM Resolution Mode** 0 PWM operates in 11-bit resolution mode, duty cycle registers of all channels are switched to word mode. 1 PWM operates in 7-bit resolution (fast) mode, duty cycle registers of all channels are switched to byte mode.
2 DITH	**Motor Control/Driver Dither Feature Enable** (refer to Section 9.4.1.3.5, “Dither Bit (DITH)”) 0 Dither feature is disabled. 1 Dither feature is enabled.
0 MCTOIF	**Motor Controller Timer Counter Overflow Interrupt Flag** — This bit is set when a motor controller timer counter overflow occurs. The bit is cleared by writing a 1 to the bit. 0 A motor controller timer counter overflow has not occurred since the last reset or since the bit was cleared. 1 A motor controller timer counter overflow has occurred.

Table 9-3. Prescaler Values

MCPRE[1:0]	f_{TC}
00	f_{Bus}
01	$f_{Bus}/2$
10	$f_{Bus}/4$
11	$f_{Bus}/8$

9.3.2.2 Motor Controller Control Register 1

This register controls the behavior of the analog section of the motor controller as well as the interrupt enables.

	7	6	5	4	3	2	1	0
R	RECIRC	0	0	0	0	0	0	MCTOIE
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-4. Motor Controller Control Register 1 (MCCTL1)

Table 9-4. MCCTL1 Field Descriptions

Field	Description
7 RECIRC	**Recirculation in (Dual) Full H-Bridge Mode** (refer to Section 9.4.1.3.3, “RECIRC Bit”)— RECIRC only affects the outputs in (dual) full H-bridge modes. In half H-bridge mode, the PWM output is always active low. RECIRC = 1 will also invert the effect of the S bits (refer to Section 9.4.1.3.2, “Sign Bit (S)”) in (dual) full H-bridge modes. RECIRC must be changed only while no PWM channel is operating in (dual) full H-bridge mode; otherwise, erroneous output pattern may occur. 0 Recirculation on the high side transistors. Active state for PWM output is logic low, the static channel will output logic high. 1 Recirculation on the low side transistors. Active state for PWM output is logic high, the static channel will output logic low.
0 MCTOIE	**Motor Controller Timer Counter Overflow Interrupt Enable** 0 Interrupt disabled. 1 Interrupt enabled. An interrupt will be generated when the motor controller timer counter overflow interrupt flag (MCTOIF) is set.

9.3.2.3 Motor Controller Period Register

The period register defines PER, the number of motor controller timer counter clocks a PWM period lasts. The motor controller timer counter is clocked with the frequency f_{TC}. If dither mode is enabled (DITH = 1, refer to Section 9.4.1.3.5, “Dither Bit (DITH)”), P0 is ignored and reads as a 0. In this case PER = 2 * D[10:1].

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-5. Motor Controller Period Register (MCPER) with DITH = 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	0	0	0	0	0	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-6. Motor Controller Period Register (MCPER) with DITH = 1

For example, programming MCPER to 0x0022 (PER = 34 decimal) will result in 34 counts for each complete PWM period. Setting MCPER to 0 will shut off all PWM channels as if MCAM[1:0] is set to 0 in all channel control registers after the next period timer counter overflow. In this case, the motor controller releases all pins.

NOTE

Programming MCPER to 0x0001 and setting the DITH bit will be managed as if MCPER is programmed to 0x0000. All PWM channels will be shut off after the next period timer counter overflow.

9.3.2.4 Motor Controller Channel Control Registers

Each PWM channel has one associated control register to control output delay, PWM alignment, and output mode. The registers are named MCCC0... MCCC7. In the following, MCCC0 is described as a reference for all eight registers.

	7	6	5	4	3	2	1	0
R	MCOM1	MCOM0	MCAM1	MCAM0	0	0	CD1	CD0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-7. Motor Controller Control Register Channel 0–7 (MCCC0–MCCC7)

Table 9-5. MCCC0–MCCC7 Field Descriptions

Field	Description
7:6 MCOM[1:0]	**Output Mode** — MCOM1, MCOM0 control the PWM channel's output mode. See Table 9-6.
5:4 MCAM[1:0]	**PWM Channel Alignment Mode** — MCAM1, MCAM0 control the PWM channel's PWM alignment mode and operation. See Table 9-7. MCAM[1:0] and MCOM[1:0] are double buffered. The values used for the generation of the output waveform will be copied to the working registers either at once (if all PWM channels are disabled or MCPER is set to 0) or if a timer counter overflow occurs. Reads of the register return the most recent written value, which are not necessarily the currently active values.
1:0 CD[1:0]	**PWM Channel Delay** — Each PWM channel can be individually delayed by a programmable number of PWM timer counter clocks. The delay will be n/f_{TC}. See Table 9-8.

Table 9-6. Output Mode

MCOM[1:0]	Output Mode
00	Half H-bridge mode, PWM on MnCxM, MnCxP is released
01	Half H-bridge mode, PWM on MnCxP, MnCxM is released
10	Full H-bridge mode
11	Dual full H-bridge mode

Table 9-7. PWM Alignment Mode

MCAM[1:0]	PWM Alignment Mode
00	Channel disabled
01	Left aligned
10	Right aligned
11	Center aligned

Table 9-8. Channel Delay

CD[1:0]	n [# of PWM Clocks]
00	0
01	1
10	2
11	3

NOTE

The PWM motor controller will release the pins after the next PWM timer counter overflow without accommodating any channel delay if a single channel has been disabled or if the period register has been cleared or all channels have been disabled. Program one or more inactive PWM frames (duty cycle = 0) before writing a configuration that disables a single channel or the entire PWM motor controller.

9.3.2.5 Motor Controller Duty Cycle Registers

Each duty cycle register sets the sign and duty functionality for the respective PWM channel.

The contents of the duty cycle registers define DUTY, the number of motor controller timer counter clocks the corresponding output is driven low (RECIRC = 0) or is driven high (RECIRC = 1). Setting all bits to 0 will give a static high output in case of RECIRC = 0; otherwise, a static low output. Values greater than or equal to the contents of the period register will generate a static low output in case of RECIRC = 0, or a static high output if RECIRC = 1. The layout of the duty cycle registers differ dependent upon the state of the FAST bit in the control register 0.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	S	S	S	S	S	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-8. Motor Controller Duty Cycle Register x (MCDCx) with FAST = 0

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	S	D8	D7	D6	D5	D4	D3	D2	0	0	0	0	0	0	0	0
W																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 9-9. Motor Controller Duty Cycle Register x (MCDCx) with FAST = 1

Table 9-9. MCDCx Field Descriptions

Field	Description
0 S	SIGN — The SIGN bit is used to define which output will drive the PWM signal in (dual) full-H-bridge modes. The SIGN bit has no effect in half-bridge modes. See Section 9.4.1.3.2, “Sign Bit (S)”, and table Table 9-11 for detailed information about the impact of RECIRC and SIGN bit on the PWM output.

Whenever FAST = 1, the bits D10, D9, D1, and D0 will be set to 0 if the duty cycle register is written.

For example setting MCDCx = 0x0158 with FAST = 0 gives the same output waveform as setting MCDCx = 0x5600 with FAST = 1 (with FAST = 1, the low byte of MCDCx needs not to be written).

The state of the FAST bit has impact only during write and read operations. A change of the FAST bit (set or clear) without writing a new value does not impact the internal interpretation of the duty cycle values.

To prevent the output from inconsistent signals, the duty cycle registers are double buffered. The motor controller module will use working registers to generate the output signals. The working registers are copied from the bus accessible registers at the following conditions:

- MCPER is set to 0 (all channels are disabled in this case)
- MCAM[1:0] of the respective channel is set to 0 (channel is disabled)
- A PWM timer counter overflow occurs while in half H-bridge or full H-bridge mode
- A PWM channel pair is configured to work in Dual Full H-Bridge mode and a PWM timer counter overflow occurs after the odd[1] duty cycle register of the channel pair has been written.

In this way, the output of the PWM will always be either the old PWM waveform or the new PWM waveform, not some variation in between.

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active sign, duty cycle, and dither functionality due to the double buffering scheme.

1. Odd duty cycle register: MCDCx+1, x = 2·n

9.4 Functional Description

9.4.1 Modes of Operation

9.4.1.1 PWM Output Modes

The motor controller is configurable between three output modes.

- Dual full H-bridge mode can be used to control either a stepper motor or a 360° air core instrument. In this case two PWM channels are combined.
- In full H-bridge mode, each PWM channel is updated independently.
- In half H-bridge mode, one pin of the PWM channel can generate a PWM signal to control a 90° air core instrument (or other load requiring a PWM signal) and the other pin is unused.

The mode of operation for each PWM channel is determined by the corresponding MCOM[1:0] bits in channel control registers. After a reset occurs, each PWM channel will be disabled, the corresponding pins are released.

Each PWM channel consists of two pins. One output pin will generate a PWM signal. The other will operate as logic high or low output depending on the state of the RECIRC bit (refer to Section 9.4.1.3.3, “RECIRC Bit”), while in (dual) full H-bridge mode, or will be released, while in half H-bridge mode. The state of the S bit in the duty cycle register determines the pin where the PWM signal is driven in full H-bridge mode. While in half H-bridge mode, the state of the released pin is determined by other modules associated with this pin.

Associated with each PWM channel pair n are two PWM channels, x and x + 1, where x = 2 * n and n (0, 1, 2, 3) is the PWM channel pair number. Duty cycle register x controls the sign of the PWM signal (which pin drives the PWM signal) and the duty cycle of the PWM signal for motor controller channel x. The pins associated with PWM channel x are MnC0P and MnC0M. Similarly, duty cycle register x + 1 controls the sign of the PWM signal and the duty cycle of the PWM signal for channel x + 1. The pins associated with PWM channel x + 1 are MnC1P and MnC1M. This is summarized in Table 9-10.

Table 9-10. Corresponding Registers and Pin Names for Each PWM Channel Pair

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
n	MCMCx	MCDCx	PWM Channel x, x = 2·n	MnC0M
				MnC0P
	MCMCx + 1	MCDCx + 1	PWM Channel x + 1, x = 2·n	MnC1M
				MnC1P
0	MCMC0	MCDC0	PWM Channel 0	M0C0M
				M0C0P
	MCMC1	MCDC1	PWM Channel 1	M0C1M
				M0C1P

Table 9-10. Corresponding Registers and Pin Names for Each PWM Channel Pair (continued)

PWM Channel Pair Number	PWM Channel Control Register	Duty Cycle Register	Channel Number	Pin Names
1	MCMC2	MCDC2	PWM Channel 2	M1C0M
				M1C0P
	MCMC3	MCDC3	PWM Channel 3	M1C1M
				M1C1P
2	MCMC4	MCDC4	PWM Channel 4	M2C0M
				M2C0P
	MCMC5	MCDC5	PWM Channel 5	M2C1M
				M2C1P
3	MCMC6	MCDC6	PWM Channel 6	M3C0M
				M3C0P
	MCMC7	MCDC7	PWM Channel 7	M3C1M
				M3C1P

9.4.1.1.1 Dual Full H-Bridge Mode (MCOM = 11)

PWM channel pairs x and x + 1 operate in dual full H-bridge mode if both channels have been enabled (MCAM[1:0]=01, 10, or 11) and both of the corresponding output mode bits MCOM[1:0] in both PWM channel control registers are set.

A typical configuration in dual full H-bridge mode is shown in Figure 9-10. PWM channel x drives the PWM output signal on either MnC0P or MnC0M. If MnC0P drives the PWM signal, MnC0M will be output either high or low depending on the RECIRC bit. If MnC0M drives the PWM signal, MnC0P will be an output high or low. PWM channel x + 1 drives the PWM output signal on either MnC1P or MnC1M. If MnC1P drives the PWM signal, MnC1M will be an output high or low. If MnC1M drives the PWM signal, MnC1P will be an output high or low. This results in motor recirculation currents on the high side drivers (RECIRC = 0) while the PWM signal is at a logic high level, or motor recirculation currents on the low side drivers (RECIRC = 1) while the PWM signal is at a logic low level. The pin driving the PWM signal is determined by the S (sign) bit in the corresponding duty cycle register and the state of the RECIRC bit. The value of the PWM duty cycle is determined by the value of the D[10:0] or D[8:2] bits respectively in the duty cycle register depending on the state of the FAST bit.

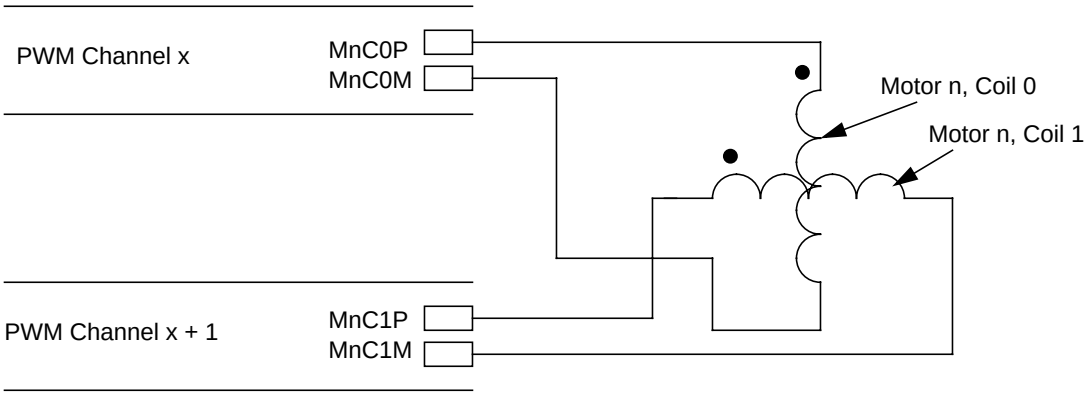


Figure 9-10. Typical Dual Full H-Bridge Mode Configuration

Whenever FAST = 0 only 16-bit write accesses to the duty cycle registers are allowed, 8-bit write accesses can lead to unpredictable duty cycles.

While fast mode is enabled (FAST = 1), 8-bit write accesses to the high byte of the duty cycle registers are allowed, because only the high byte of the duty cycle register is used to determine the duty cycle.

The following sequence should be used to update the current magnitude and direction for coil 0 and coil 1 of the motor to achieve consistent PWM output:

1. Write to duty cycle register x
2. Write to duty cycle register x + 1.

At the next timer counter overflow, the duty cycle registers will be copied to the working duty cycle registers. Sequential writes to the duty cycle register x will result in the previous data being overwritten.

9.4.1.1.2 Full H-Bridge Mode (MCOM = 10)

In full H-bridge mode, the PWM channels x and x + 1 operate independently. The duty cycle working registers are updated whenever a timer counter overflow occurs.

9.4.1.1.3 Half H-Bridge Mode (MCOM = 00 or 01)

In half H-bridge mode, the PWM channels x and x + 1 operate independently. In this mode, each PWM channel can be configured such that one pin is released and the other pin is a PWM output. Figure 9-11 shows a typical configuration in half H-bridge mode.

The two pins associated with each channel are switchable between released mode and PWM output dependent upon the state of the MCOM[1:0] bits in the MCCCx (channel control) register. See register description in Section 9.3.2.4, “Motor Controller Channel Control Registers”. In half H-bridge mode, the state of the S bit has no effect.

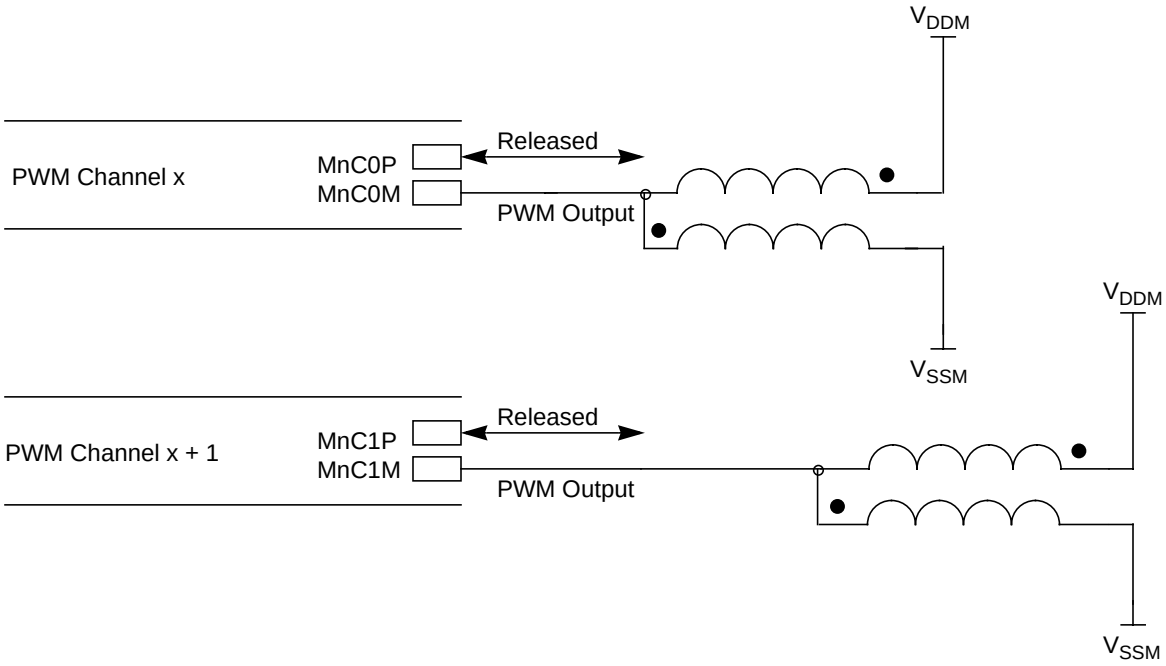


Figure 9-11. Typical Quad Half H-Bridge Mode Configuration

9.4.1.2 Relationship Between PWM Mode and PWM Channel Enable

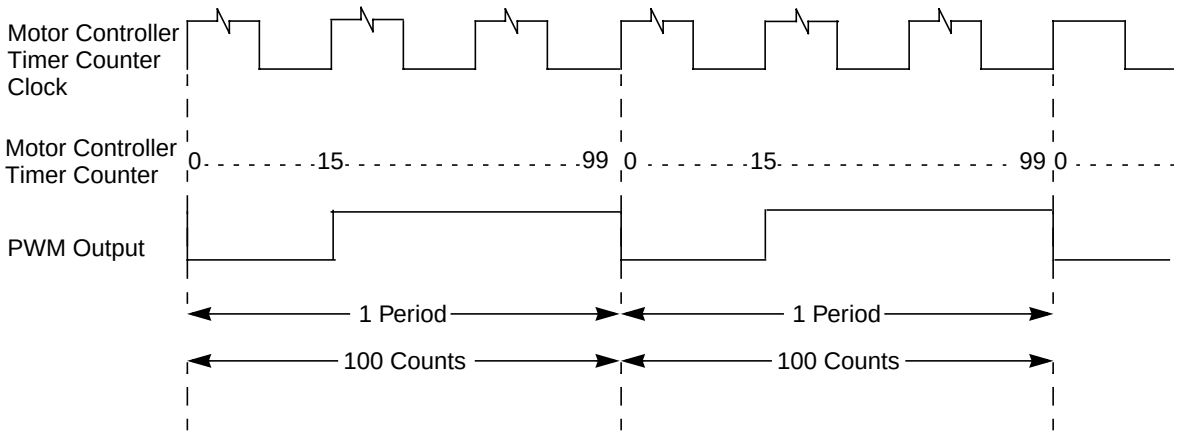
The pair of motor controller channels cannot be placed into dual full H-bridge mode unless both motor controller channels have been enabled (MCAM[1:0] not equal to 00) and dual full H-bridge mode is selected for both PWM channels (MCOM[1:0] = 11). If only one channel is set to dual full H-bridge mode, this channel will operate in full H-bridge mode, the other as programmed.

9.4.1.3 Relationship Between Sign, Duty, Dither, RECIRC, Period, and PWM Mode Functions

9.4.1.3.1 PWM Alignment Modes

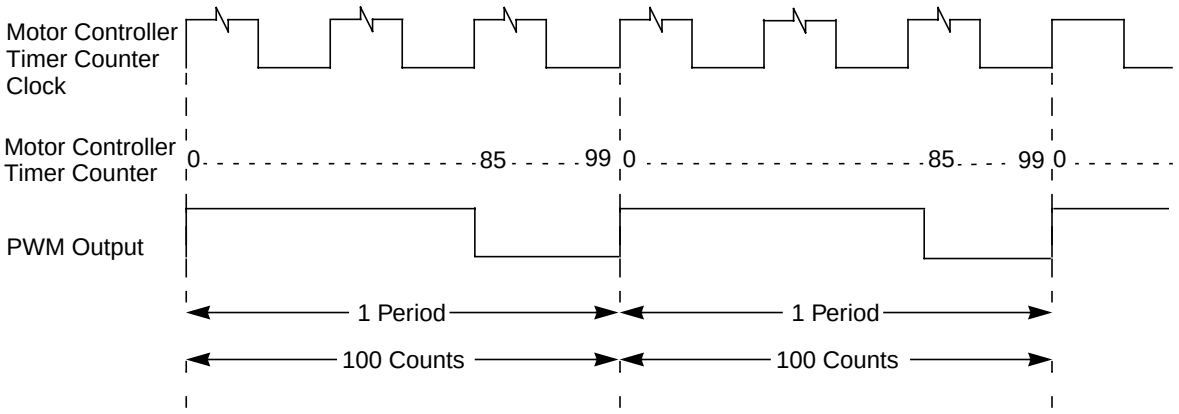
Each PWM channel can be programmed individually to three different alignment modes. The mode is determined by the MCAM[1:0] bits in the corresponding channel control register.

Left aligned (MCAM[1:0] = 01): The output will start active (low if RECIRC = 0 or high if RECIRC = 1) and will turn inactive (high if RECIRC = 0 or low if RECIRC = 1) after the number of counts specified by the corresponding duty cycle register.



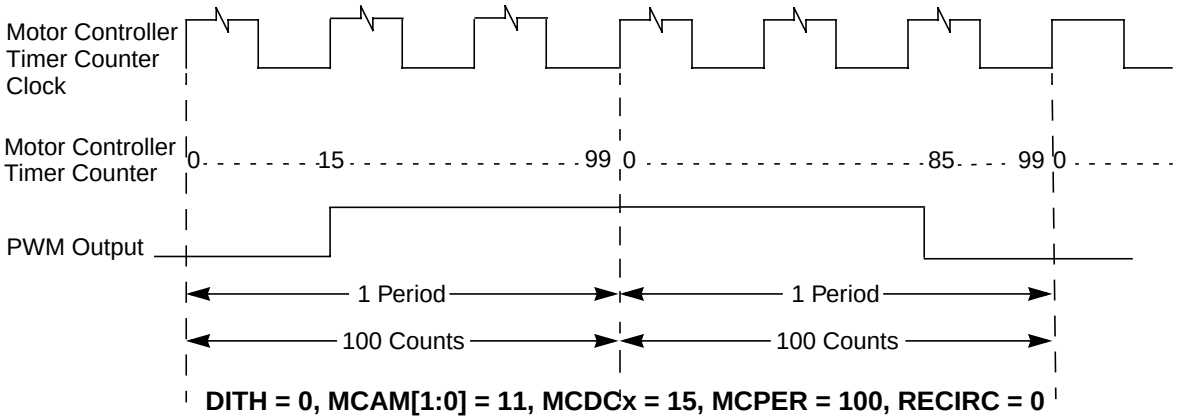
DITH = 0, MCAM[1:0] = 01, MCDCx = 15, MCPER = 100, RECIRC = 0

Right aligned (MCAM[1:0] = 10): The output will start inactive (high if RECIRC = 0 and low if RECIRC = 1) and will turn active after the number of counts specified by the difference of the contents of period register and the corresponding duty cycle register.



DITH = 0, MCAM[1:0] = 10, MCDCx = 15, MCPER = 100, RECIRC = 0

Center aligned (MCAM[1:0] = 11): Even periods will be output left aligned, odd periods will be output right aligned. PWM operation starts with the even period after the channel has been enabled. PWM operation in center aligned mode might start with the odd period if the channel has not been disabled before changing the alignment mode to center aligned.



DITH = 0, MCAM[1:0] = 11, MCDCx = 15, MCPER = 100, RECIRC = 0

9.4.1.3.2 Sign Bit (S)

Assuming RECIRC = 0 (the active state of the PWM signal is low), when the S bit for the corresponding channel is cleared, MnC0P (if the PWM channel number is even, n = 0, 1, 2, 3, see Table 9-10) or MnC1P (if the PWM channel number is odd, n = 0, 1, 2, 3, see Table 9-10), outputs a logic high while in (dual) full H-bridge mode. In half H-bridge mode the state of the S bit has no effect. The PWM output signal is generated on MnC0M (if the PWM channel number is even, n = 0, 1, 2, 3, see Table 9-10) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2, 3).

Assuming RECIRC = 0 (the active state of the PWM signal is low), when the S bit for the corresponding channel is set, MnC0M (if the PWM channel number is even, n = 0, 1, 2, 3, see Table 9-10) or MnC1M (if the PWM channel number is odd, n = 0, 1, 2, 3, see Table 9-10), outputs a logic high while in (dual) full H-bridge mode. In half H-bridge mode the state of the S bit has no effect. The PWM output signal is generated on MnC0P (if the PWM channel number is even, n = 0, 1, 2, 3, see Table 9-10) or MnC1P (if the PWM channel number is odd, n = 0, 1, 2, 3).

Setting RECIRC = 1 will also invert the effect of the S bit such that while S = 0, MnC0P or MnC1P will generate the PWM signal and MnC0M or MnC1M will be a static low output. While S = 1, MnC0M or MnC1M will generate the PWM signal and MnC0P or MnC1P will be a static low output. In this case the active state of the PWM signal will be high.

See Table 9-11 for detailed information about the impact of SIGN and RECIRC bit on the PWM output.

Table 9-11. Impact of RECIRC and SIGN Bit on the PWM Output

Output Mode	RECIRC	SIGN	MnCyM	MnCyP
(Dual) Full H-Bridge	0	0	$\overline{\text{PWM}}$[1]	1
(Dual) Full H-Bridge	0	1	1	PWM
(Dual) Full H-Bridge	1	0	0	PWM[2]
(Dual) Full H-Bridge	1	1	PWM	1
Half H-Bridge: PWM on MnCyM	Don't care	Don't care	PWM	—[3]
Half H-Bridge: PWM on MnCyP	Don't care	Don't care	—	PWM

1 $\overline{\text{PWM}}$: The PWM signal is low active. e.g., the waveform starts with 0 in left aligned mode. Output M generates the PWM signal. Output P is static high.
2 PWM: The PWM signal is high active. e.g., the waveform starts with 1 in left aligned mode. output P generates the PWM signal. Output M is static low.
3 The state of the output transistors is not controlled by the motor controller.

9.4.1.3.3 RECIRC Bit

The RECIRC bit controls the flow of the recirculation current of the load. Setting RECIRC = 0 will cause recirculation current to flow through the high side transistors, and RECIRC = 1 will cause the recirculation current to flow through the low side transistors. The RECIRC bit is only active in (dual) full H-bridge modes.

Effectively, RECIRC = 0 will cause a static high output on the output terminal not driven by the PWM, RECIRC = 1 will cause a static low output on the output terminals not driven by the PWM. To achieve the same current direction, the S bit behavior is inverted if RECIRC = 1. Figure 9-12, Figure 9-13, Figure 9-14, and Figure 9-15 illustrate the effect of the RECIRC bit in (dual) full H-bridge modes.

RECIRC bit must be changed only while no PWM channel is operated in (dual) full H-bridge mode.

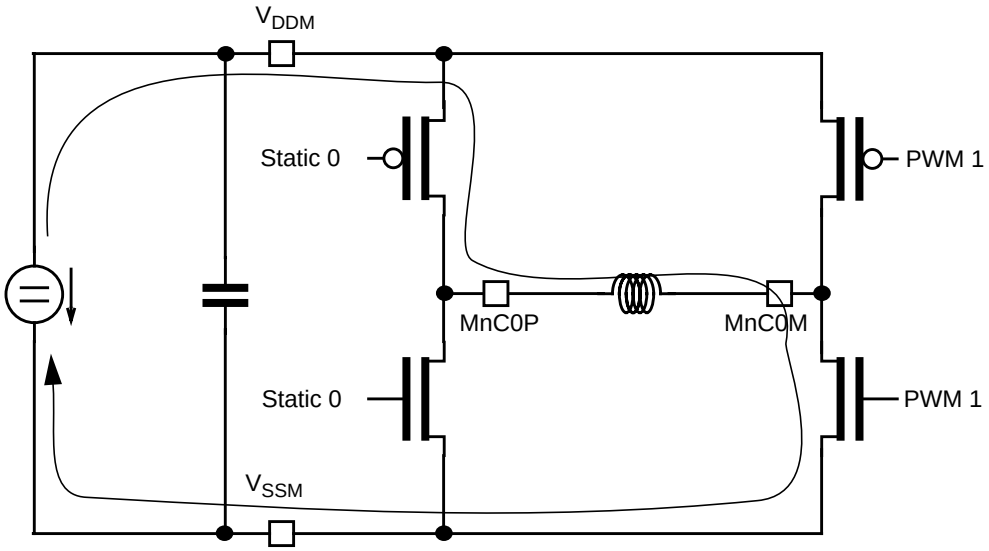


Figure 9-12. PWM Active Phase, RECIRC = 0, S = 0

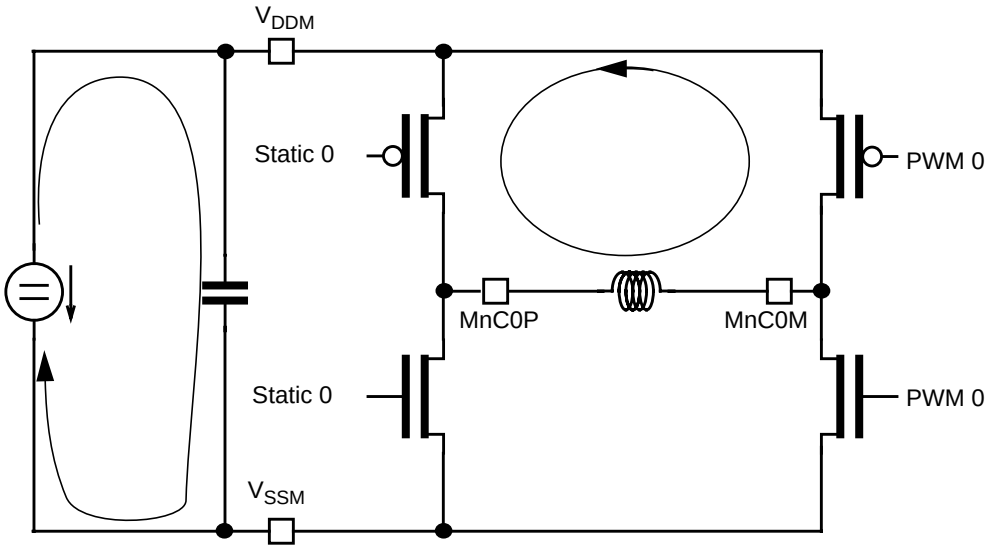


Figure 9-13. PWM Passive Phase, RECIRC = 0, S = 0

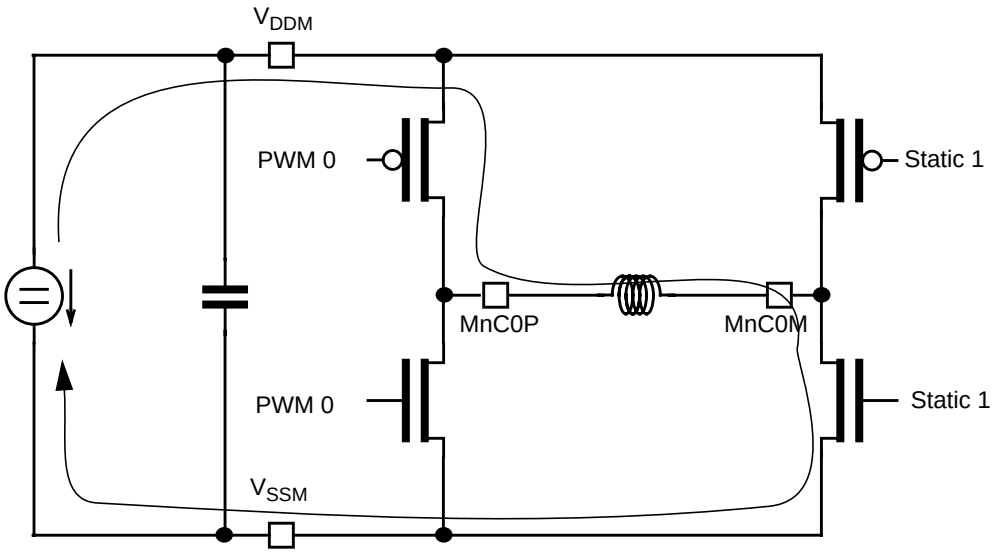


Figure 9-14. PWM Active Phase, RECIRC = 1, S = 0

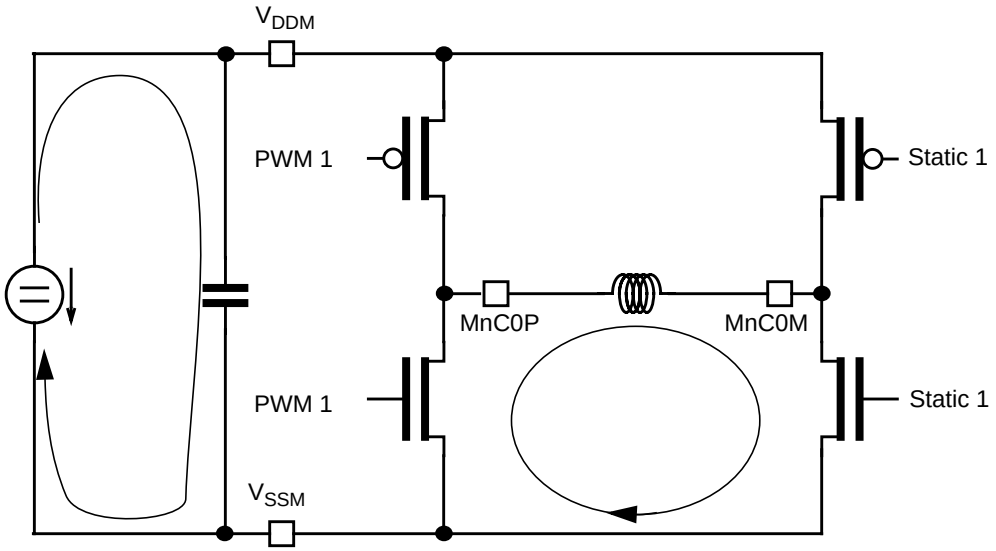


Figure 9-15. PWM Passive Phase, RECIRC = 1, S = 0

9.4.1.3.4 Relationship Between RECIRC Bit, S Bit, MCOM Bits, PWM State, and Output Transistors

Please refer to Figure 9-16 for the output transistor assignment.

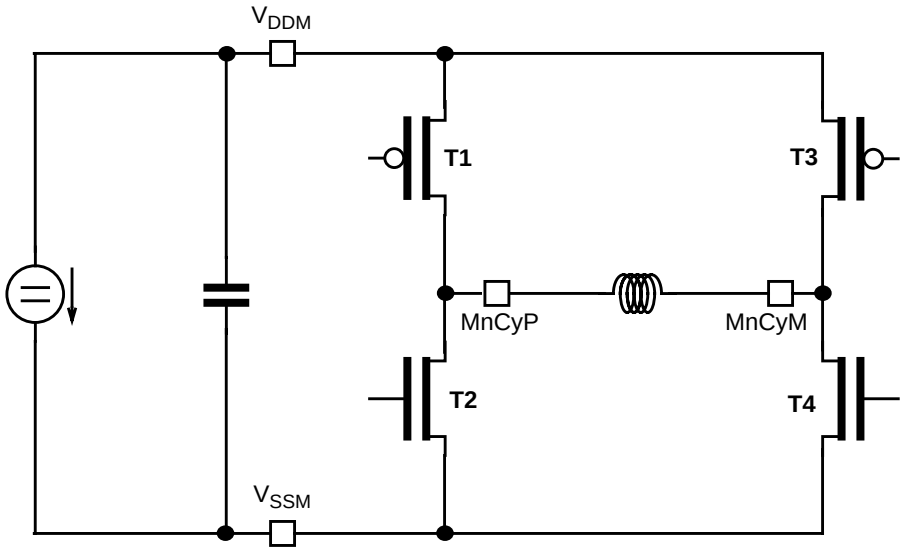


Figure 9-16. Output Transistor Assignment

Table 9-12 illustrates the state of the output transistors in different states of the PWM motor controller module. '—' means that the state of the output transistor is not controlled by the motor controller.

Table 9-12. State of Output Transistors in Various Modes

Mode	MCOM[1:0]	PWM Duty	RECIRC	S	T1	T2	T3	T4
Off	Don't care	—	Don't care	Don't care	—	—	—	—
Half H-Bridge	00	Active	Don't care	Don't care	—	—	OFF	ON
Half H-Bridge	00	Passive	Don't care	Don't care	—	—	ON	OFF
Half H-Bridge	01	Active	Don't care	Don't care	OFF	ON	—	—
Half H-Bridge	01	Passive	Don't care	Don't care	ON	OFF	—	—
(Dual) Full	10 or 11	Active	0	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	Passive	0	0	ON	OFF	ON	OFF
(Dual) Full	10 or 11	Active	0	1	OFF	ON	ON	OFF
(Dual) Full	10 or 11	Passive	0	1	ON	OFF	ON	OFF
(Dual) Full	10 or 11	Active	1	0	ON	OFF	OFF	ON
(Dual) Full	10 or 11	Passive	1	0	OFF	ON	OFF	ON
(Dual) Full	10 or 11	Active	1	1	OFF	ON	ON	OFF
(Dual) Full	10 or 11	Passive	1	1	OFF	ON	OFF	ON

9.4.1.3.5 Dither Bit (DITH)

The purpose of the dither mode is to increase the minimum length of output pulses without decreasing the PWM resolution, in order to limit the pulse distortion introduced by the slew rate control of the outputs. If dither mode is selected the output pattern will repeat after two timer counter overflows. For the same output frequency, the shortest output pulse will have twice the length while dither feature is selected. To achieve the same output frame frequency, the prescaler of the MC10B8C module has to be set to twice the division rate if dither mode is selected; e.g., with the same prescaler division rate the repeat rate of the output pattern is the same as well as the shortest output pulse with or without dither mode selected.

The DITH bit in control register 0 enables or disables the dither function.

DITH = 0: dither function is disabled.

When DITH is cleared and assuming left aligned operation and RECIRC = 0, the PWM output will start at a logic low level at the beginning of the PWM period (motor controller timer counter = 0x000). The PWM output remains low until the motor controller timer counter matches the 11-bit PWM duty cycle value, DUTY, contained in D[10:0] in MCDCx. When a match (output compare between motor controller timer counter and DUTY) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the contents of MCPER – 1). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level. This completes one PWM period. The PWM period repeats every P counts (as defined by the bits P[10:0] in the motor controller period register) of the motor controller timer counter. If DUTY >= P, the output will be static low. If DUTY = 0x0000, the output will be continuously at a logic high level. The relationship between the motor controller timer counter clock, motor controller timer counter value, and PWM output while DITH = 0 is shown in Figure 9-17.

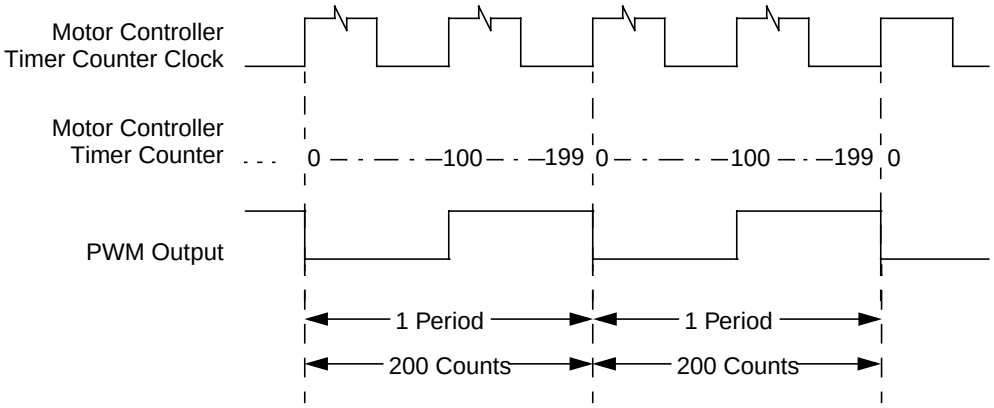


Figure 9-17. PWM Output: DITH = 0, MCAM[1:0] = 01, MCDC = 100, MCPER = 200, RECIRC = 0

DITH = 1: dither function is enabled

Please note if DITH = 1, the bit P0 in the motor controller period register will be internally forced to 0 and read always as 0.

When DITH is set and assuming left aligned operation and RECIRC = 0, the PWM output will start at a logic low level at the beginning of the PWM period (when the motor controller timer counter = 0x000). The PWM output remains low until the motor controller timer counter matches the 10-bit PWM duty cycle

value, DUTY, contained in D[10:1] in MCDCx. When a match (output compare between motor controller timer counter and DUTY) occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the value defined by P[10:1] – 1 in MCPER). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level. This completes the first half of the PWM period. During the second half of the PWM period, the PWM output will remain at a logic low level until either the motor controller timer counter matches the 10-bit PWM duty cycle value, DUTY, contained in D[10:1] in MCDCx if D0 = 0, or the motor controller timer counter matches the 10-bit PWM duty cycle value + 1 (the value of D[10:1] in MCDCx is increment by 1 and is compared with the motor controller timer counter value) if D0 = 1 in the corresponding duty cycle register. When a match occurs, the PWM output will toggle to a logic high level and will remain at a logic high level until the motor controller timer counter overflows (reaches the value defined by P[10:1] – 1 in MCPER). After the motor controller timer counter resets to 0x000, the PWM output will return to a logic low level.

This process will repeat every number of counts of the motor controller timer counter defined by the period register contents (P[10:0]). If the output is neither set to 0% nor to 100% there will be four edges on the PWM output per PWM period in this case. Therefore, the PWM output compare function will alternate between DUTY and DUTY + 1 every half PWM period if D0 in the corresponding duty cycle register is set to 1. The relationship between the motor controller timer counter clock (f_{TC}), motor controller timer counter value, and left aligned PWM output if DITH = 1 is shown in Figure 9-18 and Figure 9-19. Figure 9-20 and Figure 9-21 show right aligned and center aligned PWM operation respectively, with dither feature enabled and D0 = 1. Please note: In the following examples, the MCPER value is defined by the bits P[10:0], which is, if DITH = 1, always an even number.

NOTE

The DITH bit must be changed only if the motor controller is disabled (all channels disabled or period register cleared) to avoid erroneous waveforms.

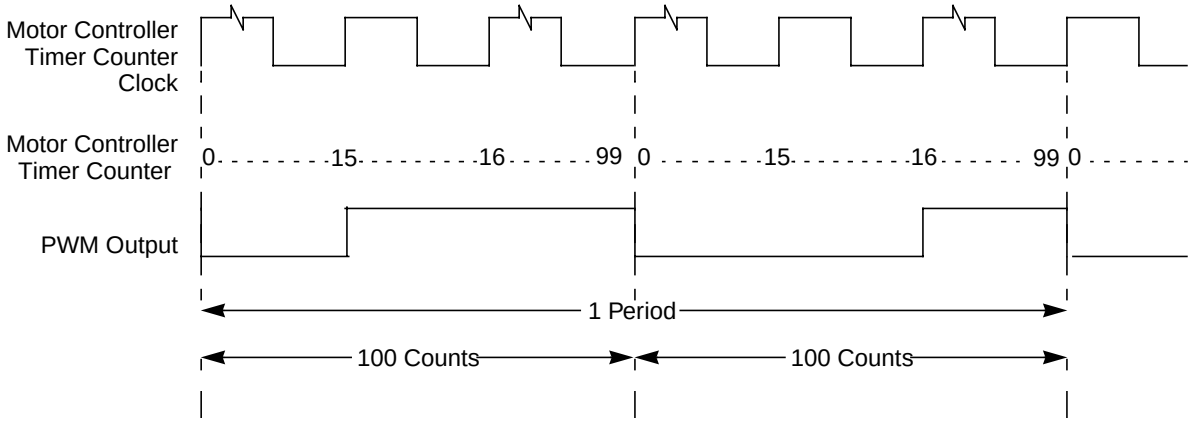


Figure 9-18. PWM Output: DITH = 1, MCAM[1:0] = 01, MCDC = 31, MCPER = 200, RECIRC = 0

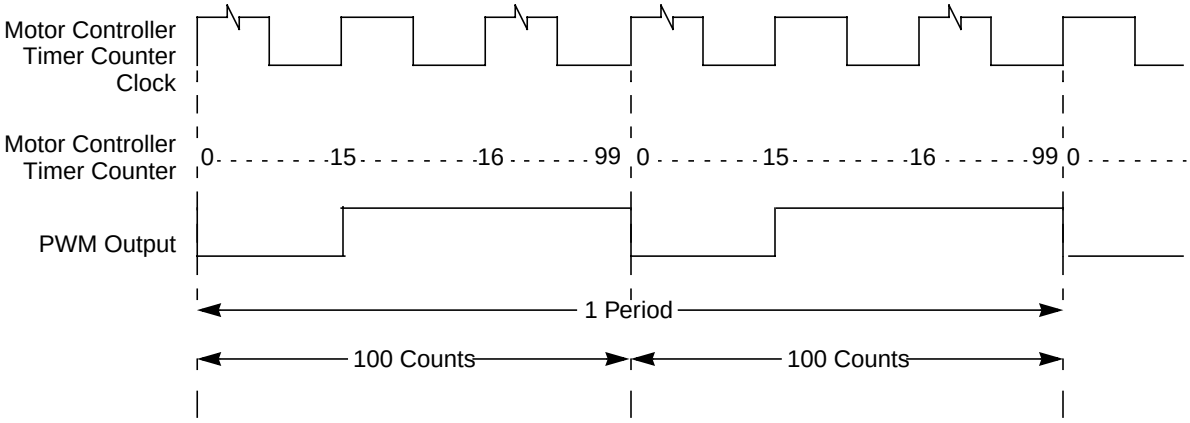


Figure 9-19. PWM Output: DITH = 1, MCAM[1:0] = 01, MCDC = 30, MCPER = 200, RECIRC = 0

.

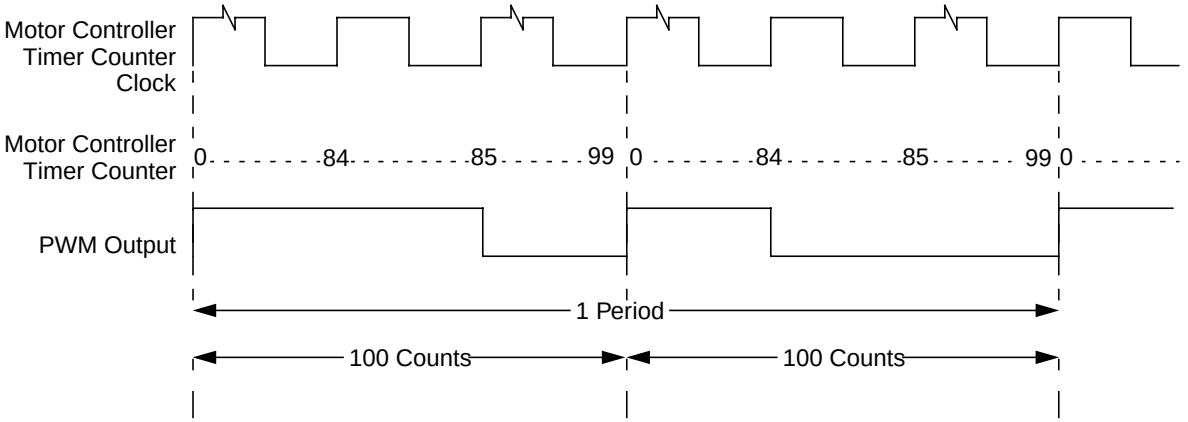


Figure 9-20. PWM Output: DITH = 1, MCAM[1:0] = 10, MCDC = 31, MCPER = 200, RECIRC = 0

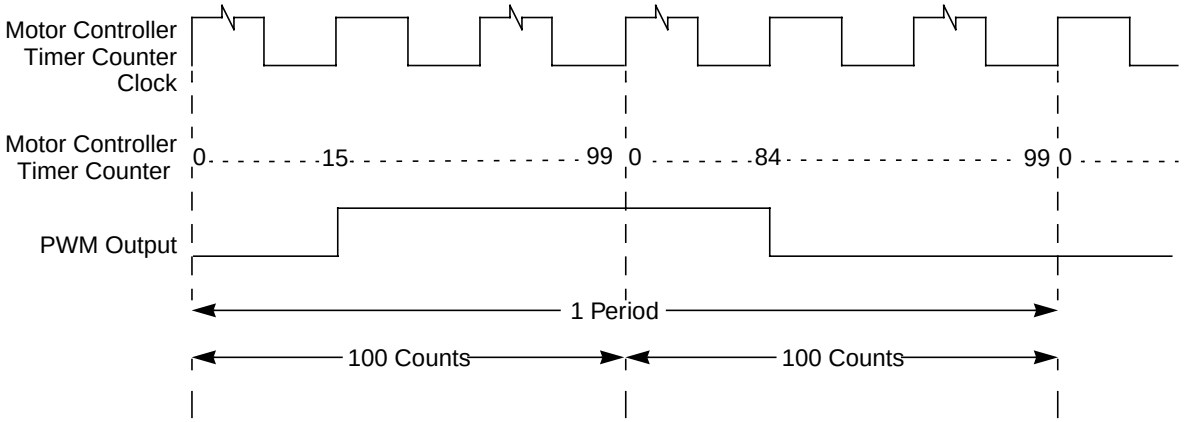


Figure 9-21. PWM Output: DITH = 1, MCAM[1:0] = 11, MCDC = 31, MCPER = 200, RECIRC = 0

9.4.2 PWM Duty Cycle

The PWM duty cycle for the motor controller channel x can be determined by dividing the decimal representation of bits D[10:0] in MCDCx by the decimal representation of the bits P[10:0] in MCPER and multiplying the result by 100% as shown in the equation below:

$$\text{Effective PWM Channel X \% Duty Cycle} = \frac{\text{DUTY}}{\text{MCPER}} \cdot 100\%$$

NOTE

x = PWM Channel Number = 0, 1, 2, 3 ... 8. This equation is only valid if DUTY <= MCPER and MCPER is not equal to 0.

Whenever D[10:0] >= P[10:0], a constant low level (RECIRC = 0) or high level (RECIRC = 1) will be output.

9.4.3 Motor Controller Counter Clock Source

Figure 9-22 shows how the PWM motor controller timer counter clock source is selected.

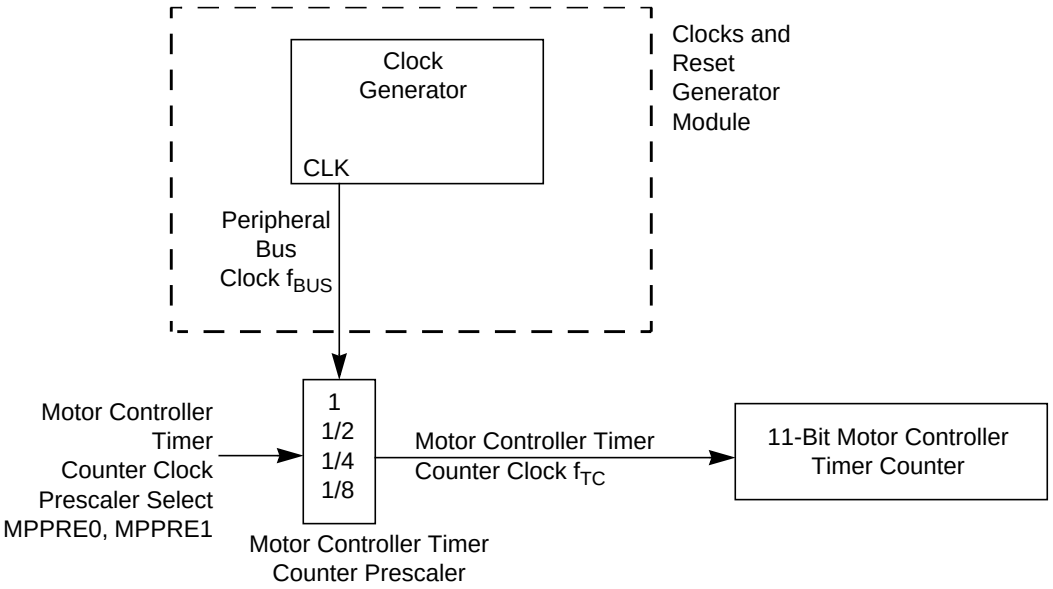


Figure 9-22. Motor Controller Counter Clock Selection

The peripheral bus clock is the source for the motor controller counter prescaler. The motor controller counter clock rate, f_{TC}, is set by selecting the appropriate prescaler value. The prescaler is selected with the MCPRE[1:0] bits in motor controller control register 0 (MCCTL0). The motor controller channel frequency of operation can be calculated using the following formula if DITH = 0:

$$\text{Motor Channel Frequency (Hz)} = \frac{f_{TC}}{\text{MCPER} \cdot \text{M}}$$

The motor controller channel frequency of operation can be calculated using the following formula if DITH = 1:

$$\text{Motor Channel Frequency (Hz)} = \frac{f_{TC}}{MCPER \cdot M/2}$$

NOTE

Both equations are only valid if MCPER is not equal to 0. M = 1 for left or right aligned mode, M = 2 for center aligned mode.

Table 9-13 shows examples of the motor controller channel frequencies that can be generated based on different peripheral bus clock frequencies and the prescaler value.

Table 9-13. Motor Controller Channel Frequencies (Hz), MCPER = 256, DITH = 0, MCAM = 10, 01

Prescaler	Peripheral Bus Clock Frequency				
	16 MHz	10 MHz	8 MHz	5 MHz	4 MHz
1	62500	39063	31250	19531	15625
1/2	31250	19531	15625	9766	7813
1/4	15625	9766	7813	4883	3906
1/8	7813	4883	3906	2441	1953

NOTE

Due to the selectable slew rate control of the outputs, clipping may occur on short output pulses.

9.4.4 Output Switching Delay

In order to prevent large peak current draw from the motor power supply, selectable delays can be used to stagger the high logic level to low logic level transitions on the motor controller outputs. The timing delay, t_d, is determined by the CD[1:0] bits in the corresponding channel control register (MCMCx) and is selectable between 0, 1, 2, or 3 motor controller timer counter clock cycles.

NOTE

A PWM channel gets disabled at the next timer counter overflow without notice of the switching delay.

9.4.5 Operation in Wait Mode

During wait mode, the operation of the motor controller pins are selectable between the following two options:

1. MCSWAI = 1: All module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the RECIRC bit during wait mode. The motor controller module registers stay the same as they were prior to entering wait mode. Therefore, after exiting from wait mode, the associated port pins will resume to the same functionality they had prior to entering wait mode.
2. MCSWAI = 0: The PWM clocks continue to run and the associated port pins maintain the functionality they had prior to entering wait mode both during wait mode and after exiting wait mode.

9.4.6 Operation in Stop and Pseudo-Stop Modes

All module clocks are stopped and the associated port pins are set to their inactive state, which is defined by the state of the RECIRC bit. The motor controller module registers stay the same as they were prior to entering stop or pseudo-stop modes. Therefore, after exiting from stop or pseudo-stop modes, the associated port pins will resume to the same functionality they had prior to entering stop or pseudo-stop modes.

9.5 Reset

The motor controller is reset by system reset. All associated ports are released, all registers of the motor controller module will switch to their reset state as defined in Section 9.3.2, “Register Descriptions”.

9.6 Interrupts

The motor controller has one interrupt source.

9.6.1 Timer Counter Overflow Interrupt

An interrupt will be requested when the MCTOIE bit in the motor controller control register 1 is set and the running PWM frame is finished. The interrupt is cleared by either setting the MCTOIE bit to 0 or to write a 1 to the MCTOIF bit in the motor controller control register 0.

9.7 Initialization/Application Information

This section provides an example of how the PWM motor controller can be initialized and used by application software. The configuration parameters (e.g., timer settings, duty cycle values, etc.) are not guaranteed to be adequate for any real application.

The example software is implemented in assembly language.

9.7.1 Code Example

One way to use the motor controller is:

1. Perform global initialization
   a) Set the motor controller control registers MCCTL0 and MCCTL1 to appropriate values.
      i) Prescaler disabled (MCPRE1 = 0, MCPRE0 = 0).
      ii) Fast mode and dither disabled (FAST = 0, DITH = 0).
      iii) Recirculation feature in dual full H-bridge mode disabled (RECIRC = 0).
      All other bits in MCCTL0 and MCCTL1 are set to 0.
   b) Configure the channel control registers for the desired mode.
      i) Dual full H-bridge mode (MCOM[1:0] = 11).
      ii) Left aligned PWM (MCAM[1:0] = 01).
      iii) No channel delay (MCCD[1:0] = 00).
2. Perform the startup phase
   a) Clear the duty cycle registers MCDC0 and MCDC1
   b) Initialize the period register MCPER, which is equivalent to enabling the motor controller.
   c) Enable the timer which generates the timebase for the updates of the duty cycle registers.
3. Main program
   a) Check if pin PB0 is set to “1” and execute the sub program if a timer interrupt is pending.
   b) Initiate the shutdown procedure if pin PB0 is set to “0”.
4. Sub program
   a) Update the duty cycle registers
      Load the duty cycle registers MCDC0 and MCDC1 with new values from the table and clear the timer interrupt flag.
      The sub program will initiate the shutdown procedure if pin PB0 is set to “0”.
   b) Shutdown procedure

The timer is disabled and the duty cycle registers are cleared to drive an inactive value on the PWM output as long as the motor controller is enabled. The period register is cleared after a certain time, which disables the motor controller. The table address is restored and the timer interrupt flag is cleared.

```
;-------------------------------------------------------------------------------------------
; Motor Controller (MC10B8C) setup example
;-------------------------------------------------------------------------------------------
; Timer defines
;-------------------------------------------------------------------------------------------
T_START                 EQU  $0040
TSCR1                   EQU  T_START+$06
TFLG2                   EQU  T_START+$0F
;-------------------------------------------------------------------------------------------
; Motor Controller defines
;-------------------------------------------------------------------------------------------
MC_START                EQU  $0200
MCCTL0                  EQU  MC_START+$00
MCCTL1                  EQU  MC_START+$01
MCPER_HI                EQU  MC_START+$02
MCPER_LO                EQU  MC_START+$03
MCCC0                   EQU  MC_START+$10
MCCC1                   EQU  MC_START+$11
MCCC2                   EQU  MC_START+$12
MCCC3                   EQU  MC_START+$13
MCDC0_HI                EQU  MC_START+$20
MCDC0_LO                EQU  MC_START+$21
MCDC1_HI                EQU  MC_START+$22
MCDC1_LO                EQU  MC_START+$23
MCDC2_HI                EQU  MC_START+$24
MCDC2_LO                EQU  MC_START+$25
MCDC3_HI                EQU  MC_START+$26
MCDC3_LO                EQU  MC_START+$27
;-------------------------------------------------------------------------------------------
; Port defines
;-------------------------------------------------------------------------------------------
DDRB                    EQU  $0003
PORTB                   EQU  $0001
;-------------------------------------------------------------------------------------------
; Flash defines
;-------------------------------------------------------------------------------------------
FLASH_START             EQU  $0100
FCMD                    EQU  FLASH_START+$06
FCLKDIV                 EQU  FLASH_START+$00
FSTAT                   EQU  FLASH_START+$05
FTSTMOD                 EQU  FLASH_START+$02
; Variables
CODE_START              EQU  $1000          ; start of program code
DTYDAT                  EQU  $1500          ; start of motor controller duty cycle data
TEMP_X                  EQU  $1700          ; save location for IX reg in ISR
TABLESIZE               EQU  $1704          ; number of config entries in the table
MCPERIOD                EQU  $0250          ; motor controller period
;-------------------------------------------------------------------------------------------
;-------------------------------------------------------------------------------------------
        ORG        CODE_START               ; start of code
          LDS     #$1FFF                    ; set stack pointer
          MOVW    #$000A,TABLESIZE          ; number of configurations in the table
          MOVW    TABLESIZE,TEMP_X
```

```
;-------------------------------------------------------------------------------------
;global motor controller init
;-------------------------------------------------------------------------------------
GLB_INIT: MOVB    #$0000,MCCTL0             ; fMC = fBUS, FAST=0, DITH=0
          MOVB    #$0000,MCCTL1             ; RECIRC=0, MCTOIE=0
          MOVW    #$D0D0,MCCC0              ; dual full h-bridge mode, left aligned,
                                            ; no channel delay
          MOVW    #$0000,MCPER_HI           ; disable motor controller
;-------------------------------------------------------------------------------------
;motor controller startup
;-------------------------------------------------------------------------------------
STARTUP:
          MOVW    #$0000,MCDC0_HI           ; define startup duty cycles
          MOVW    #$0000,MCDC1_HI
          MOVW    #MCPERIOD,MCPER_HI        ; define PWM period
          MOVB    #$80,TSCR1                ; enable timer
MAIN:     LDAA    PORTB                     ; if PB=0, activate shutdown
          ANDA    #$01
          BEQ     MN0
          JSR     TIM_SR
MN0:      TST     TFLG2                     ; poll for timer counter overflow flag
          BEQ     MAIN                      ; TOF set?
          JSR     TIM_SR                    ; yes, go to TIM_SR
          BRA     MAIN
TIM_SR:   LDX     TEMP_X                    ; restore index register X
          LDAA    PORTB                     ; if PB=0, enter shutdown routine
          ANDA    #$01
          BNE     SHUTDOWN
          LDX     TEMP_X                    ; restore index register X
          BEQ     NEW_SEQ                   ; all mc configurations done?
NEW_CFG:  LDD     DTYDAT,X                  ; load new config's
          STD     MCDC0_HI
          DEX
          DEX
          LDD     DTYDAT,X
          STD     MCDC1_HI
          BRA     END_SR                    ; leave sub-routine
SHUTDOWN: MOVB    #$00,TSCR1                ; disable timer
          MOVW    #$0000,MCDC0_HI           ; define startup duty cycle
          MOVW    #$0000,MCDC1_HI           ; define startup duty cycle
          LDAA    #$0000                    ; ensure that duty cycle registers are
                                            ; cleared for some time before disabling
                                            ; the motor controller
LOOP      DECA
          BNE     LOOP
          MOVW    #$0000,MCPER_HI           ; define pwm period
NEW_SEQ:  MOVW    TABLESIZE,TEMP_X          ; start new tx loop
          LDX     TEMP_X
END_SR:   STX     TEMP_X                    ; save byte counter
          MOVB    #$80,TFLG2                ; clear TOF
          RTS                               ; wait for new timer overflow
```

```
;-------------------------------------------------------------------------------------------
; motor controller duty cycles
;-------------------------------------------------------------------------------------------
        org     DTYDAT
          DC.B    $02, $FF[1]; MCDC1_HI, MCDC1_LO
          DC.B    $02, $D0 ; MCDC0_HI, MCDC0_LO
          DC.B    $02, $A0 ; MCDC1_HI, MCDC1_LO
          DC.B    $02, $90 ; MCDC0_HI, MCDC0_LO
          DC.B    $02, $60 ; MCDC1_HI, MCDC1_LO
          DC.B    $02, $25 ; MCDC0_HI, MCDC0_LO
```

1. The values for the duty cycle table have to be defined for the needs of the target application.

Chapter 10
Stepper Stall Detector (SSDV1)

10.1 Introduction

The stepper stall detector (SSD) block provides a circuit to measure and integrate the induced voltage on the non-driven coil of a stepper motor using full steps when the gauge pointer is returning to zero (RTZ). During the RTZ event, the pointer is returned to zero using full steps in either clockwise or counter clockwise direction, where only one coil is driven at any point in time. The back electromotive force (EMF) signal present on the non-driven coil is integrated after a blanking time, and its results stored in a 16-bit accumulator. The 16-bit modulus down counter can be used to monitor the blanking time and the integration time. The value in the accumulator represents the change in linked flux (magnetic flux times the number of turns in the coil) and can be compared to a stored threshold. Values above the threshold indicate a moving motor, in which case the pointer can be advanced another full step in the same direction and integration be repeated. Values below the threshold indicate a stalled motor, thereby marking the cessation of the RTZ event. The SSD is capable of multiplexing two stepper motors.

10.1.1 Modes of Operation

- Return to zero modes
  - Blanking with no drive
  - Blanking with drive
  - Conversion
  - Integration
- Low-power modes

10.1.2 Features

- Programmable full step state
- Programmable integration polarity
- Blanking (recirculation) state
- 16-bit integration accumulator register
- 16-bit modulus down counter with interrupt
- Multiplex two stepper motors

10.1.3 Block Diagram

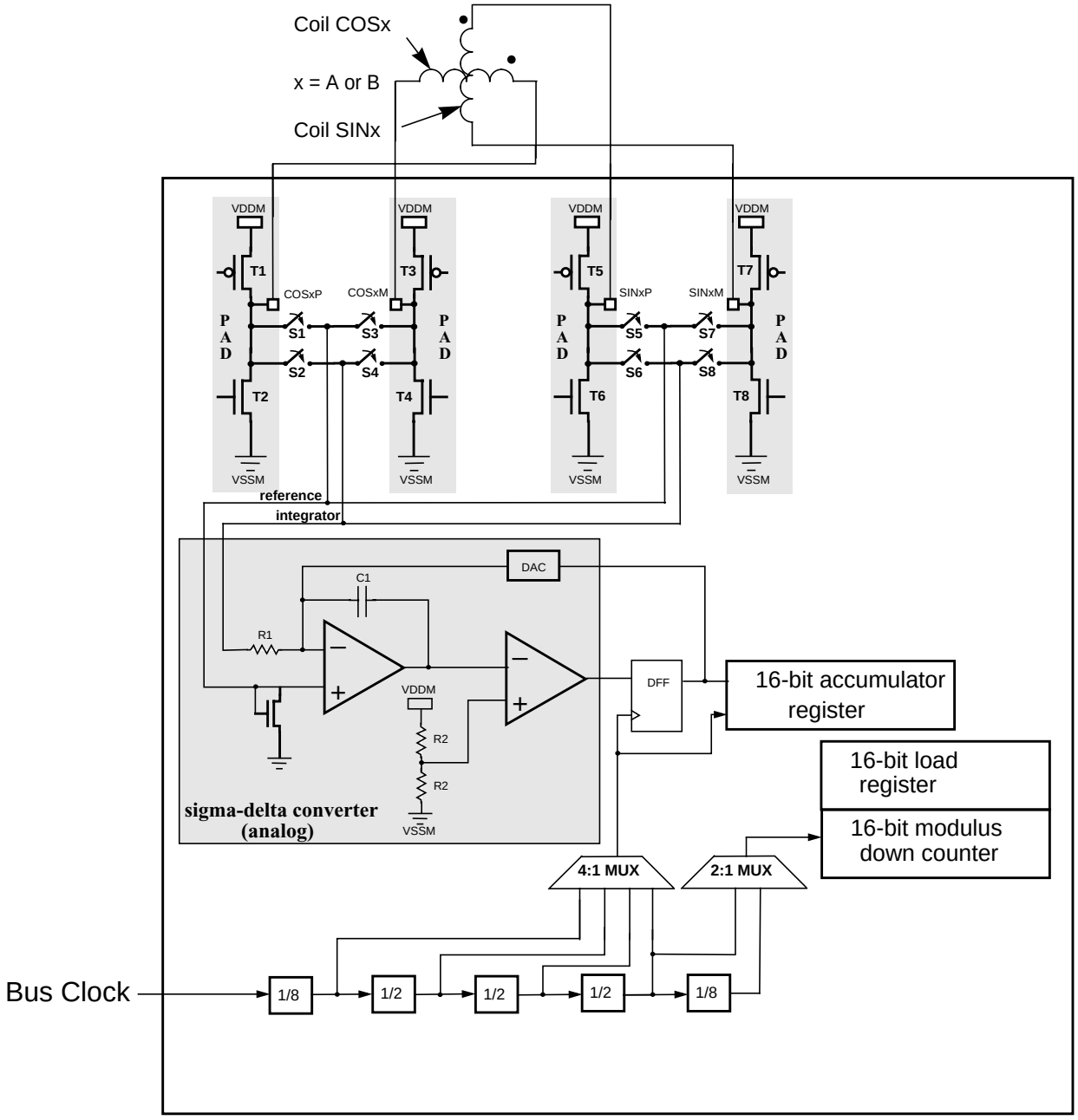


Figure 10-1. SSD Block Diagram

10.2 External Signal Description

Each SSD signal is the output pin of a half bridge, designed to source or sink current. The H-bridge pins drive the sine and cosine coils of a stepper motor to provide four-quadrant operation. The SSD is capable of multiplexing between stepper motor A and stepper motor B if two motors are connected.

Table 10-1. Pin Table[1]

Pin Name	Node	Coil
COSxM	Minus	COSx
COSxP	Plus	
SINxM	Minus	SINx
SINxP	Plus	

[1] x = A or B indicating motor A or motor B

10.2.1 COSxM/COSxP — Cosine Coil Pins for Motor x

These pins interface to the cosine coils of a stepper motor to measure the back EMF for calibration of the pointer reset position.

10.2.2 SINxM/SINxP — Sine Coil Pins for Motor x

These pins interface to the sine coils of a stepper motor to measure the back EMF for calibration of the pointer reset position.

10.3 Memory Map and Register Definition

This section provides a detailed description of all registers of the stepper stall detector (SSD) block.

10.3.1 Module Memory Map

Table 10-2 gives an overview of all registers in the SSD memory map. The SSD occupies eight bytes in the memory space. The register address results from the addition of *base address* and *address offset.* The *base address* is determined at the MCU level and is given in the Device Overview chapter. The *address offset* is defined at the block level and is given here.

Table 10-2. SSD Memory Map

Address Offset	Use	Access
0x0000	RTZCTL	R/W
0x0001	MDCCTL	R/W
0x0002	SSDCTL	R/W
0x0003	SSDFLG	R/W
0x0004	MDCCNT (High)	R/W
0x0005	MDCCNT (Low)	R/W
0x0006	ITGACC (High)	R
0x0007	ITGACC (Low)	R

10.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the SSD block. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

10.3.2.1 Return-to-Zero Control Register (RTZCTL)

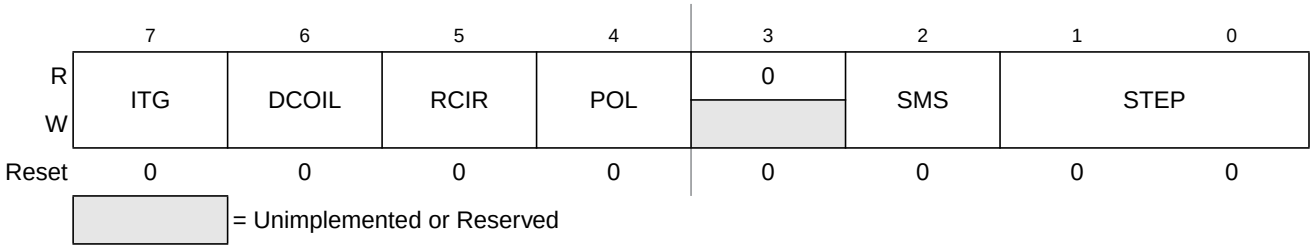


Figure 10-2. Return-to-Zero Control Register (RTZCTL)

Read: anytime

Write: anytime

Table 10-3. RTZCTL Field Descriptions

Field	Description
7 ITG	**Integration** — During return to zero (RTZE = 1), one of the coils must be recirculated or non-driven determined by the STEP field. If the ITG bit is set, the coil is non-driven, and if the ITG bit is clear, the coil is being recirculated. Table 10-4 shows the condition state of each transistor from Figure 10-1 based on the STEP, ITG, DCOIL and RCIR bits. Regardless of the RTZE bit value, if the ITG bit is set, one end of the non-driven coil connects to the (non-zero) reference input and the other end connects to the integrator input of the sigma-delta converter. Regardless of the RTZE bit value, if the ITG bit is clear, the non-driven coil is in a blanking state, the converter is in a reset state, and the accumulator is initialized to zero. Table 10-5 shows the condition state of each switch from Figure 10-1 based on the ITG, STEP and POL bits. 0 Blanking 1 Integration
6 DCOIL	**Drive Coil** — During return to zero (RTZE=1), one of the coils must be driven determined by the STEP field. If the DCOIL bit is set, this coil is driven. If the DCOIL bit is clear, this coil is disconnected or drivers turned off. Table 10-4 shows the condition state of each transistor from Figure 10-1 based on the STEP, ITG, DCOIL and RCIR bits. 0 Disconnect Coil 1 Drive Coil
5 RCIR	**Recirculation in Blanking Mode** — During return to zero (RTZE = 1), one of the coils is recirculated prior to integration during the blanking period. This bit determines if the coil is recirculated via VDDM or via VSSM. Table 10-4 shows the condition state of each transistor from Figure 10-1 based on the STEP, ITG, DCOIL and RCIR bits. 0 Recirculation on the high side transistors 1 Recirculation on the low side transistors
4 POL	**Polarity** — This bit determines which end of the non-driven coil is routed to the sigma-delta converter during conversion or integration mode. Table 10-5 shows the condition state of each switch from Figure 10-1 based on the ITG, STEP and POL bits.
2 SMS	**Stepper Motor Select** — This bit selects one of two possible stepper motors to be used for stall detection. See top level chip description for the stepper motor assignments to the SSD. 0 Stepper Motor A is selected for stall detection 1 Stepper Motor B is selected for stall detection
1:0 STEP	**Full Step State** — This field indicates one of the four possible full step states. Step 0 is considered the east pole or 0° angle, step 1 is the north Pole or 90° angle, step 2 is the west pole or 180° angle, and step 3 is the south pole or 270° angle. For each full step state, Table 10-6 shows the current through each of the two coils, and the coil nodes that are multiplexed to the sigma-delta converter during conversion or integration mode.

Table 10-4. Transistor Condition States (RTZE = 1)

STEP	ITG	DCOIL	RCIR	T1	T2	T3	T4	T5	T6	T7	T8
xx	1	0	x	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
00	0	0	0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
00	0	0	1	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
00	0	1	0	ON	OFF	OFF	ON	ON	OFF	ON	OFF
00	0	1	1	ON	OFF	OFF	ON	OFF	ON	OFF	ON
00	1	1	x	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF
01	0	0	0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
01	0	0	1	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
01	0	1	0	ON	OFF	ON	OFF	ON	OFF	OFF	ON
01	0	1	1	OFF	ON	OFF	ON	ON	OFF	OFF	ON
01	1	1	x	OFF	OFF	OFF	OFF	ON	OFF	OFF	ON
10	0	0	0	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF
10	0	0	1	OFF	OFF	OFF	OFF	OFF	ON	OFF	ON
10	0	1	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF
10	0	1	1	OFF	ON	ON	OFF	OFF	ON	OFF	ON
10	1	1	x	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF
11	0	0	0	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF
11	0	0	1	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF
11	0	1	0	ON	OFF	ON	OFF	OFF	ON	ON	OFF
11	0	1	1	OFF	ON	OFF	ON	OFF	ON	ON	OFF
11	1	1	x	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF

Table 10-5. Switch Condition States (RTZE = 1 or 0)

ITG	STEP	POL	S1	S2	S3	S4	S5	S6	S7	S8
0	xx	x	Open	Open	Open	Open	Open	Open	Open	Open
1	00	0	Open	Open	Open	Open	Close	Open	Open	Close
1	00	1	Open	Open	Open	Open	Open	Close	Close	Open
1	01	0	Open	Close	Close	Open	Open	Open	Open	Open
1	01	1	Close	Open	Open	Close	Open	Open	Open	Open
1	10	0	Open	Open	Open	Open	Open	Close	Close	Open
1	10	1	Open	Open	Open	Open	Close	Open	Open	Close
1	11	0	Close	Open	Open	Close	Open	Open	Open	Open
1	11	1	Open	Close	Close	Open	Open	Open	Open	Open

Table 10-6. Full Step States

STEP	Pole	Angle	COSINE Coil Current		SINE Coil Current		Coil Node to Integrator input (Close Switch)		Coil Node to Reference input (Close Switch)	
			DCOIL = 0	DCOIL = 1	DCOIL = 0	DCOIL = 1	ITG = 1 POL = 0	ITG = 1 POL = 1	ITG = 1 POL = 0	ITG = 1 POL = 1
0	East	0°	0	+ I max	0	0	SINxM (S8)	SINxP (S6)	SINxP (S5)	SINxM (S7)
1	North	90°	0	0	0	+ I max	COSxP (S2)	COSxM (S4)	COSxM (S3)	COSxP (S1)
2	West	180°	0	– I max	0	0	SINxP (S6)	SINxM (S8)	SINxM (S7)	SINxP (S5)
3	South	270°	0	0	0	– I max	COSxM (S4)	COSxP (S2)	COSxP (S1)	COSxM (S3)

10.3.2.2 Modulus Down Counter Control Register (MDCCTL)

	7	6	5	4	3	2	1	0
R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
W					FLMC			
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-3. Modulus Down Counter Control Register (MDCCTL)

Read: anytime

Write: anytime.

Table 10-7. MDCCTL Field Descriptions

Field	Description
7 MCZIE	**Modulus Counter Underflow Interrupt Enable** 0 Interrupt disabled. 1 Interrupt enabled. An interrupt will be generated when the modulus counter underflow interrupt flag (MCZIF) is set.
6 MODMC	**Modulus Mode Enable** 0 The modulus counter counts down from the value in the counter register and will stop at 0x0000. 1 Modulus mode is enabled. When the counter reaches 0x0000, the counter is loaded with the latest value written to the modulus counter register. **Note:** For proper operation, the MCEN bit should be cleared before modifying the MODMC bit in order to reset the modulus counter to 0xFFFF.
5 RDMCL	**Read Modulus Down-Counter Load** 0 Reads of the modulus count register (MDCCNT) will return the present value of the count register. 1 Reads of the modulus count register (MDCCNT) will return the contents of the load register.
4 PRE	**Prescaler** 0 The modulus down counter clock frequency is the bus frequency divided by 64. 1 The modulus down counter clock frequency is the bus frequency divided by 512. **Note:** A change in the prescaler division rate will not be effective until a load of the load register into the modulus counter count register occurs.

Table 10-7. MDCCTL Field Descriptions (continued)

Field	Description
3 FLMC	**Force Load Register into the Modulus Counter Count Register** — This bit always reads zero. 0 Write zero to this bit has no effect. 1 Write one into this bit loads the load register into the modulus counter count register.
2 MCEN	**Modulus Down-Counter Enable** 0 Modulus down-counter is disabled. The modulus counter (MDCCNT) is preset to 0xFFFF. This will prevent an early interrupt flag when the modulus down-counter is enabled. 1 Modulus down-counter is enabled.
0 AOVIE	**Accumulator Overflow Interrupt Enable** 0 Interrupt disabled. 1 Interrupt enabled. An interrupt will be generated when the accumulator overflow interrupt flag (AOVIF) is set.

10.3.2.3 Stepper Stall Detector Control Register (SSDCTL)

	7	6	5	4	3	2	1	0
R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-4. Stepper Stall Detector Control Register (SSDCTL)

Read: anytime

Write: anytime

Table 10-8. SSDCTL Field Descriptions

Field	Description
7 RTZE	**Return to Zero Enable** — If this bit is set, the coils are controlled by the SSD and are configured into one of the four full step states as shown in Table 10-6. If this bit is cleared, the coils are not controlled by the SSD. 0 RTZ is disabled. 1 RTZ is enabled.
6 SDCPU	**Sigma-Delta Converter Power Up** — This bit provides on/off control for the sigma-delta converter allowing reduced MCU power consumption. Because the analog circuit is turned off when powered down, the sigma-delta converter requires a recovery time after it is powered up. 0 Sigma-delta converter is powered down. 1 Sigma-delta converter is powered up.
5 SSDWAI	**SSD Disabled during Wait Mode** — When entering Wait Mode, this bit provides on/off control over the SSD allowing reduced MCU power consumption. Because the analog circuit is turned off when powered down, the sigma-delta converter requires a recovery time after exit from Wait Mode. 0 SSD continues to run in WAIT mode. 1 Entering WAIT mode freezes the clock to the prescaler divider, powers down the sigma-delta converter, and if RTZE bit is set, the sine and cosine coils are recirculated via VSSM.

Table 10-8. SSDCTL Field Descriptions (continued)

Field	Description
4 FTST	**Factory Test** — This bit is reserved for factory test and reads zero in user mode.
1:0 ACLKS	**Accumulator Sample Frequency Select** — This field sets the accumulator sample frequency by pre-scaling the bus frequency by a factor of 8, 16, 32, or 64. A faster sample frequency can provide more accurate results but cause the accumulator to overflow. Best results are achieved with a frequency between 500 kHz and 2 MHz. Accumulator Sample Frequency = f_{BUS} / (8 x 2^{ACLKS})

Table 10-9. Accumulator Sample Frequency

ACLKS	Frequency	f_{BUS} = 40 MHz	f_{BUS} = 25 MHz	f_{BUS} = 16 MHz
0	f_{BUS} / 8	5.00 MHz	3.12 MHz	2.00 MHz
1	f_{BUS} / 16	2.50 MHz	1.56 MHz	1.00 MHz
2	f_{BUS} / 32	1.25 MHz	781 kHz	500 kHz
3	f_{BUS} / 64	625 kHz	391 kHz	250 kHz

NOTE

A change in the accumulator sample frequency will not be effective until the ITG bit is cleared.

10.3.2.4 Stepper Stall Detector Flag Register (SSDFLG)

	7	6	5	4	3	2	1	0
R	MCZIF	0	0	0	0	0	0	AOVIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 10-5. Stepper Stall Detector Flag Register (SSDFLG)

Read: anytime

Write: anytime.

Table 10-10. SSDFLG Field Descriptions

Field	Description
7 MCZIF	**Modulus Counter Underflow Interrupt Flag** — This flag is set when the modulus down-counter reaches 0x0000. If not masked (MCZIE = 1), a modulus counter underflow interrupt is pending while this flag is set. This flag is cleared by writing a ‘1’ to the bit. A write of ‘0’ has no effect.
0 AOVIF	**Accumulator Overflow Interrupt Flag** — This flag is set when the Integration Accumulator has a positive or negative overflow. If not masked (AOVIE = 1), an accumulator overflow interrupt is pending while this flag is set. This flag is cleared by writing a ‘1’ to the bit. A write of ‘0’ has no effect.

10.3.2.5 Modulus Down-Counter Count Register (MDCCNT)

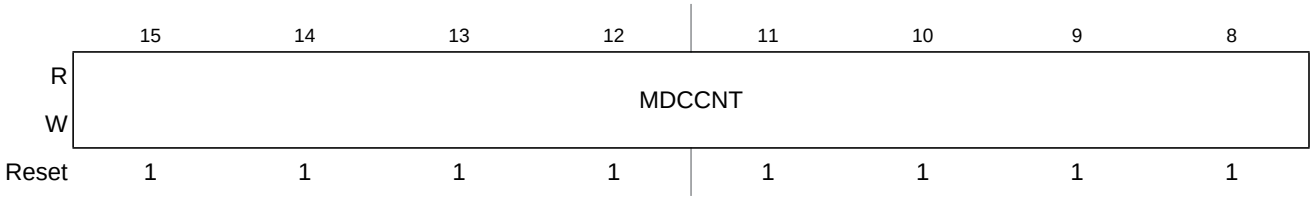


Figure 10-6. Modulus Down-Counter Count Register High (MDCCNT)

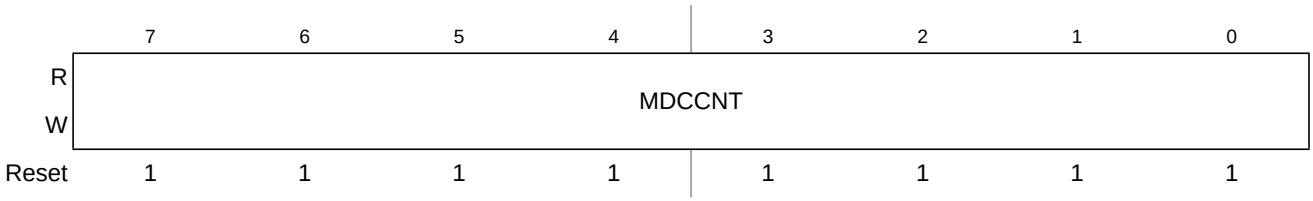


Figure 10-7. Modulus Down-Counter Count Register Low (MDCCNT)

Read: anytime

Write: anytime.

NOTE

A separate read/write for high byte and low byte gives a different result than accessing the register as a word.

If the RDMCL bit in the MDCCTL register is cleared, reads of the MDCCNT register will return the present value of the count register. If the RDMCL bit is set, reads of the MDCCNT register will return the contents of the load register.

With a 0x0000 write to the MDCCNT register, the modulus counter stays at zero and does not set the MCZIF flag in the SSDFLG register.

If modulus mode is not enabled (MODMC = 0), a write to the MDCCNT register immediately updates the load register and the counter register with the value written to it. The modulus counter will count down from this value and will stop at 0x0000.

If modulus mode is enabled (MODMC = 1), a write to the MDCCNT register updates the load register with the value written to it. The count register will not be updated with the new value until the next counter underflow. The FLMC bit in the MDCCTL register can be used to immediately update the count register with the new value if an immediate load is desired.

The modulus down counter clock frequency is the bus frequency divided by 64 or 512.

10.3.2.6 Integration Accumulator Register (ITGACC)

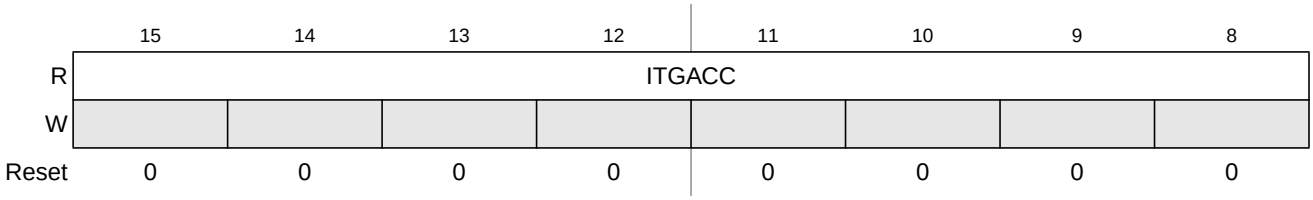


Figure 10-8. Integration Accumulator Register High (ITGACC)

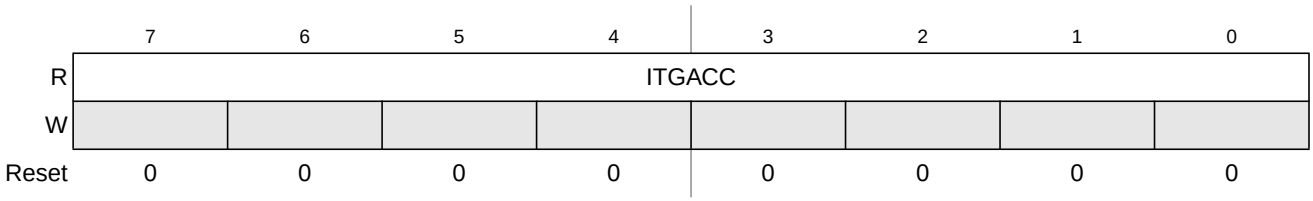


Figure 10-9. Integration Accumulator Register Low (ITGACC)

Read: anytime.

Write: Never.

NOTE

A separate read for high byte and low byte gives a different result than accessing the register as a word.

This 16-bit field is signed and is represented in two's complement. It indicates the change in flux while integrating the back EMF present in the non-driven coil during a return to zero event.

When ITG is zero, the accumulator is initialized to 0x0000 and the sigma-delta converter is in a reset state.

When ITG is one, the accumulator increments or decrements depending on the sigma-delta conversion sample. The accumulator sample frequency is determined by the ACLKS field. The accumulator freezes at 0x7FFF on a positive overflow and freezes at 0x8000 on a negative overflow.

10.4 Functional Description

The stepper stall detector (SSD) has a simple control block to configure the H-bridge drivers of a stepper motor in four different full step states with four available modes during a return to zero event. The SSD has a detect circuit using a sigma-delta converter to measure and integrate changes in flux of the de-energized winding in the stepping motor and the conversion result is accumulated in a 16-bit signed register. The SSD also has a 16-bit modulus down counter to monitor blanking and integration times. DC offset compensation is implemented when using the modulus down counter to monitor integration times.

10.4.1 Return to Zero Modes

There are four return to zero modes as shown in Table 10-11.

Table 10-11. Return to Zero Modes

ITG	DCOIL	Mode

Table 10-11. Return to Zero Modes

0	0	Blanking with no drive
0	1	Blanking with drive
1	0	Conversion
1	1	Integration

10.4.1.1 Blanking with No Drive

In blanking mode with no drive, one of the coils is masked from the sigma-delta converter, and if RTZ is enabled (RTZE = 1), it is set up to recirculate its current. If RTZ is enabled (RTZE = 1), the other coil is disconnected to prevent any loss of flux change that would occur when the motor starts moving before the end of recirculation and start of integration. In blanking mode with no drive, the accumulator is initialized to 0x0000 and the converter is in a reset state.

10.4.1.2 Blanking with Drive

In blanking mode with drive, one of the coils is masked from the sigma-delta converter, and if RTZ is enabled (RTZE = 1), it is set up to recirculate its current. If RTZ is enabled (RTZE = 1), the other coil is driven. In blanking mode with drive, the accumulator is initialized to 0x0000 and the converter is in a reset state.

10.4.1.3 Conversion

In conversion mode, one of the coils is routed for integration with one end connected to the (non-zero) reference input and the other end connected to the integrator input of the sigma-delta converter. If RTZ is enabled (RTZE=1), both coils are disconnected. This mode is not useful for stall detection.

10.4.1.4 Integration

In integration mode, one of the coils is routed for integration with one end connected to the (non-zero) reference input and the other end connected to the integrator input of the sigma-delta converter. If RTZ is enabled (RTZE = 1), the other coil is driven. This mode is used to rectify and integrate the back EMF produced by the coils to detect stepped rotary motion.

DC offset compensation is implemented when using the modulus down counter to monitor integration time.

10.4.2 Full Step States

During a return to zero (RTZ) event, the stepper motor pointer requires a 90° full motor electrical step with full amplitude pulses applied to each phase in turn. For counter clockwise rotation (CCW), the STEP value is incremented 0, 1, 2, 3, 0 and so on, and for a clockwise rotation the STEP value is decremented 3, 2, 1, 0 and so on. Figure 10-10 shows the current level through each coil for each full step in CCW rotation when DCOIL is set.

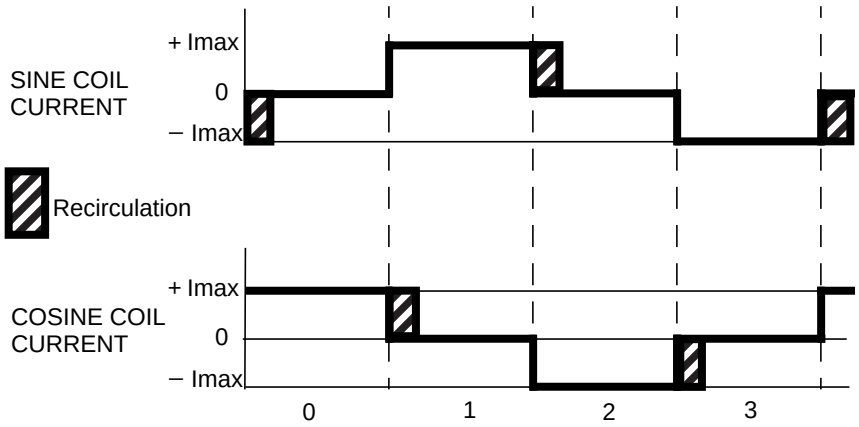


Figure 10-10. Full Steps (CCW)

Figure 10-11 shows the current flow in the SINx and COSx H-bridges when STEP = 0, DCOIL = 1, ITG = 0 and RCIR = 0.

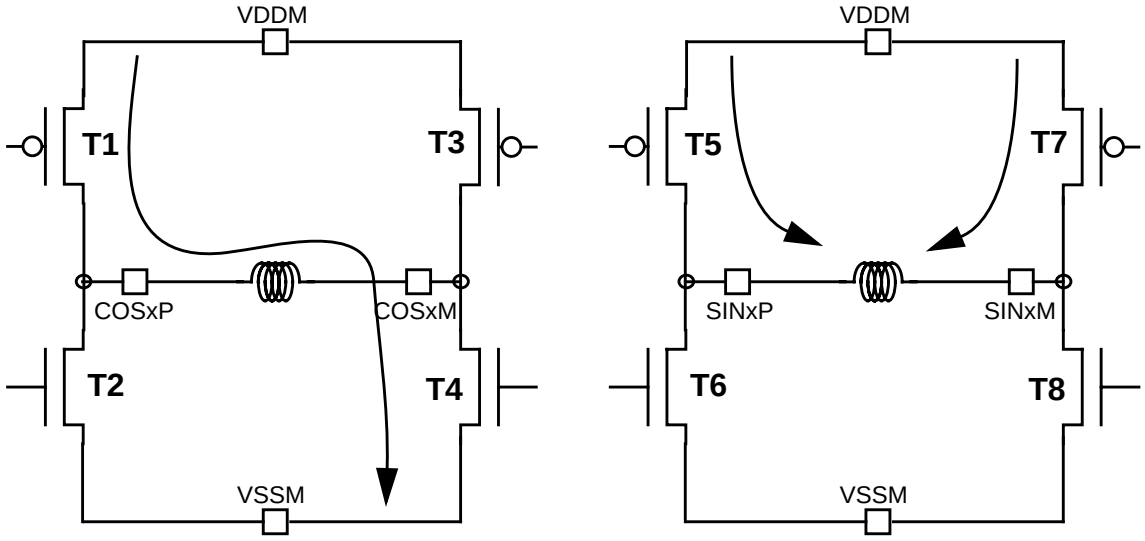


Figure 10-11. Current Flow when STEP = 0, DCOIL = 1, ITG = 0, RCIR = 0

Figure 10-12 shows the current flow in the SINx and COSx H-bridges when STEP = 1, DCOIL = 1, ITG = 0 and RCIR = 1.

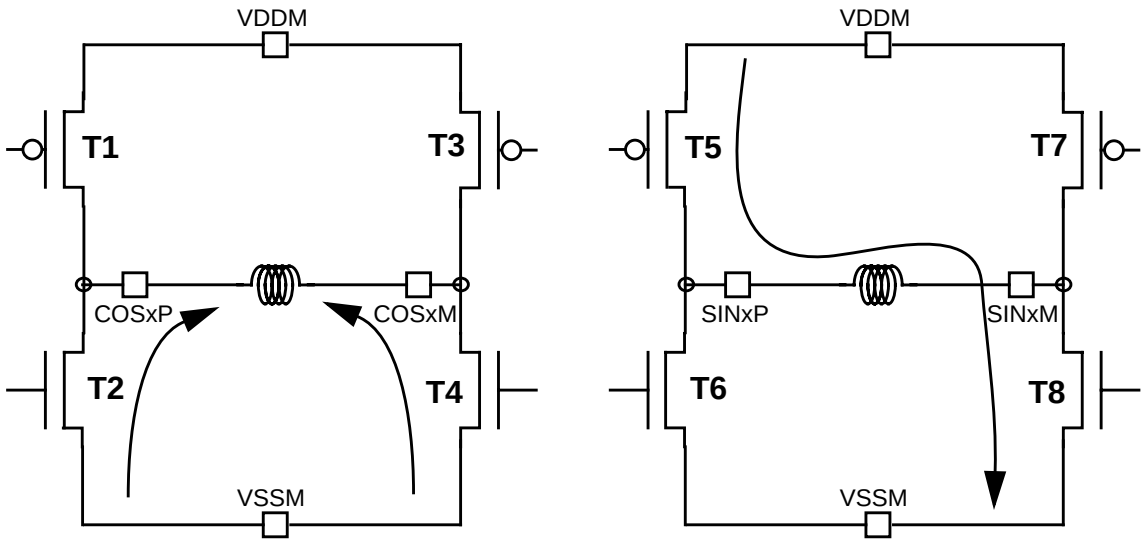


Figure 10-12. Current Flow when STEP = 1, DCOIL = 1, ITG = 0, RCIR = 1

Figure 10-13 shows the current flow in the SINx and COSx H-bridges when STEP = 2, DCOIL = 1 and ITG = 1.

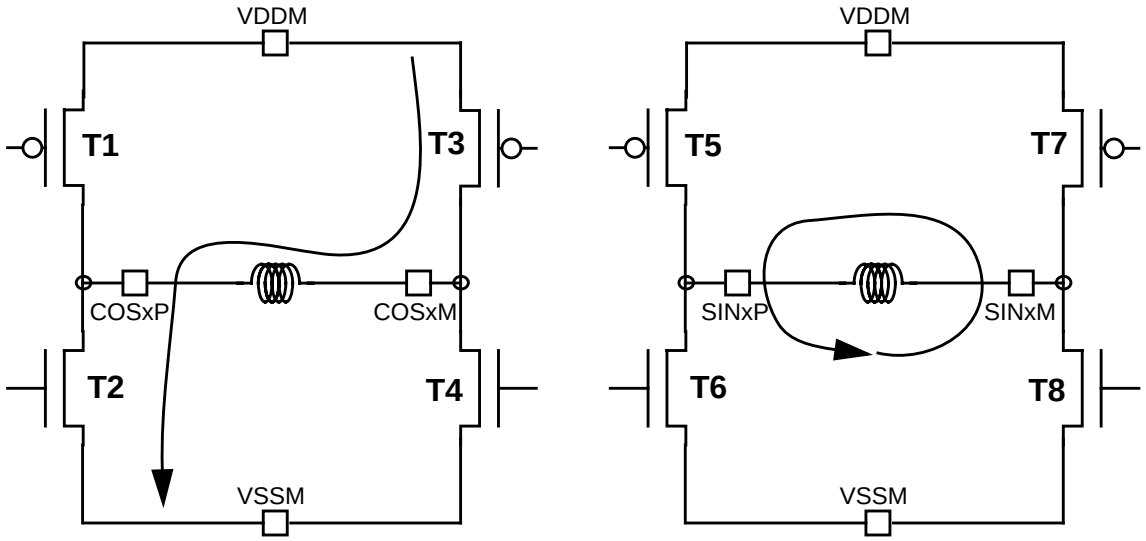


Figure 10-13. Current flow when STEP = 2, DCOIL = 1, ITG = 1

Figure 10-14 shows the current flow in the SINx and COSx H-bridges when STEP = 3, DCOIL = 1 and ITG = 1.

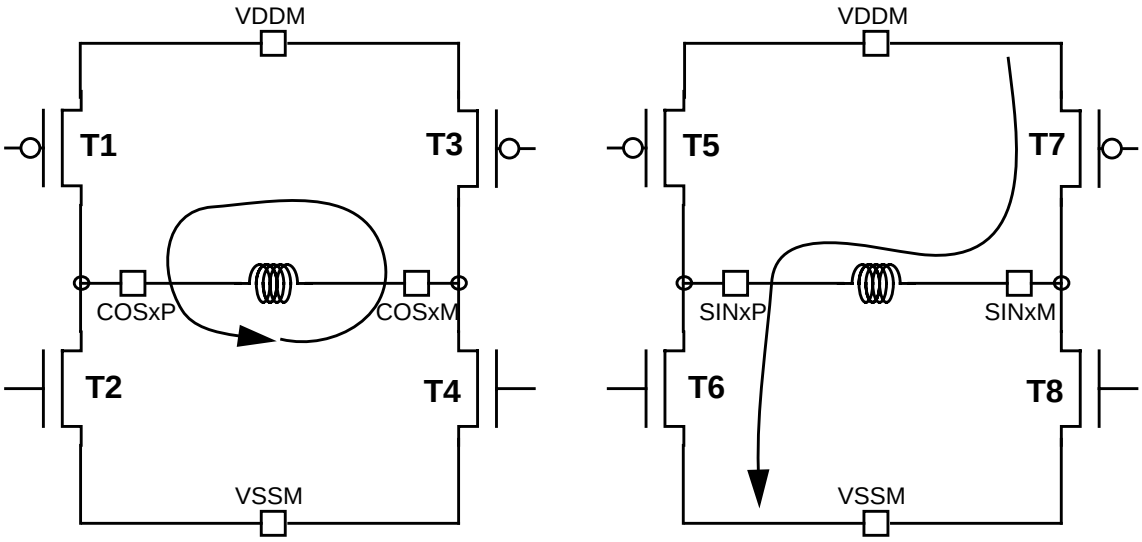


Figure 10-14. Current flow when STEP = 3, DCOIL = 1, ITG = 1

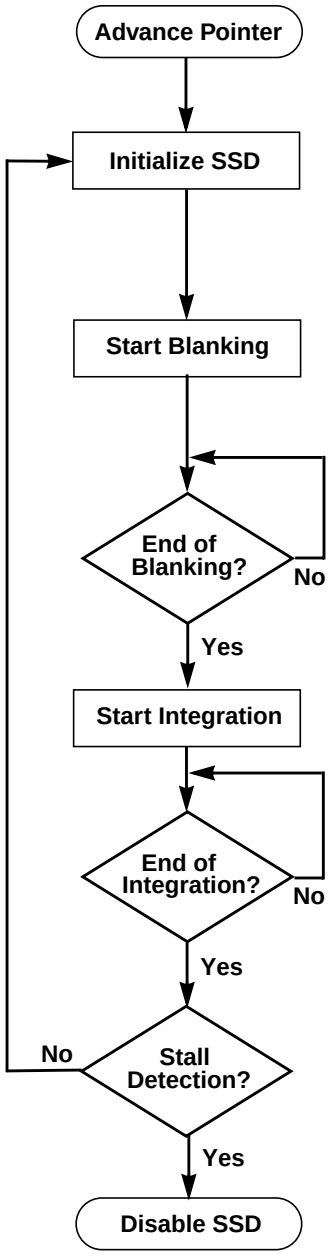
10.4.3 Operation in Low Power Modes

The SSD block can be configured for lower MCU power consumption in three different ways.

- Stop mode powers down the sigma-delta converter and halts clock to the modulus counter. Exit from Stop enables the sigma-delta converter and the clock to the modulus counter but due to the converter recovery time, the integration result should be ignored.
- Wait mode with SSDWAI bit set powers down the sigma-delta converter and halts the clock to the modulus counter. Exit from Wait enables the sigma-delta converter and clock to the modulus counter but due to the converter recovery time, the integration result should be ignored.
- Clearing SDCPU bit powers down the sigma-delta converter.

10.4.4 Stall Detection Flow

Figure 10-15 shows a flowchart and software setup for stall detection of a stepper motor. To control a second stepper motor, the SMS bit must be toggled during the SSD initialization.



Using Motor Control module, drive pointer to within 3 full steps of calibrated zero position.
1. Clear (or set) RCIR; clear (or set) POL; clear (or set) SMS; 2. Set MCZIE; clear MODMC; clear (or set) PRE; set MCEN. 3. Set RTZE; set SDCPU; write ACLKS (select sample frequency). 4. Store threshold value in RAM.
1. Clear MCZIF. 2. Write MDCCNT with blanking time value. 3. Clear ITG; clear (or set) DCOIL; increment (or decrement) STEP for CCW (or CW) motion.
MDCCNT = 0x0000? or MCZIF = 1?
1. Clear MCZIF. 2. Write MDCCNT with integration time value. 3. Set ITG; set DCOIL.
MDCCNT = 0x0000? or MCZIF = 1?
ITGACC < Threshold (RAM value)?
1. Clear MCZIF. 2. Clear MCEN. 3. Clear ITG. 4. Clear RTZE; clear SDCPU.

Figure 10-15. Return-to-Zero Flowchart

Chapter 11
Inter-Integrated Circuit (IICV2)

11.1 Introduction

The inter-IC bus (IIC) is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange between devices. Being a two-wire device, the IIC bus minimizes the need for large numbers of connections between devices, and eliminates the need for an address decoder.

This bus is suitable for applications requiring occasional communications over a short distance between a number of devices. It also provides flexibility, allowing additional devices to be connected to the bus for further expansion and system development.

The interface is designed to operate up to 100 kbps with maximum bus loading and timing. The device is capable of operating at higher baud rates, up to a maximum of clock/20, with reduced bus loading. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400 pF.

11.1.1 Features

The IIC module has the following key features:

- Compatible with I2C bus standard
- Multi-master operation
- Software programmable for one of 256 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus busy detection

11.1.2 Modes of Operation

The IIC functions the same in normal, special, and emulation modes. It has two low power modes: wait and stop modes.

11.1.3 Block Diagram

The block diagram of the IIC module is shown in Figure 11-1.

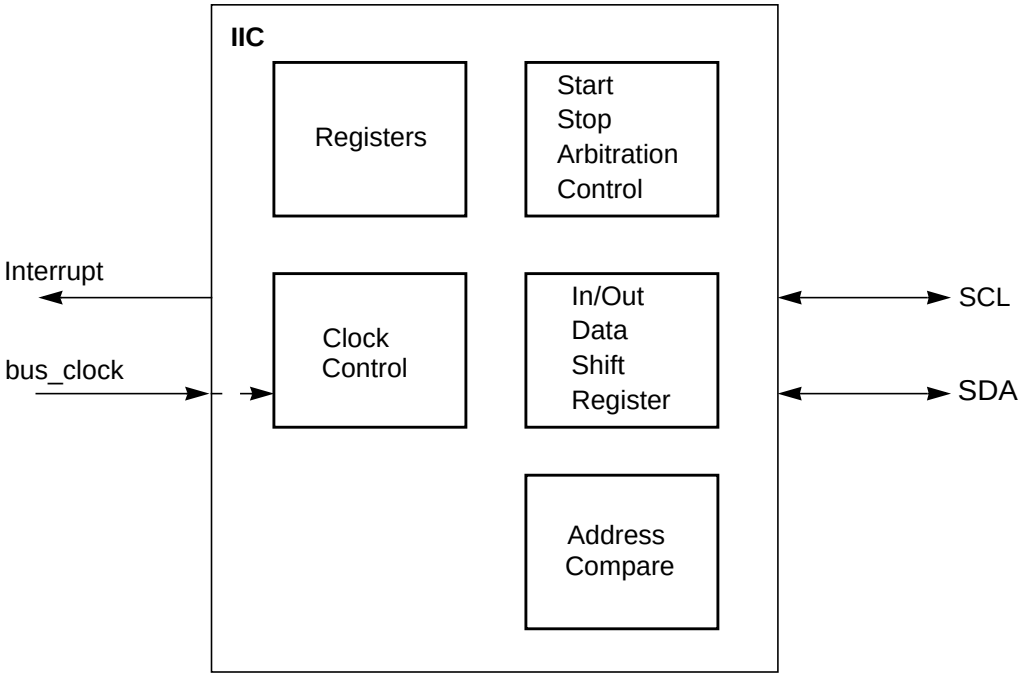


Figure 11-1. IIC Block Diagram

11.2 External Signal Description

The IIC module has two external pins.

11.2.1 IIC_SCL — Serial Clock Line Pin

This is the bidirectional serial clock line (SCL) of the module, compatible to the IIC bus specification.

11.2.2 IIC_SDA — Serial Data Line Pin

This is the bidirectional serial data line (SDA) of the module, compatible to the IIC bus specification.

11.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers for the IIC module.

11.3.1 Module Memory Map

The memory map for the IIC module is given below in Table 11-1. The address listed for each register is the address offset.The total address for each register is the sum of the base address for the IIC module and the address offset for each register.

11.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
	W								
IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
	W								
IBCR	R	IBEN	IBIE	MS/$\overline{SL}$	Tx/$\overline{Rx}$	TXAK	0	0	IBSWAI
	W						RSTA		
IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
	W								
IBDR	R	D7	D6	D5	D4	D3	D2	D1	D0
	W								

= Unimplemented or Reserved

Table 11-1. IIC Register Summary

11.3.2.1 IIC Address Register (IBAD)

	7	6	5	4	3	2	1	0
R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-2. IIC Bus Address Register (IBAD)

Read and write anytime

This register contains the address the IIC bus will respond to when addressed as a slave; note that it is not the address sent on the bus during the address transfer.

Table 11-2. IBAD Field Descriptions

Field	Description
7:1 ADR[7:1]	**Slave Address** — Bit 1 to bit 7 contain the specific slave address to be used by the IIC bus module.The default mode of IIC bus is slave mode for an address match on the bus.
0 Reserved	Reserved — Bit 0 of the IBAD is reserved for future compatibility. This bit will always read 0.

11.3.2.2 IIC Frequency Divider Register (IBFD)

	7	6	5	4	3	2	1	0
R W	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-3. IIC Bus Frequency Divider Register (IBFD)

Read and write anytime

Table 11-3. IBFD Field Descriptions

Field	Description
7:0 IBC[7:0]	**I Bus Clock Rate 7:0** — This field is used to prescale the clock for bit rate selection. The bit clock generator is implemented as a prescale divider — IBC7:6, prescaled shift register — IBC5:3 select the prescaler divider and IBC2-0 select the shift register tap point. The IBC bits are decoded to give the tap and prescale values as shown in Table 11-4.

Table 11-4. I-Bus Tap and Prescale Values

IBC2-0 (bin)	SCL Tap (clocks)	SDA Tap (clocks)
000	5	1
001	6	1
010	7	2
011	8	2
100	9	3
101	10	3
110	12	4
111	15	4

IBC5-3 (bin)	scl2start (clocks)	scl2stop (clocks)	scl2tap (clocks)	tap2tap (clocks)
000	2	7	4	1
001	2	7	4	2
010	2	9	6	4
011	6	9	6	8
100	14	17	14	16
101	30	33	30	32
110	62	65	62	64
111	126	129	126	128

Table 11-5. Multiplier Factor

IBC7-6	MUL
00	01
01	02
10	04
11	RESERVED

The number of clocks from the falling edge of SCL to the first tap (Tap[1]) is defined by the values shown in the scl2tap column of Table 11-4, all subsequent tap points are separated by 2^{IBC5-3} as shown in the tap2tap column in Table 11-4. The SCL Tap is used to generated the SCL period and the SDA Tap is used to determine the delay from the falling edge of SCL to SDA changing, the SDA hold time.

IBC7–6 defines the multiplier factor MUL. The values of MUL are shown in the Table 11-5.

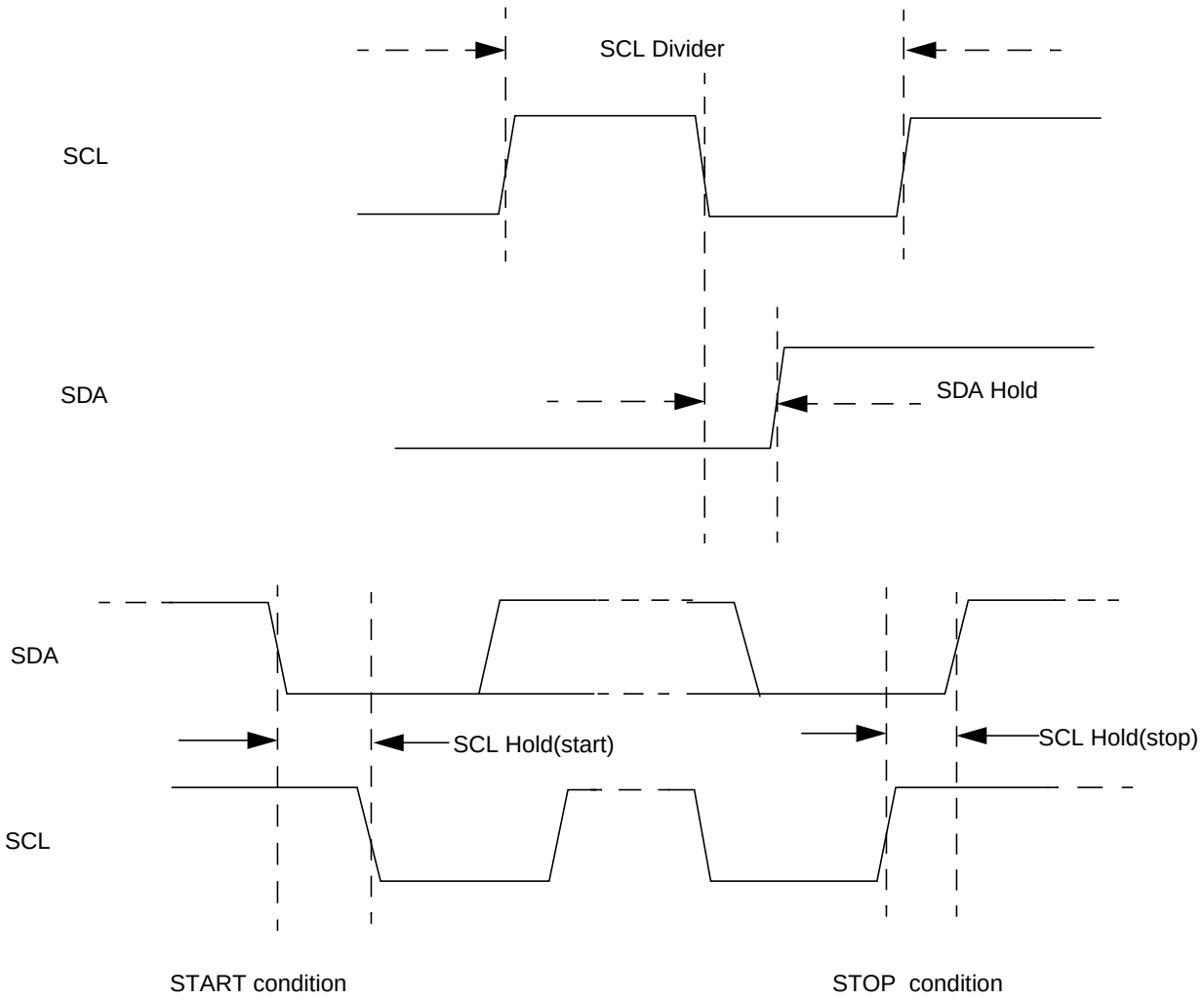


Figure 11-4. SCL Divider and SDA Hold

The equation used to generate the divider values from the IBFD bits is:

SCL Divider = MUL x {2 x (scl2tap + [(SCL_Tap -1) x tap2tap] + 2)}

The SDA hold delay is equal to the CPU clock period multiplied by the SDA Hold value shown in Table 11-6. The equation used to generate the SDA Hold value from the IBFD bits is:

SDA Hold = MUL x {scl2tap + [(SDA_Tap - 1) x tap2tap] + 3}

The equation for SCL Hold values to generate the start and stop conditions from the IBFD bits is:

SCL Hold(start) = MUL x [scl2start + (SCL_Tap - 1) x tap2tap]

SCL Hold(stop) = MUL x [scl2stop + (SCL_Tap - 1) x tap2tap]

Table 11-6. IIC Divider and Hold Values (Sheet 1 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
MUL=1				
00	20	7	6	11
01	22	7	7	12
02	24	8	8	13
03	26	8	9	14
04	28	9	10	15
05	30	9	11	16
06	34	10	13	18
07	40	10	16	21
08	28	7	10	15
09	32	7	12	17
0A	36	9	14	19
0B	40	9	16	21
0C	44	11	18	23
0D	48	11	20	25
0E	56	13	24	29
0F	68	13	30	35
10	48	9	18	25
11	56	9	22	29
12	64	13	26	33
13	72	13	30	37
14	80	17	34	41
15	88	17	38	45
16	104	21	46	53
17	128	21	58	65
18	80	9	38	41
19	96	9	46	49
1A	112	17	54	57
1B	128	17	62	65
1C	144	25	70	73
1D	160	25	78	81
1E	192	33	94	97
1F	240	33	118	121
20	160	17	78	81
21	192	17	94	97
22	224	33	110	113

Table 11-6. IIC Divider and Hold Values (Sheet 2 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
23	256	33	126	129
24	288	49	142	145
25	320	49	158	161
26	384	65	190	193
27	480	65	238	241
28	320	33	158	161
29	384	33	190	193
2A	448	65	222	225
2B	512	65	254	257
2C	576	97	286	289
2D	640	97	318	321
2E	768	129	382	385
2F	960	129	478	481
30	640	65	318	321
31	768	65	382	385
32	896	129	446	449
33	1024	129	510	513
34	1152	193	574	577
35	1280	193	638	641
36	1536	257	766	769
37	1920	257	958	961
38	1280	129	638	641
39	1536	129	766	769
3A	1792	257	894	897
3B	2048	257	1022	1025
3C	2304	385	1150	1153
3D	2560	385	1278	1281
3E	3072	513	1534	1537
3F	3840	513	1918	1921
MUL=2				
40	40	14	12	22
41	44	14	14	24
42	48	16	16	26
43	52	16	18	28
44	56	18	20	30
45	60	18	22	32
46	68	20	26	36
47	80	20	32	42
48	56	14	20	30
49	64	14	24	34
4A	72	18	28	38
4B	80	18	32	42
4C	88	22	36	46
4D	96	22	40	50
4E	112	26	48	58

Table 11-6. IIC Divider and Hold Values (Sheet 3 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
4F	136	26	60	70
50	96	18	36	50
51	112	18	44	58
52	128	26	52	66
53	144	26	60	74
54	160	34	68	82
55	176	34	76	90
56	208	42	92	106
57	256	42	116	130
58	160	18	76	82
59	192	18	92	98
5A	224	34	108	114
5B	256	34	124	130
5C	288	50	140	146
5D	320	50	156	162
5E	384	66	188	194
5F	480	66	236	242
60	320	34	156	162
61	384	34	188	194
62	448	66	220	226
63	512	66	252	258
64	576	98	284	290
65	640	98	316	322
66	768	130	380	386
67	960	130	476	482
68	640	66	316	322
69	768	66	380	386
6A	896	130	444	450
6B	1024	130	508	514
6C	1152	194	572	578
6D	1280	194	636	642
6E	1536	258	764	770
6F	1920	258	956	962
70	1280	130	636	642
71	1536	130	764	770
72	1792	258	892	898
73	2048	258	1020	1026
74	2304	386	1148	1154
75	2560	386	1276	1282
76	3072	514	1532	1538
77	3840	514	1916	1922
78	2560	258	1276	1282
79	3072	258	1532	1538
7A	3584	514	1788	1794
7B	4096	514	2044	2050

Table 11-6. IIC Divider and Hold Values (Sheet 4 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
7C	4608	770	2300	2306
7D	5120	770	2556	2562
7E	6144	1026	3068	3074
7F	7680	1026	3836	3842
MUL=4				
80	80	28	24	44
81	88	28	28	48
82	96	32	32	52
83	104	32	36	56
84	112	36	40	60
85	120	36	44	64
86	136	40	52	72
87	160	40	64	84
88	112	28	40	60
89	128	28	48	68
8A	144	36	56	76
8B	160	36	64	84
8C	176	44	72	92
8D	192	44	80	100
8E	224	52	96	116
8F	272	52	120	140
90	192	36	72	100
91	224	36	88	116
92	256	52	104	132
93	288	52	120	148
94	320	68	136	164
95	352	68	152	180
96	416	84	184	212
97	512	84	232	260
98	320	36	152	164
99	384	36	184	196
9A	448	68	216	228
9B	512	68	248	260
9C	576	100	280	292
9D	640	100	312	324
9E	768	132	376	388
9F	960	132	472	484
A0	640	68	312	324
A1	768	68	376	388
A2	896	132	440	452
A3	1024	132	504	516
A4	1152	196	568	580
A5	1280	196	632	644
A6	1536	260	760	772
A7	1920	260	952	964

Table 11-6. IIC Divider and Hold Values (Sheet 5 of 5)

IBC[7:0] (hex)	SCL Divider (clocks)	SDA Hold (clocks)	SCL Hold (start)	SCL Hold (stop)
A8	1280	132	632	644
A9	1536	132	760	772
AA	1792	260	888	900
AB	2048	260	1016	1028
AC	2304	388	1144	1156
AD	2560	388	1272	1284
AE	3072	516	1528	1540
AF	3840	516	1912	1924
B0	2560	260	1272	1284
B1	3072	260	1528	1540
B2	3584	516	1784	1796
B3	4096	516	2040	2052
B4	4608	772	2296	2308
B5	5120	772	2552	2564
B6	6144	1028	3064	3076
B7	7680	1028	3832	3844
B8	5120	516	2552	2564
B9	6144	516	3064	3076
BA	7168	1028	3576	3588
BB	8192	1028	4088	4100
BC	9216	1540	4600	4612
BD	10240	1540	5112	5124
BE	12288	2052	6136	6148
BF	15360	2052	7672	7684

11.3.2.3 IIC Control Register (IBCR)

	7	6	5	4	3	2	1	0
R	IBEN	IBIE	MS/SL	Tx/Rx	TXAK	0	0	IBSWAI
W						RSTA		
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 11-5. IIC Bus Control Register (IBCR)

Read and write anytime

Table 11-7. IBCR Field Descriptions

Field	Description
7 IBEN	**I-Bus Enable** — This bit controls the software reset of the entire IIC bus module. 0 The module is reset and disabled. This is the power-on reset situation. When low the interface is held in reset but registers can be accessed 1 The IIC bus module is enabled.This bit must be set before any other IBCR bits have any effect If the IIC bus module is enabled in the middle of a byte transfer the interface behaves as follows: slave mode ignores the current transfer on the bus and starts operating whenever a subsequent start condition is detected. Master mode will not be aware that the bus is busy, hence if a start cycle is initiated then the current bus cycle may become corrupt. This would ultimately result in either the current bus master or the IIC bus module losing arbitration, after which bus operation would return to normal.
6 IBIE	**I-Bus Interrupt Enable** 0 Interrupts from the IIC bus module are disabled. Note that this does not clear any currently pending interrupt condition 1 Interrupts from the IIC bus module are enabled. An IIC bus interrupt occurs provided the IBIF bit in the status register is also set.
5 MS/SL	**Master/Slave Mode Select Bit** — Upon reset, this bit is cleared. When this bit is changed from 0 to 1, a START signal is generated on the bus, and the master mode is selected. When this bit is changed from 1 to 0, a STOP signal is generated and the operation mode changes from master to slave.A STOP signal should only be generated if the IBIF flag is set. MS/$\overline{SL}$ is cleared without generating a STOP signal when the master loses arbitration. 0 Slave Mode 1 Master Mode
4 Tx/Rx	**Transmit/Receive Mode Select Bit** — This bit selects the direction of master and slave transfers. When addressed as a slave this bit should be set by software according to the SRW bit in the status register. In master mode this bit should be set according to the type of transfer required. Therefore, for address cycles, this bit will always be high. 0 Receive 1 Transmit
3 TXAK	**Transmit Acknowledge Enable** — This bit specifies the value driven onto SDA during data acknowledge cycles for both master and slave receivers. The IIC module will always acknowledge address matches, provided it is enabled, regardless of the value of TXAK. Note that values written to this bit are only used when the IIC bus is a receiver, not a transmitter. 0 An acknowledge signal will be sent out to the bus at the 9th clock bit after receiving one byte data 1 No acknowledge signal response is sent (i.e., acknowledge bit = 1)
2 RSTA	**Repeat Start** — Writing a 1 to this bit will generate a repeated START condition on the bus, provided it is the current bus master. This bit will always be read as a low. Attempting a repeated start at the wrong time, if the bus is owned by another master, will result in loss of arbitration. 1 Generate repeat start cycle
1 RESERVED	**Reserved** — Bit 1 of the IBCR is reserved for future compatibility. This bit will always read 0.
0 IBSWAI	**I Bus Interface Stop in Wait Mode** 0 IIC bus module clock operates normally 1 Halt IIC bus module clock generation in wait mode

Wait mode is entered via execution of a CPU WAI instruction. In the event that the IBSWAI bit is set, all clocks internal to the IIC will be stopped and any transmission currently in progress will halt.If the CPU were woken up by a source other than the IIC module, then clocks would restart and the IIC would resume

from where was during the previous transmission. It is not possible for the IIC to wake up the CPU when its internal clocks are stopped.

If it were the case that the IBSWAI bit was cleared when the WAI instruction was executed, the IIC internal clocks and interface would remain alive, continuing the operation which was currently underway. It is also possible to configure the IIC such that it will wake up the CPU via an interrupt at the conclusion of the current operation. See the discussion on the IBIF and IBIE bits in the IBSR and IBCR, respectively.

11.3.2.4 IIC Status Register (IBSR)

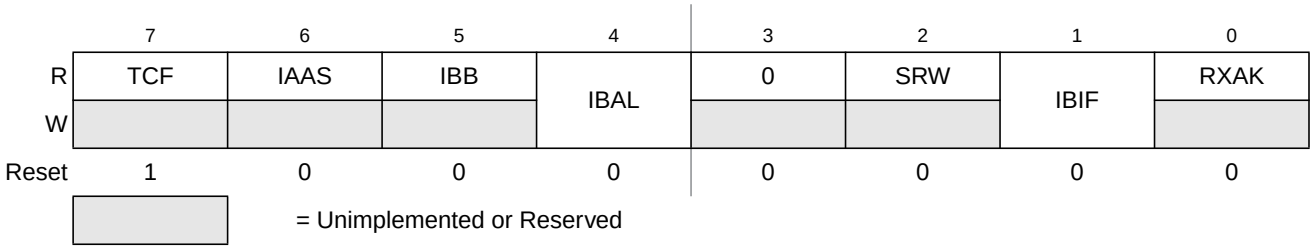


Figure 11-6. IIC Bus Status Register (IBSR)

This status register is read-only with exception of bit 1 (IBIF) and bit 4 (IBAL), which are software clearable.

Table 11-8. IBSR Field Descriptions

Field	Description
7 TCF	**Data Transferring Bit** — While one byte of data is being transferred, this bit is cleared. It is set by the falling edge of the 9th clock of a byte transfer. Note that this bit is only valid during or immediately following a transfer to the IIC module or from the IIC module. 0 Transfer in progress 1 Transfer complete
6 IAAS	**Addressed as a Slave Bit** — When its own specific address (I-bus address register) is matched with the calling address, this bit is set.The CPU is interrupted provided the IBIE is set.Then the CPU needs to check the SRW bit and set its Tx/$\overline{Rx}$ mode accordingly.Writing to the I-bus control register clears this bit. 0 Not addressed 1 Addressed as a slave
5 IBB	Bus Busy Bit 0 This bit indicates the status of the bus. When a START signal is detected, the IBB is set. If a STOP signal is detected, IBB is cleared and the bus enters idle state. 1 Bus is busy
4 IBAL	**Arbitration Lost** — The arbitration lost bit (IBAL) is set by hardware when the arbitration procedure is lost. Arbitration is lost in the following circumstances: 1. SDA sampled low when the master drives a high during an address or data transmit cycle. 2. SDA sampled low when the master drives a high during the acknowledge bit of a data receive cycle. 3. A start cycle is attempted when the bus is busy. 4. A repeated start cycle is requested in slave mode. 5. A stop condition is detected when the master did not request it. This bit must be cleared by software, by writing a one to it. A write of 0 has no effect on this bit.
3 RESERVED	**Reserved** — Bit 3 of IBSR is reserved for future use. A read operation on this bit will return 0.

Table 11-8. IBSR Field Descriptions (continued)

Field	Description
2 SRW	**Slave Read/Write** — When IAAS is set this bit indicates the value of the R/W command bit of the calling address sent from the master This bit is only valid when the I-bus is in slave mode, a complete address transfer has occurred with an address match and no other transfers have been initiated. Checking this bit, the CPU can select slave transmit/receive mode according to the command of the master. 0 Slave receive, master writing to slave 1 Slave transmit, master reading from slave
1 IBIF	**I-Bus Interrupt** — The IBIF bit is set when one of the following conditions occurs: — Arbitration lost (IBAL bit set) — Byte transfer complete (TCF bit set) — Addressed as slave (IAAS bit set) It will cause a processor interrupt request if the IBIE bit is set. This bit must be cleared by software, writing a one to it. A write of 0 has no effect on this bit.
0 RXAK	**Received Acknowledge** — The value of SDA during the acknowledge bit of a bus cycle. If the received acknowledge bit (RXAK) is low, it indicates an acknowledge signal has been received after the completion of 8 bits data transmission on the bus. If RXAK is high, it means no acknowledge signal is detected at the 9th clock. 0 Acknowledge received 1 No acknowledge received

11.3.2.5 IIC Data I/O Register (IBDR)

	7	6	5	4	3	2	1	0
R W	D7	D6	D5	D4	D3	D2	D1	D0
Reset	0	0	0	0	0	0	0	0

Figure 11-7. IIC Bus Data I/O Register (IBDR)

In master transmit mode, when data is written to the IBDR a data transfer is initiated. The most significant bit is sent first. In master receive mode, reading this register initiates next byte data receiving. In slave mode, the same functions are available after an address match has occurred.Note that the Tx/Rx bit in the IBCR must correctly reflect the desired direction of transfer in master and slave modes for the transmission to begin. For instance, if the IIC is configured for master transmit but a master receive is desired, then reading the IBDR will not initiate the receive.

Reading the IBDR will return the last byte received while the IIC is configured in either master receive or slave receive modes. The IBDR does not reflect every byte that is transmitted on the IIC bus, nor can software verify that a byte has been written to the IBDR correctly by reading it back.

In master transmit mode, the first byte of data written to IBDR following assertion of MS/$\overline{\text{SL}}$ is used for the address transfer and should com.prise of the calling address (in position D7:D1) concatenated with the required R/$\overline{\text{W}}$ bit (in position D0).

11.4 Functional Description

This section provides a complete functional description of the IIC.

11.4.1 I-Bus Protocol

The IIC bus system uses a serial data line (SDA) and a serial clock line (SCL) for data transfer. All devices connected to it must have open drain or open collector outputs. Logic AND function is exercised on both lines with external pull-up resistors. The value of these resistors is system dependent.

Normally, a standard communication is composed of four parts: START signal, slave address transmission, data transfer and STOP signal. They are described briefly in the following sections and illustrated in Figure 11-8.

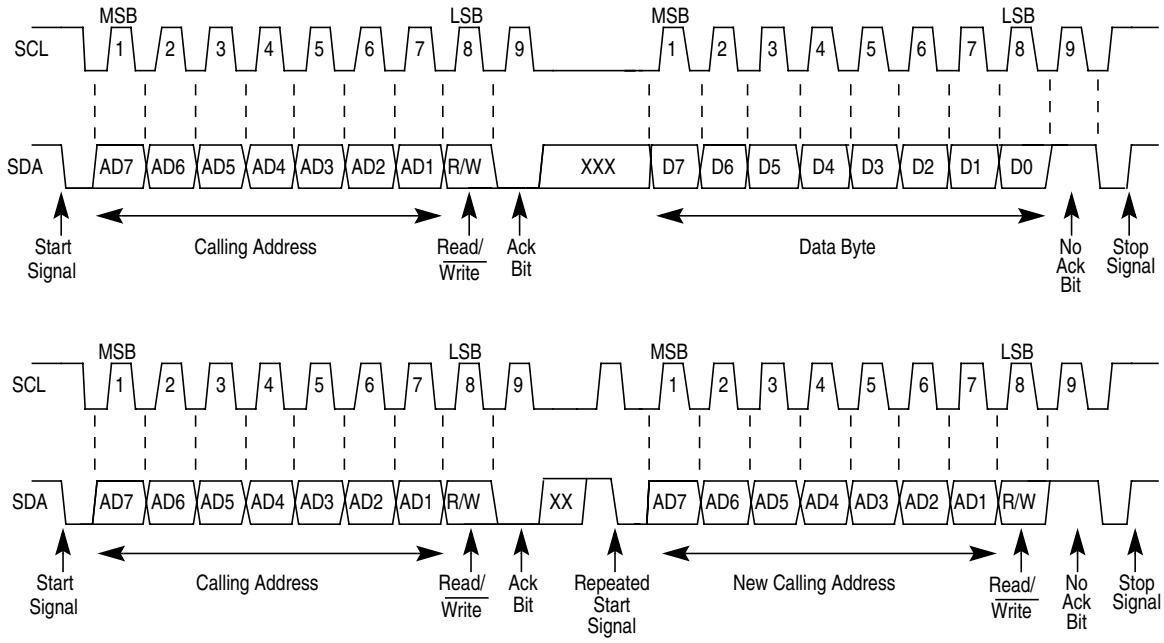


Figure 11-8. IIC-Bus Transmission Signals

11.4.1.1 START Signal

When the bus is free, i.e. no master device is engaging the bus (both SCL and SDA lines are at logical high), a master may initiate communication by sending a START signal.As shown in Figure 11-8, a START signal is defined as a high-to-low transition of SDA while SCL is high. This signal denotes the beginning of a new data transfer (each data transfer may contain several bytes of data) and brings all slaves out of their idle states.

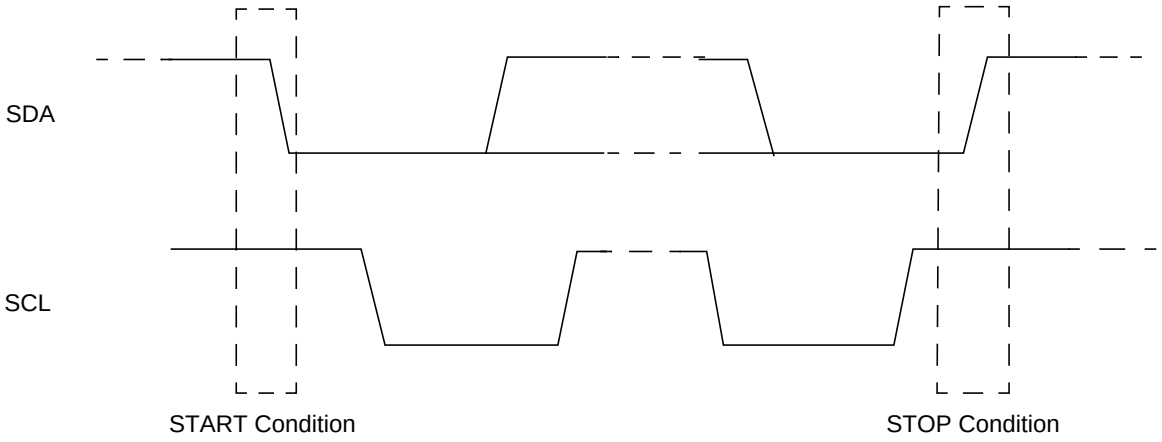


Figure 11-9. Start and Stop Conditions

11.4.1.2 Slave Address Transmission

The first byte of data transfer immediately after the START signal is the slave address transmitted by the master. This is a seven-bit calling address followed by a R/W bit. The R/W bit tells the slave the desired direction of data transfer.

1 = Read transfer, the slave transmits data to the master.
0 = Write transfer, the master transmits data to the slave.

Only the slave with a calling address that matches the one transmitted by the master will respond by sending back an acknowledge bit. This is done by pulling the SDA low at the 9th clock (see Figure 11-8).

No two slaves in the system may have the same address. If the IIC bus is master, it must not transmit an address that is equal to its own slave address. The IIC bus cannot be master and slave at the same time.However, if arbitration is lost during an address cycle the IIC bus will revert to slave mode and operate correctly even if it is being addressed by another master.

11.4.1.3 Data Transfer

As soon as successful slave addressing is achieved, the data transfer can proceed byte-by-byte in a direction specified by the R/W bit sent by the calling master

All transfers that come after an address cycle are referred to as data transfers, even if they carry sub-address information for the slave device.

Each data byte is 8 bits long. Data may be changed only while SCL is low and must be held stable while SCL is high as shown in Figure 11-8. There is one clock pulse on SCL for each data bit, the MSB being transferred first. Each data byte has to be followed by an acknowledge bit, which is signalled from the receiving device by pulling the SDA low at the ninth clock. So one complete data byte transfer needs nine clock pulses.

If the slave receiver does not acknowledge the master, the SDA line must be left high by the slave. The master can then generate a stop signal to abort the data transfer or a start signal (repeated start) to commence a new calling.

If the master receiver does not acknowledge the slave transmitter after a byte transmission, it means 'end of data' to the slave, so the slave releases the SDA line for the master to generate STOP or START signal.

11.4.1.4 STOP Signal

The master can terminate the communication by generating a STOP signal to free the bus. However, the master may generate a START signal followed by a calling command without generating a STOP signal first. This is called repeated START. A STOP signal is defined as a low-to-high transition of SDA while SCL at logical 1 (see Figure 11-8).

The master can generate a STOP even if the slave has generated an acknowledge at which point the slave must release the bus.

11.4.1.5 Repeated START Signal

As shown in Figure 11-8, a repeated START signal is a START signal generated without first generating a STOP signal to terminate the communication. This is used by the master to communicate with another slave or with the same slave in different mode (transmit/receive mode) without releasing the bus.

11.4.1.6 Arbitration Procedure

The Inter-IC bus is a true multi-master bus that allows more than one master to be connected on it. If two or more masters try to control the bus at the same time, a clock synchronization procedure determines the bus clock, for which the low period is equal to the longest clock low period and the high is equal to the shortest one among the masters. The relative priority of the contending masters is determined by a data arbitration procedure, a bus master loses arbitration if it transmits logic 1 while another master transmits logic 0. The losing masters immediately switch over to slave receive mode and stop driving SDA output. In this case the transition from master to slave mode does not generate a STOP condition. Meanwhile, a status bit is set by hardware to indicate loss of arbitration.

11.4.1.7 Clock Synchronization

Because wire-AND logic is performed on SCL line, a high-to-low transition on SCL line affects all the devices connected on the bus. The devices start counting their low period and as soon as a device's clock has gone low, it holds the SCL line low until the clock high state is reached.However, the change of low to high in this device clock may not change the state of the SCL line if another device clock is within its low period. Therefore, synchronized clock SCL is held low by the device with the longest low period. Devices with shorter low periods enter a high wait state during this time (see Figure 11-9). When all devices concerned have counted off their low period, the synchronized clock SCL line is released and pulled high. There is then no difference between the device clocks and the state of the SCL line and all the devices start counting their high periods.The first device to complete its high period pulls the SCL line low again.

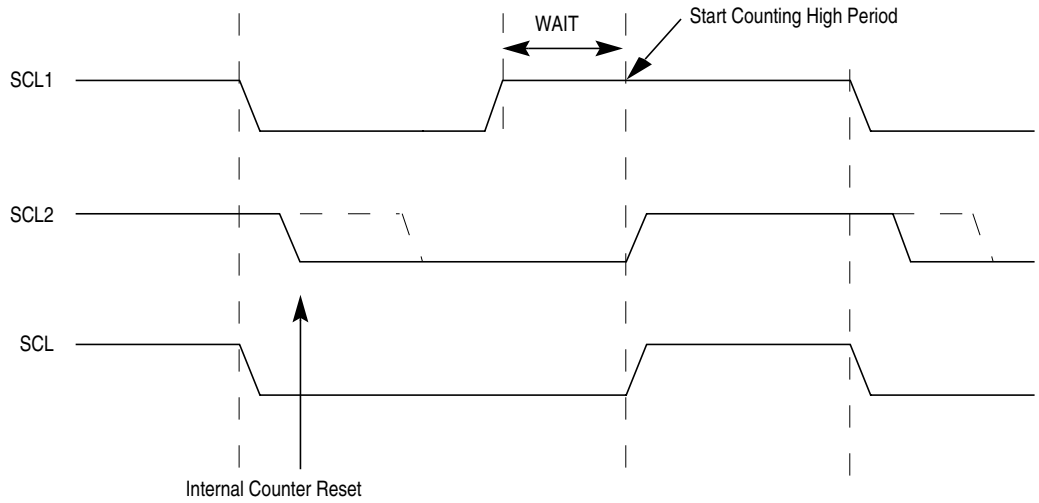


Figure 11-10. IIC-Bus Clock Synchronization

11.4.1.8 Handshaking

The clock synchronization mechanism can be used as a handshake in data transfer. Slave devices may hold the SCL low after completion of one byte transfer (9 bits). In such case, it halts the bus clock and forces the master clock into wait states until the slave releases the SCL line.

11.4.1.9 Clock Stretching

The clock synchronization mechanism can be used by slaves to slow down the bit rate of a transfer. After the master has driven SCL low the slave can drive SCL low for the required period and then release it.If the slave SCL low period is greater than the master SCL low period then the resulting SCL bus signal low period is stretched.

11.4.2 Operation in Run Mode

This is the basic mode of operation.

11.4.3 Operation in Wait Mode

IIC operation in wait mode can be configured. Depending on the state of internal bits, the IIC can operate normally when the CPU is in wait mode or the IIC clock generation can be turned off and the IIC module enters a power conservation state during wait mode. In the later case, any transmission or reception in progress stops at wait mode entry.

11.4.4 Operation in Stop Mode

The IIC is inactive in stop mode for reduced power consumption. The STOP instruction does not affect IIC register states.

11.5 Resets

The reset state of each individual bit is listed in Section 11.3, “Memory Map and Register Definition,” which details the registers and their bit-fields.

11.6 Interrupts

IIC uses only one interrupt vector.

Table 11-9. Interrupt Summary

Interrupt	Offset	Vector	Priority	Source	Description
IIC Interrupt	—	—	—	IBAL, TCF, IAAS bits in IBSR register	When either of IBAL, TCF or IAAS bits is set may cause an interrupt based on arbitration lost, transfer complete or address detect conditions

Internally there are three types of interrupts in IIC. The interrupt service routine can determine the interrupt type by reading the status register.

IIC Interrupt can be generated on

1. Arbitration lost condition (IBAL bit set)
2. Byte transfer condition (TCF bit set)
3. Address detect condition (IAAS bit set)

The IIC interrupt is enabled by the IBIE bit in the IIC control register. It must be cleared by writing 0 to the IBF bit in the interrupt service routine.

11.7 Initialization/Application Information

11.7.1 IIC Programming Examples

11.7.1.1 Initialization Sequence

Reset will put the IIC bus control register to its default status. Before the interface can be used to transfer serial data, an initialization procedure must be carried out, as follows:

1. Update the frequency divider register (IBFD) and select the required division ratio to obtain SCL frequency from system clock.
2. Update the IIC bus address register (IBAD) to define its slave address.
3. Set the IBEN bit of the IIC bus control register (IBCR) to enable the IIC interface system.
4. Modify the bits of the IIC bus control register (IBCR) to select master/slave mode, transmit/receive mode and interrupt enable or not.

11.7.1.2 Generation of START

After completion of the initialization procedure, serial data can be transmitted by selecting the 'master transmitter' mode. If the device is connected to a multi-master bus system, the state of the IIC bus busy bit (IBB) must be tested to check whether the serial bus is free.

If the bus is free (IBB=0), the start condition and the first byte (the slave address) can be sent. The data written to the data register comprises the slave calling address and the LSB set to indicate the direction of transfer required from the slave.

The bus free time (i.e., the time between a STOP condition and the following START condition) is built into the hardware that generates the START cycle. Depending on the relative frequencies of the system clock and the SCL period it may be necessary to wait until the IIC is busy after writing the calling address to the IBDR before proceeding with the following instructions. This is illustrated in the following example.

An example of a program which generates the START signal and transmits the first byte of data (slave address) is shown below:

```
CHFLAG      BRSET   IBSR,#$20,*     ;WAIT FOR IBB FLAG TO CLEAR
TXSTART     BSET    IBCR,#$30       ;SET TRANSMIT AND MASTER MODE;i.e. GENERATE START CONDITION
            MOVB    CALLING,IBDR    ;TRANSMIT THE CALLING ADDRESS, D0=R/W
IBFREE      BRCLR   IBSR,#$20,*     ;WAIT FOR IBB FLAG TO SET
```

11.7.1.3 Post-Transfer Software Response

Transmission or reception of a byte will set the data transferring bit (TCF) to 1, which indicates one byte communication is finished. The IIC bus interrupt bit (IBIF) is set also; an interrupt will be generated if the interrupt function is enabled during initialization by setting the IBIE bit. Software must clear the IBIF bit in the interrupt routine first. The TCF bit will be cleared by reading from the IIC bus data I/O register (IBDR) in receive mode or writing to IBDR in transmit mode.

Software may service the IIC I/O in the main program by monitoring the IBIF bit if the interrupt function is disabled. Note that polling should monitor the IBIF bit rather than the TCF bit because their operation is different when arbitration is lost.

Note that when an interrupt occurs at the end of the address cycle the master will always be in transmit mode, i.e. the address is transmitted. If master receive mode is required, indicated by R/W bit in IBDR, then the Tx/Rx bit should be toggled at this stage.

During slave mode address cycles (IAAS=1), the SRW bit in the status register is read to determine the direction of the subsequent transfer and the Tx/Rx bit is programmed accordingly. For slave mode data cycles (IAAS=0) the SRW bit is not valid, the Tx/Rx bit in the control register should be read to determine the direction of the current transfer.

The following is an example of a software response by a 'master transmitter' in the interrupt routine.

```
ISR         BCLR    IBSR,#$02           ;CLEAR THE IBIF FLAG
            BRCLR   IBCR,#$20,SLAVE     ;BRANCH IF IN SLAVE MODE
            BRCLR   IBCR,#$10,RECEIVE   ;BRANCH IF IN RECEIVE MODE
            BRSET   IBSR,#$01,END       ;IF NO ACK, END OF TRANSMISSION
TRANSMIT    MOVB    DATABUF,IBDR        ;TRANSMIT NEXT BYTE OF DATA
```

11.7.1.4 Generation of STOP

A data transfer ends with a STOP signal generated by the 'master' device. A master transmitter can simply generate a STOP signal after all the data has been transmitted. The following is an example showing how a stop condition is generated by a master transmitter.

```
MASTX   TST     TXCNT           ;GET VALUE FROM THE TRANSMITING COUNTER
        BEQ     END             ;END IF NO MORE DATA
        BRSET   IBSR,#$01,END   ;END IF NO ACK
        MOVB    DATABUF,IBDR    ;TRANSMIT NEXT BYTE OF DATA
        DEC     TXCNT           ;DECREASE THE TXCNT
        BRA     EMASTX          ;EXIT
END     BCLR    IBCR,#$20       ;GENERATE A STOP CONDITION
EMASTX  RTI                     ;RETURN FROM INTERRUPT
```

If a master receiver wants to terminate a data transfer, it must inform the slave transmitter by not acknowledging the last byte of data which can be done by setting the transmit acknowledge bit (TXAK) before reading the 2nd last byte of data. Before reading the last byte of data, a STOP signal must be generated first. The following is an example showing how a STOP signal is generated by a master receiver.

```
MASR    DEC     RXCNT           ;DECREASE THE RXCNT
        BEQ     ENMASR          ;LAST BYTE TO BE READ
        MOVB    RXCNT,D1        ;CHECK SECOND LAST BYTE
        DEC     D1              ;TO BE READ
        BNE     NXMAR           ;NOT LAST OR SECOND LAST
LAMAR   BSET    IBCR,#$08       ;SECOND LAST, DISABLE ACK
                                ;TRANSMITTING
        BRA     NXMAR
ENMASR  BCLR    IBCR,#$20       ;LAST ONE, GENERATE 'STOP' SIGNAL
NXMAR   MOVB    IBDR,RXBUF      ;READ DATA AND STORE
        RTI
```

11.7.1.5 Generation of Repeated START

At the end of data transfer, if the master continues to want to communicate on the bus, it can generate another START signal followed by another slave address without first generating a STOP signal. A program example is as shown.

```
RESTART BSET    IBCR,#$04       ;ANOTHER START (RESTART)
        MOVB    CALLING,IBDR    ;TRANSMIT THE CALLING ADDRESS;D0=R/W
```

11.7.1.6 Slave Mode

In the slave interrupt service routine, the module addressed as slave bit (IAAS) should be tested to check if a calling of its own address has just been received. If IAAS is set, software should set the transmit/receive mode select bit (Tx/Rx bit of IBCR) according to the R/W command bit (SRW). Writing to the IBCR clears the IAAS automatically. Note that the only time IAAS is read as set is from the interrupt at the end of the address cycle where an address match occurred, interrupts resulting from subsequent data transfers will have IAAS cleared. A data transfer may now be initiated by writing information to IBDR, for slave transmits, or dummy reading from IBDR, in slave receive mode. The slave will drive SCL low in-between byte transfers, SCL is released when the IBDR is accessed in the required mode.

In slave transmitter routine, the received acknowledge bit (RXAK) must be tested before transmitting the next byte of data. Setting RXAK means an 'end of data' signal from the master receiver, after which it must be switched from transmitter mode to receiver mode by software. A dummy read then releases the SCL line so that the master can generate a STOP signal.

11.7.1.7 Arbitration Lost

If several masters try to engage the bus simultaneously, only one master wins and the others lose arbitration. The devices which lost arbitration are immediately switched to slave receive mode by the hardware. Their data output to the SDA line is stopped, but SCL continues to be generated until the end of the byte during which arbitration was lost. An interrupt occurs at the falling edge of the ninth clock of this transfer with IBAL=1 and MS/SL=0. If one master attempts to start transmission while the bus is being engaged by another master, the hardware will inhibit the transmission; switch the MS/SL bit from 1 to 0 without generating STOP condition; generate an interrupt to CPU and set the IBAL to indicate that the attempt to engage the bus is failed. When considering these cases, the slave service routine should test the IBAL first and the software should clear the IBAL bit if it is set.

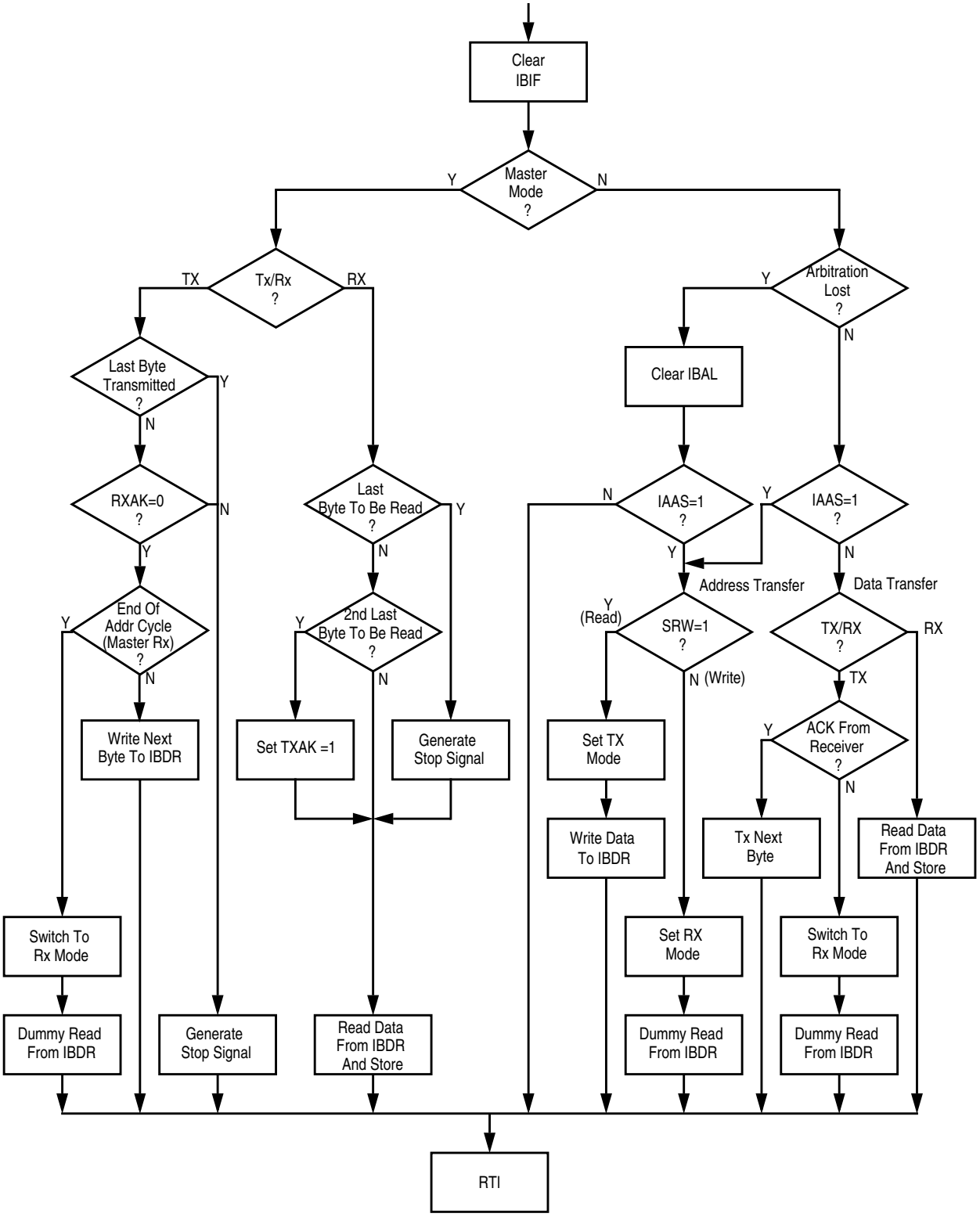


Figure 11-11. Flow-Chart of Typical IIC Interrupt Routine

Chapter 12
Freescale's Scalable Controller Area Network (MSCANV2)

12.1 Introduction

Freescale's scalable controller area network (MSCAN) definition is based on the MSCAN12 definition, which is the specific implementation of the MSCAN concept targeted for the M68HC12 microcontroller family.

The module is a communication controller implementing the CAN 2.0A/B protocol as defined in the Bosch specification dated September 1991. For users to fully understand the MSCAN specification, it is recommended that the Bosch specification be read first to familiarize the reader with the terms and concepts contained within this document.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

MSCAN uses an advanced buffer arrangement resulting in predictable real-time behavior and simplified application software.

12.1.1 Block Diagram

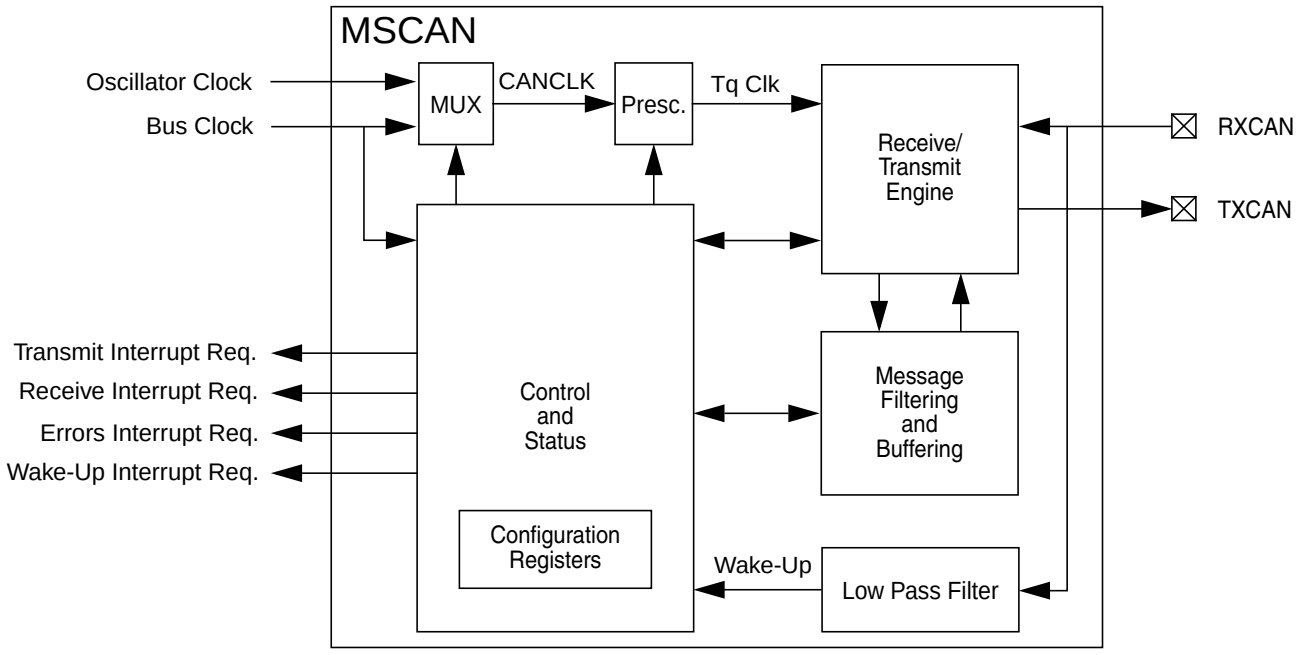


Figure 12-1. MSCAN Block Diagram

12.1.2 Features

The basic features of the MSCAN are as follows:

- Implementation of the CAN protocol — Version 2.0A/B
  - — Standard and extended data frames
  - — Zero to eight bytes data length
  - — Programmable bit rate up to 1 Mbps[1]
  - — Support for remote frames
- Five receive buffers with FIFO storage scheme
- Three transmit buffers with internal prioritization using a "local priority" concept
- Flexible maskable identifier filter supports two full-size (32-bit) extended identifier filters, or four 16-bit filters, or eight 8-bit filters
- Programmable wakeup functionality with integrated low-pass filter
- Programmable loopback mode supports self-test operation
- Programmable listen-only mode for monitoring of CAN bus
- Separate signalling and interrupt capabilities for all CAN receiver and transmitter error states (warning, error passive, bus-off)
- Programmable MSCAN clock source either bus clock or oscillator clock
- Internal timer for time-stamping of received and transmitted messages
- Three low-power modes: sleep, power down, and MSCAN enable
- Global initialization of configuration registers

12.1.3 Modes of Operation

The following modes of operation are specific to the MSCAN. See Section 12.4, "Functional Description," for details.

- Listen-Only Mode
- MSCAN Sleep Mode
- MSCAN Initialization Mode
- MSCAN Power Down Mode

12.2 External Signal Description

The MSCAN uses two external pins:

12.2.1 RXCAN — CAN Receiver Input Pin

RXCAN is the MSCAN receiver input pin.

1. Depending on the actual bit timing and the clock jitter of the PLL.

12.2.2 TXCAN — CAN Transmitter Output Pin

TXCAN is the MSCAN transmitter output pin. The TXCAN output pin represents the logic level on the CAN bus:

0 = Dominant state
1 = Recessive state

12.2.3 CAN System

A typical CAN system with MSCAN is shown in Figure 12-2. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations.

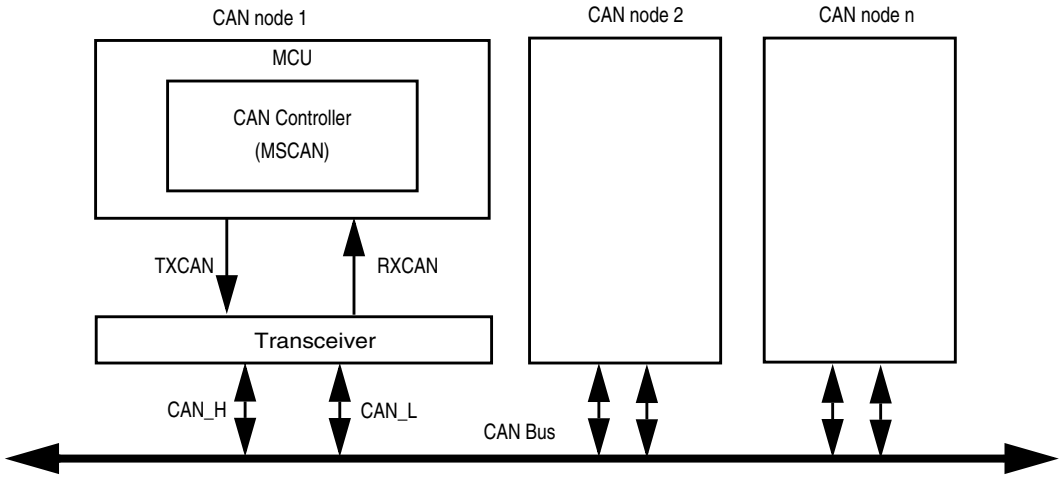


Figure 12-2. CAN System

12.3 Memory Map and Register Definition

This section provides a detailed description of all registers accessible in the MSCAN.

12.3.1 Module Memory Map

Table 12-1 gives an overview on all registers and their individual bits in the MSCAN memory map. The *register address* results from the addition of *base address* and *address offset*. The *base address* is determined at the MCU level and can be found in the Memory block description chapter. The *address offset* is defined at the module level.

The MSCAN occupies 64 bytes in the memory space. The base address of the MSCAN module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset.

Table 12-1 shows the individual registers associated with the MSCAN and their relative offset from the base address. The detailed register descriptions follow in the order they appear in the register map.

Table 12-1. MSCAN Memory Map

Address Offset	Register	Access
0x0000	MSCAN Control Register 0 (CANCTL0)	R/W[1]
0x0001	MSCAN Control Register 1 (CANCTL1)	R/W[1]
0x0002	MSCAN Bus Timing Register 0 (CANBTR0)	R/W
0x0003	MSCAN Bus Timing Register 1 (CANBTR1)	R/W
0x0004	MSCAN Receiver Flag Register (CANRFLG)	R/W[1]
0x0005	MSCAN Receiver Interrupt Enable Register (CANRIER)	R/W
0x0006	MSCAN Transmitter Flag Register (CANTFLG)	R/W[1]
0x0007	MSCAN Transmitter Interrupt Enable Register (CANTIER)	R/W[1]
0x0008	MSCAN Transmitter Message Abort Request Register (CANTARQ)	R/W[1]
0x0009	MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)	R
0x000A	MSCAN Transmit Buffer Selection Register (CANTBSEL)	R/W[1]
0x000B	MSCAN Identifier Acceptance Control Register (CANIDAC)	R/W[1]
0x000C	RESERVED	
0x000D	RESERVED	
0x000E	MSCAN Receive Error Counter (CANRXERR)	R
0x000F	MSCAN Transmit Error Counter (CANTXERR)	R
0x0010	MSCAN Identifier Acceptance Register 0(CANIDAR0)	R/W
0x0011	MSCAN Identifier Acceptance Register 1(CANIDAR1)	R/W
0x0012	MSCAN Identifier Acceptance Register 2 (CANIDAR2)	R/W
0x0013	MSCAN Identifier Acceptance Register 3 (CANIDAR3)	R/W
0x0014	MSCAN Identifier Mask Register 0 (CANIDMR0)	R/W
0x0015	MSCAN Identifier Mask Register 1 (CANIDMR1)	R/W
0x0016	MSCAN Identifier Mask Register 2 (CANIDMR2)	R/W
0x0017	MSCAN Identifier Mask Register 3 (CANIDMR3)	R/W
0x0018	MSCAN Identifier Acceptance Register 4 (CANIDAR4)	R/W
0x0019	MSCAN Identifier Acceptance Register 5 (CANIDAR5)	R/W
0x001A	MSCAN Identifier Acceptance Register 6 (CANIDAR6)	R/W
0x001B	MSCAN Identifier Acceptance Register 7 (CANIDAR7)	R/W
0x001C	MSCAN Identifier Mask Register 4 (CANIDMR4)	R/W
0x001D	MSCAN Identifier Mask Register 5 (CANIDMR5)	R/W
0x001E	MSCAN Identifier Mask Register 6 (CANIDMR6)	R/W
0x001F	MSCAN Identifier Mask Register 7 (CANIDMR7)	R/W
0x0020 -0x002F	Foreground Receive Buffer (CANRXFG)	R[2]
0x0030 -0x003F	Foreground Transmit Buffer (CANTXFG)	R[2]/W

1 Refer to detailed register description for write access restrictions on per bit basis.

2 Reserved bits and unused bits within the TX- and RX-buffers (CANTXFG, CANRXFG) will be read as "X", because of RAM-based implementation.

Table 12-2. MSCAN Memory Map

Offset Address	Register	Access
0x0000	This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.	R/W[1]
0x0001	MSCAN Control Register 1 (CANCTL1)	R/W[1]
0x0002	MSCAN Bus Timing Register 0 (CANBTR0)	R/W
0x0003	MSCAN Bus Timing Register 1 (CANBTR1)	R/W
0x0004	MSCAN Receiver Flag Register (CANRFLG)	R/W[1]
0x0005	MSCAN Receiver Interrupt Enable Register (CANRIER)	R/W
0x0006	MSCAN Transmitter Flag Register (CANTFLG)	R/W[1]
0x0007	MSCAN Transmitter Interrupt Enable Register (CANTIER)	R/W[1]
0x0008	MSCAN Transmitter Message Abort Request Register (CANTARQ)	R/W[1]
0x0009	MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)	R
0x000A	MSCAN Transmit Buffer Selection Register (CANTBSEL)	R/W[1]
0x000B	MSCAN Identifier Acceptance Control Register (CANIDAC)	R/W[1]
0x000C	RESERVED	
0x000D	RESERVED	
0x000E	MSCAN Receive Error Counter (CANRXERR)	R
0x000F	MSCAN Transmit Error Counter (CANTXERR)	R
0x0010	MSCAN Identifier Acceptance Register 0(CANIDAR0)	R/W
0x0011	MSCAN Identifier Acceptance Register 1(CANIDAR1)	R/W
0x0012	MSCAN Identifier Acceptance Register 2 (CANIDAR2)	R/W
0x0013	MSCAN Identifier Acceptance Register 3 (CANIDAR3)	R/W
0x0014	MSCAN Identifier Mask Register 0 (CANIDMR0)	R/W
0x0015	MSCAN Identifier Mask Register 1 (CANIDMR1)	R/W
0x0016	MSCAN Identifier Mask Register 2 (CANIDMR2)	R/W
0x0017	MSCAN Identifier Mask Register 3 (CANIDMR3)	R/W
0x0018	MSCAN Identifier Acceptance Register 4 (CANIDAR4)	R/W
0x0019	MSCAN Identifier Acceptance Register 5 (CANIDAR5)	R/W
0x001A	MSCAN Identifier Acceptance Register 6 (CANIDAR6)	R/W
0x001B	MSCAN Identifier Acceptance Register 7 (CANIDAR7)	R/W
0x001C	MSCAN Identifier Mask Register 4 (CANIDMR4)	R/W
0x001D	MSCAN Identifier Mask Register 5 (CANIDMR5)	R/W
0x001E	MSCAN Identifier Mask Register 6 (CANIDMR6)	R/W
0x001F	MSCAN Identifier Mask Register 7 (CANIDMR7)	R/W
0x0020 -0x002F	Foreground Receive Buffer (CANRXFG)	R[2]
0x0030 -0x003F	Foreground Transmit Buffer (CANTXFG)	R[2]/W

[1] Refer to detailed register description for write access restrictions on per bit basis.

[2] Reserved bits and unused bits within the TX- and RX-buffers (CANTXFG, CANRXFG) will be read as "x", because of RAM-based implementation.

12.3.2 Register Descriptions

This section describes in detail all the registers and register bits in the MSCAN module. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order. All bits of all registers in this module are completely synchronous to internal clocks during a register read.

12.3.2.1 MSCAN Control Register 0 (CANCTL0)

The CANCTL0 register provides various control bits of the MSCAN module as described below.

	7	6	5	4	3	2	1	0
R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
W								
Reset:	0	0	0	0	0	0	0	1

= Unimplemented

Figure 12-3. MSCAN Control Register 0 (CANCTL0)

NOTE

The CANCTL0 register, except WUPE, INITRQ, and SLPRQ, is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Read: Anytime

Write: Anytime when out of initialization mode; exceptions are read-only RXACT and SYNCH, RXFRM (which is set by the module only), and INITRQ (which is also writable in initialization mode).

Table 12-3. CANCTL0 Register Field Descriptions

Field	Description
7 RXFRM[1]	**Received Frame Flag** — This bit is read and clear only. It is set when a receiver has received a valid message correctly, independently of the filter configuration. After it is set, it remains set until cleared by software or reset. Clearing is done by writing a 1. Writing a 0 is ignored. This bit is not valid in loopback mode. 0 No valid message was received since last clearing this flag 1 A valid message was received since last clearing of this flag
6 RXACT	**Receiver Active Status** — This read-only flag indicates the MSCAN is receiving a message. The flag is controlled by the receiver front end. This bit is not valid in loopback mode. 0 MSCAN is transmitting or idle[2] 1 MSCAN is receiving a message (including when arbitration is lost)[2]
5 CSWAI[3]	**CAN Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling all the clocks at the CPU bus interface to the MSCAN module. 0 The module is not affected during wait mode 1 The module ceases to be clocked during wait mode

Table 12-3. CANCTL0 Register Field Descriptions (continued)

Field	Description
4 SYNCH	**Synchronized Status** — This read-only flag indicates whether the MSCAN is synchronized to the CAN bus and able to participate in the communication process. It is set and cleared by the MSCAN. 0 MSCAN is not synchronized to the CAN bus 1 MSCAN is synchronized to the CAN bus
3 TIME	**Timer Enable** — This bit activates an internal 16-bit wide free running timer which is clocked by the bit clock rate. If the timer is enabled, a 16-bit time stamp will be assigned to each transmitted/received message within the active TX/RX buffer. As soon as a message is acknowledged on the CAN bus, the time stamp will be written to the highest bytes (0x000E, 0x000F) in the appropriate buffer (see Section 12.3.3, "Programmer's Model of Message Storage"). The internal timer is reset (all bits set to 0) when disabled. This bit is held low in initialization mode. 0 Disable internal MSCAN timer 1 Enable internal MSCAN timer
2 WUPE[4]	**Wake-Up Enable** — This configuration bit allows the MSCAN to restart from sleep mode when traffic on CAN is detected (see Section 12.4.6.4, "MSCAN Sleep Mode"). 0 Wake-up disabled — The MSCAN ignores traffic on CAN 1 Wake-up enabled — The MSCAN is able to restart
1 SLPRQ[5]	**Sleep Mode Request** — This bit requests the MSCAN to enter sleep mode, which is an internal power saving mode (see Section 12.4.6.4, "MSCAN Sleep Mode"). The sleep mode request is serviced when the CAN bus is idle, i.e., the module is not receiving a message and all transmit buffers are empty. The module indicates entry to sleep mode by setting SLPAK = 1 (see Section 12.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). Sleep mode will be active until SLPRQ is cleared by the CPU or, depending on the setting of WUPE, the MSCAN detects activity on the CAN bus and clears SLPRQ itself. 0 Running — The MSCAN functions normally 1 Sleep mode request — The MSCAN enters sleep mode when CAN bus idle
0 INITRQ[6,7]	**Initialization Mode Request** — When this bit is set by the CPU, the MSCAN skips to initialization mode (see Section 12.4.6.5, "MSCAN Initialization Mode"). Any ongoing transmission or reception is aborted and synchronization to the CAN bus is lost. The module indicates entry to initialization mode by setting INITAK = 1 (Section 12.3.2.2, "MSCAN Control Register 1 (CANCTL1)"). The following registers enter their hard reset state and restore their default values: CANCTL0[8], CANRFLG[9], CANRIER[10], CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0-7, and CANIDMR0-7 can only be written by the CPU when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1). The values of the error counters are not affected by initialization mode. When this bit is cleared by the CPU, the MSCAN restarts and then tries to synchronize to the CAN bus. If the MSCAN is not in bus-off state, it synchronizes after 11 consecutive recessive bits on the CAN bus; if the MSCAN is in bus-off state, it continues to wait for 128 occurrences of 11 consecutive recessive bits. Writing to other bits in CANCTL0, CANRFLG, CANRIER, CANTFLG, or CANTIER must be done only after initialization mode is exited, which is INITRQ = 0 and INITAK = 0. 0 Normal operation 1 MSCAN in initialization mode

1 The MSCAN must be in normal mode for this bit to become set.

2 See the Bosch CAN 2.0A/B specification for a detailed definition of transmitter and receiver states.

3 In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the CPU enters wait (CSWAI = 1) or stop mode (see Section 12.4.6.2, "Operation in Wait Mode" and Section 12.4.6.3, "Operation in Stop Mode").

4 The CPU has to make sure that the WUPE register and the WUPIE wake-up interrupt enable register (see Section 12.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)) is enabled, if the recovery mechanism from stop or wait is required.

5 The CPU cannot clear SLPRQ before the MSCAN has entered sleep mode (SLPRQ = 1 and SLPAK = 1).

6 The CPU cannot clear INITRQ before the MSCAN has entered initialization mode (INITRQ = 1 and INITAK = 1).

7 In order to protect from accidentally violating the CAN protocol, the TXCAN pin is immediately forced to a recessive state when the initialization mode is requested by the CPU. Thus, the recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before requesting initialization mode.

[8] Not including WUPE, INITRQ, and SLPRQ.
[9] TSTAT1 and TSTAT0 are not affected by initialization mode.
[10] RSTAT1 and RSTAT0 are not affected by initialization mode.

12.3.2.2 MSCAN Control Register 1 (CANCTL1)

The CANCTL1 register provides various control bits and handshake status information of the MSCAN module as described below.

Read: Anytime
Write: Anytime when INITRQ = 1 and INITAK = 1, except CANE which is write once in normal and anytime in special system operation modes when the MSCAN is in initialization mode (INITRQ = 1 and INITAK = 1).

Table 12-4. CANCTL1 Register Field Descriptions

Field	Description
7 CANE	**MSCAN Enable** 0 MSCAN module is disabled 1 MSCAN module is enabled
6 CLKSRC	**MSCAN Clock Source** — This bit defines the clock source for the MSCAN module (only for systems with a clock generation module; Section 12.4.3.2, "Clock System," and Section Figure 12-40., "MSCAN Clocking Scheme,"). 0 MSCAN clock source is the oscillator clock 1 MSCAN clock source is the bus clock
5 LOOPB	**Loopback Self Test Mode** — When this bit is set, the MSCAN performs an internal loopback which can be used for self test operation. The bit stream output of the transmitter is fed back to the receiver internally. The RXCAN input pin is ignored and the TXCAN output goes to the recessive state (logic 1). The MSCAN behaves as it does normally when transmitting and treats its own transmitted message as a message received from a remote node. In this state, the MSCAN ignores the bit sent during the ACK slot in the CAN frame acknowledge field to ensure proper reception of its own message. Both transmit and receive interrupts are generated. 0 Loopback self test disabled 1 Loopback self test enabled
4 LISTEN	**Listen Only Mode** — This bit configures the MSCAN as a CAN bus monitor. When LISTEN is set, all valid CAN messages with matching ID are received, but no acknowledgement or error frames are sent out (see Section 12.4.5.4, "Listen-Only Mode"). In addition, the error counters are frozen. Listen only mode supports applications which require "hot plugging" or throughput analysis. The MSCAN is unable to transmit any messages when listen only mode is active. 0 Normal operation 1 Listen only mode activated
2 WUPM	**Wake-Up Mode** — If WUPE in CANCTL0 is enabled, this bit defines whether the integrated low-pass filter is applied to protect the MSCAN from spurious wake-up (see Section 12.4.6.4, "MSCAN Sleep Mode"). 0 MSCAN wakes up the CPU after any recessive to dominant edge on the CAN bus 1 MSCAN wakes up the CPU only in case of a dominant pulse on the CAN bus that has a length of T_{wup}

Table 12-4. CANCTL1 Register Field Descriptions (continued)

Field	Description
1 SLPAK	**Sleep Mode Acknowledge** — This flag indicates whether the MSCAN module has entered sleep mode (see Section 12.4.6.4, "MSCAN Sleep Mode"). It is used as a handshake flag for the SLPRQ sleep mode request. Sleep mode is active when SLPRQ = 1 and SLPAK = 1. Depending on the setting of WUPE, the MSCAN will clear the flag if it detects activity on the CAN bus while in sleep mode. 0 Running — The MSCAN operates normally 1 Sleep mode active — The MSCAN has entered sleep mode
0 INITAK	**Initialization Mode Acknowledge** — This flag indicates whether the MSCAN module is in initialization mode (see Section 12.4.6.5, "MSCAN Initialization Mode"). It is used as a handshake flag for the INITRQ initialization mode request. Initialization mode is active when INITRQ = 1 and INITAK = 1. The registers CANCTL1, CANBTR0, CANBTR1, CANIDAC, CANIDAR0–CANIDAR7, and CANIDMR0–CANIDMR7 can be written only by the CPU when the MSCAN is in initialization mode. 0 Running — The MSCAN operates normally 1 Initialization mode active — The MSCAN has entered initialization mode

12.3.2.3 MSCAN Bus Timing Register 0 (CANBTR0)

The CANBTR0 register configures various CAN bus timing parameters of the MSCAN module.

	7	6	5	4	3	2	1	0
R W	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
Reset:	0	0	0	0	0	0	0	0

Figure 12-4. MSCAN Bus Timing Register 0 (CANBTR0)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-5. CANBTR0 Register Field Descriptions

Field	Description
7:6 SJW[1:0]	**Synchronization Jump Width** — The synchronization jump width defines the maximum number of time quanta (Tq) clock cycles a bit can be shortened or lengthened to achieve resynchronization to data transitions on the CAN bus (see Table 12-6).
5:0 BRP[5:0]	**Baud Rate Prescaler** — These bits determine the time quanta (Tq) clock which is used to build up the bit timing (see Table 12-7).

Table 12-6. Synchronization Jump Width

SJW1	SJW0	Synchronization Jump Width
0	0	1 Tq clock cycle
0	1	2 Tq clock cycles
1	0	3 Tq clock cycles
1	1	4 Tq clock cycles

Table 12-7. Baud Rate Prescaler

BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	Prescaler value (P)
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
:	:	:	:	:	:	:
1	1	1	1	1	1	64

12.3.2.4 MSCAN Bus Timing Register 1 (CANBTR1)

The CANBTR1 register configures various CAN bus timing parameters of the MSCAN module.

	7	6	5	4	3	2	1	0
R W	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
Reset:	0	0	0	0	0	0	0	0

Figure 12-5. MSCAN Bus Timing Register 1 (CANBTR1)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-8. CANBTR1 Register Field Descriptions

Field	Description
7 SAMP	**Sampling** — This bit determines the number of CAN bus samples taken per bit time. 0 One sample per bit. 1 Three samples per bit[1]. If SAMP = 0, the resulting bit value is equal to the value of the single bit positioned at the sample point. If SAMP = 1, the resulting bit value is determined by using majority rule on the three total samples. For higher bit rates, it is recommended that only one sample is taken per bit time (SAMP = 0).
6:4 TSEG2[2:0]	**Time Segment 2** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 12-41). Time segment 2 (TSEG2) values are programmable as shown in Table 12-9.
3:0 TSEG1[3:0]	**Time Segment 1** — Time segments within the bit time fix the number of clock cycles per bit time and the location of the sample point (see Figure 12-41). Time segment 1 (TSEG1) values are programmable as shown in Table 12-10.

[1] In this case, PHASE_SEG1 must be at least 2 time quanta (Tq).

Table 12-9. Time Segment 2 Values

TSEG22	TSEG21	TSEG20	Time Segment 2
0	0	0	1 Tq clock cycle[1]
0	0	1	2 Tq clock cycles
:	:	:	:
1	1	0	7 Tq clock cycles
1	1	1	8 Tq clock cycles

[1] This setting is not valid. Please refer to Table 12-36 for valid settings.

Table 12-10. Time Segment 1 Values

TSEG13	TSEG12	TSEG11	TSEG10	Time segment 1
0	0	0	0	1 Tq clock cycle[1]
0	0	0	1	2 Tq clock cycles[1]
0	0	1	0	3 Tq clock cycles[1]
0	0	1	1	4 Tq clock cycles
:	:	:	:	:
1	1	1	0	15 Tq clock cycles
1	1	1	1	16 Tq clock cycles

1 This setting is not valid. Please refer to Table 12-36 for valid settings.

The bit time is determined by the oscillator frequency, the baud rate prescaler, and the number of time quanta (Tq) clock cycles per bit (as shown in Table 12-9 and Table 12-10).

Eqn. 12-1

$$\text{Bit Time} = \frac{(\text{Prescaler value})}{f_{CANCLK}} \bullet (1 + \text{TimeSegment1} + \text{TimeSegment2})$$

12.3.2.5 MSCAN Receiver Flag Register (CANRFLG)

A flag can be cleared only by software (writing a 1 to the corresponding bit position) when the condition which caused the setting is no longer valid. Every flag has an associated interrupt enable bit in the CANRIER register.

	7	6	5	4	3	2	1	0
R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-6. MSCAN Receiver Flag Register (CANRFLG)

NOTE

The CANRFLG register is held in the reset state[1] when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable again as soon as the initialization mode is exited (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime when out of initialization mode, except RSTAT[1:0] and TSTAT[1:0] flags which are read-only; write of 1 clears flag; write of 0 is ignored.

1. The RSTAT[1:0], TSTAT[1:0] bits are not affected by initialization mode.

Table 12-11. CANRFLG Register Field Descriptions

Field	Description
7 WUPIF	**Wake-Up Interrupt Flag** — If the MSCAN detects CAN bus activity while in sleep mode (see Section 12.4.6.4, "MSCAN Sleep Mode,") and WUPE = 1 in CANTCTL0 (see Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)"), the module will set WUPIF. If not masked, a wake-up interrupt is pending while this flag is set. 0 No wake-up activity observed while in sleep mode 1 MSCAN detected activity on the CAN bus and requested wake-up
6 CSCIF	**CAN Status Change Interrupt Flag** — This flag is set when the MSCAN changes its current CAN bus status due to the actual value of the transmit error counter (TEC) and the receive error counter (REC). An additional 4-bit (RSTAT[1:0], TSTAT[1:0]) status register, which is split into separate sections for TEC/REC, informs the system on the actual CAN bus status (see Section 12.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)"). If not masked, an error interrupt is pending while this flag is set. CSCIF provides a blocking interrupt. That guarantees that the receiver/transmitter status bits (RSTAT/TSTAT) are only updated when no CAN status change interrupt is pending. If the TECs/RECs change their current value after the CSCIF is asserted, which would cause an additional state change in the RSTAT/TSTAT bits, these bits keep their status until the current CSCIF interrupt is cleared again. 0 No change in CAN bus status occurred since last interrupt 1 MSCAN changed current CAN bus status
5:4 RSTAT[1:0]	**Receiver Status Bits** — The values of the error counters control the actual CAN bus status of the MSCAN. As soon as the status change interrupt flag (CSCIF) is set, these bits indicate the appropriate receiver related CAN bus status of the MSCAN. The coding for the bits RSTAT1, RSTAT0 is: 00 RxOK: 0 ≤ receive error counter ≤ 96 01 RxWRN: 96 < receive error counter ≤ 127 10 RxERR: 127 < receive error counter 11 Bus-off[1]: transmit error counter > 255
3:2 TSTAT[1:0]	**Transmitter Status Bits** — The values of the error counters control the actual CAN bus status of the MSCAN. As soon as the status change interrupt flag (CSCIF) is set, these bits indicate the appropriate transmitter related CAN bus status of the MSCAN. The coding for the bits TSTAT1, TSTAT0 is: 00 TxOK: 0 ≤ transmit error counter ≤ 96 01 TxWRN: 96 < transmit error counter ≤ 127 10 TxERR: 127 < transmit error counter ≤ 255 11 Bus-Off: transmit error counter > 255
1 OVRIF	**Overrun Interrupt Flag** — This flag is set when a data overrun condition occurs. If not masked, an error interrupt is pending while this flag is set. 0 No data overrun condition 1 A data overrun detected
0 RXF[2]	**Receive Buffer Full Flag** — RXF is set by the MSCAN when a new message is shifted in the receiver FIFO. This flag indicates whether the shifted buffer is loaded with a correctly received message (matching identifier, matching cyclic redundancy code (CRC) and no other errors detected). After the CPU has read that message from the RxFG buffer in the receiver FIFO, the RXF flag must be cleared to release the buffer. A set RXF flag prohibits the shifting of the next FIFO entry into the foreground buffer (RxFG). If not masked, a receive interrupt is pending while this flag is set. 0 No new message available within the RxFG 1 The receiver FIFO is not empty. A new message is available in the RxFG

1 Redundant Information for the most critical CAN bus status which is "bus-off". This only occurs if the Tx error counter exceeds a number of 255 errors. Bus-off affects the receiver state. As soon as the transmitter leaves its bus-off state the receiver state skips to RxOK too. Refer also to TSTAT[1:0] coding in this register.

2 To ensure data integrity, do not read the receive buffer registers while the RXF flag is cleared. For MCUs with dual CPUs, reading the receive buffer registers while the RXF flag is cleared may result in a CPU fault condition.

12.3.2.6 MSCAN Receiver Interrupt Enable Register (CANRIER)

This register contains the interrupt enable bits for the interrupt flags described in the CANRFLG register.

	7	6	5	4	3	2	1	0
R W	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
Reset:	0	0	0	0	0	0	0	0

Figure 12-7. MSCAN Receiver Interrupt Enable Register (CANRIER)

NOTE

The CANRIER register is held in the reset state when the initialization mode is active (INITRQ=1 and INITAK=1). This register is writable when not in initialization mode (INITRQ=0 and INITAK=0).

The RSTATE[1:0], TSTATE[1:0] bits are not affected by initialization mode.

Read: Anytime
Write: Anytime when not in initialization mode

Table 12-12. CANRIER Register Field Descriptions

Field	Description
7 WUPIE[1]	**Wake-Up Interrupt Enable** 0 No interrupt request is generated from this event. 1 A wake-up event causes a Wake-Up interrupt request.
6 CSCIE	**CAN Status Change Interrupt Enable** 0 No interrupt request is generated from this event. 1 A CAN Status Change event causes an error interrupt request.
5:4 RSTATE[1:0]	**Receiver Status Change Enable** — These RSTAT enable bits control the sensitivity level in which receiver state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level the RSTAT flags continue to indicate the actual receiver state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by receiver state changes. 01 Generate CSCIF interrupt only if the receiver enters or leaves "bus-off" state. Discard other receiver state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the receiver enters or leaves "RxErr" or "bus-off"[2] state. Discard other receiver state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.
3:2 TSTATE[1:0]	**Transmitter Status Change Enable** — These TSTAT enable bits control the sensitivity level in which transmitter state changes are causing CSCIF interrupts. Independent of the chosen sensitivity level, the TSTAT flags continue to indicate the actual transmitter state and are only updated if no CSCIF interrupt is pending. 00 Do not generate any CSCIF interrupt caused by transmitter state changes. 01 Generate CSCIF interrupt only if the transmitter enters or leaves "bus-off" state. Discard other transmitter state changes for generating CSCIF interrupt. 10 Generate CSCIF interrupt only if the transmitter enters or leaves "TxErr" or "bus-off" state. Discard other transmitter state changes for generating CSCIF interrupt. 11 Generate CSCIF interrupt on all state changes.

Table 12-12. CANRIER Register Field Descriptions (continued)

Field	Description
1 OVRIE	**Overrun Interrupt Enable** 0 No interrupt request is generated from this event. 1 An overrun event causes an error interrupt request.
0 RXFIE	**Receiver Full Interrupt Enable** 0 No interrupt request is generated from this event. 1 A receive buffer full (successful message reception) event causes a receiver interrupt request.

1 WUPIE and WUPE (see Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)") must both be enabled if the recovery mechanism from stop or wait is required.

2 Bus-off state is defined by the CAN standard (see Bosch CAN 2.0A/B protocol specification: for only transmitters. Because the only possible state change for the transmitter from bus-off to TxOK also forces the receiver to skip its current state to RxOK, the coding of the RXSTAT[1:0] flags define an additional bus-off state for the receiver (see Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

12.3.2.7 MSCAN Transmitter Flag Register (CANTFLG)

The transmit buffer empty flags each have an associated interrupt enable bit in the CANTIER register.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXE2	TXE1	TXE0
W								
Reset:	0	0	0	0	0	1	1	1

= Unimplemented

Figure 12-8. MSCAN Transmitter Flag Register (CANTFLG)

NOTE

The CANTFLG register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime for TXEx flags when not in initialization mode; write of 1 clears flag, write of 0 is ignored

Table 12-13. CANTFLG Register Field Descriptions

Field	Description
2:0 TXE[2:0]	**Transmitter Buffer Empty** — This flag indicates that the associated transmit message buffer is empty, and thus not scheduled for transmission. The CPU must clear the flag after a message is set up in the transmit buffer and is due for transmission. The MSCAN sets the flag after the message is sent successfully. The flag is also set by the MSCAN when the transmission request is successfully aborted due to a pending abort request (see Section 12.3.2.9, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). If not masked, a transmit interrupt is pending while this flag is set. Clearing a TXEx flag also clears the corresponding ABTAKx (see Section 12.3.2.10, "MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)"). When a TXEx flag is set, the corresponding ABTRQx bit is cleared (see Section 12.3.2.9, "MSCAN Transmitter Message Abort Request Register (CANTARQ)"). When listen-mode is active (see Section 12.3.2.2, "MSCAN Control Register 1 (CANCTL1)") the TXEx flags cannot be cleared and no transmission is started. Read and write accesses to the transmit buffer will be blocked, if the corresponding TXEx bit is cleared (TXEx = 0) and the buffer is scheduled for transmission. 0 The associated message buffer is full (loaded with a message due for transmission) 1 The associated message buffer is empty (not scheduled)

12.3.2.8 MSCAN Transmitter Interrupt Enable Register (CANTIER)

This register contains the interrupt enable bits for the transmit buffer empty interrupt flags.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-9. MSCAN Transmitter Interrupt Enable Register (CANTIER)

NOTE

The CANTIER register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime when not in initialization mode

Table 12-14. CANTIER Register Field Descriptions

Field	Description
2:0 TXEIE[2:0]	**Transmitter Empty Interrupt Enable** 0 No interrupt request is generated from this event. 1 A transmitter empty (transmit buffer available for transmission) event causes a transmitter empty interrupt request.

12.3.2.9 MSCAN Transmitter Message Abort Request Register (CANTARQ)

The CANTARQ register allows abort request of queued messages as described below.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-10. MSCAN Transmitter Message Abort Request Register (CANTARQ)

NOTE

The CANTARQ register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Read: Anytime
Write: Anytime when not in initialization mode

Table 12-15. CANTARQ Register Field Descriptions

Field	Description
2:0 ABTRQ[2:0]	**Abort Request** — The CPU sets the ABTRQx bit to request that a scheduled message buffer (TXEx = 0) be aborted. The MSCAN grants the request if the message has not already started transmission, or if the transmission is not successful (lost arbitration or error). When a message is aborted, the associated TXE (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and abort acknowledge flags (ABTAK, see Section 12.3.2.10, "MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)") are set and a transmit interrupt occurs if enabled. The CPU cannot reset ABTRQx. ABTRQx is reset whenever the associated TXE flag is set. 0 No abort request 1 Abort request pending

12.3.2.10 MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

The CANTAAK register indicates the successful abort of a queued message, if requested by the appropriate bits in the CANTARQ register.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-11. MSCAN Transmitter Message Abort Acknowledge Register (CANTAAK)

NOTE

The CANTAAK register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK = 1).

Read: Anytime
Write: Unimplemented for ABTAKx flags

Table 12-16. CANTAAK Register Field Descriptions

Field	Description
2:0 ABTAK[2:0]	**Abort Acknowledge** — This flag acknowledges that a message was aborted due to a pending abort request from the CPU. After a particular message buffer is flagged empty, this flag can be used by the application software to identify whether the message was aborted successfully or was sent anyway. The ABTAKx flag is cleared whenever the corresponding TXE flag is cleared. 0 The message was not aborted. 1 The message was aborted.

12.3.2.11 MSCAN Transmit Buffer Selection Register (CANTBSEL)

The CANTBSEL register allows the selection of the actual transmit message buffer, which then will be accessible in the CANTXFG register space.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	TX2	TX1	TX0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-12. MSCAN Transmit Buffer Selection Register (CANTBSEL)

NOTE

The CANTBSEL register is held in the reset state when the initialization mode is active (INITRQ = 1 and INITAK=1). This register is writable when not in initialization mode (INITRQ = 0 and INITAK = 0).

Read: Find the lowest ordered bit set to 1, all other bits will be read as 0
Write: Anytime when not in initialization mode

Table 12-17. CANTBSEL Register Field Descriptions

Field	Description
2:0 TX[2:0]	**Transmit Buffer Select** — The lowest numbered bit places the respective transmit buffer in the CANTXFG register space (e.g., TX1 = 1 and TX0 = 1 selects transmit buffer TX0; TX1 = 1 and TX0 = 0 selects transmit buffer TX1). Read and write accesses to the selected transmit buffer will be blocked, if the corresponding TXEx bit is cleared and the buffer is scheduled for transmission (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)"). 0 The associated message buffer is deselected 1 The associated message buffer is selected, if lowest numbered bit

The following gives a short programming example of the usage of the CANTBSEL register:

To get the next available transmit buffer, application software must read the CANTFLG register and write this value back into the CANTBSEL register. In this example Tx buffers TX1 and TX2 are available. The value read from CANTFLG is therefore 0b0000_0110. When writing this value back to CANTBSEL, the Tx buffer TX1 is selected in the CANTXFG because the lowest numbered bit set to 1 is at bit position 1. Reading back this value out of CANTBSEL results in 0b0000_0010, because only the lowest numbered bit position set to 1 is presented. This mechanism eases the application software the selection of the next available Tx buffer.

- LDD CANTFLG; value read is 0b0000_0110
- STD CANTBSEL; value written is 0b0000_0110
- LDD CANTBSEL; value read is 0b0000_0010

If all transmit message buffers are deselected, no accesses are allowed to the CANTXFG registers.

12.3.2.12 MSCAN Identifier Acceptance Control Register (CANIDAC)

The CANIDAC register is used for identifier acceptance control as described below.

	7	6	5	4	3	2	1	0
R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-13. MSCAN Identifier Acceptance Control Register (CANIDAC)

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1), except bits IDHITx, which are read-only

Table 12-18. CANIDAC Register Field Descriptions

Field	Description
5:4 IDAM[1:0]	**Identifier Acceptance Mode** — The CPU sets these flags to define the identifier acceptance filter organization (see Section 12.4.3, "Identifier Acceptance Filter"). Table 12-19 summarizes the different settings. In filter closed mode, no message is accepted such that the foreground buffer is never reloaded.
2:0 IDHIT[2:0]	Identifier Acceptance Hit Indicator — The MSCAN sets these flags to indicate an identifier acceptance hit (see Section 12.4.3, "Identifier Acceptance Filter"). Table 12-20 summarizes the different settings.

Table 12-19. Identifier Acceptance Mode Settings

IDAM1	IDAM0	Identifier Acceptance Mode
0	0	Two 32-bit acceptance filters
0	1	Four 16-bit acceptance filters
1	0	Eight 8-bit acceptance filters
1	1	Filter closed

Table 12-20. Identifier Acceptance Hit Indication

IDHIT2	IDHIT1	IDHIT0	Identifier Acceptance Hit
0	0	0	Filter 0 hit
0	0	1	Filter 1 hit
0	1	0	Filter 2 hit
0	1	1	Filter 3 hit
1	0	0	Filter 4 hit
1	0	1	Filter 5 hit
1	1	0	Filter 6 hit
1	1	1	Filter 7 hit

The IDHITx indicators are always related to the message in the foreground buffer (RxFG). When a message gets shifted into the foreground buffer of the receiver FIFO the indicators are updated as well.

12.3.2.13 MSCAN Reserved Register

reserved for factory testing of the MSCAN module and is not available in normal system operation modes.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-14. MSCAN Reserved Register

Read: Always read 0x0000 in normal system operation modes
Write: Unimplemented in normal system operation modes

NOTE

Writing to this register when in special modes can alter the MSCAN functionality.

12.3.2.14 MSCAN Receive Error Counter (CANRXERR)

This register reflects the status of the MSCAN receive error counter.

	7	6	5	4	3	2	1	0
R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-15. MSCAN Receive Error Counter (CANRXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

12.3.2.15 MSCAN Transmit Error Counter (CANTXERR)

This register reflects the status of the MSCAN transmit error counter.

	7	6	5	4	3	2	1	0
R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
W								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-16. MSCAN Transmit Error Counter (CANTXERR)

Read: Only when in sleep mode (SLPRQ = 1 and SLPAK = 1) or initialization mode (INITRQ = 1 and INITAK = 1)

Write: Unimplemented

NOTE

Reading this register when in any other mode other than sleep or initialization mode, may return an incorrect value. For MCUs with dual CPUs, this may result in a CPU fault condition.

Writing to this register when in special modes can alter the MSCAN functionality.

12.3.2.16 MSCAN Identifier Acceptance Registers (CANIDAR0-7)

On reception, each message is written into the background receive buffer. The CPU is only signalled to read the message if it passes the criteria in the identifier acceptance and identifier mask registers (accepted); otherwise, the message is overwritten by the next message (dropped).

The acceptance registers of the MSCAN are applied on the IDR0–IDR3 registers (see Section 12.3.3.1, "Identifier Registers (IDR0–IDR3)") of incoming messages in a bit by bit manner (see Section 12.4.3, "Identifier Acceptance Filter").

For extended identifiers, all four acceptance and mask registers are applied. For standard identifiers, only the first two (CANIDAR0/1, CANIDMR0/1) are applied.

Module Base + 0x0010 (CANIDAR0)
0x0011 (CANIDAR1)
0x0012 (CANIDAR2)
0x0013 (CANIDAR3)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 12-17. MSCAN Identifier Acceptance Registers (First Bank) — CANIDAR0–CANIDAR3

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-21. CANIDAR0–CANIDAR3 Register Field Descriptions

Field	Description
7:0 AC[7:0]	**Acceptance Code Bits** — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

Module Base + 0x0018 (CANIDAR4)
0x0019 (CANIDAR5)
0x001A (CANIDAR6)
0x001B (CANIDAR7)

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
Reset	0	0	0	0	0	0	0	0

Figure 12-18. MSCAN Identifier Acceptance Registers (Second Bank) — CANIDAR4–CANIDAR7

Read: Anytime

Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-22. CANIDAR4–CANIDAR7 Register Field Descriptions

Field	Description
7:0 AC[7:0]	**Acceptance Code Bits** — AC[7:0] comprise a user-defined sequence of bits with which the corresponding bits of the related identifier register (IDRn) of the receive message buffer are compared. The result of this comparison is then masked with the corresponding identifier mask register.

12.3.2.17 MSCAN Identifier Mask Registers (CANIDMR0–CANIDMR7)

The identifier mask register specifies which of the corresponding bits in the identifier acceptance register are relevant for acceptance filtering. To receive standard identifiers in 32 bit filter mode, it is required to program the last three bits (AM[2:0]) in the mask registers CANIDMR1 and CANIDMR5 to "don't care." To receive standard identifiers in 16 bit filter mode, it is required to program the last three bits (AM[2:0]) in the mask registers CANIDMR1, CANIDMR3, CANIDMR5, and CANIDMR7 to "don't care."

Module Base + 0x0014 (CANIDMR0)
0x0015 (CANIDMR1)
0x0016 (CANIDMR2)
0x0017 (CANIDMR3)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 12-19. MSCAN Identifier Mask Registers (First Bank) — CANIDMR0–CANIDMR3

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-23. CANIDMR0–CANIDMR3 Register Field Descriptions

Field	Description
7:0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

Module Base + 0x001C (CANIDMR4)
0x001D (CANIDMR5)
0x001E (CANIDMR6)
0x001F (CANIDMR7)

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Reset	0	0	0	0	0	0	0	0

Figure 12-20. MSCAN Identifier Mask Registers (Second Bank) — CANIDMR4–CANIDMR7

Read: Anytime
Write: Anytime in initialization mode (INITRQ = 1 and INITAK = 1)

Table 12-24. CANIDMR4–CANIDMR7 Register Field Descriptions

Field	Description
7:0 AM[7:0]	**Acceptance Mask Bits** — If a particular bit in this register is cleared, this indicates that the corresponding bit in the identifier acceptance register must be the same as its identifier bit before a match is detected. The message is accepted if all such bits match. If a bit is set, it indicates that the state of the corresponding bit in the identifier acceptance register does not affect whether or not the message is accepted. 0 Match corresponding acceptance code register and identifier bits 1 Ignore corresponding acceptance code register bit

12.3.3 Programmer's Model of Message Storage

The following section details the organization of the receive and transmit message buffers and the associated control registers.

To simplify the programmer interface, the receive and transmit message buffers have the same outline. Each message buffer allocates 16 bytes in the memory map containing a 13 byte data structure.

An additional transmit buffer priority register (TBPR) is defined for the transmit buffers. Within the last two bytes of this memory map, the MSCAN stores a special 16-bit time stamp, which is sampled from an internal timer after successful transmission or reception of a message. This feature is only available for transmit and receiver buffers, if the TIME bit is set (see Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)").

The time stamp register is written by the MSCAN. The CPU can only read these registers.

Table 12-25. Message Buffer Organization

Offset Address	Register	Access
0x00X0	Identifier Register 0	
0x00X1	Identifier Register 1	
0x00X2	Identifier Register 2	
0x00X3	Identifier Register 3	
0x00X4	Data Segment Register 0	
0x00X5	Data Segment Register 1	
0x00X6	Data Segment Register 2	
0x00X7	Data Segment Register 3	
0x00X8	Data Segment Register 4	
0x00X9	Data Segment Register 5	
0x00XA	Data Segment Register 6	
0x00XB	Data Segment Register 7	
0x00XC	Data Length Register	
0x00XD	Transmit Buffer Priority Register[1]	
0x00XE	Time Stamp Register (High Byte)[2]	
0x00XF	Time Stamp Register (Low Byte)[3]	

1 Not applicable for receive buffers
2 Read-only for CPU
3 Read-only for CPU

Figure 12-21 shows the common 13-byte data structure of receive and transmit buffers for extended identifiers. The mapping of standard identifiers into the IDR registers is shown in Figure 12-22.

All bits of the receive and transmit buffers are 'x' out of reset because of RAM-based implementation[1]. All reserved or unused bits of the receive and transmit buffers always read 'x'.

1. Exception: The transmit priority registers are 0 out of reset.

Register Name		Bit 7	6	5	4	3	2	1	Bit0
IDR0	R W	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
IDR1	R W	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
IDR2	R W	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
IDR3	R W	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
DSR0	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR1	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR2	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR3	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR4	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR5	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR6	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DSR7	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
DLR	R W					DLC3	DLC2	DLC1	DLC0

= Unused, always read 'x'

Figure 12-21. Receive/Transmit Message Buffer — Extended Identifier Mapping

Read: For transmit buffers, anytime when TXEx flag is set (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)"). For receive buffers, only when RXF flag is set (see Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)").

Write: For transmit buffers, anytime when TXEx flag is set (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)"). Unimplemented for receive buffers.

Reset: Undefined (0x00XX) because of RAM-based implementation

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
IDR0	R W	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
IDR1	R W	ID2	ID1	ID0	RTR	IDE (=0)			
IDR2	R W								
IDR3	R W								

= Unused, always read 'x'

Figure 12-22. Receive/Transmit Message Buffer — Standard Identifier Mapping

12.3.3.1 Identifier Registers (IDR0–IDR3)

The identifier registers for an extended format identifier consist of a total of 32 bits; ID[28:0], SRR, IDE, and RTR bits. The identifier registers for a standard format identifier consist of a total of 13 bits; ID[10:0], RTR, and IDE bits.

12.3.3.1.1 IDR0–IDR3 for Extended Identifier Mapping

	7	6	5	4	3	2	1	0
R W	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
Reset:	x	x	x	x	x	x	x	x

Figure 12-23. Identifier Register 0 (IDR0) — Extended Identifier Mapping

Table 12-26. IDR0 Register Field Descriptions — Extended

Field	Description
7:0 ID[28:21]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

	7	6	5	4	3	2	1	0
R W	ID20	ID19	ID18	SRR (=1)	IDE (=1)	ID17	ID16	ID15
Reset:	x	x	x	x	x	x	x	x

Figure 12-24. Identifier Register 1 (IDR1) — Extended Identifier Mapping

Table 12-27. IDR1 Register Field Descriptions — Extended

Field	Description
7:5 ID[20:18]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
4 SRR	**Substitute Remote Request** — This fixed recessive bit is used only in extended format. It must be set to 1 by the user for transmission buffers and is stored as received on the CAN bus for receive buffers.
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)
2:0 ID[17:15]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

	7	6	5	4	3	2	1	0
R W	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
Reset:	x	x	x	x	x	x	x	x

Figure 12-25. Identifier Register 2 (IDR2) — Extended Identifier Mapping

Table 12-28. IDR2 Register Field Descriptions — Extended

Field	Description
7:0 ID[14:7]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.

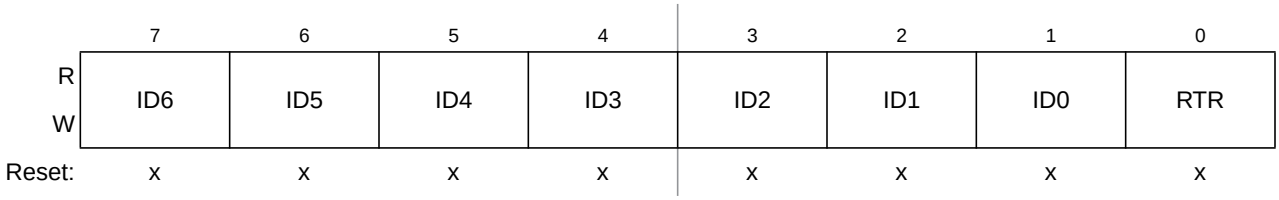


Figure 12-26. Identifier Register 3 (IDR3) — Extended Identifier Mapping

Table 12-29. IDR3 Register Field Descriptions — Extended

Field	Description
7:1 ID[6:0]	**Extended Format Identifier —** The identifiers consist of 29 bits (ID[28:0]) for the extended format. ID28 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number.
0 RTR	**Remote Transmission Request** — This flag reflects the status of the remote transmission request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame

12.3.3.1.2 IDR0–IDR3 for Standard Identifier Mapping

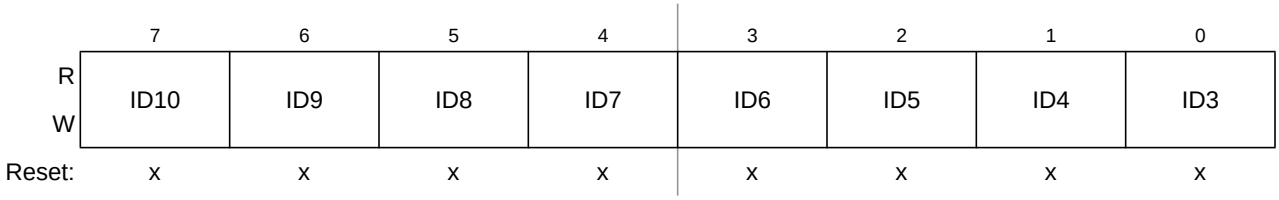


Figure 12-27. Identifier Register 0 — Standard Mapping

Table 12-30. IDR0 Register Field Descriptions — Standard

Field	Description
7:0 ID[10:3]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 12-31.

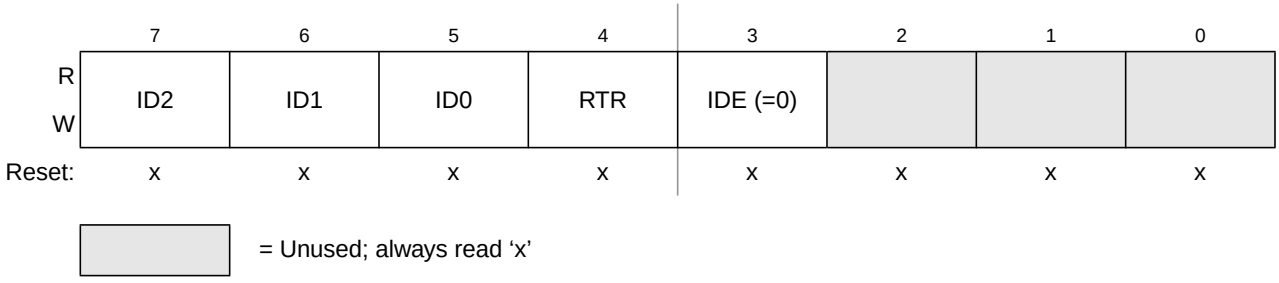


Figure 12-28. Identifier Register 1 — Standard Mapping

Table 12-31. IDR1 Register Field Descriptions

Field	Description
7:5 ID[2:0]	**Standard Format Identifier —** The identifiers consist of 11 bits (ID[10:0]) for the standard format. ID10 is the most significant bit and is transmitted first on the CAN bus during the arbitration procedure. The priority of an identifier is defined to be highest for the smallest binary number. See also ID bits in Table 12-30.
4 RTR	**Remote Transmission Request** — This flag reflects the status of the Remote Transmission Request bit in the CAN frame. In the case of a receive buffer, it indicates the status of the received frame and supports the transmission of an answering frame in software. In the case of a transmit buffer, this flag defines the setting of the RTR bit to be sent. 0 Data frame 1 Remote frame
3 IDE	**ID Extended** — This flag indicates whether the extended or standard identifier format is applied in this buffer. In the case of a receive buffer, the flag is set as received and indicates to the CPU how to process the buffer identifier registers. In the case of a transmit buffer, the flag indicates to the MSCAN what type of identifier to send. 0 Standard format (11 bit) 1 Extended format (29 bit)

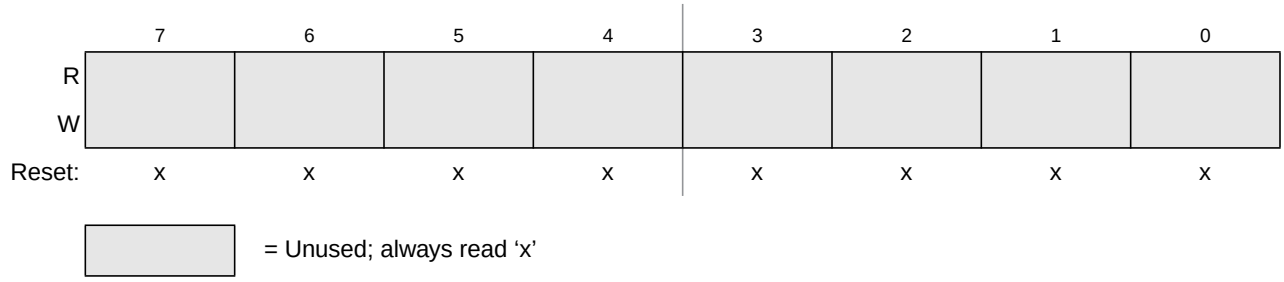


Figure 12-29. Identifier Register 2 — Standard Mapping

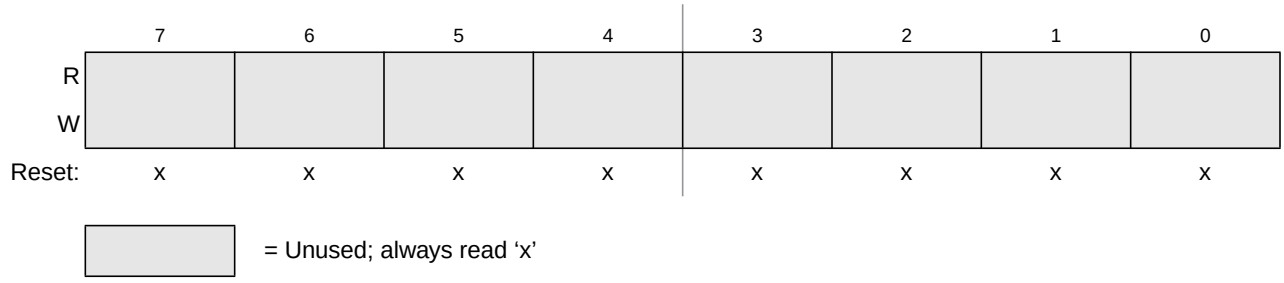


Figure 12-30. Identifier Register 3 — Standard Mapping

12.3.3.2 Data Segment Registers (DSR0-7)

The eight data segment registers, each with bits DB[7:0], contain the data to be transmitted or received. The number of bytes to be transmitted or received is determined by the data length code in the corresponding DLR register.

Module Base + 0x0004 (DSR0)
0x0005 (DSR1)
0x0006 (DSR2)
0x0007 (DSR3)
0x0008 (DSR4)
0x0009 (DSR5)
0x000A (DSR6)
0x000B (DSR7)

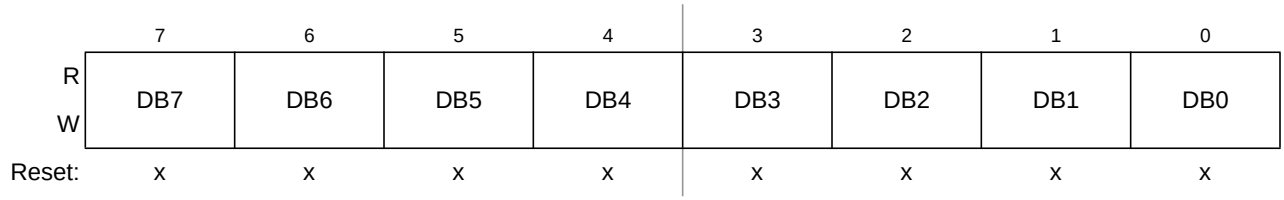


Figure 12-31. Data Segment Registers (DSR0–DSR7) — Extended Identifier Mapping

Table 12-32. DSR0–DSR7 Register Field Descriptions

Field	Description
7:0 DB[7:0]	**Data bits 7:0**

12.3.3.3 Data Length Register (DLR)

This register keeps the data length field of the CAN frame.

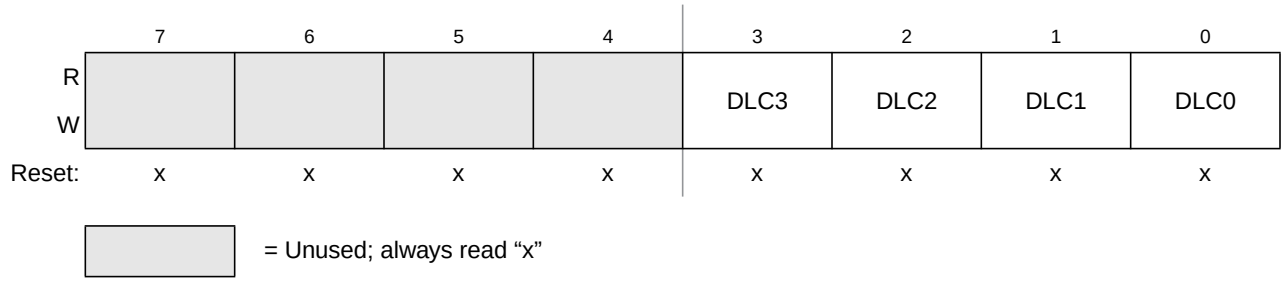


Figure 12-32. Data Length Register (DLR) — Extended Identifier Mapping

Table 12-33. DLR Register Field Descriptions

Field	Description
3:0 DLC[3:0]	**Data Length Code Bits** — The data length code contains the number of bytes (data byte count) of the respective message. During the transmission of a remote frame, the data length code is transmitted as programmed while the number of transmitted data bytes is always 0. The data byte count ranges from 0 to 8 for a data frame. Table 12-34 shows the effect of setting the DLC bits.

Table 12-34. Data Length Codes

Data Length Code				Data Byte Count
DLC3	DLC2	DLC1	DLC0	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8

12.3.3.4 Transmit Buffer Priority Register (TBPR)

This register defines the local priority of the associated message buffer. The local priority is used for the internal prioritization process of the MSCAN and is defined to be highest for the smallest binary number. The MSCAN implements the following internal prioritization mechanisms:

- All transmission buffers with a cleared TXEx flag participate in the prioritization immediately before the SOF (start of frame) is sent.
- The transmission buffer with the lowest local priority field wins the prioritization.

In cases of more than one buffer having the same lowest priority, the message buffer with the lower index number wins.

	7	6	5	4	3	2	1	0
R W	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
Reset:	0	0	0	0	0	0	0	0

Figure 12-33. Transmit Buffer Priority Register (TBPR)

Read: Anytime when TXEx flag is set (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Anytime when TXEx flag is set (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

12.3.3.5 Time Stamp Register (TSRH–TSRL)

If the TIME bit is enabled, the MSCAN will write a special time stamp to the respective registers in the active transmit or receive buffer as soon as a message has been acknowledged on the CAN bus (see

Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)"). The time stamp is written on the bit sample point for the recessive bit of the ACK delimiter in the CAN frame. In case of a transmission, the CPU can only read the time stamp after the respective transmit buffer has been flagged empty.

The timer value, which is used for stamping, is taken from a free running internal CAN bit clock. A timer overrun is not indicated by the MSCAN. The timer is reset (all bits set to 0) during initialization mode. The CPU can only read the time stamp registers.

	7	6	5	4	3	2	1	0
R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
W								
Reset:	x	x	x	x	x	x	x	x

Figure 12-34. Time Stamp Register — High Byte (TSRH)

	7	6	5	4	3	2	1	0
R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
W								
Reset:	x	x	x	x	x	x	x	x

Figure 12-35. Time Stamp Register — Low Byte (TSRL)

Read: Anytime when TXEx flag is set (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)") and the corresponding transmit buffer is selected in CANTBSEL (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)").

Write: Unimplemented

12.4 Functional Description

12.4.1 General

This section provides a complete functional description of the MSCAN. It describes each of the features and modes listed in the introduction.

12.4.2 Message Storage

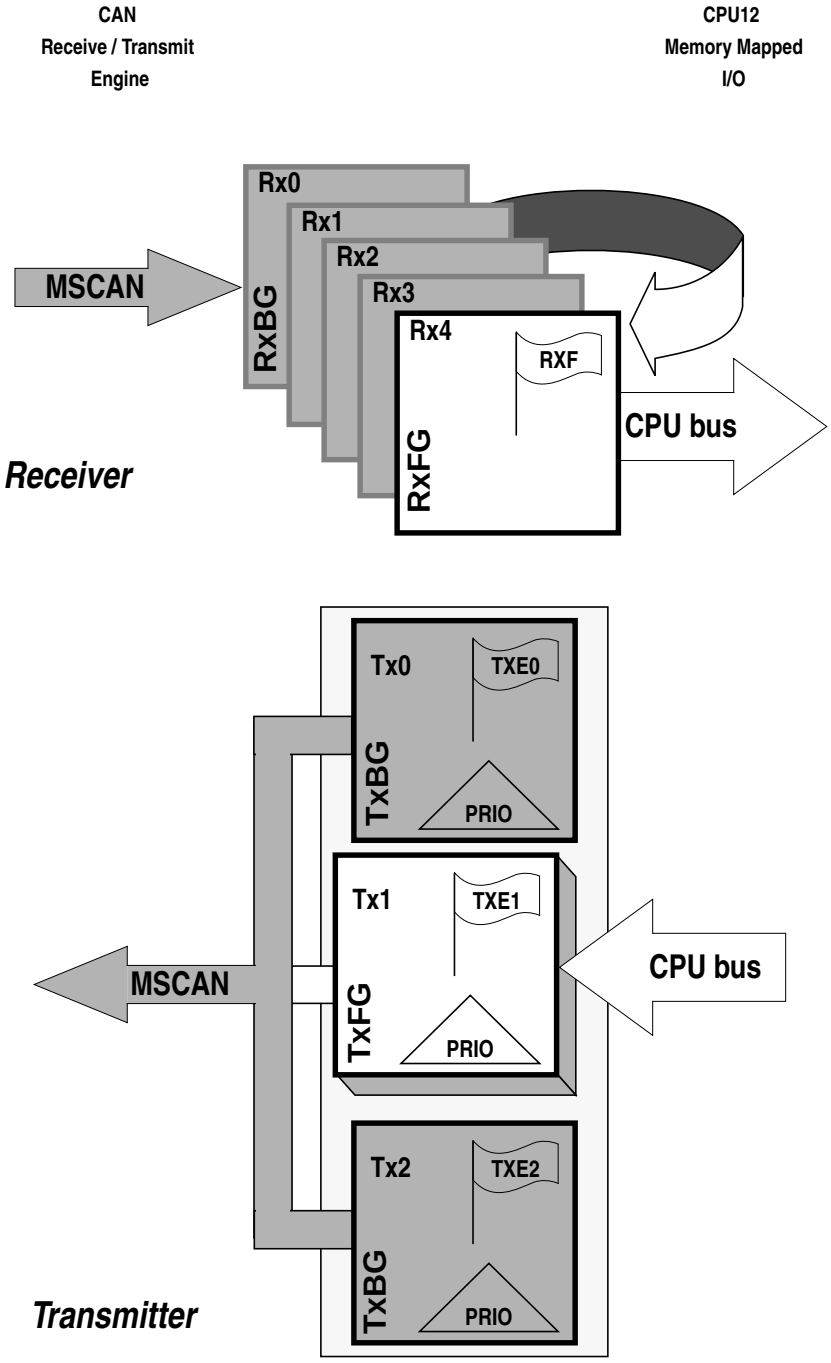


Figure 12-36. User Model for Message Buffer Organization

MSCAN facilitates a sophisticated message storage system which addresses the requirements of a broad range of network applications.

12.4.2.1 Message Transmit Background

Modern application layer software is built upon two fundamental assumptions:

- Any CAN node is able to send out a stream of scheduled messages without releasing the CAN bus between the two messages. Such nodes arbitrate for the CAN bus immediately after sending the previous message and only release the CAN bus in case of lost arbitration.
- The internal message queue within any CAN node is organized such that the highest priority message is sent out first, if more than one message is ready to be sent.

The behavior described in the bullets above cannot be achieved with a single transmit buffer. That buffer must be reloaded immediately after the previous message is sent. This loading process lasts a finite amount of time and must be completed within the inter-frame sequence (IFS) to be able to send an uninterrupted stream of messages. Even if this is feasible for limited CAN bus speeds, it requires that the CPU reacts with short latencies to the transmit interrupt.

A double buffer scheme de-couples the reloading of the transmit buffer from the actual message sending and, therefore, reduces the reactiveness requirements of the CPU. Problems can arise if the sending of a message is finished while the CPU re-loads the second buffer. No buffer would then be ready for transmission, and the CAN bus would be released.

At least three transmit buffers are required to meet the first of the above requirements under all circumstances. The MSCAN has three transmit buffers.

The second requirement calls for some sort of internal prioritization which the MSCAN implements with the "local priority" concept described in Section 12.4.2.2, "Transmit Structures."

12.4.2.2 Transmit Structures

The MSCAN triple transmit buffer scheme optimizes real-time performance by allowing multiple messages to be set up in advance. The three buffers are arranged as shown in Figure 12-36.

All three buffers have a 13-byte data structure similar to the outline of the receive buffers (see Section 12.3.3, "Programmer's Model of Message Storage"). An additional Section 12.3.3.4, "Transmit Buffer Priority Register (TBPR) contains an 8-bit local priority field (PRIO) (see Section 12.3.3.4, "Transmit Buffer Priority Register (TBPR)"). The remaining two bytes are used for time stamping of a message, if required (see Section 12.3.3.5, "Time Stamp Register (TSRH–TSRL)").

To transmit a message, the CPU must identify an available transmit buffer, which is indicated by a set transmitter buffer empty (TXEx) flag (see Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)"). If a transmit buffer is available, the CPU must set a pointer to this buffer by writing to the CANTBSEL register (see Section 12.3.2.11, "MSCAN Transmit Buffer Selection Register (CANTBSEL)"). This makes the respective buffer accessible within the CANTXFG address space (see Section 12.3.3, "Programmer's Model of Message Storage"). The algorithmic feature associated with the CANTBSEL register simplifies the transmit buffer selection. In addition, this scheme makes the handler software simpler because only one address area is applicable for the transmit process, and the required address space is minimized.

The CPU then stores the identifier, the control bits, and the data content into one of the transmit buffers. Finally, the buffer is flagged as ready for transmission by clearing the associated TXE flag.

The MSCAN then schedules the message for transmission and signals the successful transmission of the buffer by setting the associated TXE flag. A transmit interrupt (see Section 12.4.8.2, "Transmit Interrupt") is generated[1] when TXEx is set and can be used to drive the application software to re-load the buffer.

If more than one buffer is scheduled for transmission when the CAN bus becomes available for arbitration, the MSCAN uses the local priority setting of the three buffers to determine the prioritization. For this purpose, every transmit buffer has an 8-bit local priority field (PRIO). The application software programs this field when the message is set up. The local priority reflects the priority of this particular message relative to the set of messages being transmitted from this node. The lowest binary value of the PRIO field is defined to be the highest priority. The internal scheduling process takes place whenever the MSCAN arbitrates for the CAN bus. This is also the case after the occurrence of a transmission error.

When a high priority message is scheduled by the application software, it may become necessary to abort a lower priority message in one of the three transmit buffers. Because messages that are already in transmission cannot be aborted, the user must request the abort by setting the corresponding abort request bit (ABTRQ) (see Section 12.3.2.9, "MSCAN Transmitter Message Abort Request Register (CANTARQ)".) The MSCAN then grants the request, if possible, by:

1. Setting the corresponding abort acknowledge flag (ABTAK) in the CANTAAK register.
2. Setting the associated TXE flag to release the buffer.
3. Generating a transmit interrupt. The transmit interrupt handler software can determine from the setting of the ABTAK flag whether the message was aborted (ABTAK = 1) or sent (ABTAK = 0).

12.4.2.3 Receive Structures

The received messages are stored in a five stage input FIFO. The five message buffers are alternately mapped into a single memory area (see Figure 12-36). The background receive buffer (RxBG) is exclusively associated with the MSCAN, but the foreground receive buffer (RxFG) is addressable by the CPU (see Figure 12-36). This scheme simplifies the handler software because only one address area is applicable for the receive process.

All receive buffers have a size of 15 bytes to store the CAN control bits, the identifier (standard or extended), the data contents, and a time stamp, if enabled (see Section 12.3.3, "Programmer's Model of Message Storage").

The receiver full flag (RXF) (see Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)") signals the status of the foreground receive buffer. When the buffer contains a correctly received message with a matching identifier, this flag is set.

On reception, each message is checked to see whether it passes the filter (see Section 12.4.3, "Identifier Acceptance Filter") and simultaneously is written into the active RxBG. After successful reception of a valid message, the MSCAN shifts the content of RxBG into the receiver FIFO[2], sets the RXF flag, and generates a receive interrupt (see Section 12.4.8.3, "Receive Interrupt") to the CPU[3]. The user's receive handler must read the received message from the RxFG and then reset the RXF flag to acknowledge the interrupt and to release the foreground buffer. A new message, which can follow immediately after the IFS

1. The transmit interrupt occurs only if not masked. A polling scheme can be applied on TXEx also.
2. Only if the RXF flag is not set.
3. The receive interrupt occurs only if not masked. A polling scheme can be applied on RXF also.

field of the CAN frame, is received into the next available RxBG. If the MSCAN receives an invalid message in its RxBG (wrong identifier, transmission errors, etc.) the actual contents of the buffer will be over-written by the next message. The buffer will then not be shifted into the FIFO.

When the MSCAN module is transmitting, the MSCAN receives its own transmitted messages into the background receive buffer, RxBG, but does not shift it into the receiver FIFO, generate a receive interrupt, or acknowledge its own messages on the CAN bus. The exception to this rule is in loopback mode (see Section 12.3.2.2, "MSCAN Control Register 1 (CANCTL1)") where the MSCAN treats its own messages exactly like all other incoming messages. The MSCAN receives its own transmitted messages in the event that it loses arbitration. If arbitration is lost, the MSCAN must be prepared to become a receiver.

An overrun condition occurs when all receive message buffers in the FIFO are filled with correctly received messages with accepted identifiers and another message is correctly received from the CAN bus with an accepted identifier. The latter message is discarded and an error interrupt with overrun indication is generated if enabled (see Section 12.4.8.5, "Error Interrupt"). The MSCAN remains able to transmit messages while the receiver FIFO being filled, but all incoming messages are discarded. As soon as a receive buffer in the FIFO is available again, new valid messages will be accepted.

12.4.3 Identifier Acceptance Filter

The MSCAN identifier acceptance registers (see Section 12.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)") define the acceptable patterns of the standard or extended identifier (ID[10:0] or ID[28:0]). Any of these bits can be marked 'don't care' in the MSCAN identifier mask registers (see Section 12.3.2.17, "MSCAN Identifier Mask Registers (CANIDMR0–CANIDMR7)").

A filter hit is indicated to the application software by a set receive buffer full flag (RXF = 1) and three bits in the CANIDAC register (see Section 12.3.2.12, "MSCAN Identifier Acceptance Control Register (CANIDAC)"). These identifier hit flags (IDHIT[2:0]) clearly identify the filter section that caused the acceptance. They simplify the application software's task to identify the cause of the receiver interrupt. If more than one hit occurs (two or more filters match), the lower hit has priority.

A very flexible programmable generic identifier acceptance filter has been introduced to reduce the CPU interrupt loading. The filter is programmable to operate in four different modes (see Bosch CAN 2.0A/B protocol specification):

- Two identifier acceptance filters, each to be applied to:
  - The full 29 bits of the extended identifier and to the following bits of the CAN 2.0B frame:
    - Remote transmission request (RTR)
    - Identifier extension (IDE)
    - Substitute remote request (SRR)
  - The 11 bits of the standard identifier plus the RTR and IDE bits of the CAN 2.0A/B messages[1]. This mode implements two filters for a full length CAN 2.0B compliant extended identifier. Figure 12-37 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces a filter 0 hit. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces a filter 1 hit.

1. Although this mode can be used for standard identifiers, it is recommended to use the four or eight identifier acceptance filters for standard identifiers

- Four identifier acceptance filters, each to be applied to
  - a) the 14 most significant bits of the extended identifier plus the SRR and IDE bits of CAN 2.0B messages or
  - b) the 11 bits of the standard identifier, the RTR and IDE bits of CAN 2.0A/B messages. Figure 12-38 shows how the first 32-bit filter bank (CANIDAR0–CANIDA3, CANIDMR0–3CANIDMR) produces filter 0 and 1 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 2 and 3 hits.
- Eight identifier acceptance filters, each to be applied to the first 8 bits of the identifier. This mode implements eight independent filters for the first 8 bits of a CAN 2.0A/B compliant standard identifier or a CAN 2.0B compliant extended identifier. Figure 12-39 shows how the first 32-bit filter bank (CANIDAR0–CANIDAR3, CANIDMR0–CANIDMR3) produces filter 0 to 3 hits. Similarly, the second filter bank (CANIDAR4–CANIDAR7, CANIDMR4–CANIDMR7) produces filter 4 to 7 hits.
- Closed filter. No CAN message is copied into the foreground buffer RxFG, and the RXF flag is never set.

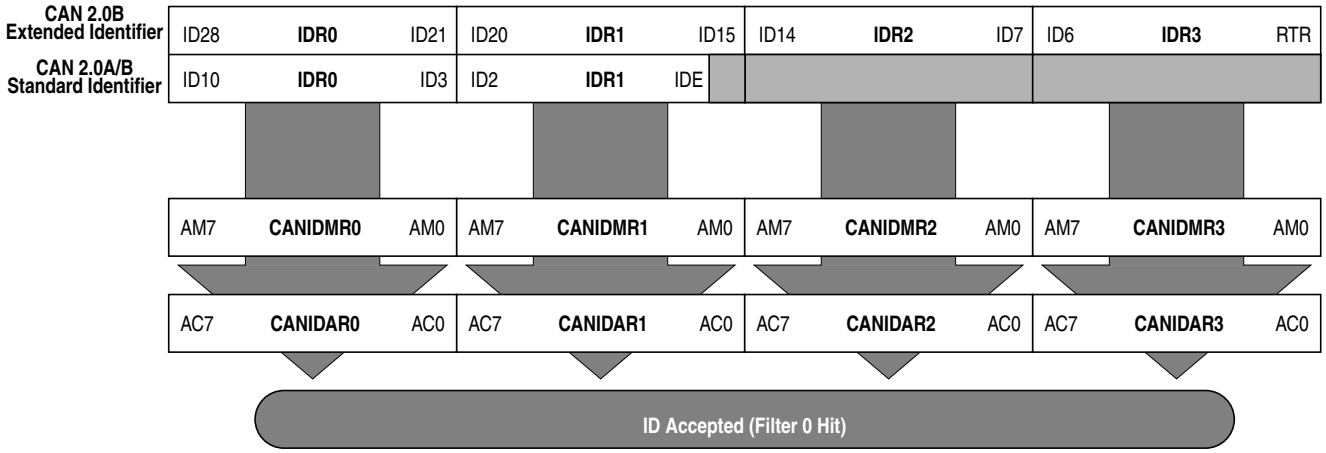


Figure 12-37. 32-bit Maskable Identifier Acceptance Filter

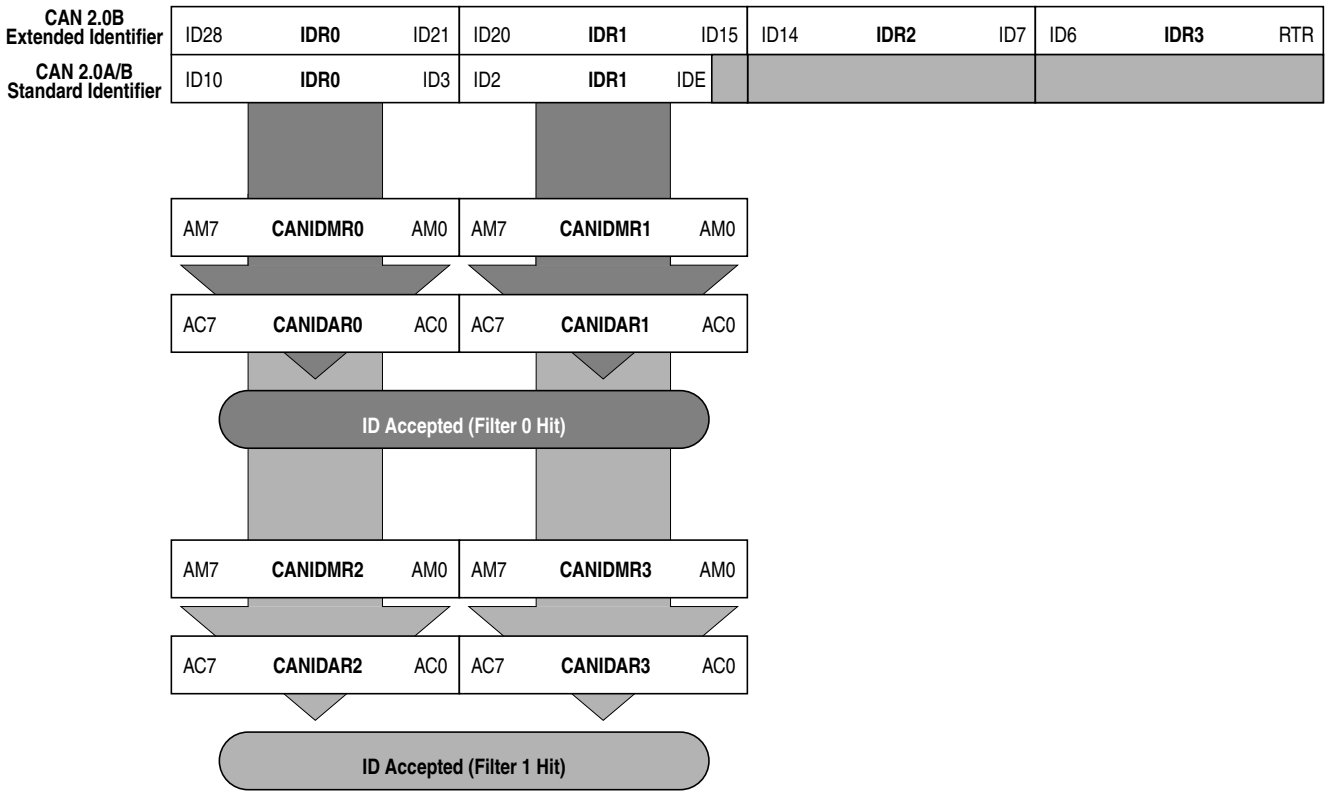


Figure 12-38. 16-bit Maskable Identifier Acceptance Filters

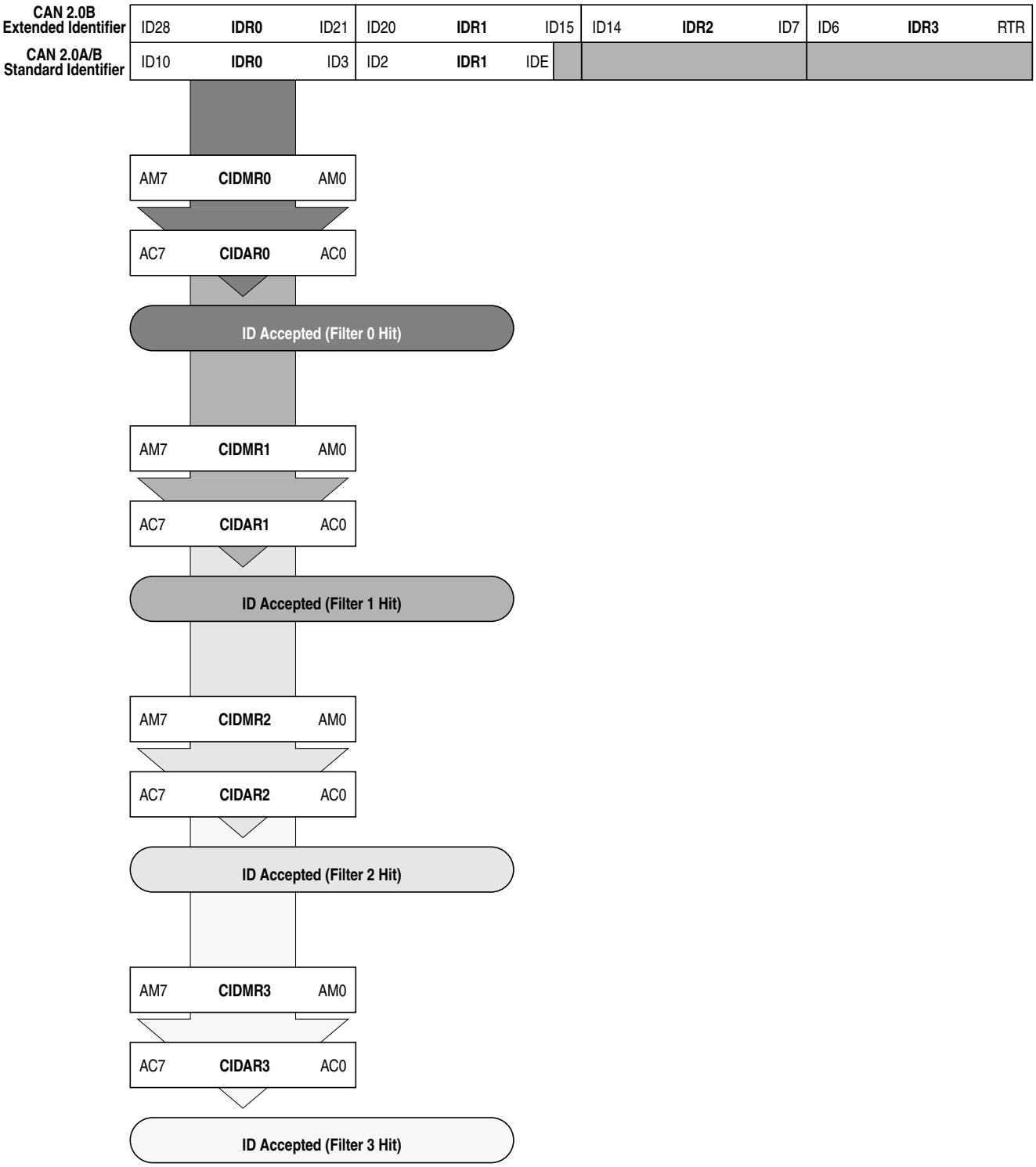


Figure 12-39. 8-bit Maskable Identifier Acceptance Filters

12.4.3.1 Protocol Violation Protection

The MSCAN protects the user from accidentally violating the CAN protocol through programming errors. The protection logic implements the following features:

- The receive and transmit error counters cannot be written or otherwise manipulated.
- All registers which control the configuration of the MSCAN cannot be modified while the MSCAN is on-line. The MSCAN has to be in Initialization Mode. The corresponding INITRQ/INITAK handshake bits in the CANCTL0/CANCTL1 registers (see Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)") serve as a lock to protect the following registers:
  - MSCAN control 1 register (CANCTL1)
  - MSCAN bus timing registers 0 and 1 (CANBTR0, CANBTR1)
  - MSCAN identifier acceptance control register (CANIDAC)
  - MSCAN identifier acceptance registers (CANIDAR0–CANIDAR7)
  - MSCAN identifier mask registers (CANIDMR0–CANIDMR7)
- The TXCAN pin is immediately forced to a recessive state when the MSCAN goes into the power down mode or initialization mode (see Section 12.4.6.6, "MSCAN Power Down Mode," and Section 12.4.6.5, "MSCAN Initialization Mode").
- The MSCAN enable bit (CANE) is writable only once in normal system operation modes, which provides further protection against inadvertently disabling the MSCAN.

12.4.3.2 Clock System

Figure 12-40 shows the structure of the MSCAN clock generation circuitry.

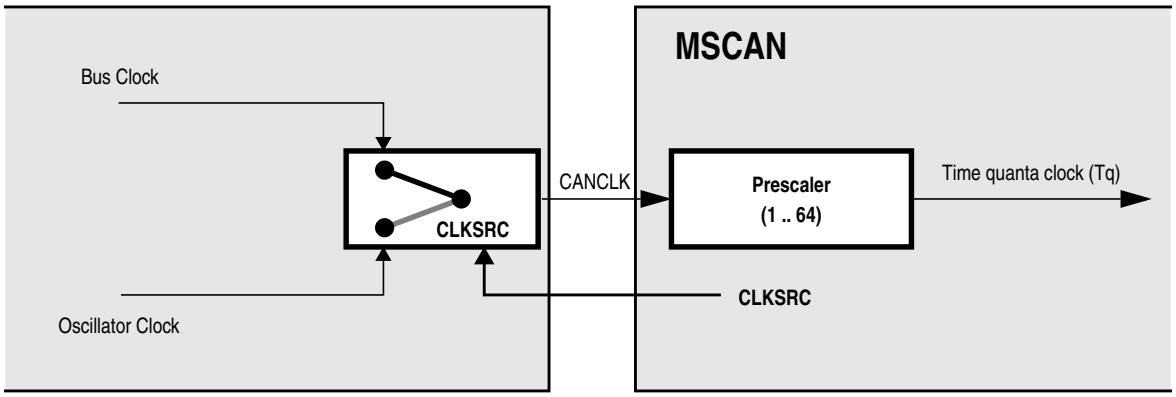


Figure 12-40. MSCAN Clocking Scheme

The clock source bit (CLKSRC) in the CANCTL1 register (12.3.2.2/12-340) defines whether the internal CANCLK is connected to the output of a crystal oscillator (oscillator clock) or to the bus clock.

The clock source has to be chosen such that the tight oscillator tolerance requirements (up to 0.4%) of the CAN protocol are met. Additionally, for high CAN bus rates (1 Mbps), a 45% to 55% duty cycle of the clock is required.

If the bus clock is generated from a PLL, it is recommended to select the oscillator clock rather than the bus clock due to jitter considerations, especially at the faster CAN bus rates.

For microcontrollers without a clock and reset generator (CRG), CANCLK is driven from the crystal oscillator (oscillator clock).

A programmable prescaler generates the time quanta (Tq) clock from CANCLK. A time quantum is the atomic unit of time handled by the MSCAN.

Eqn. 12-2

$$Tq = \frac{f_{CANCLK}}{(\text{Prescaler value})}$$

A bit time is subdivided into three segments as described in the Bosch CAN specification. (see Figure 12-41):

- SYNC_SEG: This segment has a fixed length of one time quantum. Signal edges are expected to happen within this section.
- Time Segment 1: This segment includes the PROP_SEG and the PHASE_SEG1 of the CAN standard. It can be programmed by setting the parameter TSEG1 to consist of 4 to 16 time quanta.
- Time Segment 2: This segment represents the PHASE_SEG2 of the CAN standard. It can be programmed by setting the TSEG2 parameter to be 2 to 8 time quanta long.

Eqn. 12-3

$$\text{Bit Rate} = \frac{f_{Tq}}{(\text{number of Time Quanta})}$$

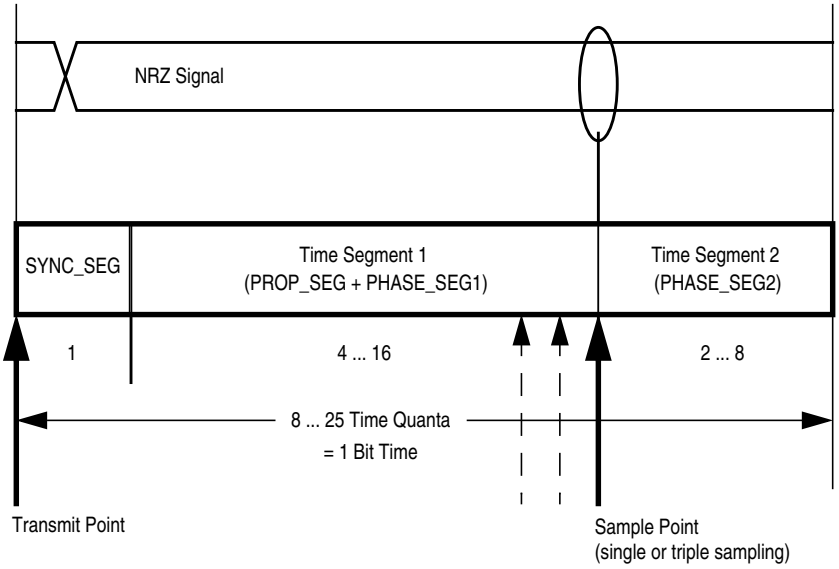


Figure 12-41. Segments within the Bit Time

Table 12-35. Time Segment Syntax

Syntax	Description
SYNC_SEG	System expects transitions to occur on the CAN bus during this period.
Transmit Point	A node in transmit mode transfers a new value to the CAN bus at this point.
Sample Point	A node in receive mode samples the CAN bus at this point. If the three samples per bit option is selected, then this point marks the position of the third sample.

The synchronization jump width (see the Bosch CAN specification for details) can be programmed in a range of 1 to 4 time quanta by setting the SJW parameter.

The SYNC_SEG, TSEG1, TSEG2, and SJW parameters are set by programming the MSCAN bus timing registers (CANBTR0, CANBTR1) (see Section 12.3.2.3, "MSCAN Bus Timing Register 0 (CANBTR0)" and Section 12.3.2.4, "MSCAN Bus Timing Register 1 (CANBTR1)").

Table 12-36 gives an overview of the CAN compliant segment settings and the related parameter values.

NOTE

It is the user's responsibility to ensure the bit time settings are in compliance with the CAN standard.

Table 12-36. CAN Standard Compliant Bit Time Segment Settings

Time Segment 1	TSEG1	Time Segment 2	TSEG2	Synchronization Jump Width	SJW
5 .. 10	4 .. 9	2	1	1 .. 2	0 .. 1
4 .. 11	3 .. 10	3	2	1 .. 3	0 .. 2
5 .. 12	4 .. 11	4	3	1 .. 4	0 .. 3
6 .. 13	5 .. 12	5	4	1 .. 4	0 .. 3
7 .. 14	6 .. 13	6	5	1 .. 4	0 .. 3
8 .. 15	7 .. 14	7	6	1 .. 4	0 .. 3
9 .. 16	8 .. 15	8	7	1 .. 4	0 .. 3

12.4.4 Timer Link

The MSCAN generates an internal time stamp whenever a valid frame is received or transmitted and the TIME bit is enabled. Because the CAN specification defines a frame to be valid if no errors occur before the end of frame (EOF) field is transmitted successfully, the actual value of an internal timer is written at EOF to the appropriate time stamp position within the transmit buffer. For receive frames, the time stamp is written to the receive buffer.

12.4.5 Modes of Operation

12.4.5.1 Normal Modes

The MSCAN module behaves as described within this specification in all normal system operation modes.

12.4.5.2 Special Modes

The MSCAN module behaves as described within this specification in all special system operation modes.

12.4.5.3 Emulation Modes

In all emulation modes, the MSCAN module behaves just like normal system operation modes as described within this specification.

12.4.5.4 Listen-Only Mode

In an optional CAN bus monitoring mode (listen-only), the CAN node is able to receive valid data frames and valid remote frames, but it sends only "recessive" bits on the CAN bus. In addition, it cannot start a transmision. If the MAC sub-layer is required to send a "dominant" bit (ACK bit, overload flag, or active error flag), the bit is rerouted internally so that the MAC sub-layer monitors this "dominant" bit, although the CAN bus may remain in recessive state externally.

12.4.5.5 Security Modes

The MSCAN module has no security features.

12.4.6 Low-Power Options

If the MSCAN is disabled (CANE = 0), the MSCAN clocks are stopped for power saving.

If the MSCAN is enabled (CANE = 1), the MSCAN has two additional modes with reduced power consumption, compared to normal mode: sleep and power down mode. In sleep mode, power consumption is reduced by stopping all clocks except those to access the registers from the CPU side. In power down mode, all clocks are stopped and no power is consumed.

Table 12-37 summarizes the combinations of MSCAN and CPU modes. A particular combination of modes is entered by the given settings on the CSWAI and SLPRQ/SLPAK bits.

For all modes, an MSCAN wake-up interrupt can occur only if the MSCAN is in sleep mode (SLPRQ = 1 and SLPAK = 1), wake-up functionality is enabled (WUPE = 1), and the wake-up interrupt is enabled (WUPIE = 1).

Table 12-37. CPU vs. MSCAN Operating Modes

CPU Mode	MSCAN Mode			
	Normal	Reduced Power Consumption		
		Sleep	Power Down	Disabled (CANE=0)
RUN	CSWAI = X[1] SLPRQ = 0 SLPAK = 0	CSWAI = X SLPRQ = 1 SLPAK = 1		CSWAI = X SLPRQ = X SLPAK = X
WAIT	CSWAI = 0 SLPRQ = 0 SLPAK = 0	CSWAI = 0 SLPRQ = 1 SLPAK = 1	CSWAI = 1 SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X
STOP			CSWAI = X SLPRQ = X SLPAK = X	CSWAI = X SLPRQ = X SLPAK = X

1 'X' means don't care.

12.4.6.1 Operation in Run Mode

As shown in Table 12-37, only MSCAN sleep mode is available as low power option when the CPU is in run mode.

12.4.6.2 Operation in Wait Mode

The WAI instruction puts the MCU in a low power consumption stand-by mode. If the CSWAI bit is set, additional power can be saved in power down mode because the CPU clocks are stopped. After leaving this power down mode, the MSCAN restarts its internal controllers and enters normal mode again.

While the CPU is in wait mode, the MSCAN can be operated in normal mode and generate interrupts (registers can be accessed via background debug mode). The MSCAN can also operate in any of the low-power modes depending on the values of the SLPRQ/SLPAK and CSWAI bits as seen in Table 12-37.

12.4.6.3 Operation in Stop Mode

The STOP instruction puts the MCU in a low power consumption stand-by mode. In stop mode, the MSCAN is set in power down mode regardless of the value of the SLPRQ/SLPAK and CSWAI bits Table 12-37.

12.4.6.4 MSCAN Sleep Mode

The CPU can request the MSCAN to enter this low power mode by asserting the SLPRQ bit in the CANCTL0 register. The time when the MSCAN enters sleep mode depends on a fixed synchronization delay and its current activity:

- If there are one or more message buffers scheduled for transmission (TXEx = 0), the MSCAN will continue to transmit until all transmit message buffers are empty (TXEx = 1, transmitted successfully or aborted) and then goes into sleep mode.
- If the MSCAN is receiving, it continues to receive and goes into sleep mode as soon as the CAN bus next becomes idle.
- If the MSCAN is neither transmitting nor receiving, it immediately goes into sleep mode.

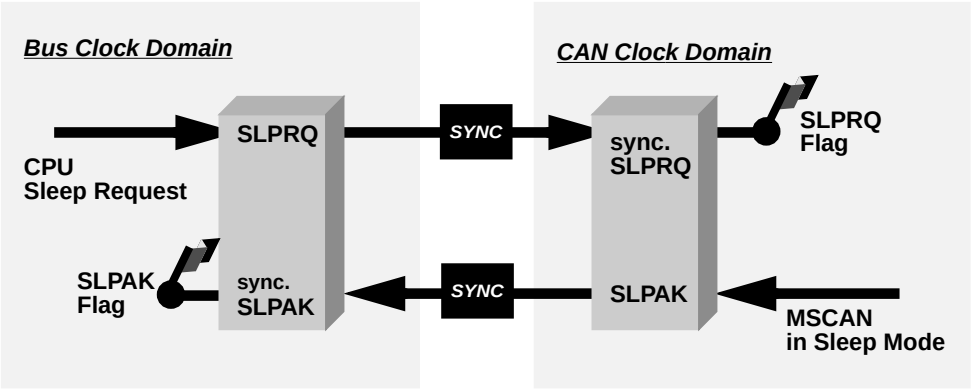


Figure 12-42. Sleep Request / Acknowledge Cycle

NOTE

The application software must avoid setting up a transmission (by clearing one or more TXEx flag(s)) and immediately request sleep mode (by setting SLPRQ). Whether the MSCAN starts transmitting or goes into sleep mode directly depends on the exact sequence of operations.

If sleep mode is active, the SLPRQ and SLPAK bits are set (Figure 12-42). The application software must use SLPAK as a handshake indication for the request (SLPRQ) to go into sleep mode.

When in sleep mode (SLPRQ = 1 and SLPAK = 1), the MSCAN stops its internal clocks. However, clocks that allow register accesses from the CPU side continue to run.

If the MSCAN is in bus-off state, it stops counting the 128 occurrences of 11 consecutive recessive bits due to the stopped clocks. The TXCAN pin remains in a recessive state. If RXF = 1, the message can be read and RXF can be cleared. Shifting a new message into the foreground buffer of the receiver FIFO (RxFG) does not take place while in sleep mode.

It is possible to access the transmit buffers and to clear the associated TXE flags. No message abort takes place while in sleep mode.

If the WUPE bit in CANCLT0 is not asserted, the MSCAN will mask any activity it detects on CAN. The RXCAN pin is therefore held internally in a recessive state. This locks the MSCAN in sleep mode (Figure 12-43).

The MSCAN is able to leave sleep mode (wake up) only when:

- CAN bus activity occurs and WUPE = 1
  or
- the CPU clears the SLPRQ bit

NOTE

The CPU cannot clear the SLPRQ bit before sleep mode (SLPRQ = 1 and SLPAK = 1) is active.

After wake-up, the MSCAN waits for 11 consecutive recessive bits to synchronize to the CAN bus. As a consequence, if the MSCAN is woken-up by a CAN frame, this frame is not received.

The receive message buffers (RxFG and RxBG) contain messages if they were received before sleep mode was entered. All pending actions will be executed upon wake-up; copying of RxBG into RxFG, message aborts and message transmissions. If the MSCAN remains in bus-off state after sleep mode was exited, it continues counting the 128 occurrences of 11 consecutive recessive bits.

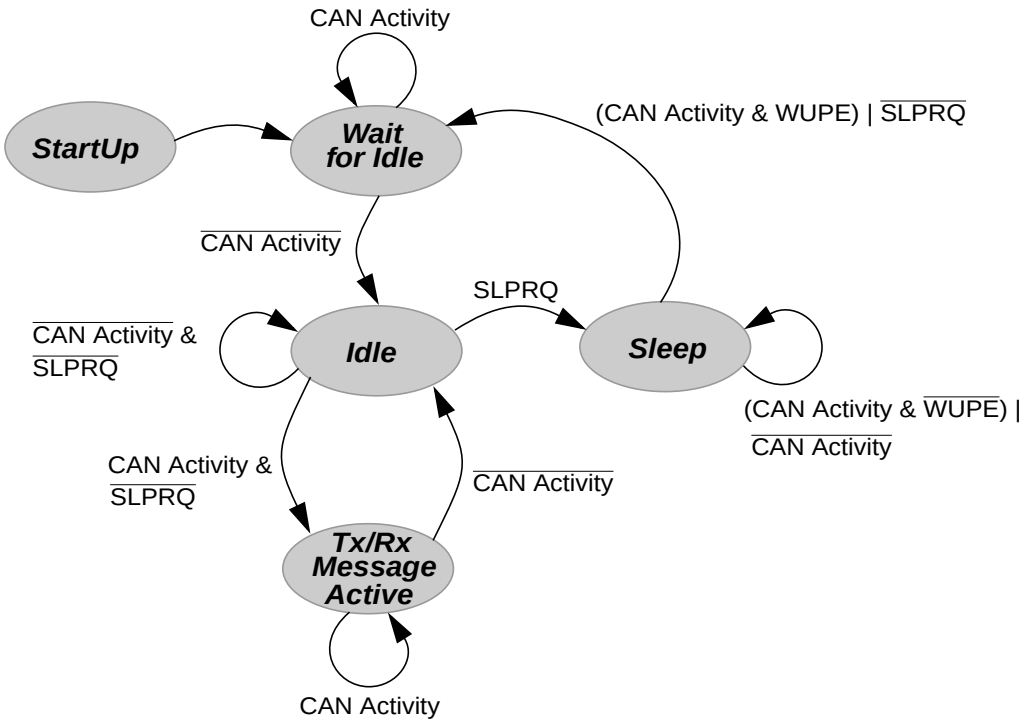


Figure 12-43. Simplified State Transitions for Entering/Leaving Sleep Mode

12.4.6.5 MSCAN Initialization Mode

In initialization mode, any on-going transmission or reception is immediately aborted and synchronization to the CAN bus is lost, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations, the MSCAN immediately drives the TXCAN pin into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when initialization mode is entered. The recommended procedure is to bring the MSCAN into sleep mode (SLPRQ = 1 and SLPAK = 1) before setting the INITRQ bit in the CANCTL0 register. Otherwise, the abort of an on-going message can cause an error condition and can impact other CAN bus devices.

In initialization mode, the MSCAN is stopped. However, interface registers remain accessible. This mode is used to reset the CANCTL0, CANRFLG, CANRIER, CANTFLG, CANTIER, CANTARQ, CANTAAK, and CANTBSEL registers to their default values. In addition, the MSCAN enables the configuration of the CANBTR0, CANBTR1 bit timing registers; CANIDAC; and the CANIDAR, CANIDMR message filters. See Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)," for a detailed description of the initialization mode.

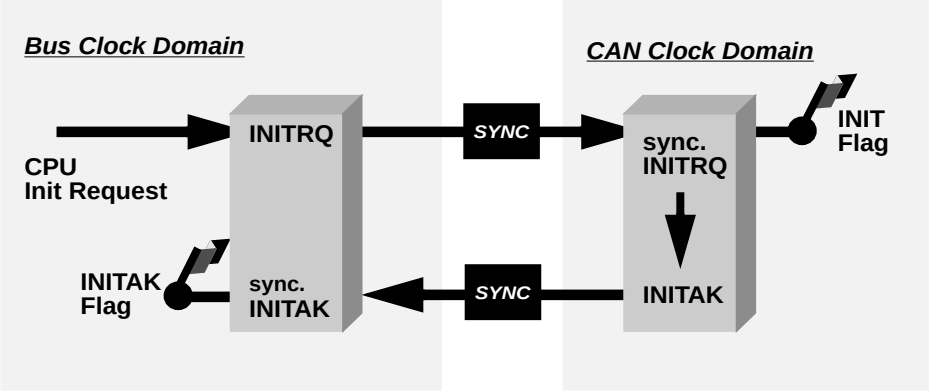


Figure 12-44. Initialization Request/Acknowledge Cycle

Due to independent clock domains within the MSCAN, INITRQ must be synchronized to all domains by using a special handshake mechanism. This handshake causes additional synchronization delay (see Section Figure 12-44., "Initialization Request/Acknowledge Cycle").

If there is no message transfer ongoing on the CAN bus, the minimum delay will be two additional bus clocks and three additional CAN clocks. When all parts of the MSCAN are in initialization mode, the INITAK flag is set. The application software must use INITAK as a handshake indication for the request (INITRQ) to go into initialization mode.

NOTE

The CPU cannot clear INITRQ before initialization mode (INITRQ = 1 and INITAK = 1) is active.

12.4.6.6 MSCAN Power Down Mode

The MSCAN is in power down mode (Table 12-37) when

- CPU is in stop mode
  or
- CPU is in wait mode and the CSWAI bit is set

When entering the power down mode, the MSCAN immediately stops all ongoing transmissions and receptions, potentially causing CAN protocol violations. To protect the CAN bus system from fatal consequences of violations to the above rule, the MSCAN immediately drives the TXCAN pin into a recessive state.

NOTE

The user is responsible for ensuring that the MSCAN is not active when power down mode is entered. The recommended procedure is to bring the MSCAN into Sleep mode before the STOP or WAI instruction (if CSWAI is set) is executed. Otherwise, the abort of an ongoing message can cause an error condition and impact other CAN bus devices.

In power down mode, all clocks are stopped and no registers can be accessed. If the MSCAN was not in sleep mode before power down mode became active, the module performs an internal recovery cycle after powering up. This causes some fixed delay before the module enters normal mode again.

12.4.6.7 Programmable Wake-Up Function

The MSCAN can be programmed to wake up the MSCAN as soon as CAN bus activity is detected (see control bit WUPE in Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)"). The sensitivity to existing CAN bus action can be modified by applying a low-pass filter function to the RXCAN input line while in sleep mode (see control bit WUPM in Section 12.3.2.2, "MSCAN Control Register 1 (CANCTL1)").

This feature can be used to protect the MSCAN from wake-up due to short glitches on the CAN bus lines. Such glitches can result from—for example—electromagnetic interference within noisy environments.

12.4.7 Reset Initialization

The reset state of each individual bit is listed in Section 12.3.2, "Register Descriptions," which details all the registers and their bit-fields.

12.4.8 Interrupts

This section describes all interrupts originated by the MSCAN. It documents the enable bits and generated flags. Each interrupt is listed and described separately.

12.4.8.1 Description of Interrupt Operation

The MSCAN supports four interrupt vectors (see Table 12-38), any of which can be individually masked (for details see sections from Section 12.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)," to Section 12.3.2.8, "MSCAN Transmitter Interrupt Enable Register (CANTIER)").

NOTE

The dedicated interrupt vector addresses are defined in the Resets and Interrupts chapter.

Table 12-38. Interrupt Vectors

Interrupt Source	CCR Mask	Local Enable
Wake-Up Interrupt (WUPIF)	I bit	CANRIER (WUPIE)
Error Interrupts Interrupt (CSCIF, OVRIF)	I bit	CANRIER (CSCIE, OVRIE)
Receive Interrupt (RXF)	I bit	CANRIER (RXFIE)
Transmit Interrupts (TXE[2:0])	I bit	CANTIER (TXEIE[2:0])

12.4.8.2 Transmit Interrupt

At least one of the three transmit buffers is empty (not scheduled) and can be loaded to schedule a message for transmission. The TXEx flag of the empty message buffer is set.

12.4.8.3 Receive Interrupt

A message is successfully received and shifted into the foreground buffer (RxFG) of the receiver FIFO. This interrupt is generated immediately after receiving the EOF symbol. The RXF flag is set. If there are multiple messages in the receiver FIFO, the RXF flag is set as soon as the next message is shifted to the foreground buffer.

12.4.8.4 Wake-Up Interrupt

A wake-up interrupt is generated if activity on the CAN bus occurs during MSCN internal sleep mode. WUPE (see Section 12.3.2.1, "MSCAN Control Register 0 (CANCTL0)") must be enabled.

12.4.8.5 Error Interrupt

An error interrupt is generated if an overrun of the receiver FIFO, error, warning, or bus-off condition occurrs. Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG) indicates one of the following conditions:

- **Overrun** — An overrun condition of the receiver FIFO as described in Section 12.4.2.3, "Receive Structures," occurred.
- **CAN Status Change** — The actual value of the transmit and receive error counters control the CAN bus state of the MSCAN. As soon as the error counters skip into a critical range (Tx/Rx-warning, Tx/Rx-error, bus-off) the MSCAN flags an error condition. The status change, which caused the error condition, is indicated by the TSTAT and RSTAT flags (see

Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)" and Section 12.3.2.6, "MSCAN Receiver Interrupt Enable Register (CANRIER)").

12.4.8.6 Interrupt Acknowledge

Interrupts are directly associated with one or more status flags in either the Section 12.3.2.5, "MSCAN Receiver Flag Register (CANRFLG)" or the Section 12.3.2.7, "MSCAN Transmitter Flag Register (CANTFLG)." Interrupts are pending as long as one of the corresponding flags is set. The flags in CANRFLG and CANTFLG must be reset within the interrupt handler to handshake the interrupt. The flags are reset by writing a 1 to the corresponding bit position. A flag cannot be cleared if the respective condition prevails.

NOTE

It must be guaranteed that the CPU clears only the bit causing the current interrupt. For this reason, bit manipulation instructions (BSET) must not be used to clear interrupt flags. These instructions may cause accidental clearing of interrupt flags which are set after entering the current interrupt service routine.

12.4.8.7 Recovery from Stop or Wait

The MSCAN can recover from stop or wait via the wake-up interrupt. This interrupt can only occur if the MSCAN was in sleep mode (SLPRQ = 1 and SLPAK = 1) before entering power down mode, the wake-up option is enabled (WUPE = 1), and the wake-up interrupt is enabled (WUPIE = 1).

12.5 Initialization/Application Information

12.5.1 MSCAN initialization

The procedure to initially start up the MSCAN module out of reset is as follows:

1. Assert CANE
2. Write to the configuration registers in initialization mode
3. Clear INITRQ to leave initialization mode and enter normal mode

If the configuration of registers which are writable in initialization mode needs to be changed only when the MSCAN module is in normal mode:

1. Bring the module into sleep mode by setting SLPRQ and awaiting SLPAK to assert after the CAN bus becomes idle.
2. Enter initialization mode: assert INITRQ and await INITAK
3. Write to the configuration registers in initialization mode
4. Clear INITRQ to leave initialization mode and continue in normal mode

Chapter 13
Serial Communication Interface (SCIV4)

13.1 Introduction

This block description chapter provides an overview of serial communication interface (SCI) module.

The SCI allows full duplex, asynchronous, serial communication between the CPU and remote devices, including other CPUs. The SCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

13.1.1 Glossary

IR: infrared

IrDA: Infrared Design Association

IRQ: interrupt request

LSB: least significant bit

MSB: most significant bit

NRZ: non-return-to-Zero

RZI: return-to-zero-inverted

RXD: receive pin

SCI: serial communication interface

TXD: transmit pin

13.1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver

- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

13.1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low-power modes, wait and stop modes.

13.1.3.1 Run Mode

Normal mode of operation.

13.1.3.2 Wait Mode

SCI operation in wait mode depends on the state of the SCISWAI bit in the SCI control register 1 (SCICR1).

- If SCISWAI is clear, the SCI operates normally when the CPU is in wait mode.
- If SCISWAI is set, SCI clock generation ceases and the SCI module enters a power-conservation state when the CPU is in wait mode. Setting SCISWAI does not affect the state of the receiver enable bit, RE, or the transmitter enable bit, TE.

  If SCISWAI is set, any transmission or reception in progress stops at wait mode entry. The transmission or reception resumes when either an internal or external interrupt brings the CPU out of wait mode. Exiting wait mode by reset aborts any transmission or reception in progress and resets the SCI.

13.1.3.3 Stop Mode

The SCI is inactive during stop mode for reduced power consumption. The STOP instruction does not affect the SCI register states, but the SCI bus clock will be disabled. The SCI operation resumes after an external interrupt brings the CPU out of stop mode. Exiting stop mode by reset aborts any transmission or reception in progress and resets the SCI.

13.1.4 Block Diagram

Figure 13-1 is a high level block diagram of the SCI module, showing the interaction of various function blocks.

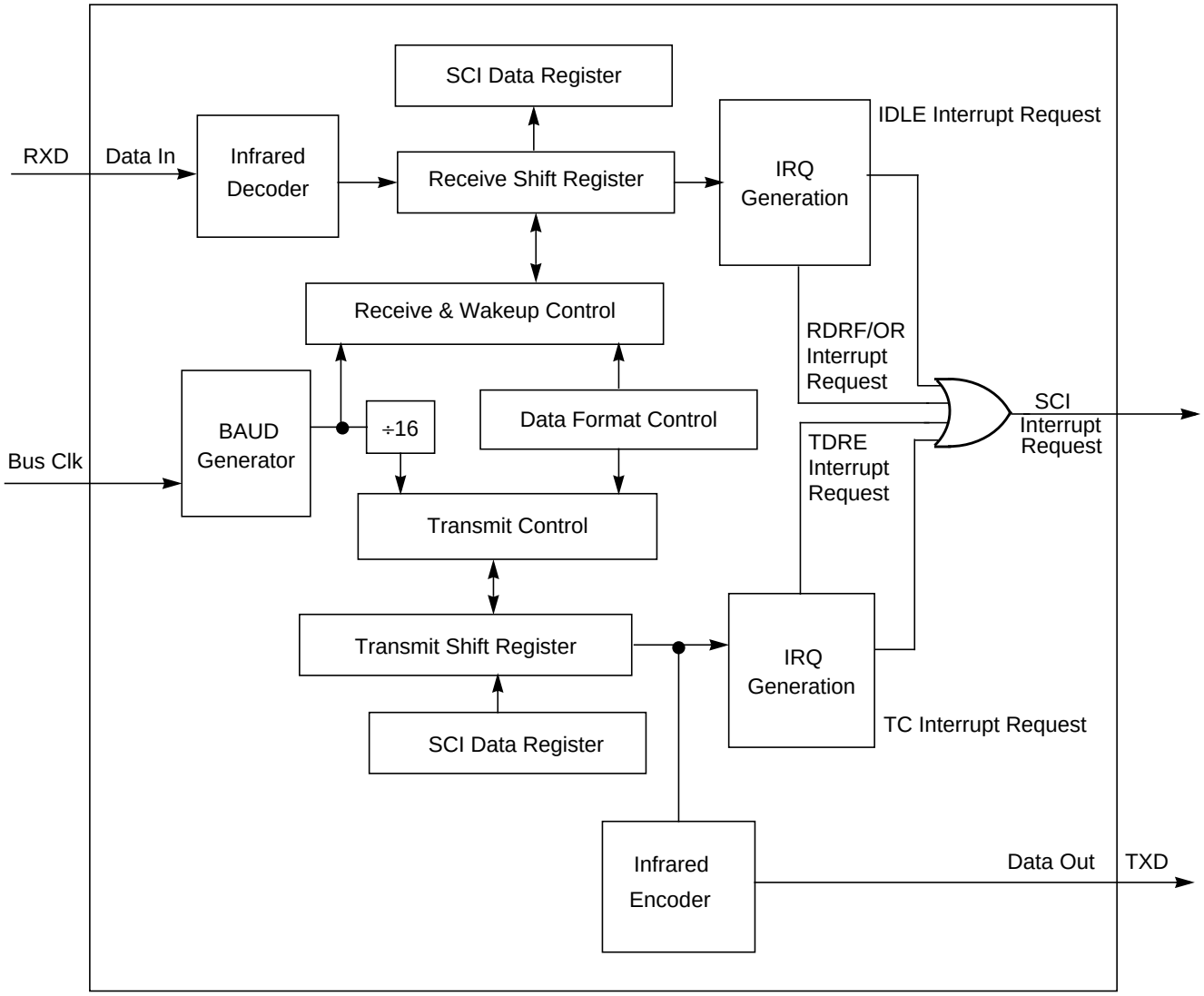


Figure 13-1. SCI Block Diagram

13.2 External Signal Descriptions

The SCI module has a total of two external pins.

13.2.1 TXD — SCI Transmit Pin

The TXD pin transmits SCI (standard or infrared) data. It will idle high in either mode and is high impedance anytime the transmitter is disabled.

13.2.2 RXD — SCI Receive Pin

The RXD pin receives SCI (standard or infrared) data. An idle line is detected as a line high. This input is ignored when the receiver is disabled and should be terminated to a known voltage.

13.3 Memory Map and Register Definition

This subsection provides a detailed description of all the SCI registers.

13.3.1 Module Memory Map

The memory map for the SCI module is given in Figure 13-2. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

13.3.2 Register Descriptions

This subsection consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to reserved register locations do not have any effect and reads of these locations return a 0. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
SCIBDH	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
	W								
SCIBDL	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
	W								
SCICR1	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
	W								

= Unimplemented or Reserved

Figure 13-2. SCI Registers Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
SCICR2	R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
SCISR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
	W								
SCISR2	R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
	W								
SCIDRH	R	R8	T8	0	0	0	0	0	0
	W								
SCIDRL	R	R7	R6	R5	R4	R3	R2	R1	R0
	W	T7	T6	T5	T4	T3	T2	T1	T0

= Unimplemented or Reserved

Figure 13-2. SCI Registers Summary

13.3.2.1 SCI Baud Rate Registers (SCIBDH and SCIBDL)

	7	6	5	4	3	2	1	0
R W	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
Reset	0	0	0	0	0	0	0	0

Figure 13-3. SCI Baud Rate Register High (SCIBDH)

Table 13-1. SCIBDH Field Descriptions

Field	Description
7 IREN	**Infrared Enable Bit** — This bit enables/disables the infrared modulation/demodulation submodule. 0 IR disabled 1 IR enabled
6:5 TNP[1:0]	**Transmitter Narrow Pulse Bits** — These bits determine if the SCI will transmit a 1/16, 3/16, 1/32, or 1/4 narrow pulse. Refer to Table 13-3.
4:0 SBR[11:8]	**SCI Baud Rate Bits** — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit. The formulas for calculating the baud rate are: When IREN = 0 then, SCI baud rate = SCI module clock / (16 x SBR[12:0]) When IREN = 1 then, SCI baud rate = SCI module clock / (32 x SBR[12:1])

	7	6	5	4	3	2	1	0
R W	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
Reset	0	0	0	0	0	1	0	0

Figure 13-4. SCI Baud Rate Register Low (SCIBDL)

Table 13-2. SCIBDL Field Descriptions

Field	Description
7:0 SBR[7:0]	**SCI Baud Rate Bits** — The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit. The formulas for calculating the baud rate are: When IREN = 0 then, SCI baud rate = SCI module clock / (16 x SBR[12:0]) When IREN = 1 then, SCI baud rate = SCI module clock / (32 x SBR[12:1])

Read: anytime

NOTE

If only SCIBDH is written to, a read will not return the correct data until SCIBDL is written to as well, following a write to SCIBDH.

Write: anytime

The SCI baud rate register is used to determine the baud rate of the SCI and to control the infrared modulation/demodulation submodule.

Table 13-3. IRSCI Transmit Pulse Width

TNP[1:0]	Narrow Pulse Width
11	1/4
10	1/32
01	1/16
00	3/16

NOTE

The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1).

Writing to SCIBDH has no effect without writing to SCIBDL, because writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.

13.3.2.2 SCI Control Register 1 (SCICR1)

	7	6	5	4	3	2	1	0
R W	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
Reset	0	0	0	0	0	0	0	0

Figure 13-5. SCI Control Register 1 (SCICR1)

Read: anytime

Write: anytime

Table 13-4. SCICR1 Field Descriptions

Field	Description
7 LOOPS	**Loop Select Bit** — LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function. 0 Normal operation enabled 1 Loop operation enabled The receiver input is determined by the RSRC bit.
6 SCISWAI	**SCI Stop in Wait Mode Bit** — SCISWAI disables the SCI in wait mode. 0 SCI enabled in wait mode 1 SCI disabled in wait mode
5 RSRC	**Receiver Source Bit** — When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input. 0 Receiver input internally connected to transmitter output 1 Receiver input connected externally to transmitter Refer to Table 13-5.
4 M	**Data Format Mode Bit** — MODE determines whether data characters are eight or nine bits long. 0 One start bit, eight data bits, one stop bit 1 One start bit, nine data bits, one stop bit
3 WAKE	**Wakeup Condition Bit** — WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin. 0 Idle line wakeup 1 Address mark wakeup
2 ILT	**Idle Line Type Bit** — ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions. 0 Idle character bit count begins after start bit 1 Idle character bit count begins after stop bit
1 PE	**Parity Enable Bit** — PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position. 0 Parity function disabled 1 Parity function enabled
0 PT	**Parity Type Bit** — PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit. 0 Even parity 1 Odd parity

Table 13-5. Loop Functions

LOOPS	RSRC	Function
0	x	Normal operation
1	0	Loop mode with transmitter output internally connected to receiver input
1	1	Single-wire mode with TXD pin connected to receiver input

13.3.2.3 SCI Control Register 2 (SCICR2)

	7	6	5	4	3	2	1	0
R W	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
Reset	0	0	0	0	0	0	0	0

Figure 13-6. SCI Control Register 2 (SCICR2)

Read: anytime

Write: anytime

Table 13-6. SCICR2 Field Descriptions

Field	Description
7 TIE	**Transmitter Interrupt Enable Bit** —TIE enables the transmit data register empty flag, TDRE, to generate interrupt requests. 0 TDRE interrupt requests disabled 1 TDRE interrupt requests enabled
6 TCIE	**Transmission Complete Interrupt Enable Bit** — TCIE enables the transmission complete flag, TC, to generate interrupt requests. 0 TC interrupt requests disabled 1 TC interrupt requests enabled
5 RIE	**Receiver Full Interrupt Enable Bit** — RIE enables the receive data register full flag, RDRF, or the overrun flag, OR, to generate interrupt requests. 0 RDRF and OR interrupt requests disabled 1 RDRF and OR interrupt requests enabled
4 ILIE	**Idle Line Interrupt Enable Bit** — ILIE enables the idle line flag, IDLE, to generate interrupt requests. 0 IDLE interrupt requests disabled 1 IDLE interrupt requests enabled
3 TE	**Transmitter Enable Bit** — TE enables the SCI transmitter and configures the TXD pin as being controlled by the SCI. The TE bit can be used to queue an idle preamble. 0 Transmitter disabled 1 Transmitter enabled
2 RE	**Receiver Enable Bit** — RE enables the SCI receiver. 0 Receiver disabled 1 Receiver enabled
1 RWU	**Receiver Wakeup Bit** — Standby state 0 Normal operation. 1 RWU enables the wakeup function and inhibits further receiver interrupt requests. Normally, hardware wakes the receiver by automatically clearing RWU.
0 SBK	**Send Break Bit** — Toggling SBK sends one break character (10 or 11 logic 0s, respectively 13 or 14 logics 0s if BRK13 is set). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters (10 or 11 bits, respectively 13 or 14 bits). 0 No break characters 1 Transmit break characters

13.3.2.4 SCI Status Register 1 (SCISR1)

The SCISR1 and SCISR2 registers provide inputs to the MCU for generation of SCI interrupts. Also, these registers can be polled by the MCU to check the status of these bits. The flag-clearing procedures require that the status register be read followed by a read or write to the SCI data register. It is permissible to execute other instructions between the two steps as long as it does not compromise the handling of I/O. Note that the order of operations is important for flag clearing.

	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W								
Reset	1	1	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-7. SCI Status Register 1 (SCISR1)

Read: anytime

Write: has no meaning or effect

Table 13-7. SCISR1 Field Descriptions

Field	Description
7 TDRE	**Transmit Data Register Empty Flag** — TDRE is set when the transmit shift register receives a byte from the SCI data register. When TDRE is 1, the transmit data register (SCIDRH/L) is empty and can receive a new value to transmit.Clear TDRE by reading SCI status register 1 (SCISR1), with TDRE set and then writing to SCI data register low (SCIDRL). 0 No byte transferred to transmit shift register 1 Byte transferred to transmit shift register; transmit data register empty
6 TC	**Transmit Complete Flag** — TC is set low when there is a transmission in progress or when a preamble or break character is loaded. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted.When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL). TC is cleared automatically when data, preamble, or break is queued and ready to be sent. TC is cleared in the event of a simultaneous set and clear of the TC flag (transmission not complete). 0 Transmission in progress 1 No transmission in progress
5 RDRF	**Receive Data Register Full Flag** — RDRF is set when the data in the receive shift register transfers to the SCI data register. Clear RDRF by reading SCI status register 1 (SCISR1) with RDRF set and then reading SCI data register low (SCIDRL). 0 Data not available in SCI data register 1 Received data available in SCI data register
4 IDLE	**Idle Line Flag**[1] — IDLE is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. After the IDLE flag is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag.Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL). 0 Receiver input is either active now or has never become active since the IDLE flag was last cleared 1 Receiver input has become idle

Table 13-7. SCISR1 Field Descriptions (continued)

Field	Description
3 OR	**Overrun Flag**[2] — OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL). 0 No overrun 1 Overrun
2 NF	**Noise Flag** — NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL). 0 No noise 1 Noise
1 FE	**Framing Error Flag** — FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL). 0 No framing error 1 Framing error
0 PF	**Parity Error Flag** — PF is set when the parity enable bit (PE) is set and the parity of the received data does not match the parity type bit (PT). PF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL). 0 No parity error 1 Parity error

[1] When the receiver wakeup bit (RWU) is set, an idle line condition does not set the IDLE flag.

[2] The OR flag may read back as set when RDRF flag is clear. This may happen if the following sequence of events occurs:

1. After the first frame is received, read status register SCISR1 (returns RDRF set and OR flag clear);
2. Receive second frame without reading the first frame in the data register (the second frame is not received and OR flag is set);
3. Read data register SCIDRL (returns first frame and clears RDRF flag in the status register);
4. Read status register SCISR1 (returns RDRF clear and OR set).

Event 3 may be at exactly the same time as event 2 or any time after. When this happens, a dummy SCIDRL read following event 4 will be required to clear the OR flag if further frames are to be received.

13.3.2.5 SCI Status Register 2 (SCISR2)

	7	6	5	4	3	2	1	0
R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-8. SCI Status Register 2 (SCISR2)

Read: anytime

Write: anytime

Table 13-8. SCISR2 Field Descriptions

Field	Description
4 TXPOL	**Transmit Polarity** — This bit control the polarity of the transmitted data. In NRZ format, a 1 is represented by a mark and a 0 is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a 0 is represented by short high pulse in the middle of a bit time remaining idle low for a 1 for normal polarity, and a 0 is represented by short low pulse in the middle of a bit time remaining idle high for a 1 for inverted polarity. 0 Normal polarity 1 Inverted polarity
3 RXPOL	**Receive Polarity** — This bit control the polarity of the received data. In NRZ format, a 1 is represented by a mark and a 0 is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a 0 is represented by short high pulse in the middle of a bit time remaining idle low for a 1 for normal polarity, and a 0 is represented by short low pulse in the middle of a bit time remaining idle high for a 1 for inverted polarity. 0 Normal polarity 1 Inverted polarity
2 BRK13	**Break Transmit Character Length** — This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit. 0 Break character is 10 or 11 bit long 1 Break character is 13 or 14 bit long
1 TXDIR	**Transmitter Pin Data Direction in Single-Wire Mode** — This bit determines whether the TXD pin is going to be used as an input or output, in the single-wire mode of operation. This bit is only relevant in the single-wire mode of operation. 0 TXD pin to be used as an input in single-wire mode 1 TXD pin to be used as an output in single-wire mode
0 RAF	**Receiver Active Flag** — RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character. 0 No reception in progress 1 Reception in progress

13.3.2.6 SCI Data Registers (SCIDRH and SCIDRL)

	7	6	5	4	3	2	1	0
R	R8	T8	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 13-9. SCI Data Register High (SCIDRH)

Table 13-9. SCIDRH Field Descriptions

Field	Description
7 R8	**Received Bit 8** — R8 is the ninth data bit received when the SCI is configured for 9-bit data format (M = 1).
6 T8	**Transmit Bit 8** — T8 is the ninth data bit transmitted when the SCI is configured for 9-bit data format (M = 1).

	7	6	5	4	3	2	1	0
R	R7	R6	R5	R4	R3	R2	R1	R0
W	T7	T6	T5	T4	T3	T2	T1	T0
Reset	0	0	0	0	0	0	0	0

Figure 13-10. SCI Data Register Low (SCIDRL)

Read: anytime; reading accesses SCI receive data register

Write: anytime; writing accesses SCI transmit data register; writing to R8 has no effect

Table 13-10. SCIDRL Field Descriptions

Field	Description
7:0 R[7:0] T[7:0}	**Received bits 7 through 0** — For 9-bit or 8-bit data formats **Transmit bits 7 through 0** — For 9-bit or 8-bit formats

NOTE

If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten.The same value is transmitted until T8 is rewritten

In 8-bit data format, only SCI data register low (SCIDRL) needs to be accessed.

When transmitting in 9-bit data format and using 8-bit write instructions, write first to SCI data register high (SCIDRH) then to SCIDRL.

13.4 Functional Description

This subsection provides a complete functional description of the SCI block, detailing the operation of the design from the end user's perspective in a number of descriptions.

Figure 13-11 shows the structure of the SCI module. The SCI allows full duplex, asynchronous, serial communication between the CPU and remote devices, including other CPUs. The SCI transmitter and receiver operate independently, although they use the same baud rate generator. The CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

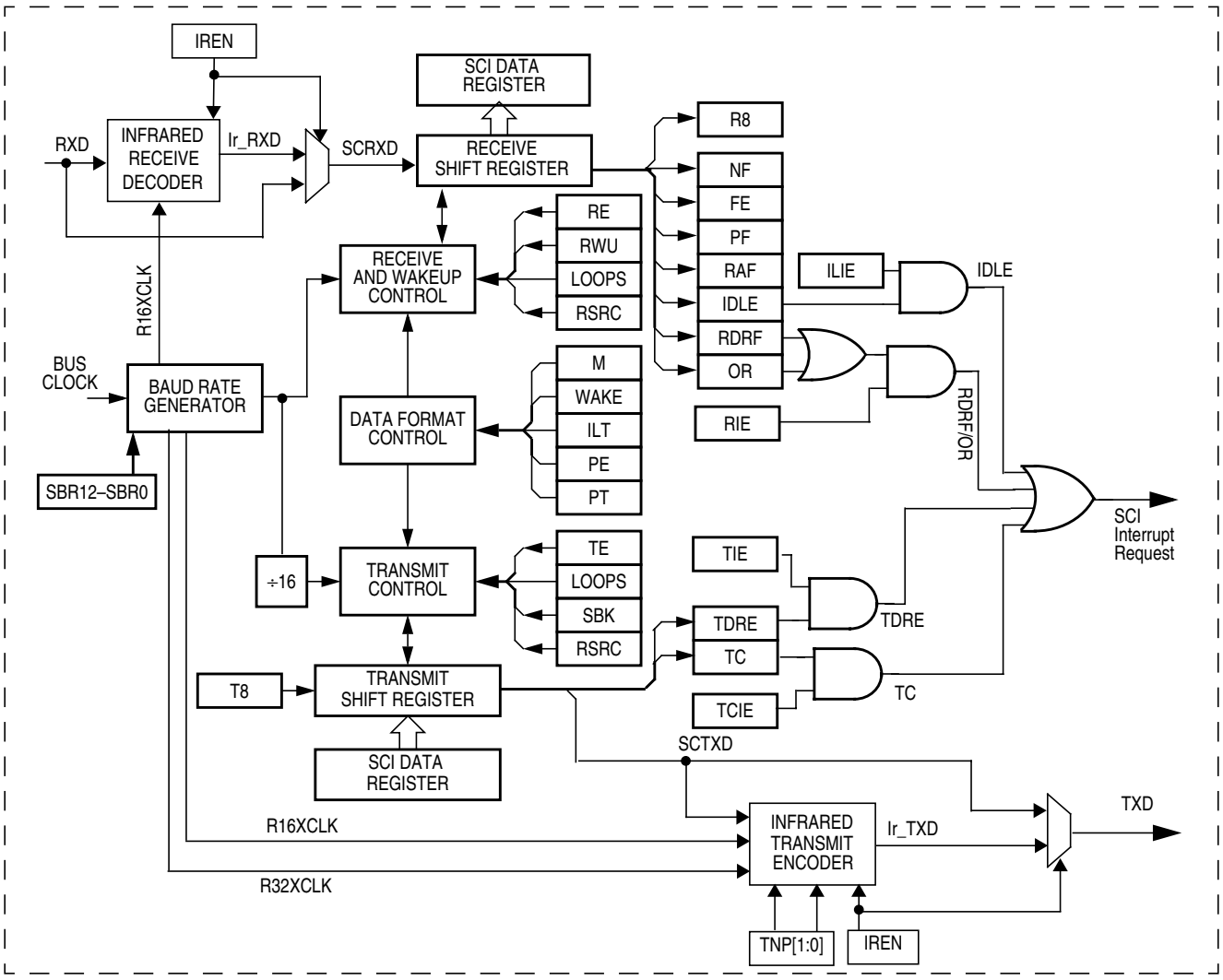


Figure 13-11. Detailed SCI Block Diagram

13.4.1 Infrared Interface Submodule

This module provides the capability of transmitting narrow pulses to an IR LED and receiving narrow pulses and transforming them to serial bits, which are sent to the SCI. The IrDA physical layer specification defines a half-duplex infrared communication link for exchange data. The full standard includes data rates up to 16 Mbits/s. This design covers only data rates between 2.4 kbits/s and 115.2 kbits/s.

The infrared submodule consists of two major blocks: the transmit encoder and the receive decoder. The SCI transmits serial bits of data which are encoded by the infrared submodule to transmit a narrow pulse for every 0 bit. No pulse is transmitted for every 1 bit. When receiving data, the IR pulses should be detected using an IR photo diode and transformed to CMOS levels by the IR receive decoder (external from the MCU). The narrow pulses are then stretched by the infrared submodule to get back to a serial bit stream to be received by the SCI. The polarity of transmitted pulses and expected receive pulses can be inverted so that a direct connection can be made to external IrDA transceiver modules that uses active low pulses.

The infrared submodule receives its clock sources from the SCI. One of these two clocks are selected in the infrared submodule in order to generate either 3/16, 1/16, 1/32, or 1/4 narrow pulses during transmission. The infrared block receives two clock sources from the SCI, R16XCLK, and R32XCLK, which are configured to generate the narrow pulse width during transmission. The R16XCLK and R32XCLK are internal clocks with frequencies 16 and 32 times the baud rate respectively. Both R16XCLK and R32XCLK clocks are used for transmitting data. The receive decoder uses only the R16XCLK clock.

13.4.1.1 Infrared Transmit Encoder

The infrared transmit encoder converts serial bits of data from transmit shift register to the TXD pin. A narrow pulse is transmitted for a 0 bit and no pulse for a 1 bit. The narrow pulse is sent in the middle of the bit with a duration of 1/32, 1/16, 3/16, or 1/4 of a bit time. A narrow high pulse is transmitted for a 0 bit when TXPOL is cleared, while a narrow low pulse is transmitted for a 0 bit when TXPOL is set.

13.4.1.2 Infrared Receive Decoder

The infrared receive block converts data from the RXD pin to the receive shift register. A narrow pulse is expected for each 0 received and no pulse is expected for each 1 received. A narrow high pulse is expected for a 0 bit when RXPOL is cleared, while a narrow low pulse is expected for a 0 bit when RXPOL is set. This receive decoder meets the edge jitter requirement as defined by the IrDA serial infrared physical layer specification.

13.4.2 Data Format

The SCI uses the standard NRZ mark/space data format. When Infrared is enabled, the SCI uses RZI data format where 0s are represented by light pulses and 1s remain low. See Figure 13-12.

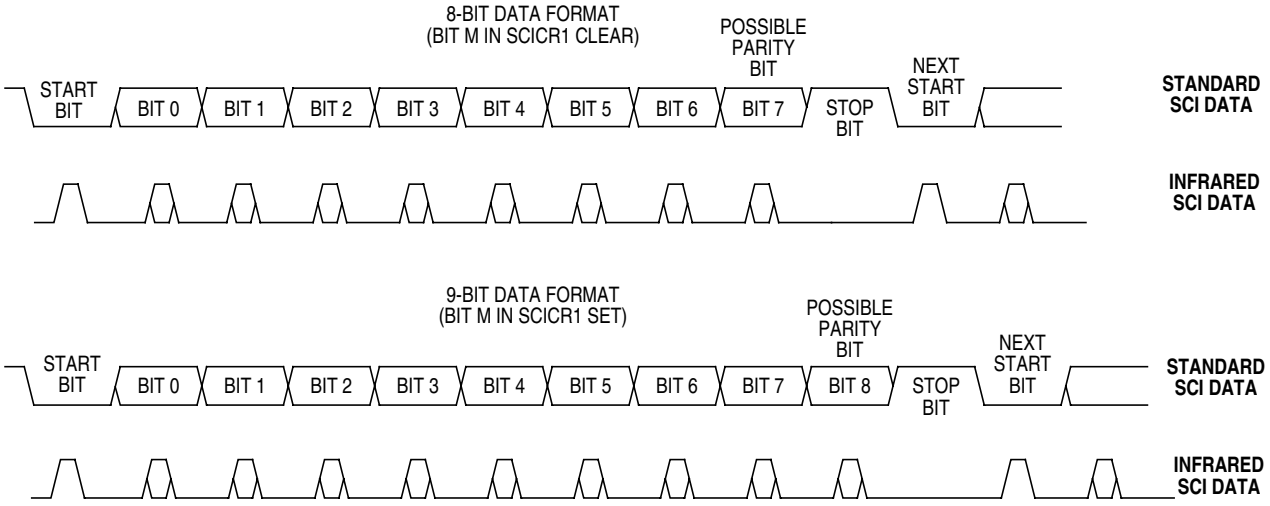


Figure 13-12. SCI Data Formats

Each data character is contained in a frame that includes a start bit, eight or nine data bits, and a stop bit. Clearing the M bit in SCI control register 1 configures the SCI for 8-bit data characters. A frame with eight data bits has a total of 10 bits. Setting the M bit configures the SCI for nine-bit data characters. A frame with nine data bits has a total of 11 bits

Table 13-11. Example of 8-bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	8	0	0	1
1	7	0	1	1
1	7	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 13.4.5.6, “Receiver Wakeup”.

When the SCI is configured for 9-bit data characters, the ninth data bit is the T8 bit in SCI data register high (SCIDRH). It remains unchanged after transmission and can be used repeatedly without rewriting it. A frame with nine data bits has a total of 11 bits.

Table 13-12. Example of 9-Bit Data Formats

Start Bit	Data Bits	Address Bits	Parity Bits	Stop Bit
1	9	0	0	1
1	8	0	1	1
1	8	1[1]	0	1

1 The address bit identifies the frame as an address character. See Section 13.4.5.6, “Receiver Wakeup”.

13.4.3 Baud Rate Generation

A 13-bit modulus counter in the baud rate generator derives the baud rate for both the receiver and the transmitter. The value from 0 to 8191 written to the SBR[12:0] bits determines the module clock divisor. The SBR bits are in the SCI baud rate registers (SCIBDH and SCIBDL). The baud rate clock is synchronized with the bus clock and drives the receiver. The baud rate clock divided by 16 drives the transmitter. The receiver has an acquisition rate of 16 samples per bit time.

Baud rate generation is subject to one source of error:

- Integer division of the module clock may not give the exact target frequency.

Table 13-13 lists some examples of achieving target baud rates with a module clock frequency of 10.2 MHz.

When IREN = 0 then,

SCI baud rate = SCI module clock / (16 * SCIBR[12:0])

Table 13-13. Baud Rates (Example: Module Clock = 10.2 MHz)

Bits SBR[12–0]	Receiver Clock (Hz)	Transmitter Clock (Hz)	Target Baud Rate	Error (%)
17	600,000.0	37,500.0	38,400	2.3
33	309,090.9	19,318.2	19,200	.62
66	154,545.5	9659.1	9600	.62
133	76,691.7	4793.2	4800	.14
266	38,345.9	2396.6	2400	.14
531	19,209.0	1200.6	1200	.11
1062	9604.5	600.3	600	.05
2125	4800.0	300.0	300	.00
4250	2400.0	150.0	150	.00
5795	1760.1	110.0	110	.00

13.4.4 Transmitter

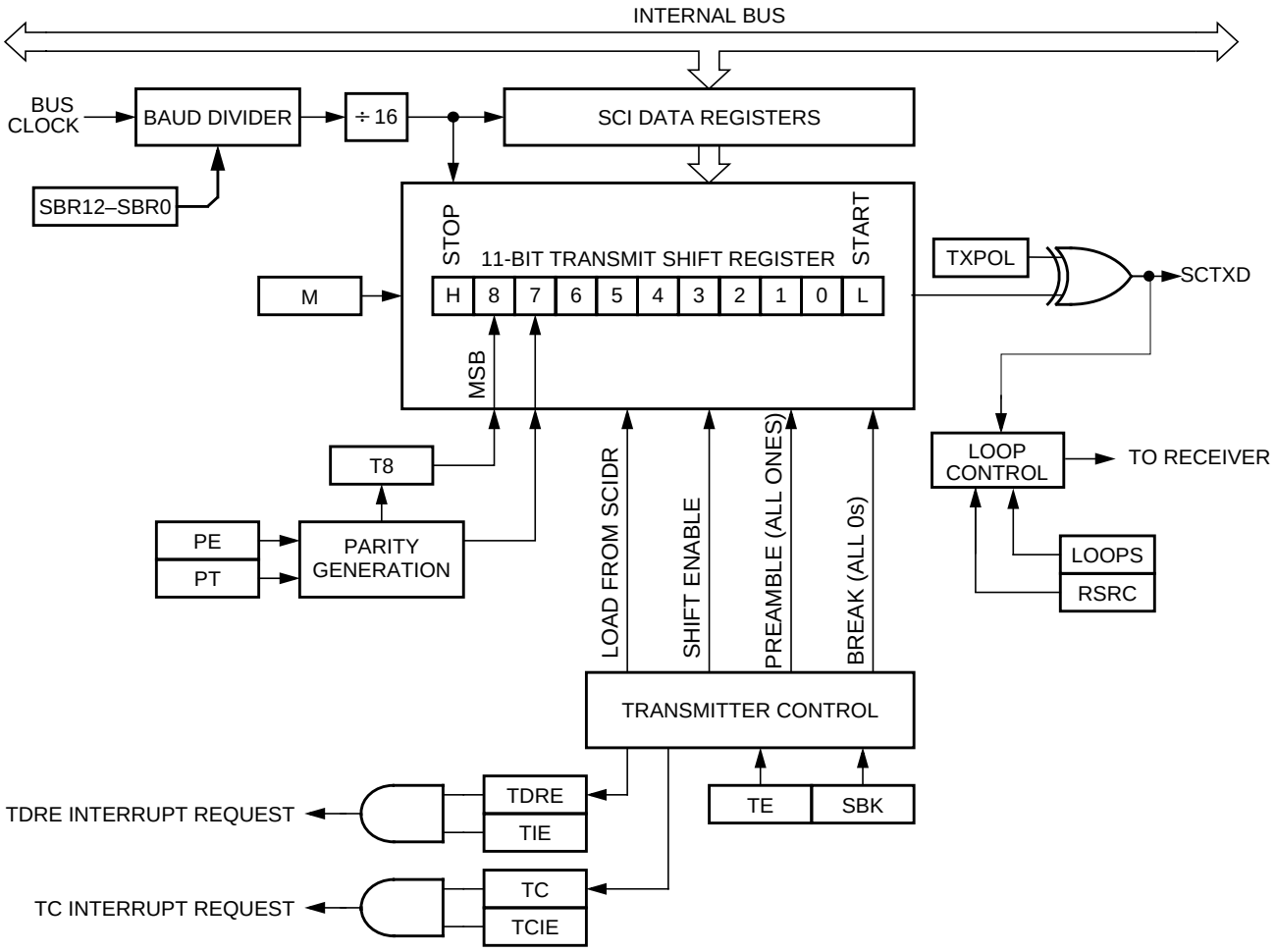


Figure 13-13. Transmitter Block Diagram

13.4.4.1 Transmitter Character Length

The SCI transmitter can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When transmitting 9-bit data, bit T8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

13.4.4.2 Character Transmission

To transmit data, the MCU writes the data bits to the SCI data registers (SCIDRH/SCIDRL), which in turn are transferred to the transmitter shift register. The transmit shift register then shifts a frame out through the TXD pin, after it has prefaced them with a start bit and appended them with a stop bit. The SCI data registers (SCIDRH and SCIDRL) are the write-only buffers between the internal data bus and the transmit shift register.

The SCI also sets a flag, the transmit data register empty flag (TDRE), every time it transfers data from the buffer (SCIDRH/L) to the transmitter shift register. The transmit driver routine may respond to this

flag by writing another byte to the transmitter buffer (SCIDRH/SCIDRL), while the shift register is shifting out the first byte.

To initiate an SCI transmission:

1. Configure the SCI:
   a) Select a baud rate. Write this value to the SCI baud registers (SCIBDH/L) to begin the baud rate generator. Remember that the baud rate generator is disabled when the baud rate is 0. Writing to the SCIBDH has no effect without also writing to SCIBDL.
   b) Write to SCICR1 to configure word length, parity, and other configuration bits (LOOPS, RSRC, M, WAKE, ILT, PE, and PT).
   c) Enable the transmitter, interrupts, receive, and wake up as required, by writing to the SCICR2 register bits (TIE, TCIE, RIE, ILIE, TE, RE, RWU, and SBK). A preamble or idle character will now be shifted out of the transmitter shift register.
2. Transmit procedure for each byte:
   a) Poll the TDRE flag by reading the SCISR1 or responding to the TDRE interrupt. Keep in mind that the TDRE bit resets to 1.
   b) If the TDRE flag is set, write the data to be transmitted to SCIDRH/L, where the ninth bit is written to the T8 bit in SCIDRH if the SCI is in 9-bit data format. A new transmission will not result until the TDRE flag has been cleared.
3. Repeat step 2 for each subsequent transmission.

NOTE

The TDRE flag is set when the shift register is loaded with the next data to be transmitted from SCIDRH/L, which happens, generally speaking, a little over half-way through the stop bit of the previous frame. Specifically, this transfer occurs 9/16ths of a bit time AFTER the start of the stop bit of the previous frame.

Writing the TE bit from 0 to a 1 automatically loads the transmit shift register with a preamble of 10 logic 1s (if M = 0) or 11 logic 1s (if M = 1). After the preamble shifts out, control logic transfers the data from the SCI data register into the transmit shift register. A logic 0 start bit automatically goes into the least significant bit position of the transmit shift register. A logic 1 stop bit goes into the most significant bit position.

Hardware supports odd or even parity. When parity is enabled, the most significant bit (MSB) of the data character is the parity bit.

The transmit data register empty flag, TDRE, in SCI status register 1 (SCISR1) becomes set when the SCI data register transfers a byte to the transmit shift register. The TDRE flag indicates that the SCI data register can accept new data from the internal data bus. If the transmit interrupt enable bit, TIE, in SCI control register 2 (SCICR2) is also set, the TDRE flag generates a transmitter interrupt request.

When the transmit shift register is not transmitting a frame, the TXD pin goes to the idle condition, logic 1. If at any time software clears the TE bit in SCI control register 2 (SCICR2), the transmitter enable signal goes low and the transmit signal goes idle.

If software clears TE while a transmission is in progress (TC = 0), the frame in the transmit shift register continues to shift out. To avoid accidentally cutting off the last frame in a message, always wait for TDRE to go high after the last frame before clearing TE.

To separate messages with preambles with minimum idle line time, use this sequence between messages:

1. Write the last byte of the first message to SCIDRH/L.
2. Wait for the TDRE flag to go high, indicating the transfer of the last frame to the transmit shift register.
3. Queue a preamble by clearing and then setting the TE bit.
4. Write the first byte of the second message to SCIDRH/L.

13.4.4.3 Break Characters

Writing a logic 1 to the send break bit, SBK, in SCI control register 2 (SCICR2) loads the transmit shift register with a break character. A break character contains all logic 0s and has no start, stop, or parity bit. Break character length depends on the M bit in SCI control register 1 (SCICR1). As long as SBK is at logic 1, transmitter logic continuously loads break characters into the transmit shift register. After software clears the SBK bit, the shift register finishes transmitting the last break character and then transmits at least one logic 1. The automatic logic 1 at the end of a break character guarantees the recognition of the start bit of the next frame.

The SCI recognizes a break character when a start bit is followed by eight or nine logic 0 data bits and a logic 0 where the stop bit should be. Receiving a break character has these effects on SCI registers:

- Sets the framing error flag, FE
- Sets the receive data register full flag, RDRF
- Clears the SCI data registers (SCIDRH/L)
- May set the overrun flag, OR, noise flag, NF, parity error flag, PE, or the receiver active flag, RAF (see Section 13.3.2.4, “SCI Status Register 1 (SCISR1)” and Section 13.3.2.5, “SCI Status Register 2 (SCISR2)”).

13.4.4.4 Idle Characters

An idle character (or preamble) contains all logic 1s and has no start, stop, or parity bit. Idle character length depends on the M bit in SCI control register 1 (SCICR1). The preamble is a synchronizing idle character that begins the first transmission initiated after writing the TE bit from 0 to 1.

If the TE bit is cleared during a transmission, the TXD pin becomes idle after completion of the transmission in progress. Clearing and then setting the TE bit during a transmission queues an idle character to be sent after the frame currently being transmitted.

NOTE

When queueing an idle character, return the TE bit to logic 1 before the stop bit of the current frame shifts out through the TXD pin. Setting TE after the stop bit appears on TXD causes data previously written to the SCI data register to be lost. Toggle the TE bit for a queued idle character while the

TDRE flag is set and immediately before writing the next byte to the SCI data register.

If the TE bit is clear and the transmission is complete, the SCI is not the master of the TXD pin

13.4.5 Receiver

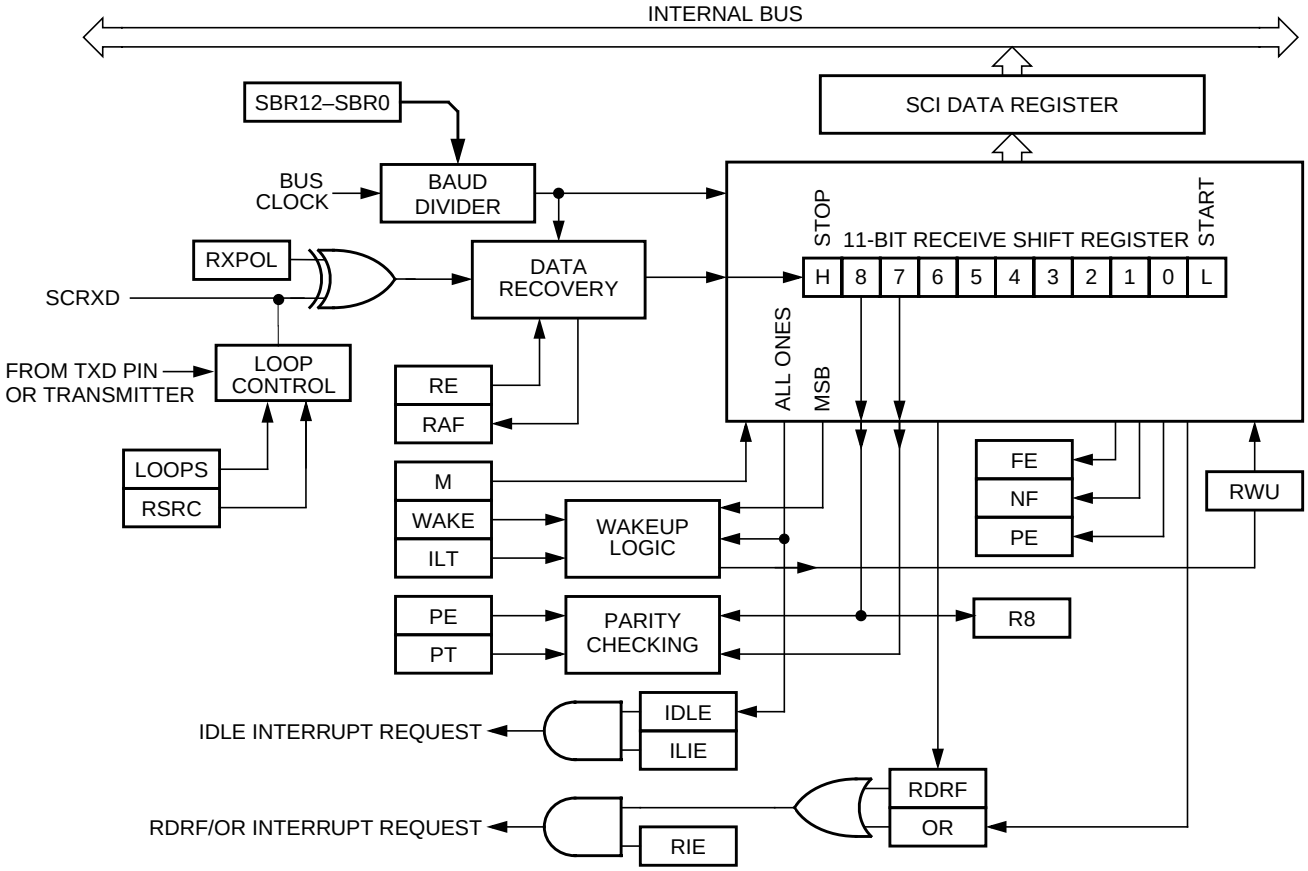


Figure 13-14. SCI Receiver Block Diagram

13.4.5.1 Receiver Character Length

The SCI receiver can accommodate either 8-bit or 9-bit data characters. The state of the M bit in SCI control register 1 (SCICR1) determines the length of data characters. When receiving 9-bit data, bit R8 in SCI data register high (SCIDRH) is the ninth bit (bit 8).

13.4.5.2 Character Reception

During an SCI reception, the receive shift register shifts a frame in from the RXD pin. The SCI data register is the read-only buffer between the internal data bus and the receive shift register.

After a complete frame shifts into the receive shift register, the data portion of the frame transfers to the SCI data register. The receive data register full flag, RDRF, in SCI status register 1 (SCISR1) becomes set,

indicating that the received byte can be read. If the receive interrupt enable bit, RIE, in SCI control register 2 (SCICR2) is also set, the RDRF flag generates an RDRF interrupt request.

13.4.5.3 Data Sampling

The receiver samples the RXD pin at the RT clock rate. The RT clock is an internal signal with a frequency 16 times the baud rate. To adjust for baud rate mismatch, the RT clock (see Figure 13-15) is re-synchronized:

- After every start bit
- After the receiver detects a data bit change from logic 1 to logic 0 (after the majority of data bit samples at RT8, RT9, and RT10 returns a valid logic 1 and the majority of the next RT8, RT9, and RT10 samples returns a valid logic 0)

To locate the start bit, data recovery logic does an asynchronous search for a logic 0 preceded by three logic 1s. When the falling edge of a possible start bit occurs, the RT clock begins to count to 16.

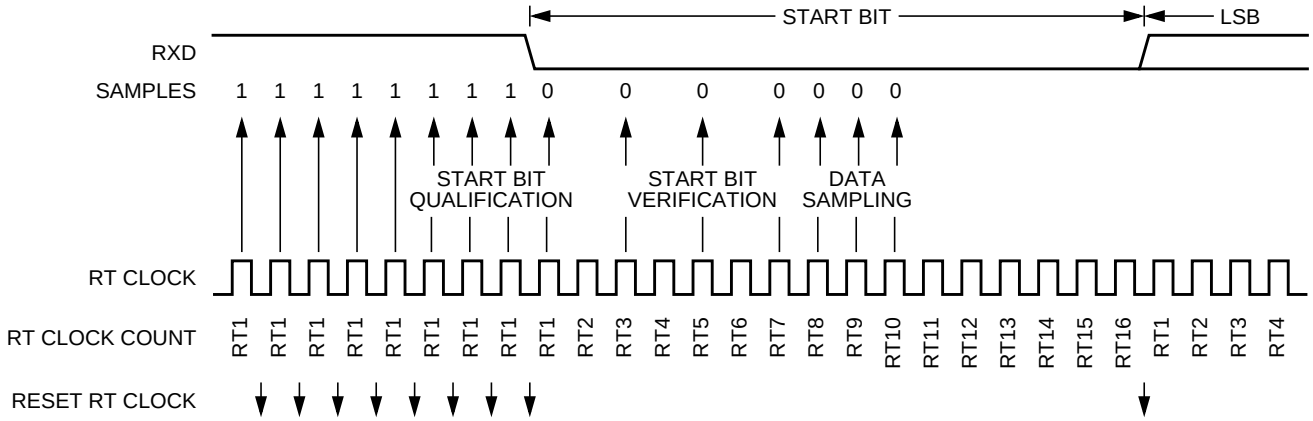


Figure 13-15. Receiver Data Sampling

To verify the start bit and to detect noise, data recovery logic takes samples at RT3, RT5, and RT7. Table 13-14 summarizes the results of the start bit verification samples.

Table 13-14. Start Bit Verification

RT3, RT5, and RT7 Samples	Start Bit Verification	Noise Flag
000	Yes	0
001	Yes	1
010	Yes	1
011	No	0
100	Yes	1
101	No	0
110	No	0
111	No	0

If start bit verification is not successful, the RT clock is reset and a new search for a start bit begins.

To determine the value of a data bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 13-15 summarizes the results of the data bit samples.

Table 13-15. Data Bit Recovery

RT8, RT9, and RT10 Samples	Data Bit Determination	Noise Flag
000	0	0
001	0	1
010	0	1
011	1	1
100	0	1
101	1	1
110	1	1
111	1	0

NOTE

The RT8, RT9, and RT10 samples do not affect start bit verification. If any or all of the RT8, RT9, and RT10 start bit samples are logic 1s following a successful start bit verification, the noise flag (NF) is set and the receiver assumes that the bit is a start bit (logic 0).

To verify a stop bit and to detect noise, recovery logic takes samples at RT8, RT9, and RT10. Table 13-16 summarizes the results of the stop bit samples.

Table 13-16. Stop Bit Recovery

RT8, RT9, and RT10 Samples	Framing Error Flag	Noise Flag
000	1	0
001	1	1
010	1	1
011	0	1
100	1	1
101	0	1
110	0	1
111	0	0

In Figure 13-16 the verification samples RT3 and RT5 determine that the first low detected was noise and not the beginning of a start bit. The RT clock is reset and the start bit search begins again. The noise flag is not set because the noise occurred before the start bit was found.

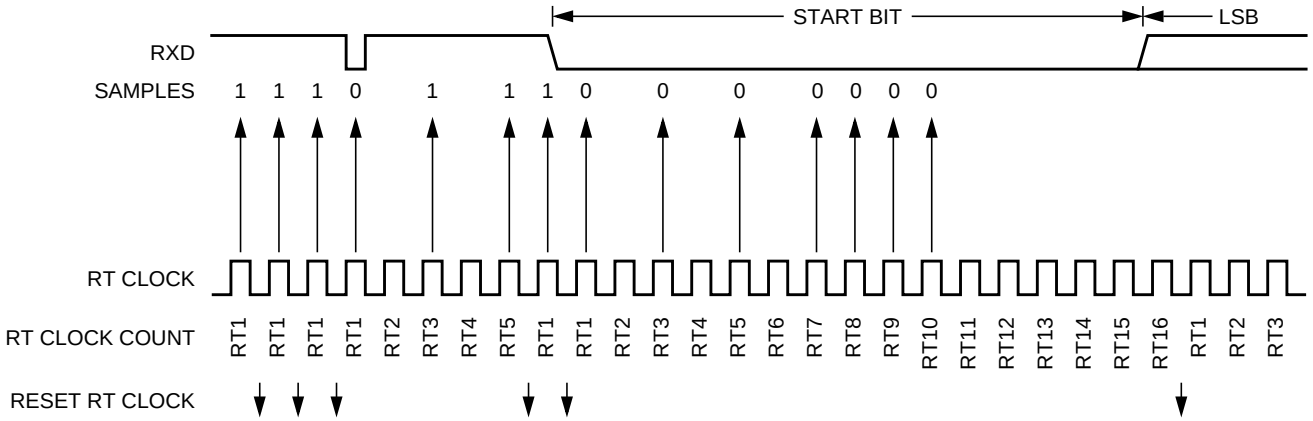


Figure 13-16. Start Bit Search Example 1

In Figure 13-17, verification sample at RT3 is high. The RT3 sample sets the noise flag. Although the perceived bit time is misaligned, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

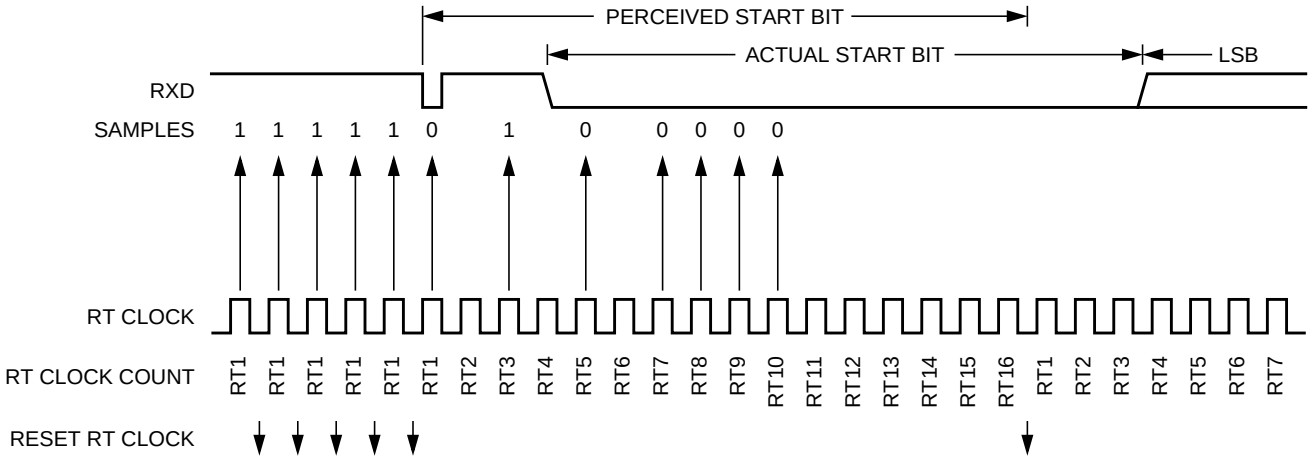


Figure 13-17. Start Bit Search Example 2

In Figure 13-18, a large burst of noise is perceived as the beginning of a start bit, although the test sample at RT5 is high. The RT5 sample sets the noise flag. Although this is a worst-case misalignment of perceived bit time, the data samples RT8, RT9, and RT10 are within the bit time and data recovery is successful.

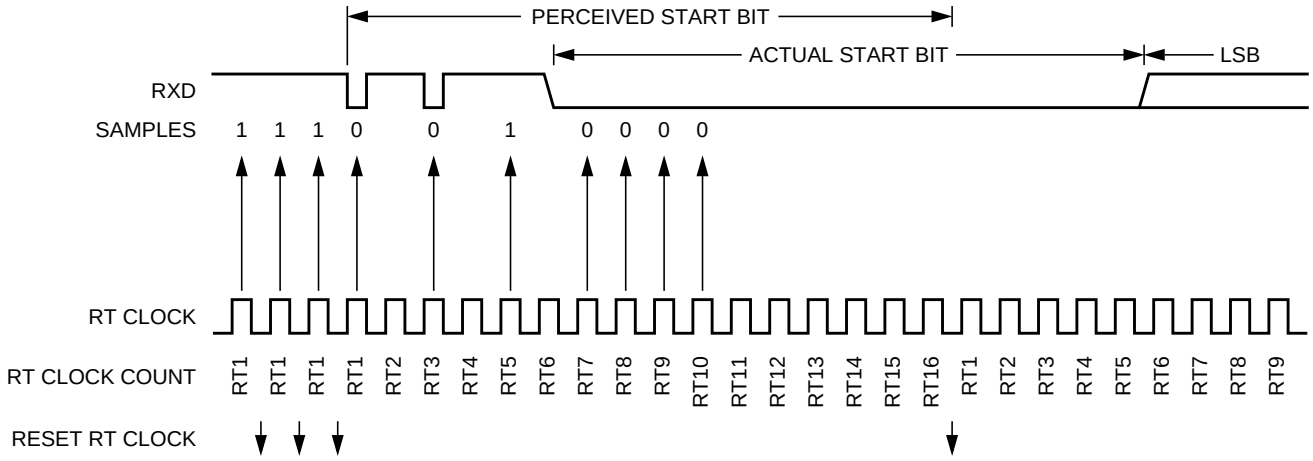


Figure 13-18. Start Bit Search Example 3

Figure 13-19 shows the effect of noise early in the start bit time. Although this noise does not affect proper synchronization with the start bit time, it does set the noise flag.

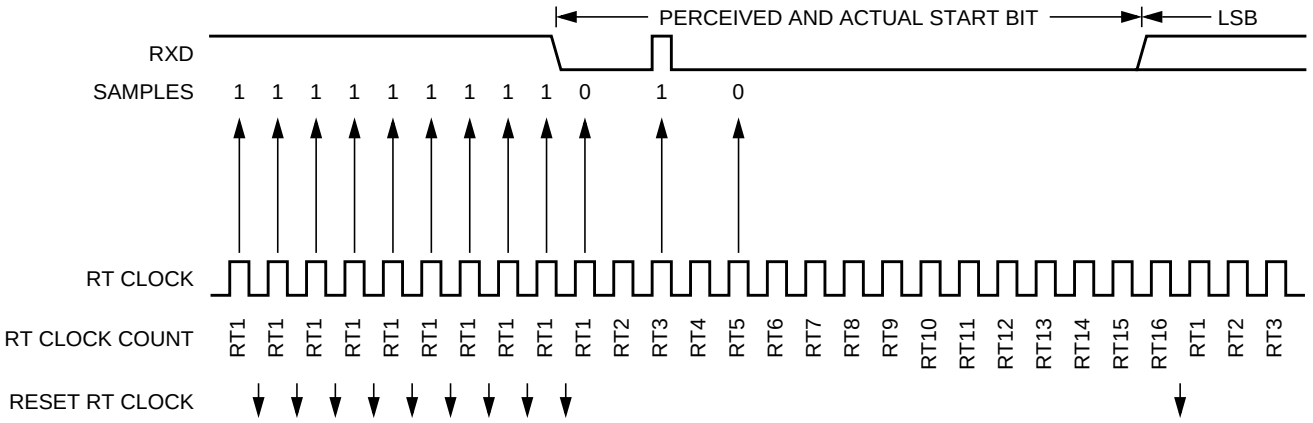


Figure 13-19. Start Bit Search Example 4

Figure 13-20 shows a burst of noise near the beginning of the start bit that resets the RT clock. The sample after the reset is low but is not preceded by three high samples that would qualify as a falling edge. Depending on the timing of the start bit search and on the data, the frame may be missed entirely or it may set the framing error flag.

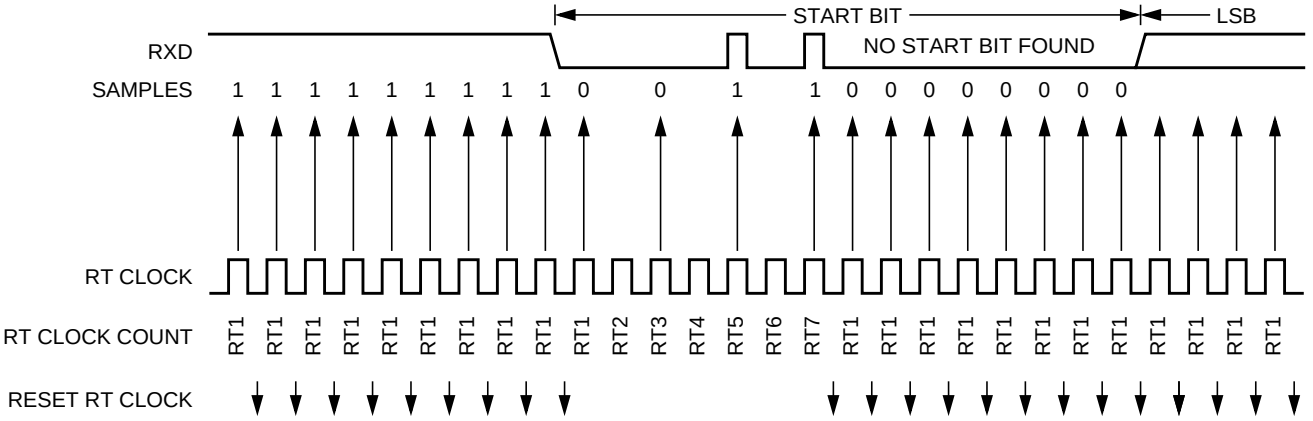


Figure 13-20. Start Bit Search Example 5

In Figure 13-21, a noise burst makes the majority of data samples RT8, RT9, and RT10 high. This sets the noise flag but does not reset the RT clock. In start bits only, the RT8, RT9, and RT10 data samples are ignored.

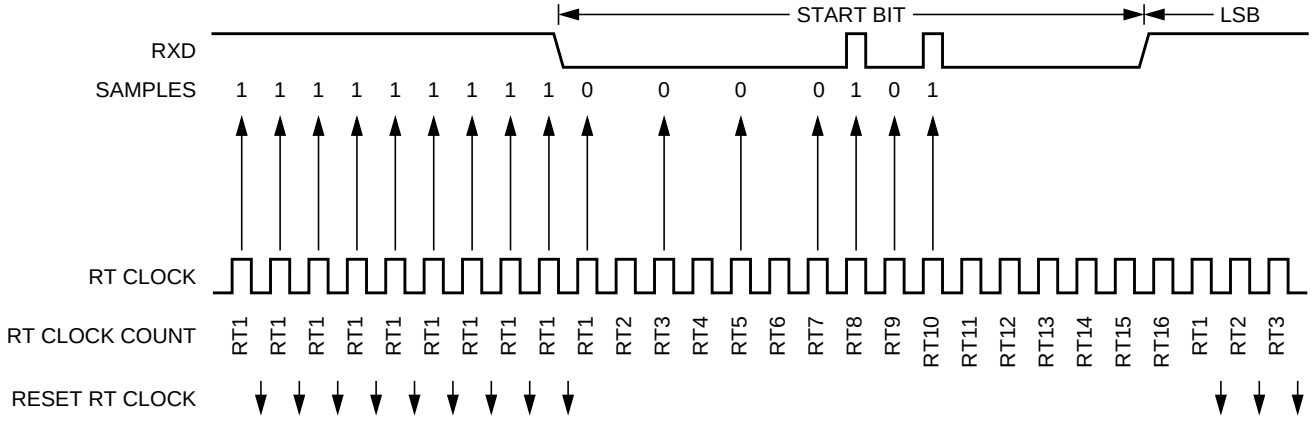


Figure 13-21. Start Bit Search Example 6

13.4.5.4 Framing Errors

If the data recovery logic does not detect a logic 1 where the stop bit should be in an incoming frame, it sets the framing error flag, FE, in SCI status register 1 (SCISR1). A break character also sets the FE flag because a break character has no stop bit. The FE flag is set at the same time that the RDRF flag is set.

13.4.5.5 Baud Rate Tolerance

A transmitting device may be operating at a baud rate below or above the receiver baud rate. Accumulated bit time misalignment can cause one of the three stop bit data samples (RT8, RT9, and RT10) to fall outside the actual stop bit. A noise error will occur if the RT8, RT9, and RT10 samples are not all the same logical values. A framing error will occur if the receiver clock is misaligned in such a way that the majority of the RT8, RT9, and RT10 stop bit samples are a logic 0.

As the receiver samples an incoming frame, it re-synchronizes the RT clock on any valid falling edge within the frame. Re synchronization within frames will correct a misalignment between transmitter bit times and receiver bit times.

13.4.5.5.1 Slow Data Tolerance

Figure 13-22 shows how much a slow received frame can be misaligned without causing a noise error or a framing error. The slow stop bit begins at RT8 instead of RT1 but arrives in time for the stop bit data samples at RT8, RT9, and RT10.

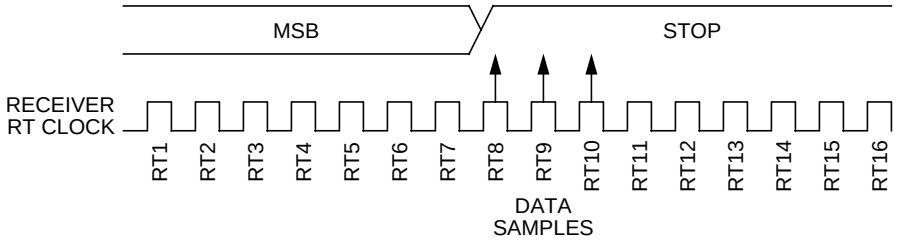


Figure 13-22. Slow Data

Let’s take RTr as receiver RT clock and RTt as transmitter RT clock.

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles +7 RTr cycles =151 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 13-22, the receiver counts 151 RTr cycles at the point when the count of the transmitting device is 9 bit times x 16 RTt cycles = 144 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 8-bit data character with no errors is:

((151 – 144) / 151) x 100 = 4.63%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 7 RTr cycles = 167 RTr cycles to start data sampling of the stop bit.

With the misaligned character shown in Figure 13-22, the receiver counts 167 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a slow 9-bit character with no errors is:

((167 – 160) / 167) X 100 = 4.19%

13.4.5.5.2 Fast Data Tolerance

Figure 13-23 shows how much a fast received frame can be misaligned. The fast stop bit ends at RT10 instead of RT16 but continues to be sampled at RT8, RT9, and RT10.

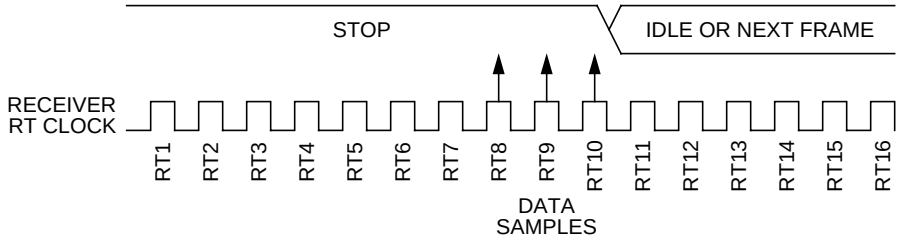


Figure 13-23. Fast Data

For an 8-bit data character, it takes the receiver 9 bit times x 16 RTr cycles + 10 RTr cycles = 154 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 13-23, the receiver counts 154 RTr cycles at the point when the count of the transmitting device is 10 bit times x 16 RTt cycles = 160 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 8-bit character with no errors is:

((160 – 154) / 160) x 100 = 3.75%

For a 9-bit data character, it takes the receiver 10 bit times x 16 RTr cycles + 10 RTr cycles = 170 RTr cycles to finish data sampling of the stop bit.

With the misaligned character shown in Figure 13-23, the receiver counts 170 RTr cycles at the point when the count of the transmitting device is 11 bit times x 16 RTt cycles = 176 RTt cycles.

The maximum percent difference between the receiver count and the transmitter count of a fast 9-bit character with no errors is:

((176 – 170) / 176) x 100 = 3.40%

13.4.5.6 Receiver Wakeup

To enable the SCI to ignore transmissions intended only for other receivers in multiple-receiver systems, the receiver can be put into a standby state. Setting the receiver wakeup bit, RWU, in SCI control register 2 (SCICR2) puts the receiver into standby state during which receiver interrupts are disabled.The SCI will continue to load the receive data into the SCIDRH/L registers, but it will not set the RDRF flag.

The transmitting device can address messages to selected receivers by including addressing information in the initial frame or frames of each message.

The WAKE bit in SCI control register 1 (SCICR1) determines how the SCI is brought out of the standby state to process an incoming message. The WAKE bit enables either idle line wakeup or address mark wakeup.

13.4.5.6.1 Idle Input Line Wakeup (WAKE = 0)

In this wakeup method, an idle condition on the RXD pin clears the RWU bit and wakes up the SCI. The initial frame or frames of every message contain addressing information. All receivers evaluate the addressing information, and receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another idle character appears on the RXD pin.

Idle line wakeup requires that messages be separated by at least one idle character and that no message contains idle characters.

The idle character that wakes a receiver does not set the receiver idle bit, IDLE, or the receive data register full flag, RDRF.

The idle line type bit, ILT, determines whether the receiver begins counting logic 1s as idle character bits after the start bit or after the stop bit. ILT is in SCI control register 1 (SCICR1).

13.4.5.6.2 Address Mark Wakeup (WAKE = 1)

In this wakeup method, a logic 1 in the most significant bit (MSB) position of a frame clears the RWU bit and wakes up the SCI. The logic 1 in the MSB position marks a frame as an address frame that contains addressing information. All receivers evaluate the addressing information, and the receivers for which the message is addressed process the frames that follow. Any receiver for which a message is not addressed can set its RWU bit and return to the standby state. The RWU bit remains set and the receiver remains on standby until another address frame appears on the RXD pin.

The logic 1 MSB of an address frame clears the receiver's RWU bit before the stop bit is received and sets the RDRF flag.

Address mark wakeup allows messages to contain idle characters but requires that the MSB be reserved for use in address frames.

NOTE

With the WAKE bit clear, setting the RWU bit after the RXD pin has been idle can cause the receiver to wake up immediately.

13.4.6 Single-Wire Operation

Normally, the SCI uses two pins for transmitting and receiving. In single-wire operation, the RXD pin is disconnected from the SCI. The SCI uses the TXD pin for both receiving and transmitting.

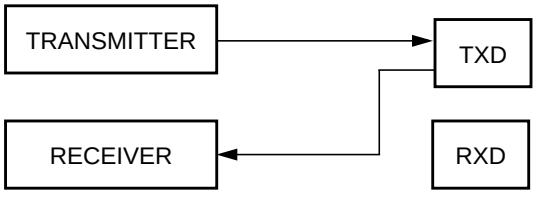


Figure 13-24. Single-Wire Operation (LOOPS = 1, RSRC = 1)

Enable single-wire operation by setting the LOOPS bit and the receiver source bit, RSRC, in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Setting the RSRC bit connects the TXD pin to the receiver. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).The TXDIR bit (SCISR2[1]) determines whether the TXD pin is going to be used as an input (TXDIR = 0) or an output (TXDIR = 1) in this mode of operation.

NOTE

In single-wire operation data from the TXD pin is inverted if RXPOL is set.

13.4.7 Loop Operation

In loop operation the transmitter output goes to the receiver input. The RXD pin is disconnected from the SCI

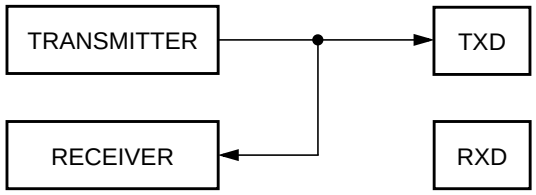


Figure 13-25. Loop Operation (LOOPS = 1, RSRC = 0)

Enable loop operation by setting the LOOPS bit and clearing the RSRC bit in SCI control register 1 (SCICR1). Setting the LOOPS bit disables the path from the RXD pin to the receiver. Clearing the RSRC bit connects the transmitter output to the receiver input. Both the transmitter and receiver must be enabled (TE = 1 and RE = 1).

NOTE

In loop operation data from the transmitter is not recognized by the receiver if RXPOL and TXPOL are not the same.

13.5 Interrupts

This section describes the interrupt originated by the SCI block.The MCU must service the interrupt requests. Table 13-17 lists the five interrupt sources of the SCI.

Table 13-17. SCI Interrupt Sources

Interrupt	Source	Local Enable	Description
TDRE	SCISR1[7]	TIE	Active high level. Indicates that a byte was transferred from SCIDRH/L to the transmit shift register.
TC	SCISR1[6]	TCIE	Active high level. Indicates that a transmit is complete.
RDRF	SCISR1[5]	RIE	Active high level. The RDRF interrupt indicates that received data is available in the SCI data register.
OR	SCISR1[3]		Active high level. This interrupt indicates that an overrun condition has occurred.

Table 13-17. SCI Interrupt Sources

IDLE	SCISR1[4]	ILIE	Active high level. Indicates that receiver input has become idle.

13.5.1 Description of Interrupt Operation

The SCI only originates interrupt requests. The following is a description of how the SCI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt number are chip dependent. The SCI only has a single interrupt line (SCI interrupt signal, active high operation) and all the following interrupts, when generated, are ORed together and issued through that port.

13.5.1.1 TDRE Description

The TDRE interrupt is set high by the SCI when the transmit shift register receives a byte from the SCI data register. A TDRE interrupt indicates that the transmit data register (SCIDRH/L) is empty and that a new byte can be written to the SCIDRH/L for transmission.Clear TDRE by reading SCI status register 1 with TDRE set and then writing to SCI data register low (SCIDRL).

13.5.1.2 TC Description

The TC interrupt is set by the SCI when a transmission has been completed.A TC interrupt indicates that there is no transmission in progress. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted. When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL).TC is cleared automatically when data, preamble, or break is queued and ready to be sent.

13.5.1.3 RDRF Description

The RDRF interrupt is set when the data in the receive shift register transfers to the SCI data register. A RDRF interrupt indicates that the received data has been transferred to the SCI data register and that the byte can now be read by the MCU. The RDRF interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

13.5.1.4 OR Description

The OR interrupt is set when software fails to read the SCI data register before the receive shift register receives the next frame. The newly acquired data in the shift register will be lost in this case, but the data already in the SCI data registers is not affected. The OR interrupt is cleared by reading the SCI status register one (SCISR1) and then reading SCI data register low (SCIDRL).

13.5.1.5 IDLE Description

The IDLE interrupt is set when 10 consecutive logic 1s (if M = 0) or 11 consecutive logic 1s (if M = 1) appear on the receiver input. After the IDLE is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag. Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

13.5.2 Recovery from Wait Mode

The SCI interrupt request can be used to bring the CPU out of wait mode.

Chapter 14
Serial Peripheral Interface (SPIV3)

14.1 Introduction

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or the SPI operation can be interrupt driven.

14.1.1 Features

The SPI includes these distinctive features:

- Master mode and slave mode
- Bidirectional mode
- Slave select output
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- Control of SPI operation during wait mode

14.1.2 Modes of Operation

The SPI functions in three modes, run, wait, and stop.

- Run Mode
  This is the basic mode of operation.
- Wait Mode
  SPI operation in wait mode is a configurable low power mode, controlled by the SPISWAI bit located in the SPICR2 register. In wait mode, if the SPISWAI bit is clear, the SPI operates like in Run Mode. If the SPISWAI bit is set, the SPI goes into a power conservative state, with the SPI clock generation turned off. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into Run Mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.
- Stop Mode
  The SPI is inactive in stop mode for reduced power consumption. If the SPI is configured as a master, any transmission in progress stops, but is resumed after CPU goes into run mode. If the SPI is configured as a slave, reception and transmission of a byte continues, so that the slave stays synchronized to the master.

This is a high level description only, detailed descriptions of operating modes are contained in Section 14.4, “Functional Description.”

14.1.3 Block Diagram

Figure 14-1 gives an overview on the SPI architecture. The main parts of the SPI are status, control, and data registers, shifter logic, baud rate generator, master/slave control logic, and port control logic.

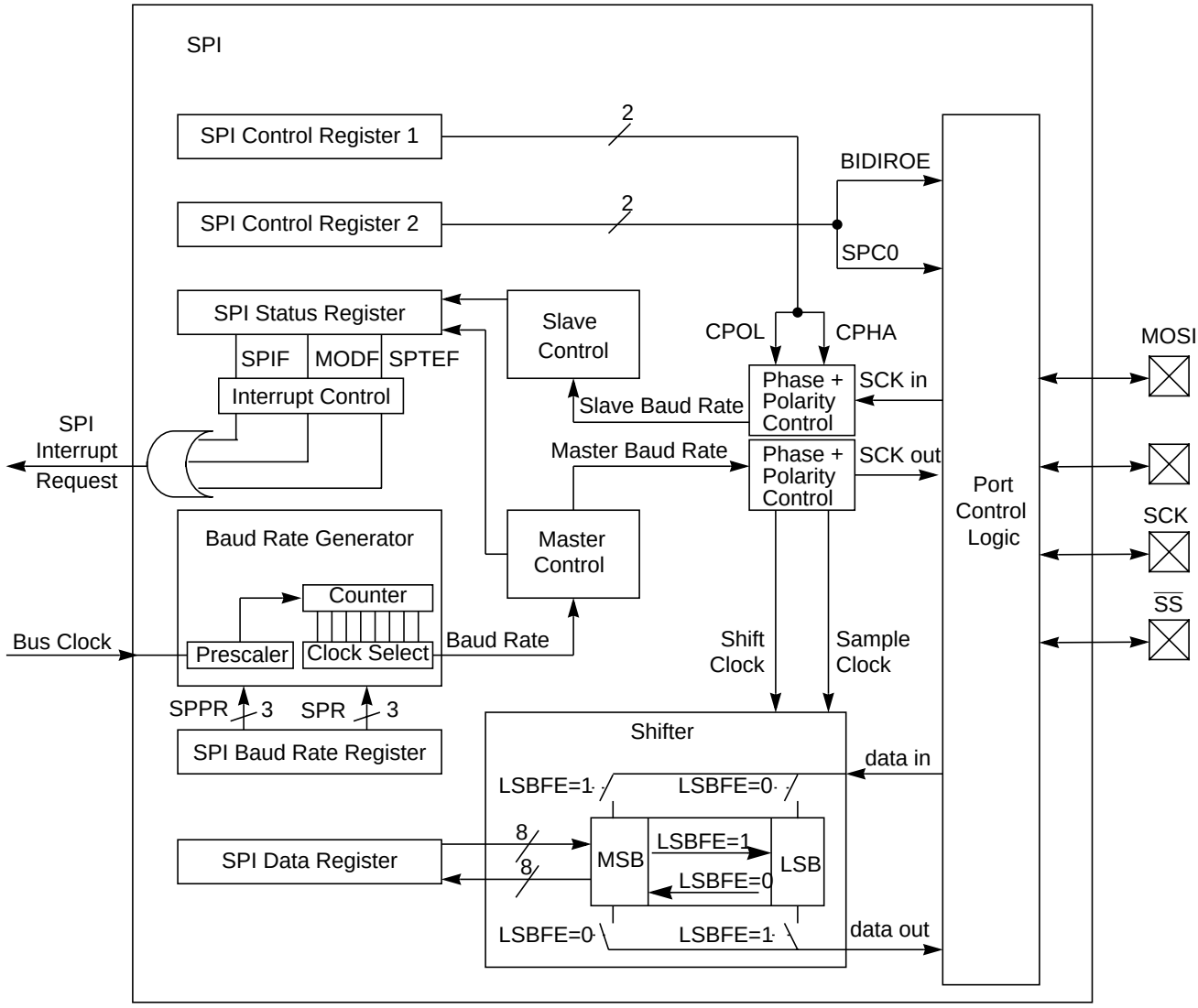


Figure 14-1. SPI Block Diagram

14.2 External Signal Description

This section lists the name and description of all ports including inputs and outputs that do, or may, connect off chip. The SPI module has a total of four external pins.

14.2.1 MOSI — Master Out/Slave In Pin

This pin is used to transmit data out of the SPI module when it is configured as a master and receive data when it is configured as slave.

14.2.2 MISO — Master In/Slave Out Pin

This pin is used to transmit data out of the SPI module when it is configured as a slave and receive data when it is configured as master.

14.2.3 $\overline{SS}$ — Slave Select Pin

This pin is used to output the select signal from the SPI module to another peripheral with which a data transfer is to take place when its configured as a master and its used as an input to receive the slave select signal when the SPI is configured as slave.

14.2.4 SCK — Serial Clock Pin

This pin is used to output the clock with respect to which the SPI transfers data or receive clock in case of slave.

14.3 Memory Map and Register Definition

This section provides a detailed description of address space and registers used by the SPI.

The memory map for the SPI is given below in Table 14-1. The address listed for each register is the sum of a base address and an address offset. The base address is defined at the SoC level and the address offset is defined at the module level. Reads from the reserved bits return zeros and writes to the reserved bits have no effect.

14.3.1 Module Memory Map

Table 14-1. SPI Memory Map

Address	Use	Access
0x0000	SPI Control Register 1 (SPICR1)	R/W
0x0001	SPI Control Register 2 (SPICR2)	R/W[1]
0x0002	SPI Baud Rate Register (SPIBR)	R/W[1]
0x0003	SPI Status Register (SPISR)	R[2]
0x0004	Reserved	—[2,3]
0x0005	SPI Data Register (SPIDR)	R/W
0x0006	Reserved	—[2,3]
0x0007	Reserved	—[2,3]

1 Certain bits are non-writable.
2 Writes to this register are ignored.
3 Reading from this register returns all zeros.

14.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Name		7	6	5	4	3	2	1	0
SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
	W								
SPICR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
	W								
SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
	W								
SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
	W								
Reserved	R								
	W								
SPIDR	R	Bit 7	6	5	4	3	2	2	Bit 0
	W								
Reserved	R								
	W								
Reserved	R								
	W								

= Unimplemented or Reserved

Figure 14-2. SPI Register Summary

14.3.2.1 SPI Control Register 1 (SPICR1)

	7	6	5	4	3	2	1	0
R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
W								
Reset	0	0	0	0	0	1	0	0

Figure 14-3. SPI Control Register 1 (SPICR1)

Read: anytime

Write: anytime

Table 14-2. SPICR1 Field Descriptions

Field	Description
7 SPIE	**SPI Interrupt Enable Bit** — This bit enables SPI interrupt requests, if SPIF or MODF status flag is set. 0 SPI interrupts disabled. 1 SPI interrupts enabled.
6 SPE	**SPI System Enable Bit** — This bit enables the SPI system and dedicates the SPI port pins to SPI system functions. If SPE is cleared, SPI is disabled and forced into idle state, status bits in SPISR register are reset. 0 SPI disabled (lower power consumption). 1 SPI enabled, port pins are dedicated to SPI functions.
5 SPTIE	**SPI Transmit Interrupt Enable** — This bit enables SPI interrupt requests, if SPTEF flag is set. 0 SPTEF interrupt disabled. 1 SPTEF interrupt enabled.
4 MSTR	**SPI Master/Slave Mode Select Bit** — This bit selects, if the SPI operates in master or slave mode. Switching the SPI from master to slave or vice versa forces the SPI system into idle state. 0 SPI is in slave mode 1 SPI is in master mode
3 CPOL	**SPI Clock Polarity Bit** — This bit selects an inverted or non-inverted SPI clock. To transmit data between SPI modules, the SPI modules must have identical CPOL values. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Active-high clocks selected. In idle state SCK is low. 1 Active-low clocks selected. In idle state SCK is high.
2 CPHA	**SPI Clock Phase Bit** — This bit is used to select the SPI clock format. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Sampling of data occurs at odd edges (1,3,5,...,15) of the SCK clock 1 Sampling of data occurs at even edges (2,4,6,...,16) of the SCK clock
1 SSOE	**Slave Select Output Enable** — The $\overline{SS}$ output feature is enabled only in master mode, if MODFEN is set, by asserting the SSOE as shown in Table 14-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state.
0 LSBFE	**LSB-First Enable** — This bit does not affect the position of the MSB and LSB in the data register. Reads and writes of the data register always have the MSB in bit 7. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 Data is transferred most significant bit first. 1 Data is transferred least significant bit first.

Table 14-3. $\overline{SS}$ Input / Output Selection

MODFEN	SSOE	Master Mode	Slave Mode
0	0	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
0	1	$\overline{SS}$ not used by SPI	$\overline{SS}$ input
1	0	$\overline{SS}$ input with MODF feature	$\overline{SS}$ input
1	1	$\overline{SS}$ is slave select output	$\overline{SS}$ input

14.3.2.2 SPI Control Register 2 (SPICR2)

	7	6	5	4	3	2	1	0
R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-4. SPI Control Register 2 (SPICR2)

Read: anytime

Write: anytime; writes to the reserved bits have no effect

Table 14-4. SPICR2 Field Descriptions

Field	Description
4 MODFEN	**Mode Fault Enable Bit** — This bit allows the MODF failure being detected. If the SPI is in master mode and MODFEN is cleared, then the $\overline{SS}$ port pin is not used by the SPI. In slave mode, the $\overline{SS}$ is available only as an input regardless of the value of MODFEN. For an overview on the impact of the MODFEN bit on the $\overline{SS}$ port pin configuration refer to Table 14-3. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state. 0 $\overline{SS}$ port pin is not used by the SPI 1 $\overline{SS}$ port pin with MODF feature
3 BIDIROE	**Output Enable in the Bidirectional Mode of Operation** — This bit controls the MOSI and MISO output buffer of the SPI, when in bidirectional mode of operation (SPC0 is set). In master mode this bit controls the output buffer of the MOSI port, in slave mode it controls the output buffer of the MISO port. In master mode, with SPC0 set, a change of this bit will abort a transmission in progress and force the SPI into idle state. 0 Output buffer disabled 1 Output buffer enabled
1 SPISWAI	**SPI Stop in Wait Mode Bit** — This bit is used for power conservation while in wait mode. 0 SPI clock operates normally in wait mode 1 Stop SPI clock generation when in wait mode
0 SPC0	**Serial Pin Control Bit 0** — This bit enables bidirectional pin configurations as shown in Table 14-5. In master mode, a change of this bit will abort a transmission in progress and force the SPI system into idle state

Table 14-5. Bidirectional Pin Configurations

Pin Mode	SPC0	BIDIROE	MISO	MOSI
Master Mode of Operation				
Normal	0	X	Master In	Master Out
Bidirectional	1	0	MISO not used by SPI	Master In
		1		Master I/O
Slave Mode of Operation				
Normal	0	X	Slave Out	Slave In
Bidirectional	1	0	Slave In	MOSI not used by SPI
		1	Slave I/O	

14.3.2.3 SPI Baud Rate Register (SPIBR)

	7	6	5	4	3	2	1	0
R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-5. SPI Baud Rate Register (SPIBR)

Read: anytime

Write: anytime; writes to the reserved bits have no effect

Table 14-6. SPIBR Field Descriptions

Field	Description
6:4 SPPR[2:0]	**SPI Baud Rate Preselection Bits** — These bits specify the SPI baud rates as shown in Table 14-7. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.
2:0 SPR[2:0}	**SPI Baud Rate Selection Bits** — These bits specify the SPI baud rates as shown in Table 14-7. In master mode, a change of these bits will abort a transmission in progress and force the SPI system into idle state.

The baud rate divisor equation is as follows:

$$BaudRateDivisor = (SPPR + 1) \bullet 2^{(SPR + 1)}$$

The baud rate can be calculated with the following equation:

$$Baud\ Rate = BusClock / BaudRateDivisor$$

Table 14-7. Example SPI Baud Rate Selection (25 MHz Bus Clock)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
0	0	0	0	0	0	2	12.5 MHz
0	0	0	0	0	1	4	6.25 MHz
0	0	0	0	1	0	8	3.125 MHz
0	0	0	0	1	1	16	1.5625 MHz
0	0	0	1	0	0	32	781.25 kHz
0	0	0	1	0	1	64	390.63 kHz
0	0	0	1	1	0	128	195.31 kHz
0	0	0	1	1	1	256	97.66 kHz
0	0	1	0	0	0	4	6.25 MHz
0	0	1	0	0	1	8	3.125 MHz
0	0	1	0	1	0	16	1.5625 MHz
0	0	1	0	1	1	32	781.25 kHz
0	0	1	1	0	0	64	390.63 kHz
0	0	1	1	0	1	128	195.31 kHz
0	0	1	1	1	0	256	97.66 kHz
0	0	1	1	1	1	512	48.83 kHz
0	1	0	0	0	0	6	4.16667 MHz
0	1	0	0	0	1	12	2.08333 MHz
0	1	0	0	1	0	24	1.04167 MHz
0	1	0	0	1	1	48	520.83 kHz
0	1	0	1	0	0	96	260.42 kHz
0	1	0	1	0	1	192	130.21 kHz
0	1	0	1	1	0	384	65.10 kHz
0	1	0	1	1	1	768	32.55 kHz
0	1	1	0	0	0	8	3.125 MHz
0	1	1	0	0	1	16	1.5625 MHz
0	1	1	0	1	0	32	781.25 kHz
0	1	1	0	1	1	64	390.63 kHz
0	1	1	1	0	0	128	195.31 kHz
0	1	1	1	0	1	256	97.66 kHz
0	1	1	1	1	0	512	48.83 kHz
0	1	1	1	1	1	1024	24.41 kHz
1	0	0	0	0	0	10	2.5 MHz
1	0	0	0	0	1	20	1.25 MHz
1	0	0	0	1	0	40	625 kHz
1	0	0	0	1	1	80	312.5 kHz
1	0	0	1	0	0	160	156.25 kHz
1	0	0	1	0	1	320	78.13 kHz
1	0	0	1	1	0	640	39.06 kHz

Table 14-7. Example SPI Baud Rate Selection (25 MHz Bus Clock) (continued)

SPPR2	SPPR1	SPPR0	SPR2	SPR1	SPR0	Baud Rate Divisor	Baud Rate
1	0	0	1	1	1	1280	19.53 kHz
1	0	1	0	0	0	12	2.08333 MHz
1	0	1	0	0	1	24	1.04167 MHz
1	0	1	0	1	0	48	520.83 kHz
1	0	1	0	1	1	96	260.42 kHz
1	0	1	1	0	0	192	130.21 kHz
1	0	1	1	0	1	384	65.10 kHz
1	0	1	1	1	0	768	32.55 kHz
1	0	1	1	1	1	1536	16.28 kHz
1	1	0	0	0	0	14	1.78571 MHz
1	1	0	0	0	1	28	892.86 kHz
1	1	0	0	1	0	56	446.43 kHz
1	1	0	0	1	1	112	223.21 kHz
1	1	0	1	0	0	224	111.61 kHz
1	1	0	1	0	1	448	55.80 kHz
1	1	0	1	1	0	896	27.90 kHz
1	1	0	1	1	1	1792	13.95 kHz
1	1	1	0	0	0	16	1.5625 MHz
1	1	1	0	0	1	32	781.25 kHz
1	1	1	0	1	0	64	390.63 kHz
1	1	1	0	1	1	128	195.31 kHz
1	1	1	1	0	0	256	97.66 kHz
1	1	1	1	0	1	512	48.83 kHz
1	1	1	1	1	0	1024	24.41 kHz
1	1	1	1	1	1	2048	12.21 kHz

NOTE

In slave mode of SPI S-clock speed DIV2 is not supported.

14.3.2.4 SPI Status Register (SPISR)

	7	6	5	4	3	2	1	0
R	SPIF	0	SPTEF	MODF	0	0	0	0
W								
Reset	0	0	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-6. SPI Status Register (SPISR)

Read: anytime

Write: has no effect

Table 14-8. SPISR Field Descriptions

Field	Description
7 SPIF	**SPIF Interrupt Flag** — This bit is set after a received data byte has been transferred into the SPI Data Register. This bit is cleared by reading the SPISR register (with SPIF set) followed by a read access to the SPI Data Register. 0 Transfer not yet complete 1 New data copied to SPIDR
5 SPTEF	**SPI Transmit Empty Interrupt Flag** — If set, this bit indicates that the transmit data register is empty. To clear this bit and place data into the transmit data register, SPISR has to be read with SPTEF = 1, followed by a write to SPIDR. Any write to the SPI Data Register without reading SPTEF = 1, is effectively ignored. 0 SPI Data register not empty 1 SPI Data register empty
4 MODF	**Mode Fault Flag** — This bit is set if the $\overline{SS}$ input becomes low while the SPI is configured as a master and mode fault detection is enabled, MODFEN bit of SPICR2 register is set. Refer to MODFEN bit description in Section 14.3.2.2, “SPI Control Register 2 (SPICR2).” The flag is cleared automatically by a read of the SPI Status Register (with MODF set) followed by a write to the SPI Control Register 1. 0 Mode fault has not occurred. 1 Mode fault has occurred.

14.3.2.5 SPI Data Register (SPIDR)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	2	Bit 0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 14-7. SPI Data Register (SPIDR)

Read: anytime; normally read only after SPIF is set

Write: anytime

The SPI Data Register is both the input and output register for SPI data. A write to this register allows a data byte to be queued and transmitted. For a SPI configured as a master, a queued data byte is transmitted immediately after the previous transmission has completed. The SPI Transmitter Empty Flag SPTEF in the SPISR register indicates when the SPI Data Register is ready to accept new data.

Reading the data can occur anytime from after the SPIF is set to before the end of the next transfer. If the SPIF is not serviced by the end of the successive transfers, those data bytes are lost and the data within the SPIDR retains the first byte until SPIF is serviced.

14.4 Functional Description

The SPI module allows a duplex, synchronous, serial communication between the MCU and peripheral devices. Software can poll the SPI status flags or SPI operation can be interrupt driven.

The SPI system is enabled by setting the SPI enable (SPE) bit in SPI Control Register 1. While SPE bit is set, the four associated SPI port pins are dedicated to the SPI function as:

- Slave select ($\overline{SS}$)
- Serial clock (SCK)
- Master out/slave in (MOSI)
- Master in/slave out (MISO)

The main element of the SPI system is the SPI Data Register. The 8-bit data register in the master and the 8-bit data register in the slave are linked by the MOSI and MISO pins to form a distributed 16-bit register. When a data transfer operation is performed, this 16-bit register is serially shifted eight bit positions by the S-clock from the master, so data is exchanged between the master and the slave. Data written to the master SPI Data Register becomes the output data for the slave, and data read from the master SPI Data Register after a transfer operation is the input data from the slave.

A read of SPISR with SPTEF = 1 followed by a write to SPIDR puts data into the transmit data register. When a transfer is complete, received data is moved into the receive data register. Data may be read from this double-buffered system any time before the next transfer has completed. This 8-bit data register acts as the SPI receive data register for reads and as the SPI transmit data register for writes. A single SPI register address is used for reading data from the read data buffer and for writing data to the transmit data register.

The clock phase control bit (CPHA) and a clock polarity control bit (CPOL) in the SPI Control Register 1 (SPICR1) select one of four possible clock formats to be used by the SPI system. The CPOL bit simply selects a non-inverted or inverted clock. The CPHA bit is used to accommodate two fundamentally different protocols by sampling data on odd numbered SCK edges or on even numbered SCK edges (see Section 14.4.3, “Transmission Formats”).

The SPI can be configured to operate as a master or as a slave. When the MSTR bit in SPI Control Register1 is set, master mode is selected, when the MSTR bit is clear, slave mode is selected.

14.4.1 Master Mode

The SPI operates in master mode when the MSTR bit is set. Only a master SPI module can initiate transmissions. A transmission begins by writing to the master SPI Data Register. If the shift register is empty, the byte immediately transfers to the shift register. The byte begins shifting out on the MOSI pin under the control of the serial clock.

- S-clock

  The SPR2, SPR1, and SPR0 baud rate selection bits in conjunction with the SPPR2, SPPR1, and SPPR0 baud rate preselection bits in the SPI Baud Rate register control the baud rate generator and determine the speed of the transmission. The SCK pin is the SPI clock output. Through the SCK pin, the baud rate generator of the master controls the shift register of the slave peripheral.
- MOSI and MISO Pins

  In master mode, the function of the serial data output pin (MOSI) and the serial data input pin (MISO) is determined by the SPC0 and BIDIROE control bits.
- $\overline{SS}$ Pin

  If MODFEN and SSOE bit are set, the $\overline{SS}$ pin is configured as slave select output. The $\overline{SS}$ output becomes low during each transmission and is high when the SPI is in idle state.

  If MODFEN is set and SSOE is cleared, the $\overline{SS}$ pin is configured as input for detecting mode fault error. If the $\overline{SS}$ input becomes low this indicates a mode fault error where another master tries to drive the MOSI and SCK lines. In this case, the SPI immediately switches to slave mode, by clearing the MSTR bit and also disables the slave output buffer MISO (or SISO in bidirectional mode). So the result is that all outputs are disabled and SCK, MOSI and MISO are inputs. If a transmission is in progress when the mode fault occurs, the transmission is aborted and the SPI is forced into idle state.

This mode fault error also sets the mode fault (MODF) flag in the SPI Status Register (SPISR). If the SPI interrupt enable bit (SPIE) is set when the MODF flag gets set, then an SPI interrupt sequence is also requested.

When a write to the SPI Data Register in the master occurs, there is a half SCK-cycle delay. After the delay, SCK is started within the master. The rest of the transfer operation differs slightly, depending on the clock format specified by the SPI clock phase bit, CPHA, in SPI Control Register 1 (see Section 14.4.3, “Transmission Formats”).

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0, BIDIROE with SPC0 set, SPPR2–SPPR0 and SPR2–SPR0 in master mode will abort a transmission in progress and force the SPI into idle state. The remote slave cannot detect this, therefore the master has to ensure that the remote slave is set back to idle state.

14.4.2 Slave Mode

The SPI operates in slave mode when the MSTR bit in SPI Control Register1 is clear.

- SCK Clock

  In slave mode, SCK is the SPI clock input from the master.

- MISO and MOSI Pins

  In slave mode, the function of the serial data output pin (MISO) and serial data input pin (MOSI) is determined by the SPC0 bit and BIDIROE bit in SPI Control Register 2.

- $\overline{SS}$ Pin

  The $\overline{SS}$ pin is the slave select input. Before a data transmission occurs, the $\overline{SS}$ pin of the slave SPI must be low. $\overline{SS}$ must remain low until the transmission is complete. If $\overline{SS}$ goes high, the SPI is forced into idle state.

  The $\overline{SS}$ input also controls the serial data output pin, if $\overline{SS}$ is high (not selected), the serial data output pin is high impedance, and, if $\overline{SS}$ is low the first bit in the SPI Data Register is driven out of the serial data output pin. Also, if the slave is not selected ($\overline{SS}$ is high), then the SCK input is ignored and no internal shifting of the SPI shift register takes place.

Although the SPI is capable of duplex operation, some SPI peripherals are capable of only receiving SPI data in a slave mode. For these simpler devices, there is no serial data out pin.

NOTE

When peripherals with duplex capability are used, take care not to simultaneously enable two receivers whose serial outputs drive the same system slave's serial data output line.

As long as no more than one slave device drives the system slave's serial data output line, it is possible for several slaves to receive the same transmission from a master, although the master would not receive return information from all of the receiving slaves.

If the CPHA bit in SPI Control Register 1 is clear, odd numbered edges on the SCK input cause the data at the serial data input pin to be latched. Even numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

If the CPHA bit is set, even numbered edges on the SCK input cause the data at the serial data input pin to be latched. Odd numbered edges cause the value previously latched from the serial data input pin to shift into the LSB or MSB of the SPI shift register, depending on the LSBFE bit.

When CPHA is set, the first edge is used to get the first data bit onto the serial data output pin. When CPHA is clear and the $\overline{SS}$ input is low (slave selected), the first bit of the SPI data is driven out of the serial data output pin. After the eighth shift, the transfer is considered complete and the received data is transferred into the SPI Data Register. To indicate transfer is complete, the SPIF flag in the SPI Status Register is set.

NOTE

A change of the bits CPOL, CPHA, SSOE, LSBFE, MODFEN, SPC0 and BIDIROE with SPC0 set in slave mode will corrupt a transmission in progress and has to be avoided.

14.4.3 Transmission Formats

During an SPI transmission, data is transmitted (shifted out serially) and received (shifted in serially) simultaneously. The serial clock (SCK) synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows selection of an individual slave SPI device, slave devices that are not selected do not interfere with SPI bus activities. Optionally, on a master SPI device, the slave select line can be used to indicate multiple-master bus contention.

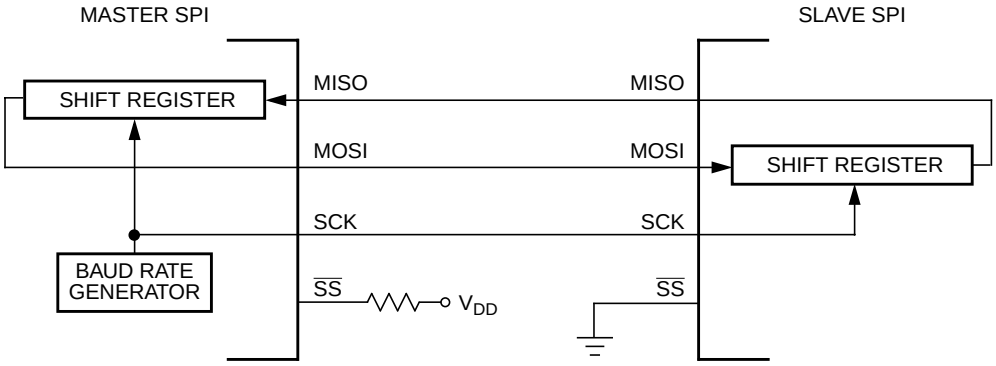


Figure 14-8. Master/Slave Transfer Block Diagram

14.4.3.1 Clock Phase and Polarity Controls

Using two bits in the SPI Control Register1, software selects one of four combinations of serial clock phase and polarity.

The CPOL clock polarity control bit specifies an active high or low clock and has no significant effect on the transmission format.

The CPHA clock phase control bit selects one of two fundamentally different transmission formats.

Clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transmissions to allow a master device to communicate with peripheral slaves having different requirements.

14.4.3.2 CPHA = 0 Transfer Format

The first edge on the SCK line is used to clock the first data bit of the slave into the master and the first data bit of the master into the slave. In some peripherals, the first bit of the slave's data is available at the slave's data out pin as soon as the slave is selected. In this format, the first SCK edge is issued a half cycle after $\overline{SS}$ has become low.

A half SCK cycle later, the second edge appears on the SCK line. When this second edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the shift register, depending on LSBFE bit.

After this second edge, the next bit of the SPI master data is transmitted out of the serial data output pin of the master to the serial input pin on the slave. This process continues for a total of 16 edges on the SCK line, with data being latched on odd numbered edges and shifted on even numbered edges.

Data reception is double buffered. Data is shifted serially into the SPI shift register during the transfer and is transferred to the parallel SPI Data Register after the last bit is shifted in.

After the 16th (last) SCK edge:

- Data that was previously in the master SPI Data Register should now be in the slave data register and the data that was in the slave data register should be in the master.
- The SPIF flag in the SPI Status Register is set indicating that the transfer is complete.

Figure 14-9 is a timing diagram of an SPI transfer where CPHA = 0. SCK waveforms are shown for CPOL = 0 and CPOL = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave and the MOSI signal is the output from the master. The $\overline{SS}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

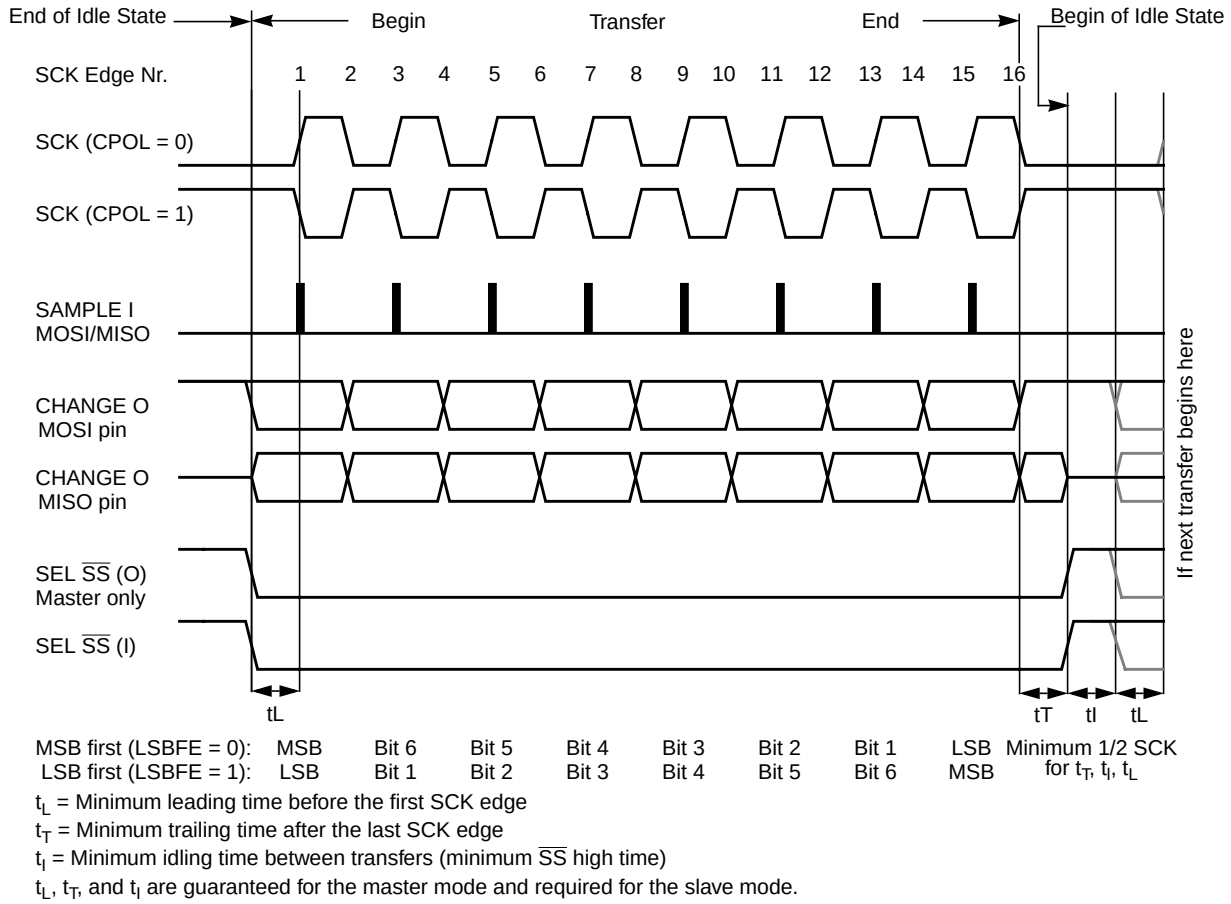


Figure 14-9. SPI Clock Format 0 (CPHA = 0)

In slave mode, if the $\overline{SS}$ line is not deasserted between the successive transmissions then the content of the SPI Data Register is not transmitted, instead the last received byte is transmitted. If the $\overline{SS}$ line is deasserted for at least minimum idle time (half SCK cycle) between successive transmissions then the content of the SPI Data Register is transmitted.

In master mode, with slave select output enabled the $\overline{SS}$ line is always deasserted and reasserted between successive transfers for at least minimum idle time.

14.4.3.3 CPHA = 1 Transfer Format

Some peripherals require the first SCK edge before the first data bit becomes available at the data out pin, the second edge clocks data into the system. In this format, the first SCK edge is issued by setting the CPHA bit at the beginning of the 8-cycle transfer operation.

The first edge of SCK occurs immediately after the half SCK clock cycle synchronization delay. This first edge commands the slave to transfer its first data bit to the serial data input pin of the master.

A half SCK cycle later, the second edge appears on the SCK pin. This is the latching edge for both the master and slave.

When the third edge occurs, the value previously latched from the serial data input pin is shifted into the LSB or MSB of the SPI shift register, depending on LSBFE bit. After this edge, the next bit of the master data is coupled out of the serial data output pin of the master to the serial input pin on the slave.

This process continues for a total of 16 edges on the SCK line with data being latched on even numbered edges and shifting taking place on odd numbered edges.

Data reception is double buffered, data is serially shifted into the SPI shift register during the transfer and is transferred to the parallel SPI Data Register after the last bit is shifted in.

After the 16th SCK edge:

- Data that was previously in the SPI Data Register of the master is now in the data register of the slave, and data that was in the data register of the slave is in the master.
- The SPIF flag bit in SPISR is set indicating that the transfer is complete.

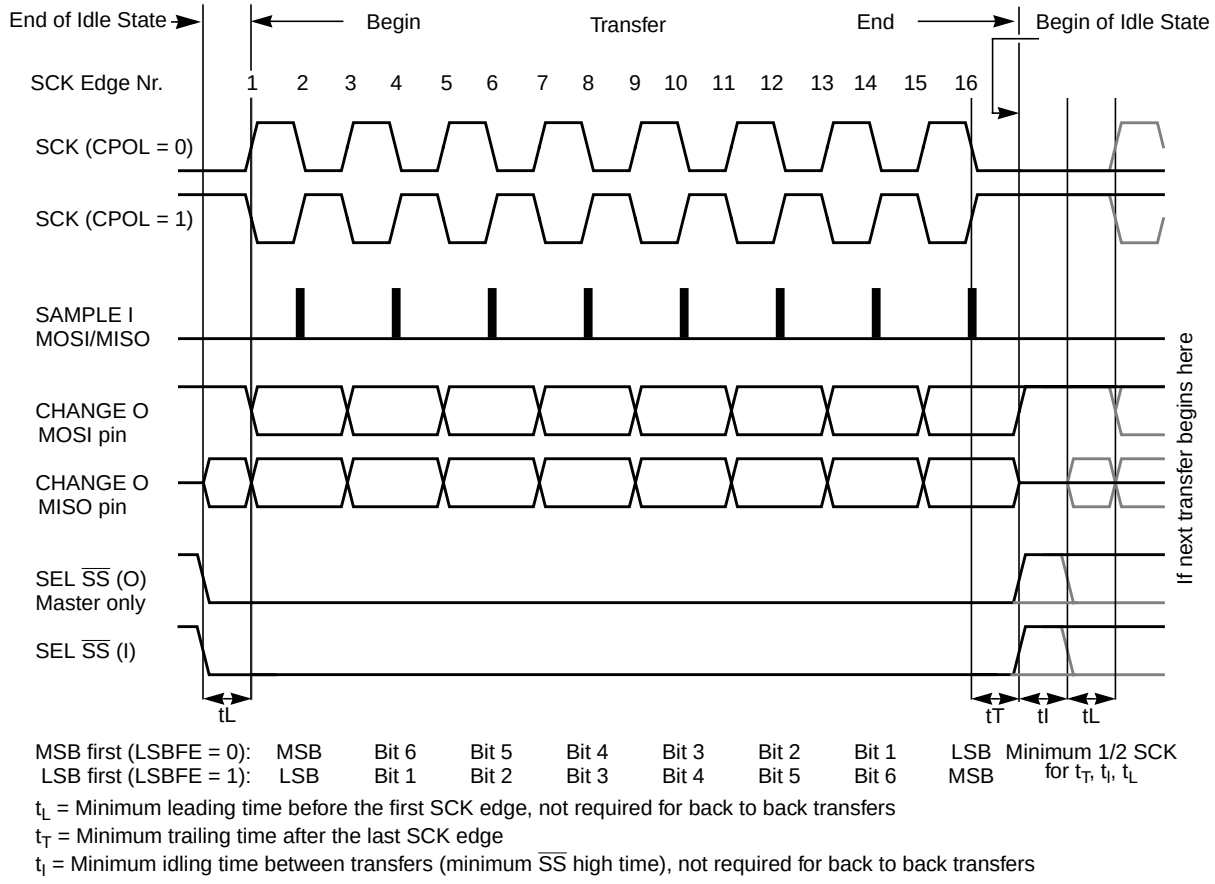
Figure 14-10 shows two clocking variations for CPHA = 1. The diagram may be interpreted as a master or slave timing diagram because the SCK, MISO, and MOSI pins are connected directly between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The $\overline{SS}$ line is the slave select input to the slave. The $\overline{SS}$ pin of the master must be either high or reconfigured as a general-purpose output not affecting the SPI.

The $\overline{SS}$ line can remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave that drive the MISO data line.

- Back-to-back transfers in master mode

In master mode, if a transmission has completed and a new data byte is available in the SPI Data Register, this byte is send out immediately without a trailing and minimum idle time.

The SPI interrupt request flag (SPIF) is common to both the master and slave modes. SPIF gets set one half SCK cycle after the last SCK edge.



t_L = Minimum leading time before the first SCK edge, not required for back to back transfers
t_T = Minimum trailing time after the last SCK edge
t_I = Minimum idling time between transfers (minimum $\overline{SS}$ high time), not required for back to back transfers

Figure 14-10. SPI Clock Format 1 (CPHA = 1)

14.4.4 SPI Baud Rate Generation

Baud rate generation consists of a series of divider stages. Six bits in the SPI Baud Rate register (SPPR2, SPPR1, SPPR0, SPR2, SPR1, and SPR0) determine the divisor to the SPI module clock which results in the SPI baud rate.

The SPI clock rate is determined by the product of the value in the baud rate preselection bits (SPPR2–SPPR0) and the value in the baud rate selection bits (SPR2–SPR0). The module clock divisor equation is shown in Figure 14-11

When all bits are clear (the default condition), the SPI module clock is divided by 2. When the selection bits (SPR2–SPR0) are 001 and the preselection bits (SPPR2–SPPR0) are 000, the module clock divisor becomes 4. When the selection bits are 010, the module clock divisor becomes 8 etc.

When the preselection bits are 001, the divisor determined by the selection bits is multiplied by 2. When the preselection bits are 010, the divisor is multiplied by 3, etc. See Table 14-7 for baud rate calculations for all bit conditions, based on a 25-MHz bus clock. The two sets of selects allows the clock to be divided by a non-power of two to achieve other baud rates such as divide by 6, divide by 10, etc.

The baud rate generator is activated only when the SPI is in the master mode and a serial transfer is taking place. In the other cases, the divider is disabled to decrease I_{DD} current.

$$BaudRateDivisor = (SPPR + 1) \bullet 2^{(SPR + 1)}$$

Figure 14-11. Baud Rate Divisor Equation

14.4.5 Special Features

14.4.5.1 $\overline{SS}$ Output

The $\overline{SS}$ output feature automatically drives the $\overline{SS}$ pin low during transmission to select external devices and drives it high during idle to deselect external devices. When $\overline{SS}$ output is selected, the $\overline{SS}$ output pin is connected to the $\overline{SS}$ input pin of the external device.

The $\overline{SS}$ output is available only in master mode during normal SPI operation by asserting SSOE and MODFEN bit as shown in Table 14-3.

The mode fault feature is disabled while $\overline{SS}$ output is enabled.

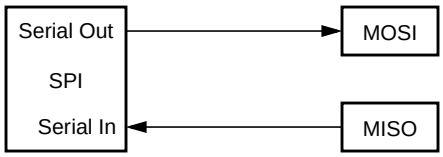
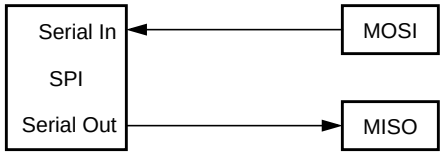
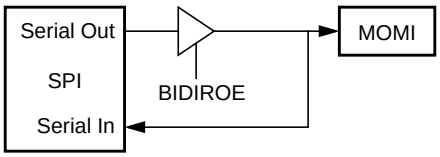
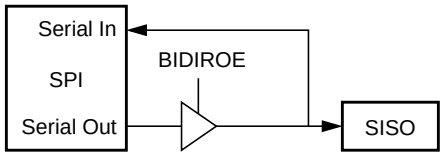
NOTE

Care must be taken when using the $\overline{SS}$ output feature in a multimaster system because the mode fault feature is not available for detecting system errors between masters.

14.4.5.2 Bidirectional Mode (MOSI or MISO)

The bidirectional mode is selected when the SPC0 bit is set in SPI Control Register 2 (see Table 14-9). In this mode, the SPI uses only one serial data pin for the interface with external device(s). The MSTR bit decides which pin to use. The MOSI pin becomes the serial data I/O (MOMI) pin for the master mode, and the MISO pin becomes serial data I/O (SISO) pin for the slave mode. The MISO pin in master mode and MOSI pin in slave mode are not used by the SPI.

Table 14-9. Normal Mode and Bidirectional Mode

When SPE = 1	Master Mode MSTR = 1	Slave Mode MSTR = 0
Normal Mode SPC0 = 0		
Bidirectional Mode SPC0 = 1		

The direction of each serial I/O pin depends on the BIDIROE bit. If the pin is configured as an output, serial data from the shift register is driven out on the pin. The same pin is also the serial input to the shift register.

The SCK is output for the master mode and input for the slave mode.

The $\overline{SS}$ is the input or output for the master mode, and it is always the input for the slave mode.

The bidirectional mode does not affect SCK and $\overline{SS}$ functions.

NOTE

In bidirectional master mode, with mode fault enabled, both data pins MISO and MOSI can be occupied by the SPI, though MOSI is normally used for transmissions in bidirectional mode and MISO is not used by the SPI. If a mode fault occurs, the SPI is automatically switched to slave mode, in this case MISO becomes occupied by the SPI and MOSI is not used. This has to be considered, if the MISO pin is used for other purpose.

14.4.6 Error Conditions

The SPI has one error condition:

- Mode fault error

14.4.6.1 Mode Fault Error

If the $\overline{SS}$ input becomes low while the SPI is configured as a master, it indicates a system error where more than one master may be trying to drive the MOSI and SCK lines simultaneously. This condition is not permitted in normal operation, the MODF bit in the SPI Status Register is set automatically provided the MODFEN bit is set.

In the special case where the SPI is in master mode and MODFEN bit is cleared, the $\overline{SS}$ pin is not used by the SPI. In this special case, the mode fault error function is inhibited and MODF remains cleared. In case the SPI system is configured as a slave, the $\overline{SS}$ pin is a dedicated input pin. Mode fault error doesn't occur in slave mode.

If a mode fault error occurs the SPI is switched to slave mode, with the exception that the slave output buffer is disabled. So SCK, MISO and MOSI pins are forced to be high impedance inputs to avoid any possibility of conflict with another output driver. A transmission in progress is aborted and the SPI is forced into idle state.

If the mode fault error occurs in the bidirectional mode for a SPI system configured in master mode, output enable of the MOMI (MOSI in bidirectional mode) is cleared if it was set. No mode fault error occurs in the bidirectional mode for SPI system configured in slave mode.

The mode fault flag is cleared automatically by a read of the SPI Status Register (with MODF set) followed by a write to SPI Control Register 1. If the mode fault flag is cleared, the SPI becomes a normal master or slave again.

14.4.7 Operation in Run Mode

In run mode with the SPI system enable (SPE) bit in the SPI control register clear, the SPI system is in a low-power, disabled state. SPI registers remain accessible, but clocks to the core of this module are disabled.

14.4.8 Operation in Wait Mode

SPI operation in wait mode depends upon the state of the SPISWAI bit in SPI Control Register 2.

- If SPISWAI is clear, the SPI operates normally when the CPU is in wait mode
- If SPISWAI is set, SPI clock generation ceases and the SPI module enters a power conservation state when the CPU is in wait mode.
  - — If SPISWAI is set and the SPI is configured for master, any transmission and reception in progress stops at wait mode entry. The transmission and reception resumes when the SPI exits wait mode.
  - — If SPISWAI is set and the SPI is configured as a slave, any transmission and reception in progress continues if the SCK continues to be driven from the master. This keeps the slave synchronized to the master and the SCK.

    If the master transmits several bytes while the slave is in wait mode, the slave will continue to send out bytes consistent with the operation mode at the start of wait mode (i.e. If the slave is currently sending its SPIDR to the master, it will continue to send the same byte. Else if the slave is currently sending the last received byte from the master, it will continue to send each previous master byte).

NOTE

Care must be taken when expecting data from a master while the slave is in wait or stop mode. Even though the shift register will continue to operate, the rest of the SPI is shut down (i.e. a SPIF interrupt will **not** be generated until exiting stop or wait mode). Also, the byte from the shift register will not be copied into the SPIDR register until after the slave SPI has exited wait or stop mode. A SPIF flag and SPIDR copy is only generated if wait mode is entered or exited during a tranmission. If the slave enters wait mode in idle mode and exits wait mode in idle mode, neither a SPIF nor a SPIDR copy will occur.

14.4.9 Operation in Stop Mode

Stop mode is dependent on the system. The SPI enters stop mode when the module clock is disabled (held high or low). If the SPI is in master mode and exchanging data when the CPU enters stop mode, the transmission is frozen until the CPU exits stop mode. After stop, data to and from the external SPI is exchanged correctly. In slave mode, the SPI will stay synchronized with the master.

The stop mode is not dependent on the SPISWAI bit.

14.5 Reset

The reset values of registers and signals are described in the Memory Map and Registers section (see Section 14.3, “Memory Map and Register Definition”) which details the registers and their bit-fields.

- If a data transmission occurs in slave mode after reset without a write to SPIDR, it will transmit garbage, or the byte last received from the master before the reset.
- Reading from the SPIDR after reset will always read a byte of zeros.

14.6 Interrupts

The SPI only originates interrupt requests when SPI is enabled (SPE bit in SPICR1 set). The following is a description of how the SPI makes a request and how the MCU should acknowledge that request. The interrupt vector offset and interrupt priority are chip dependent.

The interrupt flags MODF, SPIF and SPTEF are logically ORed to generate an interrupt request.

14.6.1 MODF

MODF occurs when the master detects an error on the $\overline{SS}$ pin. The master SPI must be configured for the MODF feature (see Table 14-3). After MODF is set, the current transfer is aborted and the following bit is changed:

- MSTR = 0, The master bit in SPICR1 resets.

The MODF interrupt is reflected in the status register MODF flag. Clearing the flag will also clear the interrupt. This interrupt will stay active while the MODF flag is set. MODF has an automatic clearing process which is described in Section 14.3.2.4, “SPI Status Register (SPISR).”

14.6.2 SPIF

SPIF occurs when new data has been received and copied to the SPI Data Register. After SPIF is set, it does not clear until it is serviced. SPIF has an automatic clearing process which is described in Section 14.3.2.4, “SPI Status Register (SPISR).” In the event that the SPIF is not serviced before the end of the next transfer (i.e. SPIF remains active throughout another transfer), the latter transfers will be ignored and no new data will be copied into the SPIDR.

14.6.3 SPTEF

SPTEF occurs when the SPI Data Register is ready to accept new data. After SPTEF is set, it does not clear until it is serviced. SPTEF has an automatic clearing process which is described in Section 14.3.2.4, “SPI Status Register (SPISR).”

Chapter 15
Pulse-Width Modulator (PWM8B6CV1)

15.1 Introduction

The pulse width modulation (PWM) definition is based on the HC12 PWM definitions. The PWM8B6C module contains the basic features from the HC11 with some of the enhancements incorporated on the HC12, that is center aligned output mode and four available clock sources. The PWM8B6C module has six channels with independent control of left and center aligned outputs on each channel.

Each of the six PWM channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs

15.1.1 Features

- Six independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches 0) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- Six 8-bit channel or three 16-bit channel PWM resolution
- Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies.
- Programmable clock select logic
- Emergency shutdown

15.1.2 Modes of Operation

There is a software programmable option for low power consumption in wait mode that disables the input clock to the prescaler.

In freeze mode there is a software programmable option to disable the input clock to the prescaler. This is useful for emulation.

15.1.3 Block Diagram

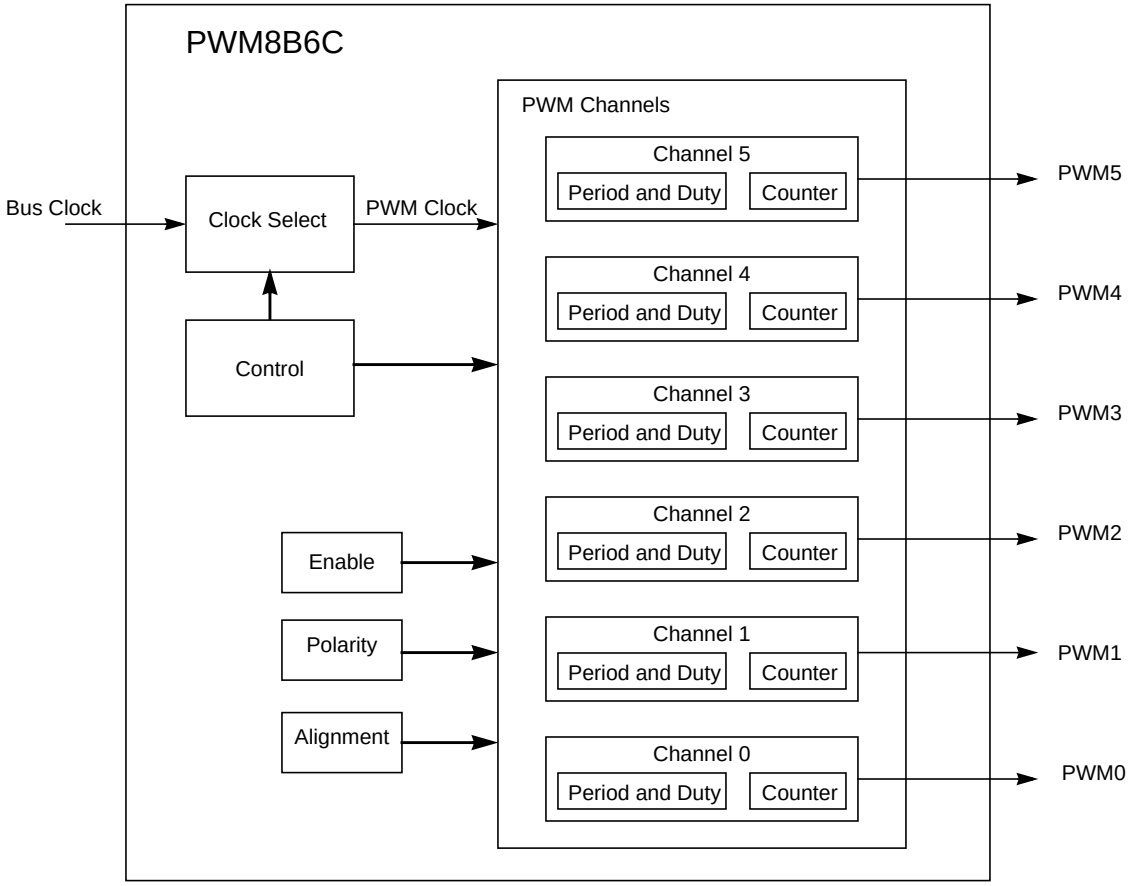


Figure 15-1. PWM8B6C Block Diagram

15.2 External Signal Description

The PWM8B6C module has a total of six external pins.

15.2.1 PWM5 — Pulse Width Modulator Channel 5 Pin

This pin serves as waveform output of PWM channel 5 and as an input for the emergency shutdown feature.

15.2.2 PWM4 — Pulse Width Modulator Channel 4 Pin

This pin serves as waveform output of PWM channel 4.

15.2.3 PWM3 — Pulse Width Modulator Channel 3 Pin

This pin serves as waveform output of PWM channel 3.

15.2.4 PWM2 — Pulse Width Modulator Channel 2 Pin

This pin serves as waveform output of PWM channel 2.

15.2.5 PWM1 — Pulse Width Modulator Channel 1 Pin

This pin serves as waveform output of PWM channel 1.

15.2.6 PWM0 — Pulse Width Modulator Channel 0 Pin

This pin serves as waveform output of PWM channel 0.

15.3 Memory Map and Register Definition

This subsection describes in detail all the registers and register bits in the PWM8B6C module.

The special-purpose registers and register bit functions that would not normally be made available to device end users, such as factory test control registers and reserved registers are clearly identified by means of shading the appropriate portions of address maps and register diagrams. Notes explaining the reasons for restricting access to the registers and functions are also explained in the individual register descriptions.

15.3.1 Module Memory Map

The following paragraphs describe the content of the registers in the PWM8B6C module. The base address of the PWM8B6C module is determined at the MCU level when the MCU is defined. The register decode map is fixed and begins at the first address of the module address offset. Table 15-1 shows the registers associated with the PWM and their relative offset from the base address. The register detail description follows the order in which they appear in the register map.

Reserved bits within a register will always read as 0 and the write will be unimplemented. Unimplemented functions are indicated by shading the bit.

Table 15-1 shows the memory map for the PWM8B6C module.

NOTE

Register address = base address + address offset, where the base address is defined at the MCU level and the address offset is defined at the module level.

Table 15-1. PWM8B6C Memory Map

Address Offset	Register	Access
0x0000	PWM Enable Register (PWME)	R/W
0x0001	PWM Polarity Register (PWMPOL)	R/W
0x0002	PWM Clock Select Register (PWMCLK)	R/W
0x0003	PWM Prescale Clock Select Register (PWMPRCLK)	R/W
0x0004	PWM Center Align Enable Register (PWMCAE)	R/W
0x0005	PWM Control Register (PWMCTL)	R/W
0x0006	PWM Test Register (PWMTST)[1]	R/W
0x0007	PWM Prescale Counter Register (PWMPRSC)[2]	R/W
0x0008	PWM Scale A Register (PWMSCLA)	R/W
0x0009	PWM Scale B Register (PWMSCLB)	R/W
0x000A	PWM Scale A Counter Register (PWMSCNTA)[3]	R/W
0x000B	PWM Scale B Counter Register (PWMSCNTB)[4]	R/W
0x000C	PWM Channel 0 Counter Register (PWMCNT0)	R/W
0x000D	PWM Channel 1 Counter Register (PWMCNT1)	R/W
0x000E	PWM Channel 2 Counter Register (PWMCNT2)	R/W
0x000F	PWM Channel 3 Counter Register (PWMCNT3)	R/W
0x0010	PWM Channel 4 Counter Register (PWMCNT4)	R/W
0x0011	PWM Channel 5 Counter Register (PWMCNT5)	R/W
0x0012	PWM Channel 0 Period Register (PWMPER0)	R/W
0x0013	PWM Channel 1 Period Register (PWMPER1)	R/W
0x0014	PWM Channel 2 Period Register (PWMPER2)	R/W
0x0015	PWM Channel 3 Period Register (PWMPER3)	R/W
0x0016	PWM Channel 4 Period Register (PWMPER4)	R/W
0x0017	PWM Channel 5 Period Register (PWMPER5)	R/W
0x0018	PWM Channel 0 Duty Register (PWMDTY0)	R/W
0x0019	PWM Channel 1 Duty Register (PWMDTY1)	R/W
0x001A	PWM Channel 2 Duty Register (PWMDTY2)	R/W
0x001B	PWM Channel 3 Duty Register (PWMDTY3)	R/W
0x001C	PWM Channel 4 Duty Register (PWMDTY4)	R/W
0x001D	PWM Channel 5 Duty Register (PWMDTY5)	R/W
0x001E	PWM Shutdown Register (PWMSDN)	R/W

1 PWMTST is intended for factory test purposes only.

2 PWMPRSC is intended for factory test purposes only.

3 PWMSCNTA is intended for factory test purposes only.

4 PWMSCNTB is intended for factory test purposes only.

15.3.2 Register Descriptions

The following paragraphs describe in detail all the registers and register bits in the PWM8B6C module.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
PWME	R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
	W								
PWMPOL	R	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
	W								
PWMCLK	R	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
	W								
PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
	W								
PWMCAE	R	0	0	CAE5	CAE4	CAE2	CAE2	CAE1	CAE0
	W								
PWMCTL	R	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
	W								
PWMTST	R	0	0	0	0	0	0	0	0
	W								
PWMPRSC	R	0	0	0	0	0	0	0	0
	W								
PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
PWMSCNTA	R	0	0	0	0	0	0	0	0
	W								
PWMSCNTB	R	0	0	0	0	0	0	0	0
	W								
PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-2. PWM Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
	W	0	0	0	0	0	0	0	0
PWMPER0	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMDTY0	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER1	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER2	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER3	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER4	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMPER5	R W	Bit 7	6	5	4	3	2	1	Bit 0
PWMSDB	R	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
	W			PWMRSTRT					

= Unimplemented or Reserved

Figure 15-2. PWM Register Summary (continued)

15.3.2.1 PWM Enable Register (PWME)

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source.

NOTE

The first PWM cycle after enabling the channel can be irregular.

An exception to this is when channels are concatenated. After concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low-order PWMEx bit. In this case, the high-order bytes PWMEx bits have no effect and their corresponding PWM output lines are disabled.

While in run mode, if all six PWM channels are disabled (PWME5–PWME0 = 0), the prescaler counter shuts off for power savings.

	7	6	5	4	3	2	1	0
R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-3. PWM Enable Register (PWME)

Read: anytime

Write: anytime

Table 15-2. PWME Field Descriptions

Field	Description
5 PWME5	**Pulse Width Channel 5 Enable** 0 Pulse width channel 5 is disabled. 1 Pulse width channel 5 is enabled. The pulse modulated signal becomes available at PWM,output bit 5 when its clock source begins its next cycle.
4 PWME4	**Pulse Width Channel 4 Enable** 0 Pulse width channel 4 is disabled. 1 Pulse width channel 4 is enabled. The pulse modulated signal becomes available at PWM, output bit 4 when its clock source begins its next cycle. If CON45 = 1, then bit has no effect and PWM output line 4 is disabled.
3 PWME3	**Pulse Width Channel 3 Enable** 0 Pulse width channel 3 is disabled. 1 Pulse width channel 3 is enabled. The pulse modulated signal becomes available at PWM, output bit 3 when its clock source begins its next cycle.
2 PWME2	**Pulse Width Channel 2 Enable** 0 Pulse width channel 2 is disabled. 1 Pulse width channel 2 is enabled. The pulse modulated signal becomes available at PWM, output bit 2 when its clock source begins its next cycle. If CON23 = 1, then bit has no effect and PWM output line 2 is disabled.

Table 15-2. PWME Field Descriptions (continued)

Field	Description
1 PWME1	**Pulse Width Channel 1 Enable** 0 Pulse width channel 1 is disabled. 1 Pulse width channel 1 is enabled. The pulse modulated signal becomes available at PWM, output bit 1 when its clock source begins its next cycle.
0 PWME0	**Pulse Width Channel 0 Enable** 0 Pulse width channel 0 is disabled. 1 Pulse width channel 0 is enabled. The pulse modulated signal becomes available at PWM, output bit 0 when its clock source begins its next cycle. If CON01 = 1, then bit has no effect and PWM output line 0 is disabled.

15.3.2.2 PWM Polarity Register (PWMPOL)

The starting polarity of each PWM channel waveform is determined by the associated PPOLx bit in the PWMPOL register. If the polarity bit is 1, the PWM channel output is high at the beginning of the cycle and then goes low when the duty count is reached. Conversely, if the polarity bit is 0 the output starts low and then goes high when the duty count is reached.

	7	6	5	4	3	2	1	0
R	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-4. PWM Polarity Register (PWMPOL)

Read: anytime

Write: anytime

NOTE

PPOLx register bits can be written anytime. If the polarity is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition

Table 15-3. PWMPOL Field Descriptions

Field	Description
5 PPOL5	**Pulse Width Channel 5 Polarity** 0 PWM channel 5 output is low at the beginning of the period, then goes high when the duty count is reached. 1 PWM channel 5 output is high at the beginning of the period, then goes low when the duty count is reached.
4 PPOL4	**Pulse Width Channel 4 Polarity** 0 PWM channel 4 output is low at the beginning of the period, then goes high when the duty count is reached. 1 PWM channel 4 output is high at the beginning of the period, then goes low when the duty count is reached.
3 PPOL3	**Pulse Width Channel 3 Polarity** 0 PWM channel 3 output is low at the beginning of the period, then goes high when the duty count is reached. 1 PWM channel 3 output is high at the beginning of the period, then goes low when the duty count is reached.

Table 15-3. PWMPOL Field Descriptions (continued)

Field	Description
2 PPOL2	**Pulse Width Channel 2 Polarity** 0 PWM channel 2 output is low at the beginning of the period, then goes high when the duty count is reached. 1 PWM channel 2 output is high at the beginning of the period, then goes low when the duty count is reached.
1 PPOL1	**Pulse Width Channel 1 Polarity** 0 PWM channel 1 output is low at the beginning of the period, then goes high when the duty count is reached. 1 PWM channel 1 output is high at the beginning of the period, then goes low when the duty count is reached.
0 PPOL0	**Pulse Width Channel 0 Polarity** 0 PWM channel 0 output is low at the beginning of the period, then goes high when the duty count is reached 1 PWM channel 0 output is high at the beginning of the period, then goes low when the duty count is reached.

15.3.2.3 PWM Clock Select Register (PWMCLK)

Each PWM channel has a choice of two clocks to use as the clock source for that channel as described below.

	7	6	5	4	3	2	1	0
R	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-5. PWM Clock Select Register (PWMCLK)

Read: anytime

Write: anytime

NOTE

Register bits PCLK0 to PCLK5 can be written anytime. If a clock select is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 15-4. PWMCLK Field Descriptions

Field	Description
5 PCLK5	**Pulse Width Channel 5 Clock Select** 0 Clock A is the clock source for PWM channel 5. 1 Clock SA is the clock source for PWM channel 5.
4 PCLK4	**Pulse Width Channel 4 Clock Select** 0 Clock A is the clock source for PWM channel 4. 1 Clock SA is the clock source for PWM channel 4.
3 PCLK3	**Pulse Width Channel 3 Clock Select** 0 Clock B is the clock source for PWM channel 3. 1 Clock SB is the clock source for PWM channel 3.

Table 15-4. PWMCLK Field Descriptions (continued)

Field	Description
2 PCLK2	**Pulse Width Channel 2 Clock Select** 0 Clock B is the clock source for PWM channel 2. 1 Clock SB is the clock source for PWM channel 2.
1 PCLK1	**Pulse Width Channel 1 Clock Select** 0 Clock A is the clock source for PWM channel 1. 1 Clock SA is the clock source for PWM channel 1.
0 PCLK0	**Pulse Width Channel 0 Clock Select** 0 Clock A is the clock source for PWM channel 0. 1 Clock SA is the clock source for PWM channel 0.

15.3.2.4 PWM Prescale Clock Select Register (PWMPRCLK)

This register selects the prescale clock source for clocks A and B independently.

	7	6	5	4	3	2	1	0
R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-6. PWM Prescaler Clock Select Register (PWMPRCLK)

Read: anytime

Write: anytime

NOTE

PCKB2–PCKB0 and PCKA2–PCKA0 register bits can be written anytime. If the clock prescale is changed while a PWM signal is being generated, a truncated or stretched pulse can occur during the transition.

Table 15-5. PWMPRCLK Field Descriptions

Field	Description
6:5 PCKB[2:0]	**Prescaler Select for Clock B** — Clock B is 1 of two clock sources which can be used for channels 2 or 3. These three bits determine the rate of clock B, as shown in Table 15-6**.**
2:0 PCKA[2:0]	**Prescaler Select for Clock A** — Clock A is 1 of two clock sources which can be used for channels 0, 1, 4, or 5. These three bits determine the rate of clock A, as shown in Table 15-7.

Table 15-6. Clock B Prescaler Selects

PCKB2	PCKB1	PCKB0	Value of Clock B
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

Table 15-7. Clock A Prescaler Selects

PCKA2	PCKA1	PCKA0	Value of Clock A
0	0	0	Bus Clock
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

15.3.2.5 PWM Center Align Enable Register (PWMCAE)

The PWMCAE register contains six control bits for the selection of center aligned outputs or left aligned outputs for each PWM channel. If the CAEx bit is set to a 1, the corresponding PWM output will be center aligned. If the CAEx bit is cleared, the corresponding PWM output will be left aligned. Reference Section 15.4.2.5, “Left Aligned Outputs,” and Section 15.4.2.6, “Center Aligned Outputs,” for a more detailed description of the PWM output modes.

	7	6	5	4	3	2	1	0
R	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-7. PWM Center Align Enable Register (PWMCAE)

Read: anytime

Write: anytime

NOTE

Write these bits only when the corresponding channel is disabled.

Table 15-8. PWMCAE Field Descriptions

Field	Description
5 CAE5	**Center Aligned Output Mode on Channel 5** 0 Channel 5 operates in left aligned output mode. 1 Channel 5 operates in center aligned output mode.
4 CAE4	**Center Aligned Output Mode on Channel 4** 0 Channel 4 operates in left aligned output mode. 1 Channel 4 operates in center aligned output mode.
3 CAE3	**Center Aligned Output Mode on Channel 3** 1 Channel 3 operates in left aligned output mode. 1 Channel 3 operates in center aligned output mode.
2 CAE2	**Center Aligned Output Mode on Channel 2** 0 Channel 2 operates in left aligned output mode. 1 Channel 2 operates in center aligned output mode.
1 CAE1	**Center Aligned Output Mode on Channel 1** 0 Channel 1 operates in left aligned output mode. 1 Channel 1 operates in center aligned output mode.
0 CAE0	**Center Aligned Output Mode on Channel 0** 0 Channel 0 operates in left aligned output mode. 1 Channel 0 operates in center aligned output mode.

15.3.2.6 PWM Control Register (PWMCTL)

The PWMCTL register provides for various control of the PWM module.

	7	6	5	4	3	2	1	0
R	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-8. PWM Control Register (PWMCTL)

Read: anytime

Write: anytime

There are three control bits for concatenation, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. When channels 4 and 5 are concatenated, channel 4 registers become the high-order bytes of the double-byte channel. When channels 2 and 3 are concatenated, channel 2 registers become the high-order bytes of the double-byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high-order bytes of the double-byte channel.

Reference Section 15.4.2.7, “PWM 16-Bit Functions,” for a more detailed description of the concatenation PWM function.

NOTE

Change these bits only when both corresponding channels are disabled.

Table 15-9. PWMCTL Field Descriptions

Field	Description
6 CON45	**Concatenate Channels 4 and 5** 0 Channels 4 and 5 are separate 8-bit PWMs. 1 Channels 4 and 5 are concatenated to create one 16-bit PWM channel. Channel 4 becomes the high-order byte and channel 5 becomes the low-order byte. Channel 5 output pin is used as the output for this 16-bit PWM (bit 5 of port PWMP). Channel 5 clock select control bit determines the clock source, channel 5 polarity bit determines the polarity, channel 5 enable bit enables the output and channel 5 center aligned enable bit determines the output mode.
5 CON23	**Concatenate Channels 2 and 3** 0 Channels 2 and 3 are separate 8-bit PWMs. 1 Channels 2 and 3 are concatenated to create one 16-bit PWM channel. Channel 2 becomes the high-order byte and channel 3 becomes the low-order byte. Channel 3 output pin is used as the output for this 16-bit PWM (bit 3 of port PWMP). Channel 3 clock select control bit determines the clock source, channel 3 polarity bit determines the polarity, channel 3 enable bit enables the output and channel 3 center aligned enable bit determines the output mode.
4 CON01	**Concatenate Channels 0 and 1** 0 Channels 0 and 1 are separate 8-bit PWMs. 1 Channels 0 and 1 are concatenated to create one 16-bit PWM channel. Channel 0 becomes the high-order byte and channel 1 becomes the low-order byte. Channel 1 output pin is used as the output for this 16-bit PWM (bit 1 of port PWMP). Channel 1 clock select control bit determines the clock source, channel 1 polarity bit determines the polarity, channel 1 enable bit enables the output and channel 1 center aligned enable bit determines the output mode.
3 PSWAI	**PWM Stops in Wait Mode** — Enabling this bit allows for lower power consumption in wait mode by disabling the input clock to the prescaler. 0 Allow the clock to the prescaler to continue while in wait mode. 1 Stop the input clock to the prescaler whenever the MCU is in wait mode.
2 PFRZ	**PWM Counters Stop in Freeze Mode** — In freeze mode, there is an option to disable the input clock to the prescaler by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode the input clock to the prescaler is disabled. This feature is useful during emulation as it allows the PWM function to be suspended. In this way, the counters of the PWM can be stopped while in freeze mode so that after normal program flow is continued, the counters are re-enabled to simulate real-time operations. Because the registers remain accessible in this mode, to re-enable the prescaler clock, either disable the PFRZ bit or exit freeze mode. 0 Allow PWM to continue while in freeze mode. 1 Disable PWM input clock to the prescaler whenever the part is in freeze mode. This is useful for emulation.

15.3.2.7 Reserved Register (PWMTST)

This register is reserved for factory testing of the PWM module and is not available in normal modes.

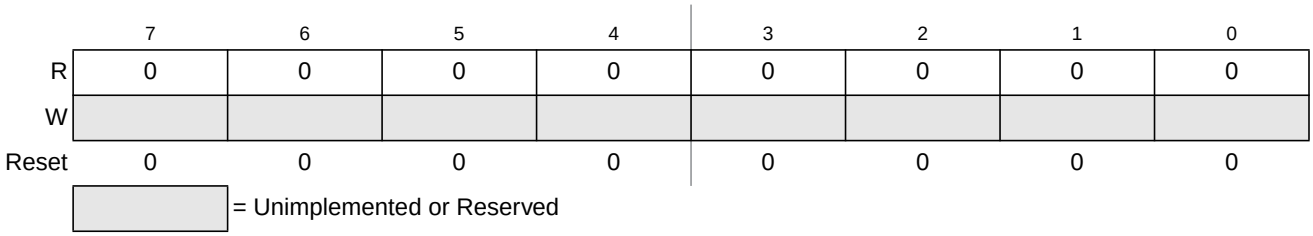


Figure 15-9. Reserved Register (PWMTST)

Read: always read 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter the PWM functionality.

15.3.2.8 Reserved Register (PWMPRSC)

This register is reserved for factory testing of the PWM module and is not available in normal modes.

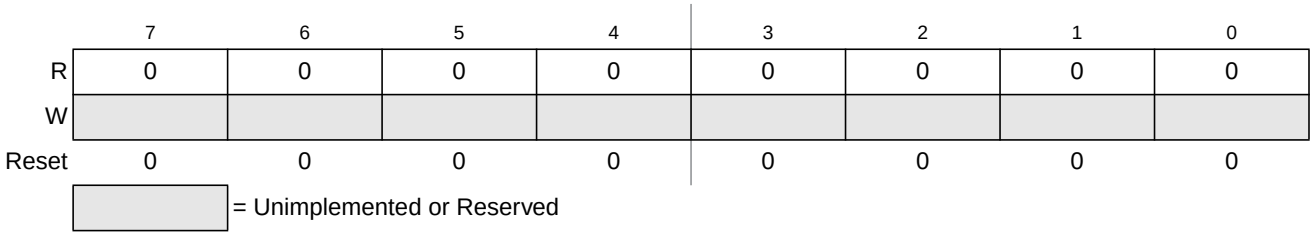


Figure 15-10. Reserved Register (PWMPRSC)

Read: always read 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to this register when in special modes can alter the PWM functionality.

15.3.2.9 PWM Scale A Register (PWMSCLA)

PWMSCLA is the programmable scale value used in scaling clock A to generate clock SA. Clock SA is generated by taking clock A, dividing it by the value in the PWMSCLA register and dividing that by two.

Clock SA = Clock A / (2 * PWMSCLA)

NOTE

When PWMSCLA = 0x0000, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLA).

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-11. PWM Scale A Register (PWMSCLA)

Read: anytime

Write: anytime (causes the scale counter to load the PWMSCLA value)

15.3.2.10 PWM Scale B Register (PWMSCLB)

PWMSCLB is the programmable scale value used in scaling clock B to generate clock SB. Clock SB is generated by taking clock B, dividing it by the value in the PWMSCLB register and dividing that by two.

Clock SB = Clock B / (2 * PWMSCLB)

NOTE

When PWMSCLB = 0x0000, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

Any value written to this register will cause the scale counter to load the new scale value (PWMSCLB).

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-12. PWM Scale B Register (PWMSCLB)

Read: anytime

Write: anytime (causes the scale counter to load the PWMSCLB value).

15.3.2.11 Reserved Registers (PWMSCNTx)

The registers PWMSCNTA and PWMSCNTB are reserved for factory testing of the PWM module and are not available in normal modes.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-13. Reserved Register (PWMSCNTA)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-14. Reserved Register (PWMSCNTB)

Read: always read 0x0000 in normal modes

Write: unimplemented in normal modes

NOTE

Writing to these registers when in special modes can alter the PWM functionality.

15.3.2.12 PWM Channel Counter Registers (PWMCNTx)

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source. The counter can be read at any time without affecting the count or the operation of the PWM channel. In left aligned output mode, the counter counts from 0 to the value in the period register – 1. In center aligned output mode, the counter counts from 0 up to the value in the period register and then back down to 0.

Any value written to the counter causes the counter to reset to 0x0000, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. The counter is also cleared at the end of the effective period (see Section 15.4.2.5, “Left Aligned Outputs,” and Section 15.4.2.6, “Center Aligned Outputs,” for more details). When the channel is disabled (PWMEx = 0), the PWMCNTx register does not count. When a channel becomes enabled (PWMEx = 1), the associated PWM counter starts at the count in the PWMCNTx register. For more detailed information on the operation of the counters, reference Section 15.4.2.4, “PWM Timer Counters.”

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low- or high-order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-15. PWM Channel Counter Registers (PWMCNT0)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-16. PWM Channel Counter Registers (PWMCNT1)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-17. PWM Channel Counter Registers (PWMCNT2)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-18. PWM Channel Counter Registers (PWMCNT3)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-19. PWM Channel Counter Registers (PWMCNT4)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	1	Bit 0
W	0	0	0	0	0	0	0	0
Reset	0	0	0	0	0	0	0	0

Figure 15-20. PWM Channel Counter Registers (PWMCNT5)

Read: anytime

Write: anytime (any value written causes PWM counter to be reset to 0x0000).

15.3.2.13 PWM Channel Period Registers (PWMPERx)

There is a dedicated period register for each channel. The value in this register determines the period of the associated PWM channel.

The period registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active period due to the double buffering scheme.

Reference Section 15.4.2.3, “PWM Period and Duty,” for more information.

To calculate the output period, take the selected clock source period for the channel of interest (A, B, SA, or SB) and multiply it by the value in the period register for that channel:

- Left aligned output (CAEx = 0)
- PWMx period = channel clock period * PWMPERx center aligned output (CAEx = 1)
- PWMx period = channel clock period * (2 * PWMPERx)

For boundary case programming values, please refer to Section 15.4.2.8, “PWM Boundary Cases.”

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-21. PWM Channel Period Registers (PWMPER0)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-22. PWM Channel Period Registers (PWMPER1)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-23. PWM Channel Period Registers (PWMPER2)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-24. PWM Channel Period Registers (PWMPER3)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-25. PWM Channel Period Registers (PWMPER4)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 15-26. PWM Channel Period Registers (PWMPER5)

Read: anytime

Write: anytime

15.3.2.14 PWM Channel Duty Registers (PWMDTYx)

There is a dedicated duty register for each channel. The value in this register determines the duty of the associated PWM channel. The duty value is compared to the counter and if it is equal to the counter value a match occurs and the output changes state.

The duty registers for each channel are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old duty waveform or the new duty waveform, not some variation in between. If the channel is not enabled, then writes to the duty register will go directly to the latches as well as the buffer.

NOTE

Reads of this register return the most recent value written. Reads do not necessarily return the value of the currently active duty due to the double buffering scheme.

Reference Section 15.4.2.3, “PWM Period and Duty,” for more information.

NOTE

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time. If the polarity bit is 1, the output starts high and then goes low when the duty count is reached, so the duty registers contain a count of the high time. If the polarity bit is 0, the output starts low and then goes high when the duty count is reached, so the duty registers contain a count of the low time.

To calculate the output duty cycle (high time as a % of period) for a particular channel:

- Polarity = 0 (PPOLx = 0)
  Duty cycle = [(PWMPERx PWMDTYx)/PWMPERx] * 100%
- Polarity = 1 (PPOLx = 1)
  Duty cycle = [PWMDTYx / PWMPERx] * 100%
- For boundary case programming values, please refer to Section 15.4.2.8, “PWM Boundary Cases.”

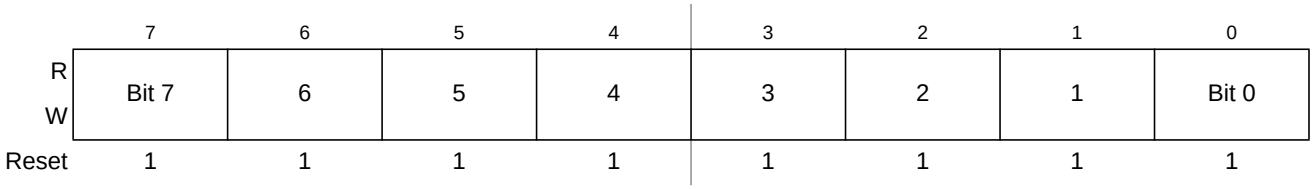


Figure 15-27. PWM Channel Duty Registers (PWMDTY0)

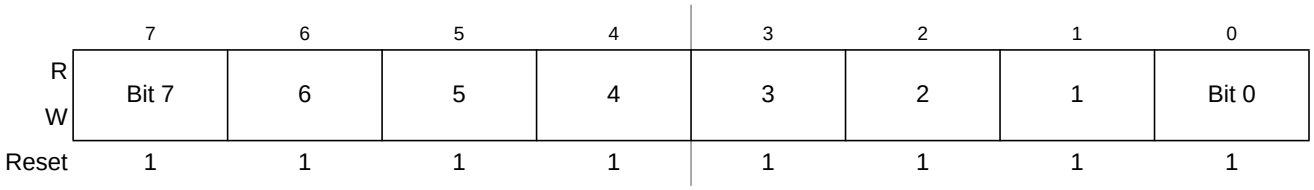


Figure 15-28. PWM Channel Duty Registers (PWMDTY1)

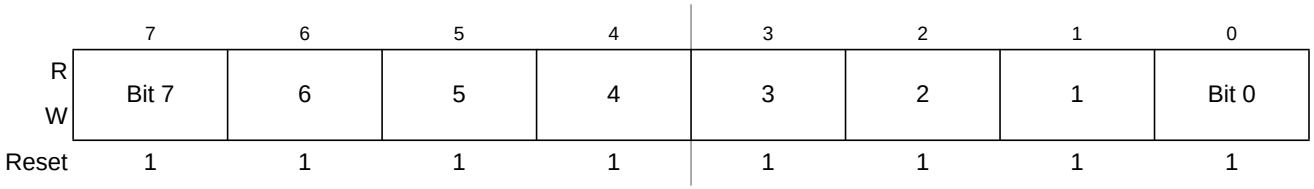


Figure 15-29. PWM Channel Duty Registers (PWMDTY2)

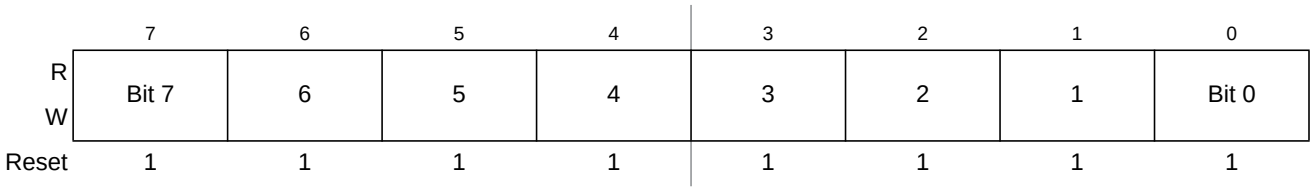


Figure 15-30. PWM Channel Duty Registers (PWMDTY3)

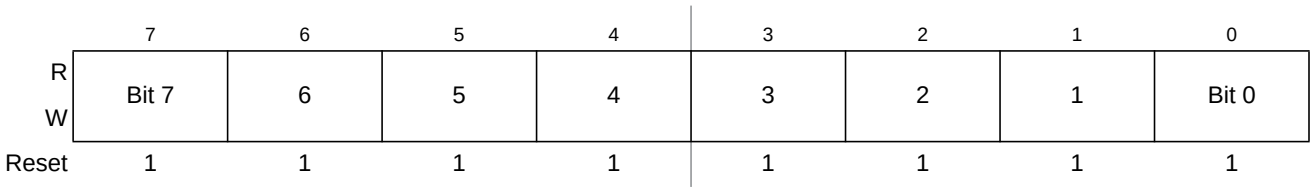


Figure 15-31. PWM Channel Duty Registers (PWMDTY4)

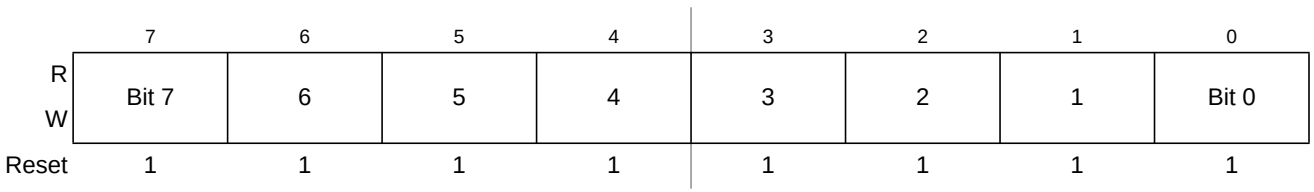


Figure 15-32. PWM Channel Duty Registers (PWMDTY5)

Read: anytime

Write: anytime

15.3.2.15 PWM Shutdown Register (PWMSDN)

The PWMSDN register provides for the shutdown functionality of the PWM module in the emergency cases.

	7	6	5	4	3	2	1	0
R	PWMIF	PWMIE	0	PWMLVL	0	PWM5IN	PWM5INL	PWM5ENA
W			PWMRSTRT					
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 15-33. PWM Shutdown Register (PWMSDN)

Read: anytime

Write: anytime

Table 15-10. PWMSDN Field Descriptions

Field	Description
7 PWMIF	**PWM Interrupt Flag** — Any change from passive to asserted (active) state or from active to passive state will be flagged by setting the PWMIF flag = 1. The flag is cleared by writing a logic 1 to it. Writing a 0 has no effect. 0 No change on PWM5IN input. 1 Change on PWM5IN input
6 PWMIE	**PWM Interrupt Enable** — If interrupt is enabled an interrupt to the CPU is asserted. 0 PWM interrupt is disabled. 1 PWM interrupt is enabled.
5 PWMRSTRT	**PWM Restart** — The PWM can only be restarted if the PWM channel input 5 is deasserted. After writing a logic 1 to the PWMRSTRT bit (trigger event) the PWM channels start running after the corresponding counter passes next “counter = 0” phase. Also, if the PWM5ENA bit is reset to 0, the PWM do not start before the counter passes 0x0000. The bit is always read as 0.
4 PWMLVL	**PWM Shutdown Output Level** — If active level as defined by the PWM5IN input, gets asserted all enabled PWM channels are immediately driven to the level defined by PWMLVL. 0 PWM outputs are forced to 0 1 PWM outputs are forced to 1.
2 PWM5IN	**PWM Channel 5 Input Status** — This reflects the current status of the PWM5 pin.
1 PWM5INL	**PWM Shutdown Active Input Level for Channel 5** — If the emergency shutdown feature is enabled (PWM5ENA = 1), this bit determines the active level of the PWM5 channel. 0 Active level is low 1 Active level is high
0 PWM5ENA	**PWM Emergency Shutdown Enable** — If this bit is logic 1 the pin associated with channel 5 is forced to input and the emergency shutdown feature is enabled. All the other bits in this register are meaningful only if PWM5ENA = 1. 0 PWM emergency feature disabled. 1 PWM emergency feature is enabled.

15.4 Functional Description

15.4.1 PWM Clock Select

There are four available clocks called clock A, clock B, clock SA (scaled A), and clock SB (scaled B). These four clocks are based on the bus clock**.**

Clock A and B can be software selected to be 1, 1/2, 1/4, 1/8,..., 1/64, 1/128 times the bus clock. Clock SA uses clock A as an input and divides it further with a reloadable counter. Similarly, clock SB uses clock B as an input and divides it further with a reloadable counter. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8, ..., or 512 in increments of divide by 2. Similar rates are available for clock SB. Each PWM channel has the capability of selecting one of two clocks, either the pre-scaled clock (clock A or B) or the scaled clock (clock SA or SB).

The block diagram in Figure 15-34 shows the four different clocks and how the scaled clocks are created.

15.4.1.1 Prescale

The input clock to the PWM prescaler is the bus clock. It can be disabled whenever the part is in freeze mode by setting the PFRZ bit in the PWMCTL register. If this bit is set, whenever the MCU is in freeze mode the input clock to the prescaler is disabled. This is useful for emulation in order to freeze the PWM. The input clock can also be disabled when all six PWM channels are disabled (PWME5–PWME0 = 0) This is useful for reducing power by disabling the prescale counter.

Clock A and clock B are scaled values of the input clock. The value is software selectable for both clock A and clock B and has options of 1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, or 1/128 times the bus clock. The value selected for clock A is determined by the PCKA2, PCKA1, and PCKA0 bits in the PWMPRCLK register. The value selected for clock B is determined by the PCKB2, PCKB1, and PCKB0 bits also in the PWMPRCLK register.

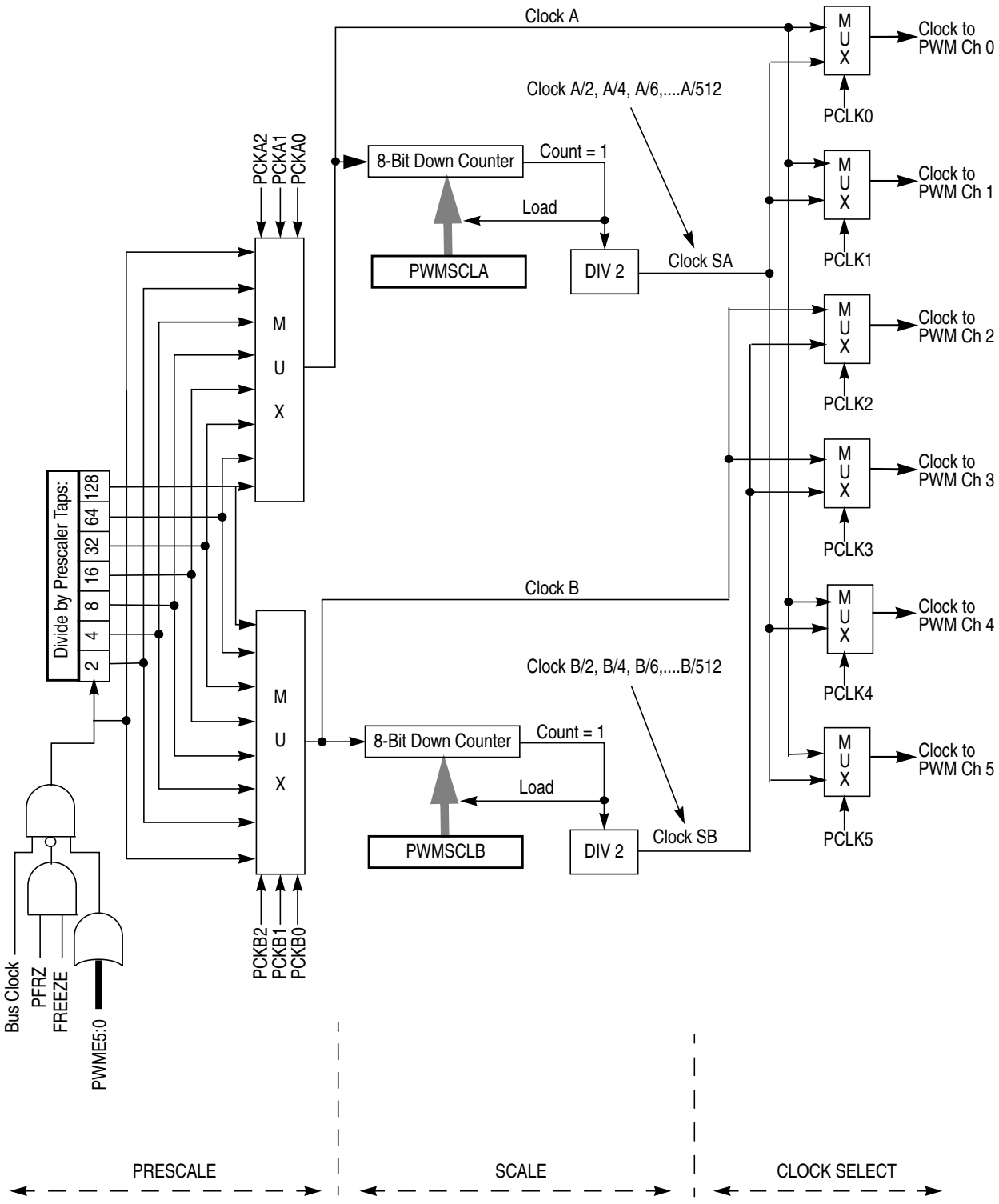


Figure 15-34. PWM Clock Select Block Diagram

15.4.1.2 Clock Scale

The scaled A clock uses clock A as an input and divides it further with a user programmable value and then divides this by 2. The scaled B clock uses clock B as an input and divides it further with a user programmable value and then divides this by 2. The rates available for clock SA are software selectable to be clock A divided by 2, 4, 6, 8, ..., or 512 in increments of divide by 2. Similar rates are available for clock SB.

Clock A is used as an input to an 8-bit down counter. This down counter loads a user programmable scale value from the scale register (PWMSCLA). When the down counter reaches 1, two things happen; a pulse is output and the 8-bit counter is re-loaded. The output signal from this circuit is further divided by two.

This gives a greater range with only a slight reduction in granularity. Clock SA equals clock A divided by two times the value in the PWMSCLA register.

NOTE

Clock SA = Clock A / (2 * PWMSCLA)

When PWMSCLA = 0x0000, PWMSCLA value is considered a full scale value of 256. Clock A is thus divided by 512.

Similarly, clock B is used as an input to an 8-bit down counter followed by a divide by two producing clock SB. Thus, clock SB equals clock B divided by two times the value in the PWMSCLB register.

NOTE

Clock SB = Clock B / (2 * PWMSCLB)

When PWMSCLB = 0x0000, PWMSCLB value is considered a full scale value of 256. Clock B is thus divided by 512.

As an example, consider the case in which the user writes 0x00FF into the PWMSCLA register. Clock A for this case will be bus clock divided by 4. A pulse will occur at a rate of once every 255 x 4 bus cycles. Passing this through the divide by two circuit produces a clock signal at a bus clock divided by 2040 rate. Similarly, a value of 0x0001 in the PWMSCLA register when clock A is bus clock divided by 4 will produce a bus clock divided by 8 rate.

Writing to PWMSCLA or PWMSCLB causes the associated 8-bit down counter to be re-loaded. Otherwise, when changing rates the counter would have to count down to 0x0001 before counting at the proper rate. Forcing the associated counter to re-load the scale register value every time PWMSCLA or PWMSCLB is written prevents this.

NOTE

Writing to the scale registers while channels are operating can cause irregularities in the PWM outputs.

15.4.1.3 Clock Select

Each PWM channel has the capability of selecting one of two clocks. For channels 0, 1, 4, and 5 the clock choices are clock A or clock SA. For channels 2 and 3 the choices are clock B or clock SB. The clock selection is done with the PCLKx control bits in the PWMCLK register.

NOTE

Changing clock control bits while channels are operating can cause irregularities in the PWM outputs.

15.4.2 PWM Channel Timers

The main part of the PWM module are the actual timers. Each of the timer channels has a counter, a period register and a duty register (each are 8 bit). The waveform output period is controlled by a match between the period register and the value in the counter. The duty is controlled by a match between the duty register and the counter value and causes the state of the output to change during the period. The starting polarity of the output is also selectable on a per channel basis. Figure 15-35 shows a block diagram for PWM timer.

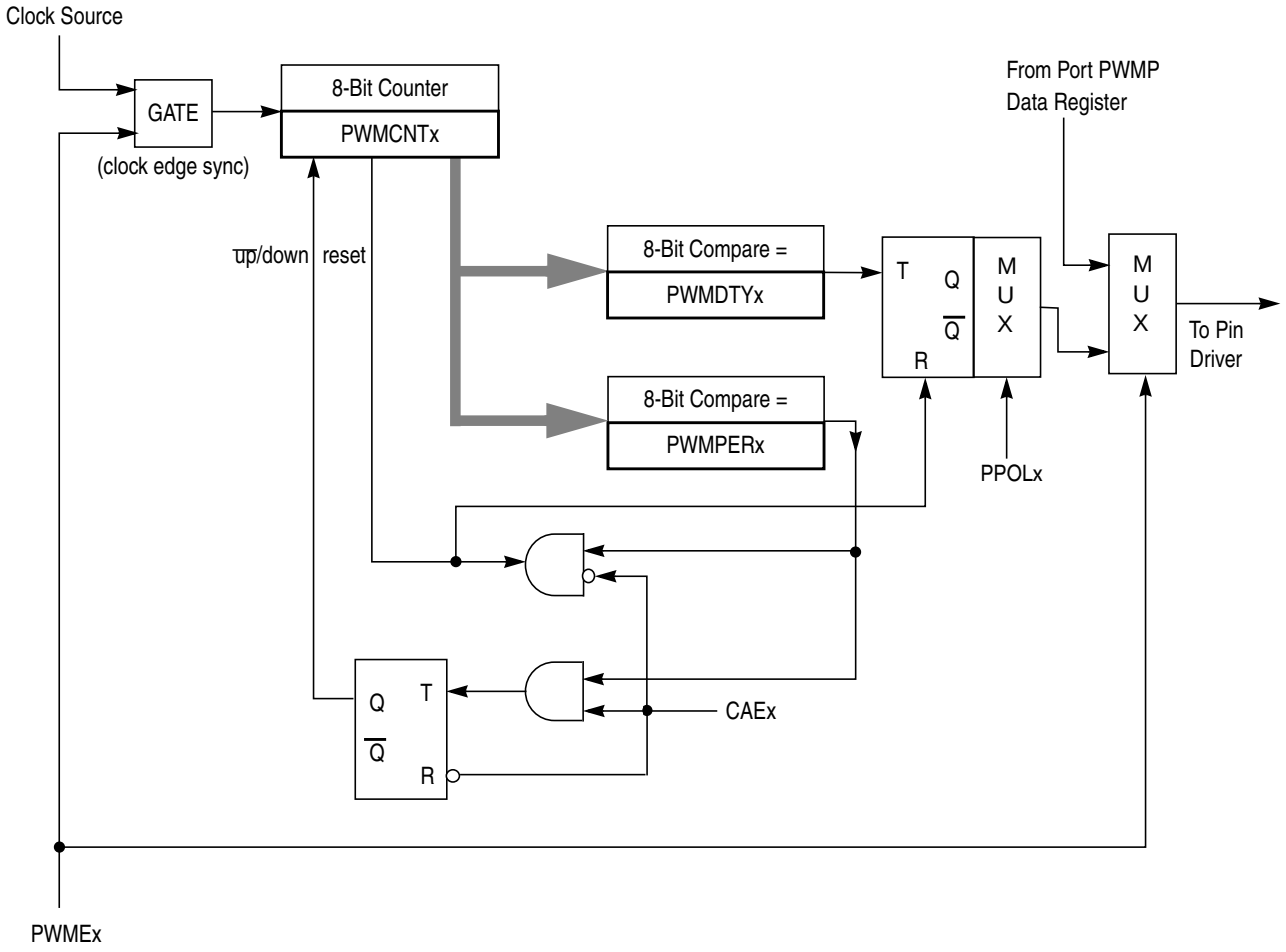


Figure 15-35. PWM Timer Channel Block Diagram

15.4.2.1 PWM Enable

Each PWM channel has an enable bit (PWMEx) to start its waveform output. When any of the PWMEx bits are set (PWMEx = 1), the associated PWM output signal is enabled immediately. However, the actual PWM waveform is not available on the associated PWM output until its clock source begins its next cycle due to the synchronization of PWMEx and the clock source. An exception to this is when channels are concatenated. Refer to Section 15.4.2.7, "PWM 16-Bit Functions," for more detail.

NOTE

The first PWM cycle after enabling the channel can be irregular.

On the front end of the PWM timer, the clock is enabled to the PWM circuit by the PWMEx bit being high. There is an edge-synchronizing circuit to guarantee that the clock will only be enabled or disabled at an edge. When the channel is disabled (PWMEx = 0), the counter for the channel does not count.

15.4.2.2 PWM Polarity

Each channel has a polarity bit to allow starting a waveform cycle with a high or low signal. This is shown on the block diagram as a mux select of either the Q output or the $\overline{Q}$ output of the PWM output flip-flop. When one of the bits in the PWMPOL register is set, the associated PWM channel output is high at the beginning of the waveform, then goes low when the duty count is reached. Conversely, if the polarity bit is 0, the output starts low and then goes high when the duty count is reached.

15.4.2.3 PWM Period and Duty

Dedicated period and duty registers exist for each channel and are double buffered so that if they change while the channel is enabled, the change will NOT take effect until one of the following occurs:

- The effective period ends
- The counter is written (counter resets to 0x0000)
- The channel is disabled

In this way, the output of the PWM will always be either the old waveform or the new waveform, not some variation in between. If the channel is not enabled, then writes to the period and duty registers will go directly to the latches as well as the buffer.

A change in duty or period can be forced into effect "immediately" by writing the new value to the duty and/or period registers and then writing to the counter. This forces the counter to reset and the new duty and/or period values to be latched. In addition, because the counter is readable it is possible to know where the count is with respect to the duty value and software can be used to make adjustments.

NOTE

When forcing a new period or duty into effect immediately, an irregular PWM cycle can occur.

Depending on the polarity bit, the duty registers will contain the count of either the high time or the low time.

15.4.2.4 PWM Timer Counters

Each channel has a dedicated 8-bit up/down counter which runs at the rate of the selected clock source (reference Figure 15-34 for the available clock sources and rates). The counter compares to two registers, a duty register and a period register as shown in Figure 15-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register behaves differently depending on what output mode is selected as shown in Figure 15-35 and described in Section 15.4.2.5, “Left Aligned Outputs,” and Section 15.4.2.6, “Center Aligned Outputs.”

Each channel counter can be read at anytime without affecting the count or the operation of the PWM channel.

Any value written to the counter causes the counter to reset to 0x0000, the counter direction to be set to up, the immediate load of both duty and period registers with values from the buffers, and the output to change according to the polarity bit. When the channel is disabled (PWMEx = 0), the counter stops. When a channel becomes enabled (PWMEx = 1), the associated PWM counter continues from the count in the PWMCNTx register. This allows the waveform to resume when the channel is re-enabled. When the channel is disabled, writing 0 to the period register will cause the counter to reset on the next selected clock.

NOTE

If the user wants to start a new “clean” PWM waveform without any “history” from the old waveform, the user must write to channel counter (PWMCNTx) prior to enabling the PWM channel (PWMEx = 1).

Generally, writes to the counter are done prior to enabling a channel to start from a known state. However, writing a counter can also be done while the PWM channel is enabled (counting). The effect is similar to writing the counter when the channel is disabled except that the new period is started immediately with the output set according to the polarity bit.

NOTE

Writing to the counter while the channel is enabled can cause an irregular PWM cycle to occur.

The counter is cleared at the end of the effective period (see Section 15.4.2.5, “Left Aligned Outputs,” and Section 15.4.2.6, “Center Aligned Outputs,” for more details).

Table 15-11. PWM Timer Counter Conditions

Counter Clears (0x0000)	Counter Counts	Counter Stops
When PWMCNTx register written to any value	When PWM channel is enabled (PWMEx = 1). Counts from last value in PWMCNTx.	When PWM channel is disabled (PWMEx = 0)
Effective period ends		

15.4.2.5 Left Aligned Outputs

The PWM timer provides the choice of two types of outputs, left aligned or center aligned outputs. They are selected with the CAEx bits in the PWMCAE register. If the CAEx bit is cleared (CAEx = 0), the corresponding PWM output will be left aligned.

In left aligned output mode, the 8-bit counter is configured as an up counter only. It compares to two registers, a duty register and a period register as shown in the block diagram in Figure 15-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register resets the counter and the output flip-flop as shown in Figure 15-35 as well as performing a load from the double buffer period and duty register to the associated registers as described in Section 15.4.2.3, “PWM Period and Duty.” The counter counts from 0 to the value in the period register – 1.

NOTE

Changing the PWM output mode from left aligned output to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

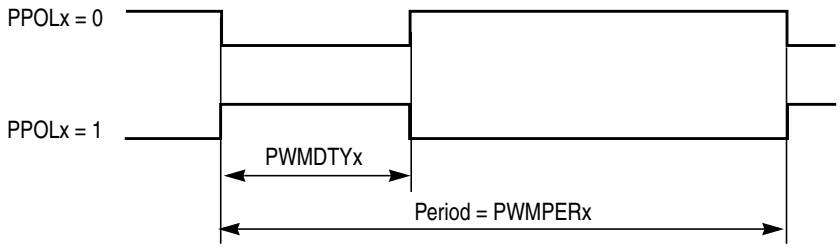


Figure 15-36. PWM Left Aligned Output Waveform

To calculate the output frequency in left aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by the value in the period register for that channel.

- PWMx frequency = clock (A, B, SA, or SB) / PWMPERx
- PWMx duty cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)
    Duty cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)
    Duty cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a left aligned output, consider the following case:

Clock source = bus clock, where bus clock = 10 MHz (100 ns period)
PPOLx = 0
PWMPERx = 4
PWMDTYx = 1
PWMx frequency = 10 MHz/4 = 2.5 MHz
PWMx period = 400 ns
PWMx duty cycle = 3/4 *100% = 75%

Shown below is the output waveform generated.

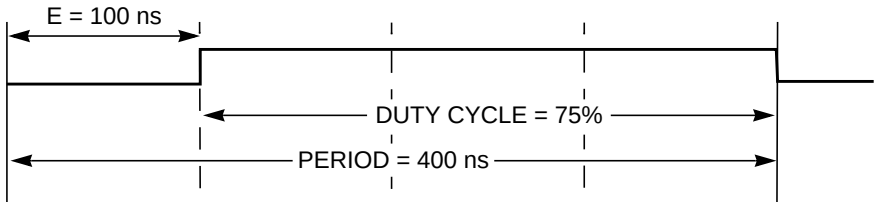


Figure 15-37. PWM Left Aligned Output Example Waveform

15.4.2.6 Center Aligned Outputs

For center aligned output mode selection, set the CAEx bit (CAEx = 1) in the PWMCAE register and the corresponding PWM output will be center aligned.

The 8-bit counter operates as an up/down counter in this mode and is set to up whenever the counter is equal to 0x0000. The counter compares to two registers, a duty register and a period register as shown in the block diagram in Figure 15-35. When the PWM counter matches the duty register the output flip-flop changes state causing the PWM waveform to also change state. A match between the PWM counter and the period register changes the counter direction from an up-count to a down-count. When the PWM counter decrements and matches the duty register again, the output flip-flop changes state causing the PWM output to also change state. When the PWM counter decrements and reaches 0, the counter direction changes from a down-count back to an up-count and a load from the double buffer period and duty registers to the associated registers is performed as described in Section 15.4.2.3, “PWM Period and Duty.” The counter counts from 0 up to the value in the period register and then back down to 0. Thus the effective period is PWMPERx*2.

NOTE

Changing the PWM output mode from left aligned output to center aligned output (or vice versa) while channels are operating can cause irregularities in the PWM output. It is recommended to program the output mode before enabling the PWM channel.

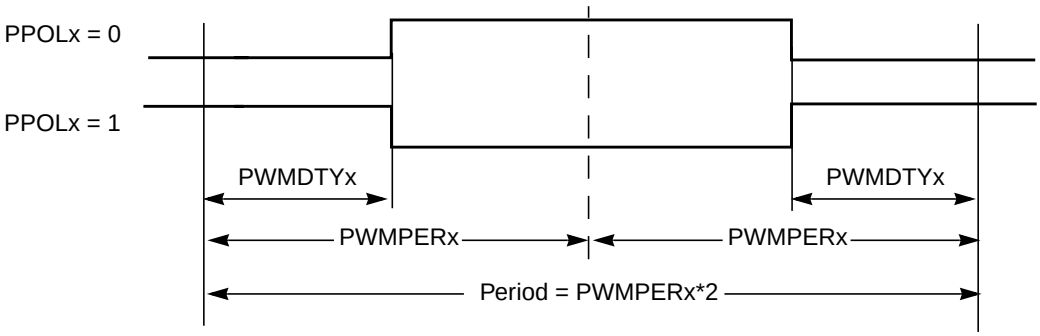


Figure 15-38. PWM Center Aligned Output Waveform

To calculate the output frequency in center aligned output mode for a particular channel, take the selected clock source frequency for the channel (A, B, SA, or SB) and divide it by twice the value in the period register for that channel.

- PWMx frequency = clock (A, B, SA, or SB) / (2*PWMPERx)
- PWMx duty cycle (high time as a% of period):
  - Polarity = 0 (PPOLx = 0)
    Duty cycle = [(PWMPERx-PWMDTYx)/PWMPERx] * 100%
  - Polarity = 1 (PPOLx = 1)
    Duty cycle = [PWMDTYx / PWMPERx] * 100%

As an example of a center aligned output, consider the following case:

Clock source = bus clock, where bus clock = 10 MHz (100 ns period)

PPOLx = 0

PWMPERx = 4

PWMDTYx = 1

PWMx frequency = 10 MHz/8 = 1.25 MHz

PWMx period = 800 ns

PWMx duty cycle = 3/4 *100% = 75%

Shown below is the output waveform generated.

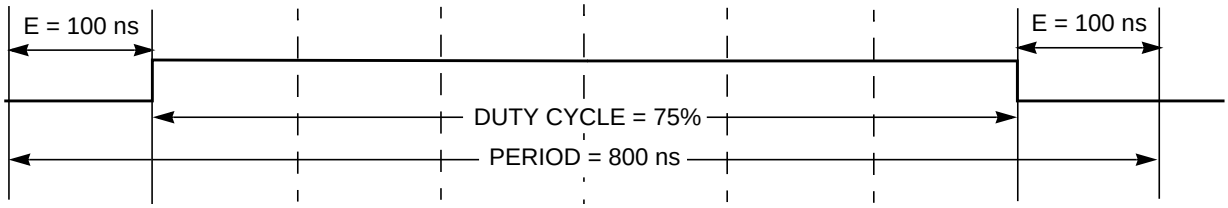


Figure 15-39. PWM Center Aligned Output Example Waveform

15.4.2.7 PWM 16-Bit Functions

The PWM timer also has the option of generating 6-channels of 8-bits or 3-channels of 16-bits for greater PWM resolution}. This 16-bit channel option is achieved through the concatenation of two 8-bit channels.

The PWMCTL register contains three control bits, each of which is used to concatenate a pair of PWM channels into one 16-bit channel. Channels 4 and 5 are concatenated with the CON45 bit, channels 2 and 3 are concatenated with the CON23 bit, and channels 0 and 1 are concatenated with the CON01 bit.

NOTE

Change these bits only when both corresponding channels are disabled.

When channels 4 and 5 are concatenated, channel 4 registers become the high-order bytes of the double byte channel as shown in Figure 15-40. Similarly, when channels 2 and 3 are concatenated, channel 2 registers become the high-order bytes of the double byte channel. When channels 0 and 1 are concatenated, channel 0 registers become the high-order bytes of the double byte channel.

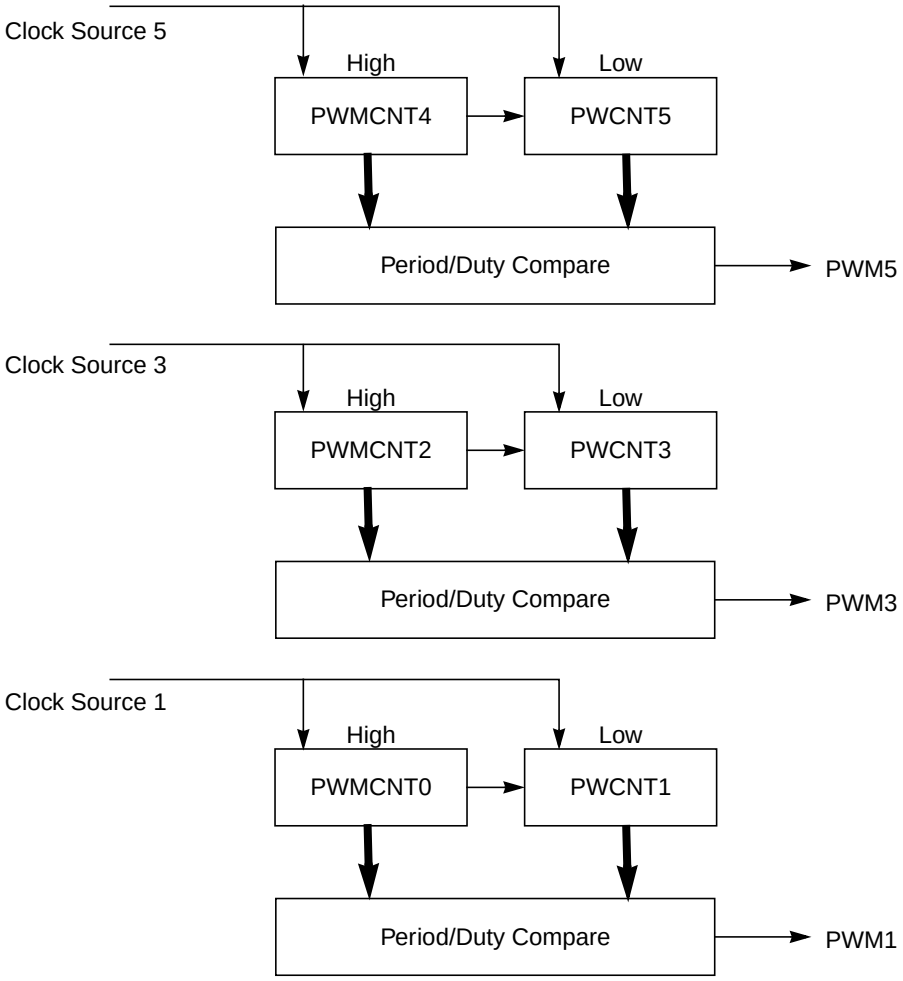


Figure 15-40. PWM 16-Bit Mode

When using the 16-bit concatenated mode, the clock source is determined by the low-order 8-bit channel clock select control bits. That is channel 5 when channels 4 and 5 are concatenated, channel 3 when channels 2 and 3 are concatenated, and channel 1 when channels 0 and 1 are concatenated. The resulting PWM is output to the pins of the corresponding low-order 8-bit channel as also shown in Figure 15-40. The polarity of the resulting PWM output is controlled by the PPOLx bit of the corresponding low-order 8-bit channel as well.

After concatenated mode is enabled (CONxx bits set in PWMCTL register), enabling/disabling the corresponding 16-bit PWM channel is controlled by the low-order PWMEx bit. In this case, the high-order bytes PWMEx bits have no effect and their corresponding PWM output is disabled.

In concatenated mode, writes to the 16-bit counter by using a 16-bit access or writes to either the low or high-order byte of the counter will reset the 16-bit counter. Reads of the 16-bit counter must be made by 16-bit access to maintain data coherency.

Either left aligned or center aligned output mode can be used in concatenated mode and is controlled by the low-order CAEx bit. The high-order CAEx bit has no effect.

Table 15-12 is used to summarize which channels are used to set the various control bits when in 16-bit mode.

Table 15-12. 16-bit Concatenation Mode Summary

CONxx	PWMEx	PPOLx	PCLKx	CAEx	PWMx Output
CON45	PWME5	PPOL5	PCLK5	CAE5	PWM5
CON23	PWME3	PPOL3	PCLK3	CAE3	PWM3
CON01	PWME1	PPOL1	PCLK1	CAE1	PWM1

15.4.2.8 PWM Boundary Cases

Table 15-13 summarizes the boundary conditions for the PWM regardless of the output mode (left aligned or center aligned) and 8-bit (normal) or 16-bit (concatenation):

Table 15-13. PWM Boundary Cases

PWMDTYx	PWMPERx	PPOLx	PWMx Output
0x0000 (indicates no duty)	>0x0000	1	Always Low
0x0000 (indicates no duty)	>0x0000	0	Always High
XX	0x0000[1] (indicates no period)	1	Always High
XX	0x0000[1] (indicates no period)	0	Always Low
>= PWMPERx	XX	1	Always High
>= PWMPERx	XX	0	Always Low

[1] Counter = 0x0000 and does not count.

15.5 Resets

The reset state of each individual bit is listed within the register description section (see Section 15.3, “Memory Map and Register Definition,” which details the registers and their bit-fields. All special functions or modes which are initialized during or just following reset are described within this section.

- The 8-bit up/down counter is configured as an up counter out of reset.
- All the channels are disabled and all the counters don’t count.

15.6 Interrupts

The PWM8B6C module has only one interrupt which is generated at the time of emergency shutdown, if the corresponding enable bit (PWMIE) is set. This bit is the enable for the interrupt. The interrupt flag PWMIF is set whenever the input level of the PWM5 channel changes while PWM5ENA=1 or when PWMENA is being asserted while the level at PWM5 is active.

A description of the registers involved and affected due to this interrupt is explained in Section 15.3.2.15, “PWM Shutdown Register (PWMSDN).”

Chapter 16
Timer Module (TIM16B8CV1)

16.1 Introduction

The basic timer consists of a 16-bit, software-programmable counter driven by a seven-stage programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

This timer contains 8 complete input capture/output compare channels and one pulse accumulator. The input capture function is used to detect a selected transition edge and record the time. The output compare function is used for generating output signals or for timer software delays. The 16-bit pulse accumulator is used to operate as a simple event counter or a gated time accumulator. The pulse accumulator shares timer channel 7 when in event mode.

A full access for the counter registers or the input capture/output compare registers should take place in one clock cycle. Accessing high byte and low byte separately for all of these registers may not yield the same result as accessing them in one word.

16.1.1 Features

The TIM16B8C includes these distinctive features:

- Eight input capture/output compare channels.
- Clock prescaling.
- 16-bit counter.
- 16-bit pulse accumulator.

16.1.2 Modes of Operation

Stop: Timer is off because clocks are stopped.

Freeze: Timer counter keep on running, unless TSFRZ in TSCR (0x0006) is set to 1.

Wait: Counters keep on running, unless TSWAI in TSCR (0x0006) is set to 1.

Normal: Timer counter keep on running, unless TEN in TSCR (0x0006) is cleared to 0.

16.1.3 Block Diagrams

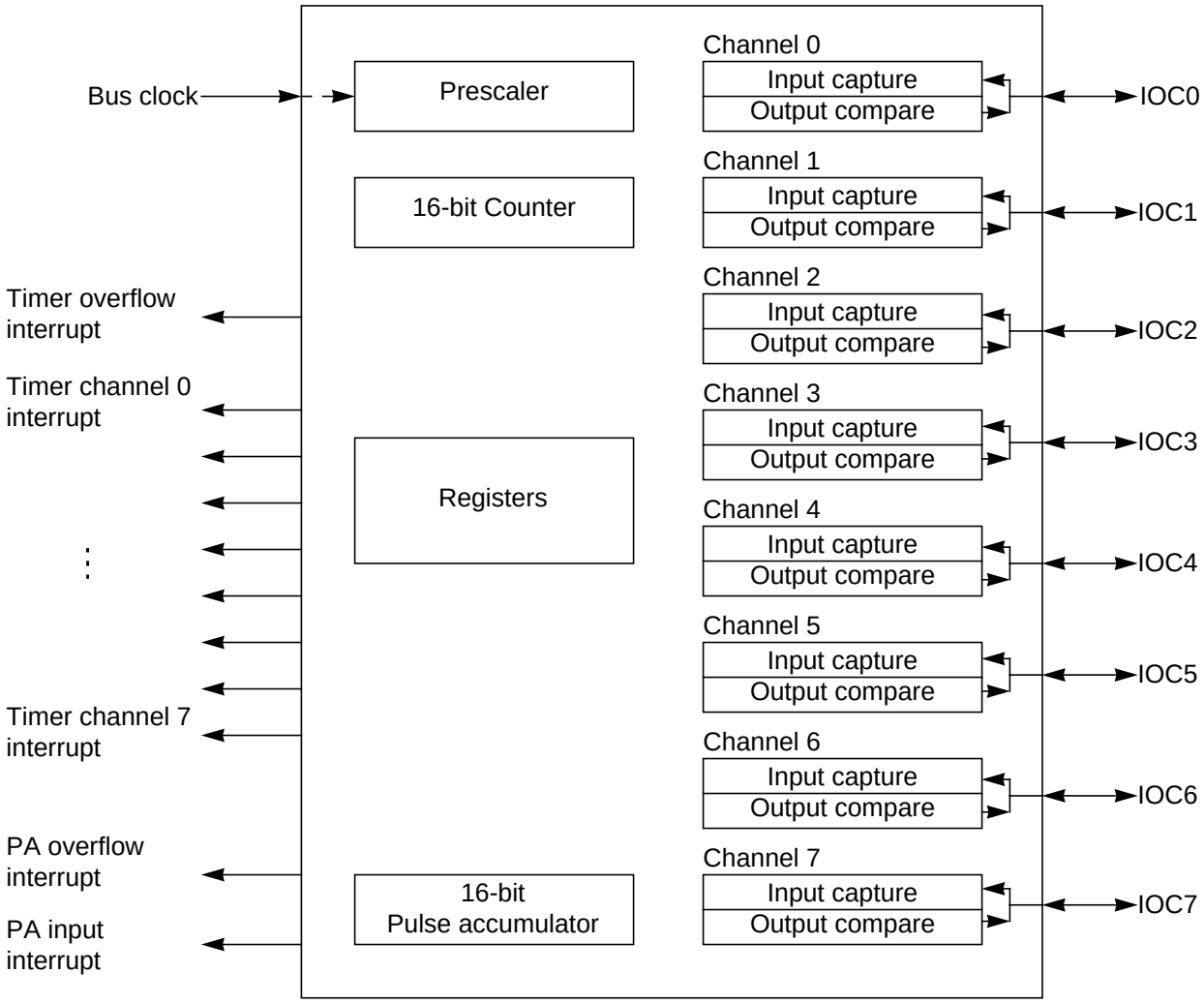


Figure 16-1. TIM16B8C Block Diagram

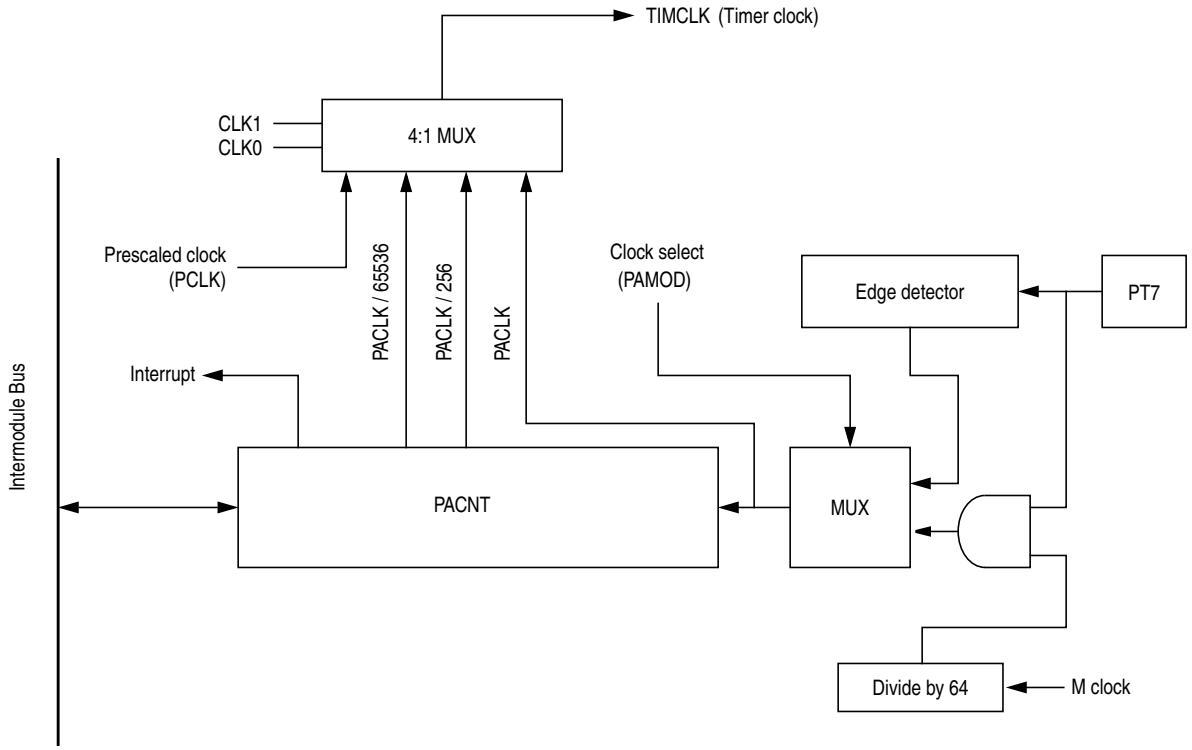


Figure 16-2. 16-Bit Pulse Accumulator Block Diagram

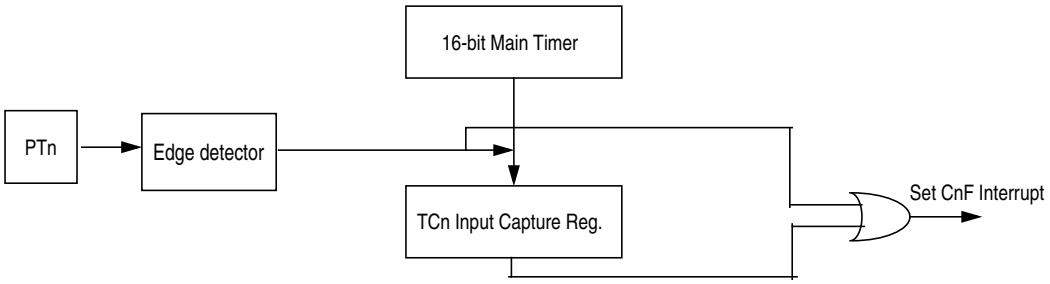


Figure 16-3. Interrupt Flag Setting

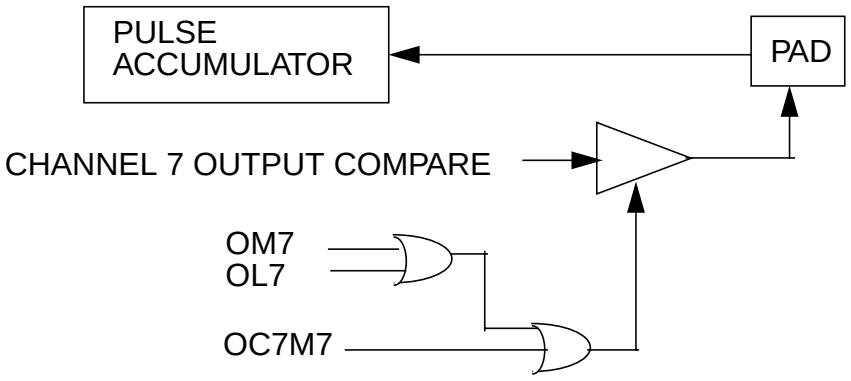


Figure 16-4. Channel 7 Output Compare/Pulse Accumulator Logic

NOTE

For more information see the respective functional descriptions in Section 16.4, "Functional Description," of this document.

16.2 External Signal Description

The TIM16B8C module has a total of eight external pins.

16.2.1 IOC7 — Input Capture and Output Compare Channel 7 Pin

This pin serves as input capture or output compare for channel 7. This can also be configured as pulse accumulator input.

16.2.2 IOC6 — Input Capture and Output Compare Channel 6 Pin

This pin serves as input capture or output compare for channel 6.

16.2.3 IOC5 — Input Capture and Output Compare Channel 5 Pin

This pin serves as input capture or output compare for channel 5.

16.2.4 IOC4 — Input Capture and Output Compare Channel 4 Pin

This pin serves as input capture or output compare for channel 4. Pin

16.2.5 IOC3 — Input Capture and Output Compare Channel 3 Pin

This pin serves as input capture or output compare for channel 3.

16.2.6 IOC2 — Input Capture and Output Compare Channel 2 Pin

This pin serves as input capture or output compare for channel 2.

16.2.7 IOC1 — Input Capture and Output Compare Channel 1 Pin

This pin serves as input capture or output compare for channel 1.

16.2.8 IOC0 — Input Capture and Output Compare Channel 0 Pin

This pin serves as input capture or output compare for channel 0.

NOTE

For the description of interrupts see Section 16.6, “Interrupts”.

16.3 Memory Map and Register Definition

This section provides a detailed description of all memory and registers.

16.3.1 Module Memory Map

The memory map for the TIM16B8C module is given below in Table 16-1. The address listed for each register is the address offset. The total address for each register is the sum of the base address for the TIM16B8C module and the address offset for each register.

Table 16-1. TIM16B8C Memory Map

Address Offset	Use	Access
0x0000	Timer Input Capture/Output Compare Select (TIOS)	R/W
0x0001	Timer Compare Force Register (CFORC)	R/W[1]
0x0002	Output Compare 7 Mask Register (OC7M)	R/W
0x0003	Output Compare 7 Data Register (OC7D)	R/W
0x0004	Timer Count Register (TCNT(hi))	R/W[2]
0x0005	Timer Count Register (TCNT(lo))	R/W[2]
0x0006	Timer System Control Register1 (TSCR1)	R/W
0x0007	Timer Toggle Overflow Register (TTOV)	R/W
0x0008	Timer Control Register1 (TCTL1)	R/W
0x0009	Timer Control Register2 (TCTL2)	R/W
0x000A	Timer Control Register3 (TCTL3)	R/W
0x000B	Timer Control Register4 (TCTL4)	R/W
0x000C	Timer Interrupt Enable Register (TIE)	R/W
0x000D	Timer System Control Register2 (TSCR2)	R/W
0x000E	Main Timer Interrupt Flag1 (TFLG1)	R/W
0x000F	Main Timer Interrupt Flag2 (TFLG2)	R/W
0x0010	Timer Input Capture/Output Compare Register 0 (TC0(hi))	R/W[3]
0x0011	Timer Input Capture/Output Compare Register 0 (TC0(lo))	R/W[3]
0x0012	Timer Input Capture/Output Compare Register 1 (TC1(hi))	R/W[3]
0x0013	Timer Input Capture/Output Compare Register 1 (TC1(lo))	R/W[3]
0x0014	Timer Input Capture/Output Compare Register 2 (TC2(hi))	R/W[3]
0x0015	Timer Input Capture/Output Compare Register 2 (TC2(lo))	R/W[3]
0x0016	Timer Input Capture/Output Compare Register 3 (TC3(hi))	R/W[3]
0x0017	Timer Input Capture/Output Compare Register 3 (TC3(lo))	R/W[3]
0x0018	Timer Input Capture/Output Compare Register4 (TC4(hi))	R/W[3]
0x0019	Timer Input Capture/Output Compare Register 4 (TC4(lo))	R/W[3]
0x001A	Timer Input Capture/Output Compare Register 5 (TC5(hi))	R/W[3]
0x001B	Timer Input Capture/Output Compare Register 5 (TC5(lo))	R/W[3]
0x001C	Timer Input Capture/Output Compare Register 6 (TC6(hi))	R/W[3]
0x001D	Timer Input Capture/Output Compare Register 6 (TC6(lo))	R/W[3]
0x001E	Timer Input Capture/Output Compare Register 7 (TC7(hi))	R/W[3]
0x001F	Timer Input Capture/Output Compare Register 7 (TC7(lo))	R/W[3]
0x0020	16-Bit Pulse Accumulator Control Register (PACTL)	R/W
0x0021	Pulse Accumulator Flag Register (PAFLG)	R/W
0x0022	Pulse Accumulator Count Register (PACNT(hi))	R/W
0x0023	Pulse Accumulator Count Register (PACNT(lo))	R/W
0x0024 – 0x002C	Reserved	—[4]
0x002D	Timer Test Register (TIMTST)	R/W[2]
0x002E – 0x002F	Reserved	—[4]

1 Always read 0x0000.

2 Only writable in special modes (test_mode = 1).

3 Write to these registers have no meaning or effect during input capture.

[4] Write has no effect; return 0 on read

16.3.2 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Details of register bit and field function follow the register diagrams, in bit order.

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x0000 TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
	W								
0x0001 CFORC	R	0	0	0	0	0	0	0	0
	W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x0002 OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
	W								
0x0003 OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
	W								
0x0004 TCNTH	R	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
	W								
0x0005 TCNTL	R	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
	W								
0x0006 TSCR2	R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
	W								
0x0007 TTOV	R	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
	W								
0x0008 TCTL1	R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
	W								
0x0009 TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
	W								
0x000A TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
	W								
0x000B TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
	W								

= Unimplemented or Reserved

Figure 16-5. TIM16B8C Register Summary

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
0x000C TIE	R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
	W								
0x000D TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
	W								
0x000E TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
	W								
0x000F TFLG2	R	TOF	0	0	0	0	0	0	0
	W								
0x0010–0x001F TCxH–TCxL	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
0x0020 PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
	W								
0x0021 PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
	W								
0x0022 PACNTH	R	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
	W								
0x0023 PACNTL	R	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
	W								
0x0024–0x002F Reserved	R								
	W								

= Unimplemented or Reserved

Figure 16-5. TIM16B8C Register Summary (continued)

16.3.2.1 Timer Input Capture/Output Compare Select (TIOS)

	7	6	5	4	3	2	1	0
R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
W								
Reset	0	0	0	0	0	0	0	0

Figure 16-6. Timer Input Capture/Output Compare Select (TIOS)

Read: Anytime

Write: Anytime

Table 16-2. TIOS Field Descriptions

Field	Description
7:0 IOS[7:0]	**Input Capture or Output Compare Channel Configuration** 0 The corresponding channel acts as an input capture. 1 The corresponding channel acts as an output compare.

16.3.2.2 Timer Compare Force Register (CFORC)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
Reset	0	0	0	0	0	0	0	0

Figure 16-7. Timer Compare Force Register (CFORC)

Read: Anytime but will always return 0x0000 (1 state is transient)

Write: Anytime

Table 16-3. CFORC Field Descriptions

Field	Description
7:0 FOC[7:0]	**Force Output Compare Action for Channel 7:0** — A write to this register with the corresponding data bit(s) set causes the action which is programmed for output compare “x” to occur immediately. The action taken is the same as if a successful comparison had just taken place with the TCx register except the interrupt flag does not get set. **Note:** A successful channel 7 output compare overrides any channel 6:0 compares. If forced output compare on any channel occurs at the same time as the successful output compare then forced output compare action will take precedence and interrupt flag won’t get set.

16.3.2.3 Output Compare 7 Mask Register (OC7M)

	7	6	5	4	3	2	1	0
R W	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
Reset	0	0	0	0	0	0	0	0

Figure 16-8. Output Compare 7 Mask Register (OC7M)

Read: Anytime

Write: Anytime

Table 16-4. OC7M Field Descriptions

Field	Description
7:0 OC7M[7:0]	**Output Compare 7 Mask** — Setting the OC7Mx (x ranges from 0 to 6) will set the corresponding port to be an output port when the corresponding TIOSx (x ranges from 0 to 6) bit is set to be an output compare. **Note:** A successful channel 7 output compare overrides any channel 6:0 compares. For each OC7M bit that is set, the output compare action reflects the corresponding OC7D bit.

16.3.2.4 Output Compare 7 Data Register (OC7D)

	7	6	5	4	3	2	1	0
R W	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
Reset	0	0	0	0	0	0	0	0

Figure 16-9. Output Compare 7 Data Register (OC7D)

Read: Anytime

Write: Anytime

Table 16-5. OC7D Field Descriptions

Field	Description
7:0 OC7D[7:0]	**Output Compare 7 Data** — A channel 7 output compare can cause bits in the output compare 7 data register to transfer to the timer port data register depending on the output compare 7 mask register.

16.3.2.5 Timer Count Register (TCNT)

	15	14	13	12	11	10	9	9
R W	TCNT15	TCNT14	TCNT13	TCNT12	TCNT11	TCNT10	TCNT9	TCNT8
Reset	0	0	0	0	0	0	0	0

Figure 16-10. Timer Count Register High (TCNTH)

	7	6	5	4	3	2	1	0
R W	TCNT7	TCNT6	TCNT5	TCNT4	TCNT3	TCNT2	TCNT1	TCNT0
Reset	0	0	0	0	0	0	0	0

Figure 16-11. Timer Count Register Low (TCNTL)

The 16-bit main timer is an up counter.

A full access for the counter register should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

Read: Anytime

Write: Has no meaning or effect in the normal mode; only writable in special modes (test_mode = 1).

The period of the first count after a write to the TCNT registers may be a different size because the write is not synchronized with the prescaler clock.

16.3.2.6 Timer System Control Register 1 (TSCR1)

	7	6	5	4	3	2	1	0
R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-12. Timer System Control Register 1 (TSCR2)

Read: Anytime

Write: Anytime

Table 16-6. TSCR1 Field Descriptions

Field	Description
7 TEN	**Timer Enable** 0 Disables the main timer, including the counter. Can be used for reducing power consumption. 1 Allows the timer to function normally. If for any reason the timer is not active, there is no ÷64 clock for the pulse accumulator because the ÷64 is generated by the timer prescaler.
6 TSWAI	**Timer Module Stops While in Wait** 0 Allows the timer module to continue running during wait. 1 Disables the timer module when the MCU is in the wait mode. Timer interrupts cannot be used to get the MCU out of wait. TSWAI also affects pulse accumulator.
5 TSFRZ	**Timer Stops While in Freeze Mode** 0 Allows the timer counter to continue running while in freeze mode. 1 Disables the timer counter whenever the MCU is in freeze mode. This is useful for emulation. TSFRZ does not stop the pulse accumulator.
4 TFFCA	**Timer Fast Flag Clear All** 0 Allows the timer flag clearing to function normally. 1 For TFLG1(0x000E), a read from an input capture or a write to the output compare channel (0x0010–0x001F) causes the corresponding channel flag, CnF, to be cleared. For TFLG2 (0x000F), any access to the TCNT register (0x0004, 0x0005) clears the TOF flag. Any access to the PACNT registers (0x0022, 0x0023) clears the PAOVF and PAIF flags in the PAFLG register (0x0021). This has the advantage of eliminating software overhead in a separate clear sequence. Extra care is required to avoid accidental flag clearing due to unintended accesses.

16.3.2.7 Timer Toggle On Overflow Register 1 (TTOV)

	7	6	5	4	3	2	1	0
R W	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
Reset	0	0	0	0	0	0	0	0

Figure 16-13. Timer Toggle On Overflow Register 1 (TTOV)

Read: Anytime

Write: Anytime

Table 16-7. TTOV Field Descriptions

Field	Description
7:0 TOV[7:0]	**Toggle On Overflow Bits** — TOVx toggles output compare pin on overflow. This feature only takes effect when in output compare mode. When set, it takes precedence over forced output compare but not channel 7 override events. 0 Toggle output compare pin on overflow feature disabled. 1 Toggle output compare pin on overflow feature enabled.

16.3.2.8 Timer Control Register 1/Timer Control Register 2 (TCTL1/TCTL2)

	7	6	5	4	3	2	1	0
R W	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
Reset	0	0	0	0	0	0	0	0

Figure 16-14. Timer Control Register 1 (TCTL1)

	7	6	5	4	3	2	1	0
R W	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
Reset	0	0	0	0	0	0	0	0

Figure 16-15. Timer Control Register 2 (TCTL2)

Read: Anytime

Write: Anytime

Table 16-8. TCTL1/TCTL2 Field Descriptions

Field	Description
7:0 OMx	**Output Mode** — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** To enable output action by OMx bits on timer port, the corresponding bit in OC7M should be cleared.
7:0 OLx	**Output Level** — These eight pairs of control bits are encoded to specify the output action to be taken as a result of a successful OCx compare. When either OMx or OLx is 1, the pin associated with OCx becomes an output tied to OCx. **Note:** To enable output action by OLx bits on timer port, the corresponding bit in OC7M should be cleared.

Table 16-9. Compare Result Output Action

OMx	OLx	Action
0	0	Timer disconnected from output pin logic
0	1	Toggle OCx output line
1	0	Clear OCx output line to zero
1	1	Set OCx output line to one

To operate the 16-bit pulse accumulator independently of input capture or output compare 7 and 0 respectively the user must set the corresponding bits IOSx = 1, OMx = 0 and OLx = 0. OC7M7 in the OC7M register must also be cleared.

16.3.2.9 Timer Control Register 3/Timer Control Register 4 (TCTL3 and TCTL4)

	7	6	5	4	3	2	1	0
R W	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
Reset	0	0	0	0	0	0	0	0

Figure 16-16. Timer Control Register 3 (TCTL3)

	7	6	5	4	3	2	1	0
R W	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
Reset	0	0	0	0	0	0	0	0

Figure 16-17. Timer Control Register 4 (TCTL4)

Read: Anytime

Write: Anytime.

Table 16-10. TCTL3/TCTL4 Field Descriptions

Field	Description
7:0 EDGnB EDGnA	**Input Capture Edge Control** — These eight pairs of control bits configure the input capture edge detector circuits.

Table 16-11. Edge Detector Circuit Configuration

EDGnB	EDGnA	Configuration
0	0	Capture disabled
0	1	Capture on rising edges only
1	0	Capture on falling edges only
1	1	Capture on any edge (rising or falling)

16.3.2.10 Timer Interrupt Enable Register (TIE)

	7	6	5	4	3	2	1	0
R W	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
Reset	0	0	0	0	0	0	0	0

Figure 16-18. Timer Interrupt Enable Register (TIE)

Read: Anytime

Write: Anytime.

Table 16-12. TIE Field Descriptions

Field	Description
7:0 C7I:C0I	**Input Capture/Output Compare "x" Interrupt Enable —** The bits in TIE correspond bit-for-bit with the bits in the TFLG1 status register. If cleared, the corresponding flag is disabled from causing a hardware interrupt. If set, the corresponding flag is enabled to cause a interrupt.

16.3.2.11 Timer System Control Register 2 (TSCR2)

	7	6	5	4	3	2	1	0
R	TOI	0	0	0	TCRE	PR2	PR1	PR0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 16-19. Timer System Control Register 2 (TSCR2)

Read: Anytime

Write: Anytime.

Table 16-13. TSCR2 Field Descriptions

Field	Description
7 TOI	**Timer Overflow Interrupt Enable** 0 Interrupt inhibited. 1 Hardware interrupt requested when TOF flag set.
3 TCRE	**Timer Counter Reset Enable** — This bit allows the timer counter to be reset by a successful output compare 7 event. This mode of operation is similar to an up-counting modulus counter. 0 Counter reset inhibited and counter free runs. 1 Counter reset by a successful output compare 7. If TC7 = 0x0000 and TCRE = 1, TCNT will stay at 0x0000 continuously. If TC7 = 0xFFFF and TCRE = 1, TOF will never be set when TCNT is reset from 0xFFFF to 0x0000.
2 PR[2:0]	**Timer Prescaler Select** — These three bits select the frequency of the timer prescaler clock derived from the Bus Clock as shown in Table 16-14.

Table 16-14. Timer Clock Selection

PR2	PR1	PR0	Timer Clock
0	0	0	Bus Clock / 1
0	0	1	Bus Clock / 2
0	1	0	Bus Clock / 4
0	1	1	Bus Clock / 8
1	0	0	Bus Clock / 16
1	0	1	Bus Clock / 32
1	1	0	Bus Clock / 64
1	1	1	Bus Clock / 128

NOTE

The newly selected prescale factor will not take effect until the next synchronized edge where all prescale counter stages equal zero.

16.3.2.12 Main Timer Interrupt Flag 1 (TFLG1)

	7	6	5	4	3	2	1	0
R W	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
Reset	0	0	0	0	0	0	0	0

Figure 16-20. Main Timer Interrupt Flag 1 (TFLG1)

Read: Anytime

Write: Used in the clearing mechanism (set bits cause corresponding bits to be cleared). Writing a zero will not affect current status of the bit.

Table 16-15. TRLG1 Field Descriptions

Field	Description
7:0 C[7:0]F	**Input Capture/Output Compare Channel “x” Flag** — These flags are set when an input capture or output compare event occurs. Clear a channel flag by writing one to it. When TFFCA bit in TSCR register is set, a read from an input capture or a write into an output compare channel (0x0010–0x001F) will cause the corresponding channel flag CxF to be cleared.

16.3.2.13 Main Timer Interrupt Flag 2 (TFLG2)

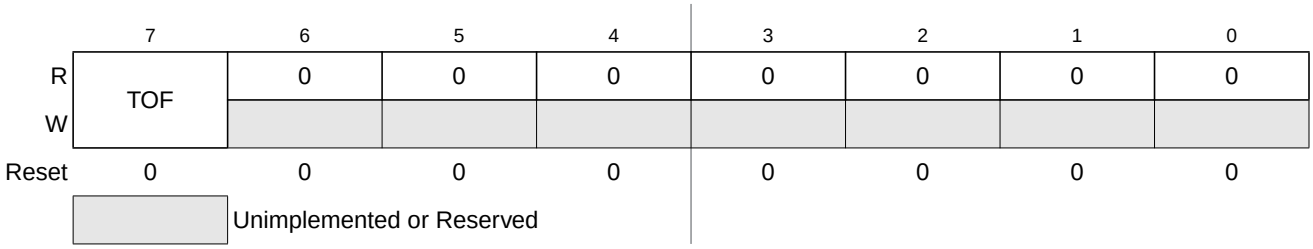


Figure 16-21. Main Timer Interrupt Flag 2 (TFLG2)

TFLG2 indicates when interrupt conditions have occurred. To clear a bit in the flag register, write the bit to one.

Read: Anytime

Write: Used in clearing mechanism (set bits cause corresponding bits to be cleared).

Any access to TCNT will clear TFLG2 register if the TFFCA bit in TSCR register is set.

Table 16-16. TRLG2 Field Descriptions

Field	Description
7 TOF	**Timer Overflow Flag** — Set when 16-bit free-running timer overflows from 0xFFFF to 0x0000. This bit is cleared automatically by a write to the TFLG2 register with bit 7 set. (See also TCRE control bit explanation.)

16.3.2.14 Timer Input Capture/Output Compare Registers High and Low 0–7 (TCxH and TCxL)

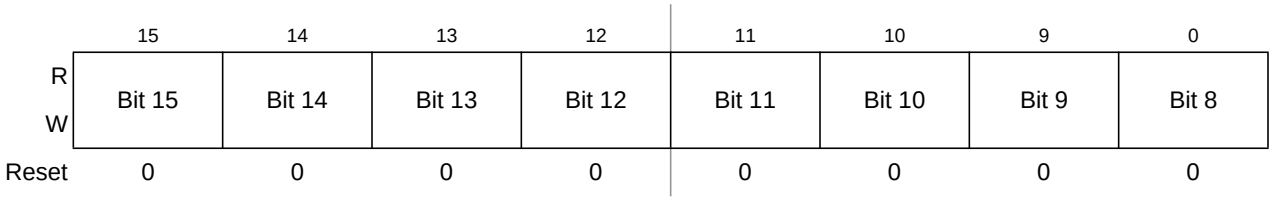


Figure 16-22. Timer Input Capture/Output Compare Register x High (TCxH)

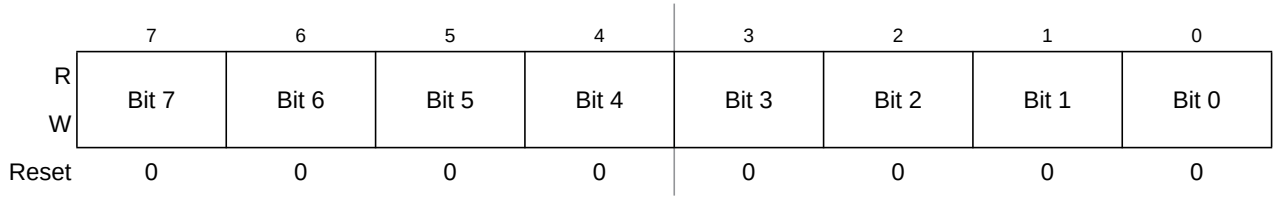


Figure 16-23. Timer Input Capture/Output Compare Register x Low (TCxL)

Depending on the TIOS bit for the corresponding channel, these registers are used to latch the value of the free-running counter when a defined transition is sensed by the corresponding input capture edge detector or to trigger an output action for output compare.

Read: Anytime

Write: Anytime for output compare function.Writes to these registers have no meaning or effect during input capture. All timer input capture/output compare registers are reset to 0x0000.

NOTE

Read/Write access in byte mode for high byte should takes place before low byte otherwise it will give a different result.

16.3.2.15 16-Bit Pulse Accumulator Control Register (PACTL)

	7	6	5	4	3	2	1	0
R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 16-24. 16-Bit Pulse Accumulator Control Register (PACTL)

When PAEN is set, the PACT is enabled.The PACT shares the input pin with IOC7.

Read: Any time

Write: Any time

Table 16-17. PACTL Field Descriptions

Field	Description
6 PAEN	**Pulse Accumulator System Enable** — PAEN is independent from TEN. With timer disabled, the pulse accumulator can function unless pulse accumulator is disabled. 0 16-Bit Pulse Accumulator system disabled. 1 Pulse Accumulator system enabled.
5 PAMOD	**Pulse Accumulator Mode** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). See Table 16-18. 0 Event counter mode. 1 Gated time accumulation mode.
4 PEDGE	**Pulse Accumulator Edge Control** — This bit is active only when the Pulse Accumulator is enabled (PAEN = 1). For PAMOD bit = 0 (event counter mode). See Table 16-18. 0 Falling edges on IOC7 pin cause the count to be incremented. 1 Rising edges on IOC7 pin cause the count to be incremented. For PAMOD bit = 1 (gated time accumulation mode). 0 IOC7 input pin high enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing falling edge on IOC7 sets the PAIF flag. 1 IOC7 input pin low enables M (bus clock) divided by 64 clock to Pulse Accumulator and the trailing rising edge on IOC7 sets the PAIF flag.
3:2 CLK[1:0]	**Clock Select Bits —** Refer to Table 16-19.

Table 16-17. PACTL Field Descriptions (continued)

Field	Description
1 PAOVI	**Pulse Accumulator Overflow Interrupt Enable** 0 Interrupt inhibited. 1 Interrupt requested if PAOVF is set.
0 PAI	**Pulse Accumulator Input Interrupt Enable** 0 Interrupt inhibited. 1 Interrupt requested if PAIF is set.

Table 16-18. Pin Action

PAMOD	PEDGE	Pin Action
0	0	Falling edge
0	1	Rising edge
1	0	Div. by 64 clock enabled with pin high level
1	1	Div. by 64 clock enabled with pin low level

NOTE

If the timer is not active (TEN = 0 in TSCR), there is no divide-by-64 because the ÷64 clock is generated by the timer prescaler.

Table 16-19. Timer Clock Selection

CLK1	CLK0	Timer Clock
0	0	Use timer prescaler clock as timer counter clock
0	1	Use PACLK as input to timer counter clock
1	0	Use PACLK/256 as timer counter clock frequency
1	1	Use PACLK/65536 as timer counter clock frequency

For the description of PACLK please refer Figure 16-24**.**

If the pulse accumulator is disabled (PAEN = 0), the prescaler clock from the timer is always used as an input clock to the timer counter. The change from one selected clock to the other happens immediately after these bits are written.

16.3.2.16 Pulse Accumulator Flag Register (PAFLG)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	PAOVF	PAIF
W								
Reset	0	0	0	0	0	0	0	0

Unimplemented or Reserved

Figure 16-25. Pulse Accumulator Flag Register (PAFLG)

Read: Anytime

Write: Anytime

When the TFFCA bit in the TSCR register is set, any access to the PACNT register will clear all the flags in the PAFLG register.

Table 16-20. PAFLG Field Descriptions

Field	Description
1 PAOVF	**Pulse Accumulator Overflow Flag** — Set when the 16-bit pulse accumulator overflows from 0xFFFF to 0x0000. This bit is cleared automatically by a write to the PAFLG register with bit 1 set.
0 PAIF	**Pulse Accumulator Input edge Flag** — Set when the selected edge is detected at the IOC7 input pin.In event mode the event edge triggers PAIF and in gated time accumulation mode the trailing edge of the gate signal at the IOC7 input pin triggers PAIF. This bit is cleared by a write to the PAFLG register with bit 0 set. Any access to the PACNT register will clear all the flags in this register when TFFCA bit in register TSCR(0x0006) is set.

16.3.2.17 Pulse Accumulators Count Registers (PACNT)

	15	14	13	12	11	10	9	0
R W	PACNT15	PACNT14	PACNT13	PACNT12	PACNT11	PACNT10	PACNT9	PACNT8
Reset	0	0	0	0	0	0	0	0

Figure 16-26. Pulse Accumulator Count Register High (PACNTH)

	7	6	5	4	3	2	1	0
R W	PACNT7	PACNT6	PACNT5	PACNT4	PACNT3	PACNT2	PACNT1	PACNT0
Reset	0	0	0	0	0	0	0	0

Figure 16-27. Pulse Accumulator Count Register Low (PACNTL)

Read: Anytime

Write: Anytime

These registers contain the number of active input edges on its input pin since the last reset.

When PACNT overflows from 0xFFFF to 0x0000, the Interrupt flag PAOVF in PAFLG (0x0021) is set.

Full count register access should take place in one clock cycle. A separate read/write for high byte and low byte will give a different result than accessing them as a word.

NOTE

Reading the pulse accumulator counter registers immediately after an active edge on the pulse accumulator input pin may miss the last count because the input has to be synchronized with the bus clock first.

16.4 Functional Description

This section provides a complete functional description of the timer TIM16B8C block. Please refer to the detailed timer block diagram in Figure 16-28 as necessary.

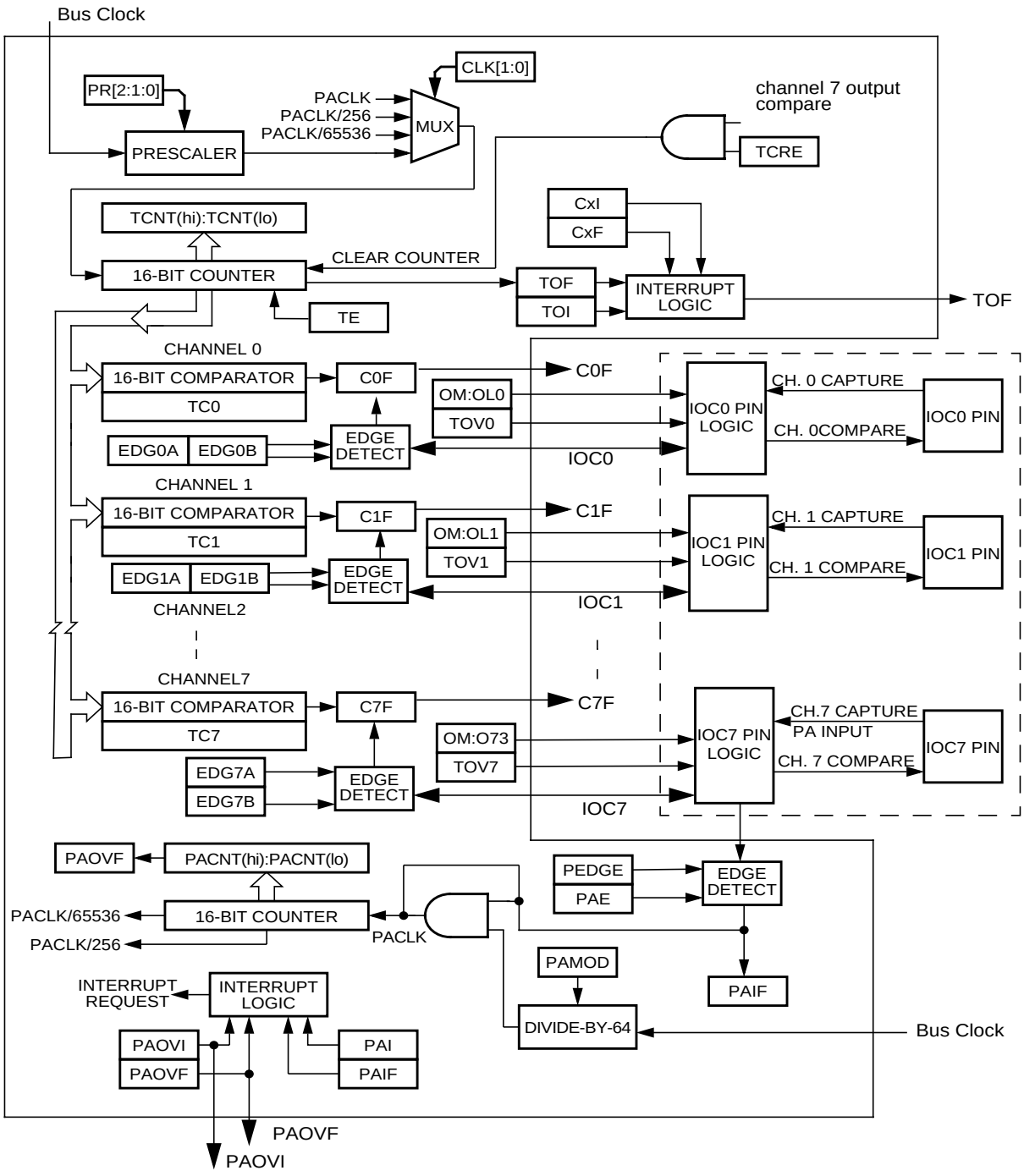


Figure 16-28. Detailed Timer Block Diagram

16.4.1 Prescaler

The prescaler divides the bus clock by 1,2,4,8,16,32,64 or 128. The prescaler select bits, PR[2:0], select the prescaler divisor. PR[2:0] are in timer system control register 2 (TSCR2).

16.4.2 Input Capture

Clearing the I/O (input/output) select bit, IOSx, configures channel x as an input capture channel. The input capture function captures the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the timer transfers the value in the timer counter into the timer channel registers, TCx.

The minimum pulse width for the input capture input is greater than two bus clocks.

An input capture on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests.

16.4.3 Output Compare

Setting the I/O select bit, IOSx, configures channel x as an output compare channel. The output compare function can generate a periodic pulse with a programmable polarity, duration, and frequency. When the timer counter reaches the value in the channel registers of an output compare channel, the timer can set, clear, or toggle the channel pin. An output compare on channel x sets the CxF flag. The CxI bit enables the CxF flag to generate interrupt requests.

The output mode and level bits, OMx and OLx, select set, clear, toggle on output compare. Clearing both OMx and OLx disconnects the pin from the output logic.

Setting a force output compare bit, FOCx, causes an output compare on channel x. A forced output compare does not set the channel flag.

A successful output compare on channel 7 overrides output compares on all other output compare channels. The output compare 7 mask register masks the bits in the output compare 7 data register. The timer counter reset enable bit, TCRE, enables channel 7 output compares to reset the timer counter. A channel 7 output compare can reset the timer counter even if the IOC7 pin is being used as the pulse accumulator input.

Writing to the timer port bit of an output compare pin does not affect the pin state. The value written is stored in an internal latch. When the pin becomes available for general-purpose output, the last value written to the bit appears at the pin.

16.4.4 Pulse Accumulator

The pulse accumulator (PACNT) is a 16-bit counter that can operate in two modes:

Event counter mode — Counting edges of selected polarity on the pulse accumulator input pin, PAI.

Gated time accumulation mode — Counting pulses from a divide-by-64 clock. The PAMOD bit selects the mode of operation.

The minimum pulse width for the PAI input is greater than two bus clocks.

16.4.5 Event Counter Mode

Clearing the PAMOD bit configures the PACNT for event counter operation. An active edge on the IOC7 pin increments the pulse accumulator counter. The PEDGE bit selects falling edges or rising edges to increment the count.

NOTE

The PACNT input and timer channel 7 use the same pin IOC7. To use the IOC7, disconnect it from the output logic by clearing the channel 7 output mode and output level bits, OM7 and OL7. Also clear the channel 7 output compare 7 mask bit, OC7M7.

The Pulse Accumulator counter register reflect the number of active input edges on the PACNT input pin since the last reset.

The PAOVF bit is set when the accumulator rolls over from 0xFFFF to 0x0000. The pulse accumulator overflow interrupt enable bit, PAOVI, enables the PAOVF flag to generate interrupt requests.

NOTE

The pulse accumulator counter can operate in event counter mode even when the timer enable bit, TEN, is clear.

16.4.6 Gated Time Accumulation Mode

Setting the PAMOD bit configures the pulse accumulator for gated time accumulation operation. An active level on the PACNT input pin enables a divided-by-64 clock to drive the pulse accumulator. The PEDGE bit selects low levels or high levels to enable the divided-by-64 clock.

The trailing edge of the active level at the IOC7 pin sets the PAIF. The PAI bit enables the PAIF flag to generate interrupt requests.

The pulse accumulator counter register reflect the number of pulses from the divided-by-64 clock since the last reset.

NOTE

The timer prescaler generates the divided-by-64 clock. If the timer is not active, there is no divided-by-64 clock.

16.5 Resets

The reset state of each individual bit is listed within Section 16.3, “Memory Map and Register Definition” which details the registers and their bit fields.

16.6 Interrupts

This section describes interrupts originated by the TIM16B8C block. Table 16-21 lists the interrupts generated by the TIM16B8C to communicate with the MCU.

Table 16-21. TIM16B8CV1 Interrupts

Interrupt	Offset[1]	Vector[1]	Priority[1]	Source	Description
C[7:0]F	—	—	—	Timer Channel 7–0	Active high timer channel interrupts 7–0
PAOVI	—	—	—	Pulse Accumulator Input	Active high pulse accumulator input interrupt
PAOVF	—	—	—	Pulse Accumulator Overflow	Pulse accumulator overflow interrupt
TOF	—	—	—	Timer Overflow	Timer Overflow interrupt

1 Chip Dependent.

The TIM16B8C uses a total of 11 interrupt vectors. The interrupt vector offsets and interrupt numbers are chip dependent.

16.6.1 Channel [7:0] Interrupt (C[7:0]F)

This active high outputs will be asserted by the module to request a timer channel 7 – 0 interrupt to be serviced by the system controller.

16.6.2 Pulse Accumulator Input Interrupt (PAOVI)

This active high output will be asserted by the module to request a timer pulse accumulator input interrupt to be serviced by the system controller.

16.6.3 Pulse Accumulator Overflow Interrupt (PAOVF)

This active high output will be asserted by the module to request a timer pulse accumulator overflow interrupt to be serviced by the system controller.

16.6.4 Timer Overflow Interrupt (TOF)

This active high output will be asserted by the module to request a timer overflow interrupt to be serviced by the system controller.

Chapter 17
Dual Output Voltage Regulator (VREG3V3V2)

17.1 Introduction

The VREG3V3 is a dual output voltage regulator providing two separate 2.5 V (typical) supplies differing in the amount of current that can be sourced. The regulator input voltage range is from 3.3 V up to 5 V (typical).

17.1.1 Features

The block VREG3V3 includes these distinctive features:

- Two parallel, linear voltage regulators
  - — Bandgap reference
- Low-voltage detect (LVD) with low-voltage interrupt (LVI)
- Power-on reset (POR)
- Low-voltage reset (LVR)

17.1.2 Modes of Operation

There are three modes VREG3V3 can operate in:

- Full-performance mode (FPM) (MCU is not in stop mode)

  The regulator is active, providing the nominal supply voltage of 2.5 V with full current sourcing capability at both outputs. Features LVD (low-voltage detect), LVR (low-voltage reset), and POR (power-on reset) are available.
- Reduced-power mode (RPM) (MCU is in stop mode)

  The purpose is to reduce power consumption of the device. The output voltage may degrade to a lower value than in full-performance mode, additionally the current sourcing capability is substantially reduced. Only the POR is available in this mode, LVD and LVR are disabled.
- Shutdown mode

  Controlled by V_{REGEN} (see device overview chapter for connectivity of V_{REGEN}).

  This mode is characterized by minimum power consumption. The regulator outputs are in a high impedance state, only the POR feature is available, LVD and LVR are disabled.

  This mode must be used to disable the chip internal regulator VREG3V3, i.e., to bypass the VREG3V3 to use external supplies.

17.1.3 Block Diagram

Figure 17-1 shows the function principle of VREG3V3 by means of a block diagram. The regulator core REG consists of two parallel sub-blocks, REG1 and REG2, providing two independent output voltages.

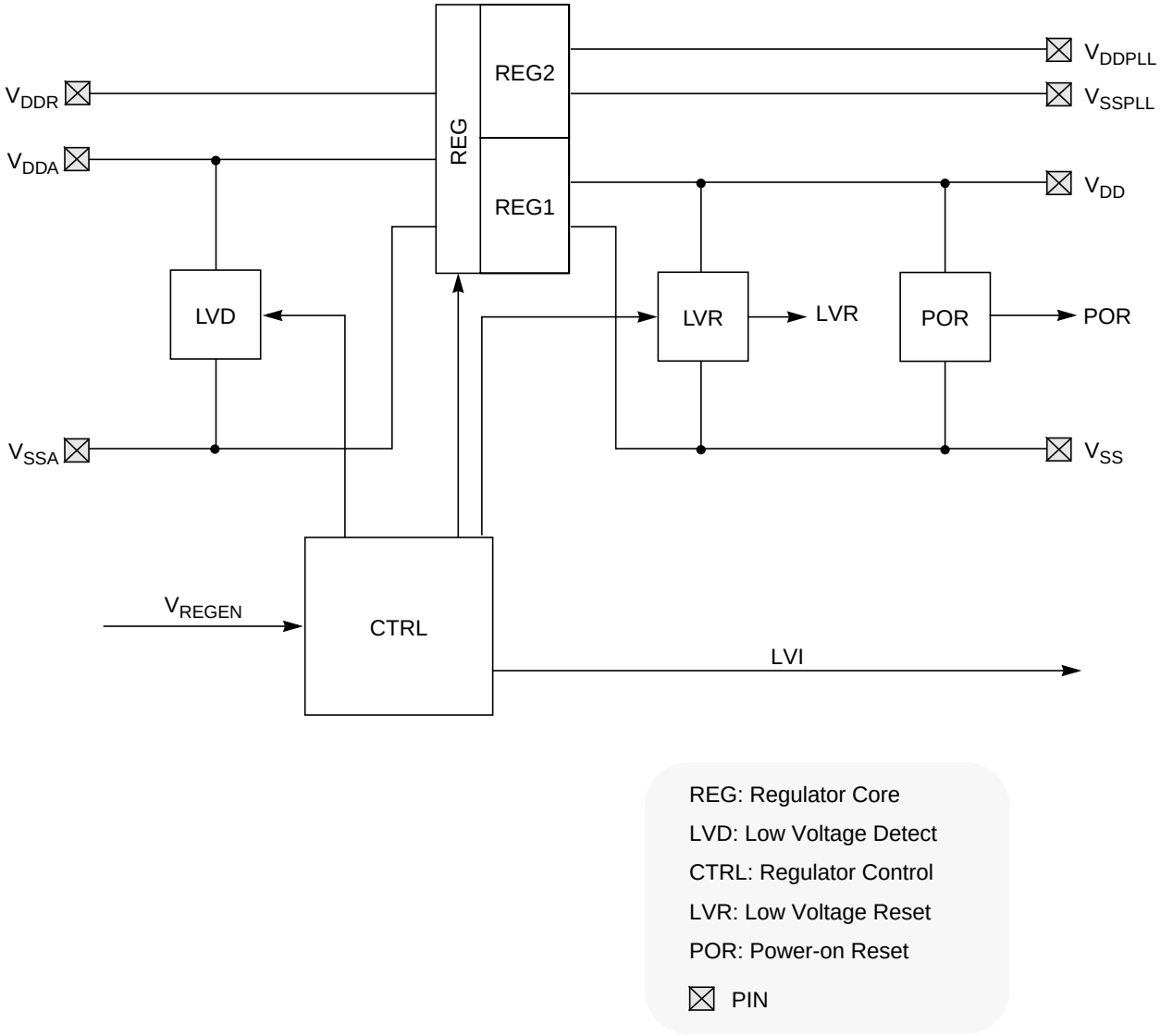


Figure 17-1. VREG3V3 Block Diagram

17.2 External Signal Description

Due to the nature of VREG3V3 being a voltage regulator providing the chip internal power supply voltages most signals are power supply signals connected to pads.

Table 17-1 shows all signals of VREG3V3 associated with pins.

Table 17-1. VREG3V3 — Signal Properties

Name	Port	Function	Reset State	Pull Up
V_{DDR}	—	VREG3V3 power input (positive supply)	—	—
V_{DDA}	—	VREG3V3 quiet input (positive supply)	—	—
V_{SSA}	—	VREG3V3 quiet input (ground)	—	—
V_{DD}	—	VREG3V3 primary output (positive supply)	—	—
V_{SS}	—	VREG3V3 primary output (ground)	—	—
V_{DDPLL}	—	VREG3V3 secondary output (positive supply)	—	—
V_{SSPLL}	—	VREG3V3 secondary output (ground)	—	—
V_{REGEN} (optional)	—	VREG3V3 (Optional) Regulator Enable	—	—

NOTE

Check device overview chapter for connectivity of the signals.

17.2.1 V_{DDR} — Regulator Power Input

Signal V_{DDR} is the power input of VREG3V3. All currents sourced into the regulator loads flow through this pin. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDR} and V_{SSR} can smoothen ripple on V_{DDR}.

For entering Shutdown Mode, pin V_{DDR} should also be tied to ground on devices without a V_{REGEN} pin.

17.2.2 V_{DDA}, V_{SSA} — Regulator Reference Supply

Signals V_{DDA}/V_{SSA} which are supposed to be relatively quiet are used to supply the analog parts of the regulator. Internal precision reference circuits are supplied from these signals. A chip external decoupling capacitor (100 nF...220 nF, X7R ceramic) between V_{DDA} and V_{SSA} can further improve the quality of this supply.

17.2.3 V_{DD}, V_{SS} — Regulator Output1 (Core Logic)

Signals V_{DD}/V_{SS} are the primary outputs of VREG3V3 that provide the power supply for the core logic. These signals are connected to device pins to allow external decoupling capacitors (100 nF...220 nF, X7R ceramic).

In Shutdown Mode an external supply at V_{DD}/V_{SS} can replace the voltage regulator.

17.2.4 V_{DDPLL}, V_{SSPLL} — Regulator Output2 (PLL)

Signals V_{DDPLL}/V_{SSPLL} are the secondary outputs of VREG3V3 that provide the power supply for the PLL and oscillator. These signals are connected to device pins to allow external decoupling capacitors (100 nF...220 nF, X7R ceramic).

In Shutdown Mode an external supply at V_{DDPLL}/V_{SSPLL} can replace the voltage regulator.

17.2.5 V_{REGEN} — Optional Regulator Enable

This optional signal is used to shutdown VREG3V3. In that case V_{DD}/V_{SS} and V_{DDPLL}/V_{SSPLL} must be provided externally. Shutdown Mode is entered with V_{REGEN} being low. If V_{REGEN} is high, the VREG3V3 is either in Full Performance Mode or in Reduced Power Mode.

For the connectivity of V_{REGEN} see device overview chapter.

NOTE

Switching from FPM or RPM to shutdown of VREG3V3 and vice versa is not supported while the MCU is powered.

17.3 Memory Map and Register Definition

This subsection provides a detailed description of all registers accessible in VREG3V3.

17.3.1 Module Memory Map

Figure 17-2 provides an overview of all used registers.

Table 17-2. VREG3V3 Memory Map

Address Offset	Use	Access
0x0000	VREG3V3 Control Register (VREGCTRL)	R/W

17.3.2 Register Descriptions

The following paragraphs describe, in address order, all the VREG3V3 registers and their individual bits.

17.3.2.1 VREG3V3 — Control Register (VREGCTRL)

The VREGCTRL register allows to separately enable features of VREG3V3.

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	LVDS	LVIE	LVIF
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 17-2. VREG3V3 — Control Register (VREGCTRL)

Table 17-3. MCCTL1 Field Descriptions

Field	Description
2 LVDS	**Low-Voltage Detect Status Bit** — This read-only status bit reflects the input voltage. Writes have no effect. 0 Input voltage V_{DDA} is above level V_{LVID} or RPM or shutdown mode. 1 Input voltage V_{DDA} is below level V_{LVIA} and FPM.
1 LVIE	**Low-Voltage Interrupt Enable Bit** 0 Interrupt request is disabled. 1 Interrupt will be requested whenever LVIF is set.
0 LVIF	**Low-Voltage Interrupt Flag** — LVIF is set to 1 when LVDS status bit changes. This flag can only be cleared by writing a 1. Writing a 0 has no effect. If enabled (LVIE = 1), LVIF causes an interrupt request. 0 No change in LVDS bit. 1 LVDS bit has changed.

NOTE

On entering the Reduced Power Mode the LVIF is not cleared by the VREG3V3.

17.4 Functional Description

Block VREG3V3 is a voltage regulator as depicted in Figure 17-1. The regulator functional elements are the regulator core (REG), a low-voltage detect module (LVD), a power-on reset module (POR) and a low-voltage reset module (LVR). There is also the regulator control block (CTRL) which represents the interface to the digital core logic but also manages the operating modes of VREG3V3.

17.4.1 REG — Regulator Core

VREG3V3, respectively its regulator core has two parallel, independent regulation loops (REG1 and REG2) that differ only in the amount of current that can be sourced to the connected loads. Therefore, only REG1 providing the supply at V_{DD}/V_{SS} is explained. The principle is also valid for REG2.

The regulator is a linear series regulator with a bandgap reference in its Full Performance Mode and a voltage clamp in Reduced Power Mode. All load currents flow from input V_{DDR} to V_{SS} or V_{SSPLL}, the reference circuits are connected to V_{DDA} and V_{SSA}.

17.4.2 Full-Performance Mode

In Full Performance Mode, a fraction of the output voltage (V_{DD}) and the bandgap reference voltage are fed to an operational amplifier. The amplified input voltage difference controls the gate of an output driver which basically is a large NMOS transistor connected to the output.

17.4.3 Reduced-Power Mode

In Reduced Power Mode, the driver gate is connected to a buffered fraction of the input voltage (V_{DDR}). The operational amplifier and the bandgap are disabled to reduce power consumption.

17.4.4 LVD — Low-Voltage Detect

sub-block LVD is responsible for generating the low-voltage interrupt (LVI). LVD monitors the input voltage (V_{DDA}–V_{SSA}) and continuously updates the status flag LVDS. Interrupt flag LVIF is set whenever status flag LVDS changes its value. The LVD is available in FPM and is inactive in Reduced Power Mode and Shutdown Mode.

17.4.5 POR — Power-On Reset

This functional block monitors output V_{DD}. If V_{DD} is below V_{PORD}, signal POR is high, if it exceeds V_{PORD}, the signal goes low. The transition to low forces the CPU in the power-on sequence.

Due to its role during chip power-up this module must be active in all operating modes of VREG3V3.

17.4.6 LVR — Low-Voltage Reset

Block LVR monitors the primary output voltage V_{DD}. If it drops below the assertion level (V_{LVRA}) signal LVR asserts and when rising above the deassertion level (V_{LVRD}) signal LVR negates again. The LVR function is available only in Full Performance Mode.

17.4.7 CTRL — Regulator Control

This part contains the register block of VREG3V3 and further digital functionality needed to control the operating modes. CTRL also represents the interface to the digital core logic.

17.5 Resets

This subsection describes how VREG3V3 controls the reset of the MCU.The reset values of registers and signals are provided in Section 17.3, “Memory Map and Register Definition”. Possible reset sources are listed in Table 17-4.

Table 17-4. VREG3V3 — Reset Sources

Reset Source	Local Enable
Power-on reset	Always active
Low-voltage reset	Available only in Full Performance Mode

17.5.1 Power-On Reset

During chip power-up the digital core may not work if its supply voltage V_{DD} is below the POR deassertion level (V_{PORD}). Therefore, signal POR which forces the other blocks of the device into reset is kept high until V_{DD} exceeds V_{PORD}. Then POR becomes low and the reset generator of the device continues the start-up sequence. The power-on reset is active in all operation modes of VREG3V3.

17.5.2 Low-Voltage Reset

For details on low-voltage reset see Section 17.4.6, “LVR — Low-Voltage Reset”.

17.6 Interrupts

This subsection describes all interrupts originated by VREG3V3.

The interrupt vectors requested by VREG3V3 are listed in Table 17-5. Vector addresses and interrupt priorities are defined at MCU level.

Table 17-5. VREG3V3 — Interrupt Vectors

Interrupt Source	Local Enable
Low Voltage Interrupt (LVI)	LVIE = 1; Available only in Full Performance Mode

17.6.1 LVI — Low-Voltage Interrupt

In FPM VREG3V3 monitors the input voltage V_{DDA}. Whenever V_{DDA} drops below level V_{LVIA} the status bit LVDS is set to 1. Vice versa, LVDS is reset to 0 when V_{DDA} rises above level V_{LVID}. An interrupt, indicated by flag LVIF = 1, is triggered by any change of the status bit LVDS if interrupt enable bit LVIE = 1.

NOTE

On entering the Reduced Power Mode, the LVIF is not cleared by the VREG3V3.

Chapter 18
Background Debug Module (BDMV4)

18.1 Introduction

This section describes the functionality of the background debug module (BDM) sub-block of the HCS12 core platform.

A block diagram of the BDM is shown in Figure 18-1.

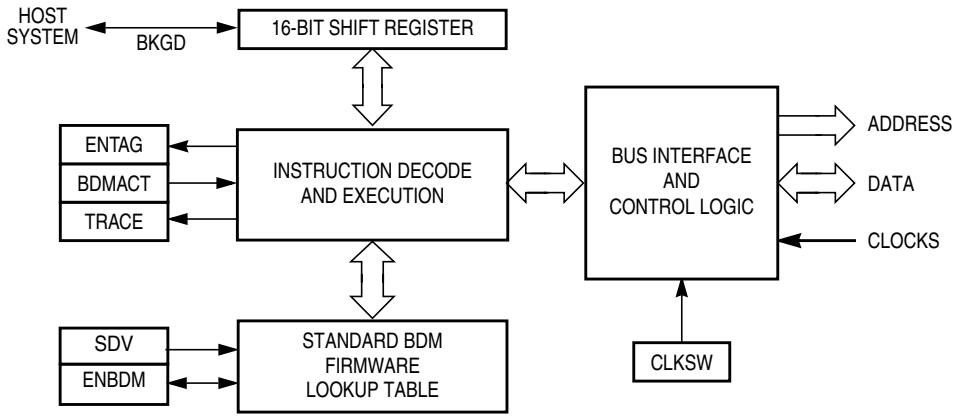


Figure 18-1. BDM Block Diagram

The background debug module (BDM) sub-block is a single-wire, background debug system implemented in on-chip hardware for minimal CPU intervention. All interfacing with the BDM is done via the BKGD pin.

BDMV4 has enhanced capability for maintaining synchronization between the target and host while allowing more flexibility in clock rates. This includes a sync signal to show the clock rate and a handshake signal to indicate when an operation is complete. The system is backwards compatible with older external interfaces.

18.1.1 Features

- Single-wire communication with host development system
- BDMV4 (and BDM2): Enhanced capability for allowing more flexibility in clock rates
- BDMV4: SYNC command to determine communication rate
- BDMV4: GO_UNTIL command
- BDMV4: Hardware handshake protocol to increase the performance of the serial communication
- Active out of reset in special single-chip mode

- Nine hardware commands using free cycles, if available, for minimal CPU intervention
- Hardware commands not requiring active BDM
- 15 firmware commands execute from the standard BDM firmware lookup table
- Instruction tagging capability
- Software control of BDM operation during wait mode
- Software selectable clocks
- When secured, hardware commands are allowed to access the register space in special single-chip mode, if the FLASH and EEPROM erase tests fail.

18.1.2 Modes of Operation

BDM is available in all operating modes but must be enabled before firmware commands are executed. Some system peripherals may have a control bit which allows suspending the peripheral function during background debug mode.

18.1.2.1 Regular Run Modes

All of these operations refer to the part in run mode. The BDM does not provide controls to conserve power during run mode.

- Normal operation

  General operation of the BDM is available and operates the same in all normal modes.
- Special single-chip mode

  In special single-chip mode, background operation is enabled and active out of reset. This allows programming a system with blank memory.
- Special peripheral mode

  BDM is enabled and active immediately out of reset. BDM can be disabled by clearing the BDMACT bit in the BDM status (BDMSTS) register. The BDM serial system should not be used in special peripheral mode.
- Emulation modes

  General operation of the BDM is available and operates the same as in normal modes.

18.1.2.2 Secure Mode Operation

If the part is in secure mode, the operation of the BDM is reduced to a small subset of its regular run mode operation. Secure operation prevents access to FLASH or EEPROM other than allowing erasure.

18.2 External Signal Description

A single-wire interface pin is used to communicate with the BDM system. Two additional pins are used for instruction tagging. These pins are part of the multiplexed external bus interface (MEBI) sub-block and all interfacing between the MEBI and BDM is done within the core interface boundary. Functional descriptions of the pins are provided below for completeness.

- BKGD — Background interface pin
- $\overline{\text{TAGHI}}$ — High byte instruction tagging pin
- $\overline{\text{TAGLO}}$ — Low byte instruction tagging pin
- BKGD and $\overline{\text{TAGHI}}$ share the same pin.
- $\overline{\text{TAGLO}}$ and $\overline{\text{LSTRB}}$ share the same pin.

NOTE

Generally these pins are shared as described, but it is best to check the device overview chapter to make certain. All MCUs at the time of this writing have followed this pin sharing scheme.

18.2.1 BKGD — Background Interface Pin

Debugging control logic communicates with external devices serially via the single-wire background interface pin (BKGD). During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the background debug mode.

18.2.2 $\overline{\text{TAGHI}}$ — High Byte Instruction Tagging Pin

This pin is used to tag the high byte of an instruction. When instruction tagging is on, a logic 0 at the falling edge of the external clock (ECLK) tags the high half of the instruction word being read into the instruction queue.

18.2.3 $\overline{\text{TAGLO}}$ — Low Byte Instruction Tagging Pin

This pin is used to tag the low byte of an instruction. When instruction tagging is on and low strobe is enabled, a logic 0 at the falling edge of the external clock (ECLK) tags the low half of the instruction word being read into the instruction queue.

18.3 Memory Map and Register Definition

A summary of the registers associated with the BDM is shown in Figure 18-2. Registers are accessed by host-driven communications to the BDM hardware using READ_BD and WRITE_BD commands. Detailed descriptions of the registers and associated bits are given in the subsections that follow.

18.3.1 Module Memory Map

Table 18-1. INT Memory Map

Register Address	Use	Access
	Reserved	—
	BDM Status Register (BDMSTS)	R/W
	Reserved	—
	BDM CCR Holding Register (BDMCCR)	R/W
7	BDM Internal Register Position (BDMINR)	R
8–	Reserved	—

18.3.2 Register Descriptions

Register Name		Bit 7	6	5	4	3	2	1	Bit 0
Reserved	R	X	X	X	X	X	X	0	0
	W								
BDMSTS	R	ENBDM	BDMACT	ENTAG	SDV	TRACE	CLKSW	UNSEC	0
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								
BDMCCR	R	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
	W								
BDMINR	R	0	REG14	REG13	REG12	REG11	0	0	0
	W								
Reserved	R	0	0	0	0	0	0	0	0
	W								
Reserved	R	0	0	0	0	0	0	0	0
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								
Reserved	R	X	X	X	X	X	X	X	X
	W								

	= Unimplemented, Reserved		= Implemented (do not alter)
X	= Indeterminate	0	= Always read zero

Figure 18-2. BDM Register Summary

18.3.2.1 BDM Status Register (BDMSTS)

	7	6	5	4	3	2	1	0
R	ENBDM	BDMACT	ENTAG	SDV	TRACE	CLKSW	UNSEC	0
W								
Reset:								
Special single-chip mode:	1[1]	1	0	0	0	0	0[2]	0
Special peripheral mode:	0	1	0	0	0	0	0	0
All other modes:	0	1	0	0	0	0	0	0
	0	0	0	0	0	0	0	0

= Unimplemented or Reserved = Implemented (do not alter)

Figure 18-3. BDM Status Register (BDMSTS)

Note:

1 ENBDM is read as "1" by a debugging environment in Special single-chip mode when the device is not secured or secured but fully erased (Flash and EEPROM).This is because the ENBDM bit is set by the standard firmware before a BDM command can be fully transmitted and executed.

2 UNSEC is read as "1" by a debugging environment in Special single-chip mode when the device is secured and fully erased, else it is "0" and can only be read if not secure (see also bit description).

Read: All modes through BDM operation

Write: All modes but subject to the following:

- BDMACT can only be set by BDM hardware upon entry into BDM. It can only be cleared by the standard BDM firmware lookup table upon exit from BDM active mode.
- CLKSW can only be written via BDM hardware or standard BDM firmware write commands.
- All other bits, while writable via BDM hardware or standard BDM firmware write commands, should only be altered by the BDM hardware or standard firmware lookup table as part of BDM command execution.
- ENBDM should only be set via a BDM hardware command if the BDM firmware commands are needed. (This does not apply in special single-chip mode).

Table 18-2. BDMSTS Field Descriptions

Field	Description
7 ENBDM	**Enable BDM** — This bit controls whether the BDM is enabled or disabled. When enabled, BDM can be made active to allow firmware commands to be executed. When disabled, BDM cannot be made active but BDM hardware commands are allowed. 0 BDM disabled 1 BDM enabled **Note:** ENBDM is set by the firmware immediately out of reset in special single-chip mode. In secure mode, this bit will not be set by the firmware until after the EEPROM and FLASH erase verify tests are complete.
6 BDMACT	**BDM Active Status** — This bit becomes set upon entering BDM. The standard BDM firmware lookup table is then enabled and put into the memory map. BDMACT is cleared by a carefully timed store instruction in the standard BDM firmware as part of the exit sequence to return to user code and remove the BDM memory from the map. 0 BDM not active 1 BDM active

Table 18-2. BDMSTS Field Descriptions (continued)

Field	Description
5 ENTAG	**Tagging Enable** — This bit indicates whether instruction tagging in enabled or disabled. It is set when the TAGGO command is executed and cleared when BDM is entered. The serial system is disabled and the tag function enabled 16 cycles after this bit is written. BDM cannot process serial commands while tagging is active. 0 Tagging not enabled or BDM active 1 Tagging enabled
4 SDV	**Shift Data Valid** — This bit is set and cleared by the BDM hardware. It is set after data has been transmitted as part of a firmware read command or after data has been received as part of a firmware write command. It is cleared when the next BDM command has been received or BDM is exited. SDV is used by the standard BDM firmware to control program flow execution. 0 Data phase of command not complete 1 Data phase of command is complete
3 TRACE	**TRACE1 BDM Firmware Command is Being Executed** — This bit gets set when a BDM TRACE1 firmware command is first recognized. It will stay set as long as continuous back-to-back TRACE1 commands are executed. This bit will get cleared when the next command that is not a TRACE1 command is recognized. 0 TRACE1 command is not being executed 1 TRACE1 command is being executed
2 CLKSW	**Clock Switch** — The CLKSW bit controls which clock the BDM operates with. It is only writable from a hardware BDM command. A 150 cycle delay at the clock speed that is active during the data portion of the command will occur before the new clock source is guaranteed to be active. The start of the next BDM command uses the new clock for timing subsequent BDM communications. Table 18-3 shows the resulting BDM clock source based on the CLKSW and the PLLSEL (Pll select from the clock and reset generator) bits. **Note:** The BDM alternate clock source can only be selected when CLKSW = 0 and PLLSEL = 1. The BDM serial interface is now fully synchronized to the alternate clock source, when enabled. This eliminates frequency restriction on the alternate clock which was required on previous versions. Refer to the device overview section to determine which clock connects to the alternate clock source input. **Note:** If the acknowledge function is turned on, changing the CLKSW bit will cause the ACK to be at the new rate for the write command which changes it.
1 UNSEC	**Unsecure** — This bit is only writable in special single-chip mode from the BDM secure firmware and always gets reset to zero. It is in a zero state as secure mode is entered so that the secure BDM firmware lookup table is enabled and put into the memory map along with the standard BDM firmware lookup table. The secure BDM firmware lookup table verifies that the on-chip EEPROM and FLASH EEPROM are erased. This being the case, the UNSEC bit is set and the BDM program jumps to the start of the standard BDM firmware lookup table and the secure BDM firmware lookup table is turned off. If the erase test fails, the UNSEC bit will not be asserted. 0 System is in a secured mode 1 System is in a unsecured mode **Note:** When UNSEC is set, security is off and the user can change the state of the secure bits in the on-chip FLASH EEPROM. Note that if the user does not change the state of the bits to “unsecured” mode, the system will be secured again when it is next taken out of reset.

Table 18-3. BDM Clock Sources

PLLSEL	CLKSW	BDMCLK
0	0	Bus clock
0	1	Bus clock

Table 18-3. BDM Clock Sources

PLLSEL	CLKSW	BDMCLK
1	0	Alternate clock (refer to the device overview chapter to determine the alternate clock source)
1	1	Bus clock dependent on the PLL

18.3.2.2 BDM CCR Holding Register (BDMCCR)

	7	6	5	4	3	2	1	0
R W	CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
Reset	0	0	0	0	0	0	0	0

Figure 18-4. BDM CCR Holding Register (BDMCCR)

Read: All modes

Write: All modes

NOTE

When BDM is made active, the CPU stores the value of the CCR register in the BDMCCR register. However, out of special single-chip reset, the BDMCCR is set to 0xD8 and not 0xD0 which is the reset value of the CCR register.

When entering background debug mode, the BDM CCR holding register is used to save the contents of the condition code register of the user's program. It is also used for temporary storage in the standard BDM firmware mode. The BDM CCR holding register can be written to modify the CCR value.

18.3.2.3 BDM Internal Register Position Register (BDMINR)

	7	6	5	4	3	2	1	0
R	0	REG14	REG13	REG12	REG11	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 18-5. BDM Internal Register Position (BDMINR)

Read: All modes

Write: Never

Table 18-4. BDMINR Field Descriptions

Field	Description
6:3 REG[14:11]	**Internal Register Map Position** — These four bits show the state of the upper five bits of the base address for the system's relocatable register block. BDMINR is a shadow of the INITRG register which maps the register block to any 2K byte space within the first 32K bytes of the 64K byte address space.

18.4 Functional Description

The BDM receives and executes commands from a host via a single wire serial interface. There are two types of BDM commands, namely, hardware commands and firmware commands.

Hardware commands are used to read and write target system memory locations and to enter active background debug mode, see Section 18.4.3, “BDM Hardware Commands.” Target system memory includes all memory that is accessible by the CPU.

Firmware commands are used to read and write CPU resources and to exit from active background debug mode, see Section 18.4.4, “Standard BDM Firmware Commands.” The CPU resources referred to are the accumulator (D), X index register (X), Y index register (Y), stack pointer (SP), and program counter (PC).

Hardware commands can be executed at any time and in any mode excluding a few exceptions as highlighted, see Section 18.4.3, “BDM Hardware Commands.” Firmware commands can only be executed when the system is in active background debug mode (BDM).

18.4.1 Security

If the user resets into special single-chip mode with the system secured, a secured mode BDM firmware lookup table is brought into the map overlapping a portion of the standard BDM firmware lookup table. The secure BDM firmware verifies that the on-chip EEPROM and FLASH EEPROM are erased. This being the case, the UNSEC bit will get set. The BDM program jumps to the start of the standard BDM firmware and the secured mode BDM firmware is turned off and all BDM commands are allowed. If the EEPROM or FLASH do not verify as erased, the BDM firmware sets the ENBDM bit, without asserting UNSEC, and the firmware enters a loop. This causes the BDM hardware commands to become enabled, but does not enable the firmware commands. This allows the BDM hardware to be used to erase the EEPROM and FLASH. After execution of the secure firmware, regardless of the results of the erase tests, the CPU registers, INITEE and PPAGE, will no longer be in their reset state.

18.4.2 Enabling and Activating BDM

The system must be in active BDM to execute standard BDM firmware commands. BDM can be activated only after being enabled. BDM is enabled by setting the ENBDM bit in the BDM status (BDMSTS) register. The ENBDM bit is set by writing to the BDM status (BDMSTS) register, via the single-wire interface, using a hardware command such as WRITE_BD_BYTE.

After being enabled, BDM is activated by one of the following[1]:

- Hardware BACKGROUND command
- BDM external instruction tagging mechanism
- CPU BGND instruction
- Breakpoint sub-block’s force or tag mechanism[2]

When BDM is activated, the CPU finishes executing the current instruction and then begins executing the firmware in the standard BDM firmware lookup table. When BDM is activated by the breakpoint

1. BDM is enabled and active immediately out of special single-chip reset.
2. This method is only available on systems that have a a breakpoint or a debug sub-block.

sub-block, the type of breakpoint used determines if BDM becomes active before or after execution of the next instruction.

NOTE

If an attempt is made to activate BDM before being enabled, the CPU resumes normal instruction execution after a brief delay. If BDM is not enabled, any hardware BACKGROUND commands issued are ignored by the BDM and the CPU is not delayed.

In active BDM, the BDM registers and standard BDM firmware lookup table are mapped to addresses 0xFF00 to 0xFFFF. BDM registers are mapped to addresses 0xFF00 to 0xFF07. The BDM uses these registers which are readable anytime by the BDM. However, these registers are not readable by user programs.

18.4.3 BDM Hardware Commands

Hardware commands are used to read and write target system memory locations and to enter active background debug mode. Target system memory includes all memory that is accessible by the CPU such as on-chip RAM, EEPROM, FLASH EEPROM, I/O and control registers, and all external memory.

Hardware commands are executed with minimal or no CPU intervention and do not require the system to be in active BDM for execution, although they can continue to be executed in this mode. When executing a hardware command, the BDM sub-block waits for a free CPU bus cycle so that the background access does not disturb the running application program. If a free cycle is not found within 128 clock cycles, the CPU is momentarily frozen so that the BDM can steal a cycle. When the BDM finds a free cycle, the operation does not intrude on normal CPU operation provided that it can be completed in a single cycle. However, if an operation requires multiple cycles the CPU is frozen until the operation is complete, even though the BDM found a free cycle.

The BDM hardware commands are listed in Table 18-5.

Table 18-5. Hardware Commands

Command	Opcode (hex)	Data	Description
BACKGROUND	90	None	Enter background mode if firmware is enabled. If enabled, an ACK will be issued when the part enters active background mode.
ACK_ENABLE	D5	None	Enable handshake. Issues an ACK pulse after the command is executed.
ACK_DISABLE	D6	None	Disable handshake. This command does not issue an ACK pulse.
READ_BD_BYTE	E4	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
READ_BD_WORD	EC	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table in map. Must be aligned access.
READ_BYTE	E0	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
READ_WORD	E8	16-bit address 16-bit data out	Read from memory with standard BDM firmware lookup table out of map. Must be aligned access.
WRITE_BD_BYTE	C4	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Odd address data on low byte; even address data on high byte.
WRITE_BD_WORD	CC	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table in map. Must be aligned access.
WRITE_BYTE	C0	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Odd address data on low byte; even address data on high byte.
WRITE_WORD	C8	16-bit address 16-bit data in	Write to memory with standard BDM firmware lookup table out of map. Must be aligned access.

NOTE:
If enabled, ACK will occur when data is ready for transmission for all BDM READ commands and will occur after the write is complete for all BDM WRITE commands.

The READ_BD and WRITE_BD commands allow access to the BDM register locations. These locations are not normally in the system memory map but share addresses with the application in memory. To distinguish between physical memory locations that share the same address, BDM memory resources are enabled just for the READ_BD and WRITE_BD access cycle. This allows the BDM to access BDM locations unobtrusively, even if the addresses conflict with the application memory map.

18.4.4 Standard BDM Firmware Commands

Firmware commands are used to access and manipulate CPU resources. The system must be in active BDM to execute standard BDM firmware commands, see Section 18.4.2, “Enabling and Activating BDM.” Normal instruction execution is suspended while the CPU executes the firmware located in the standard BDM firmware lookup table. The hardware command BACKGROUND is the usual way to activate BDM.

As the system enters active BDM, the standard BDM firmware lookup table and BDM registers become visible in the on-chip memory map at 0xFF00–0xFFFF, and the CPU begins executing the standard BDM

firmware. The standard BDM firmware watches for serial commands and executes them as they are received.

The firmware commands are shown in Table 18-6.

Table 18-6. Firmware Commands

Command[1]	Opcode (hex)	Data	Description
READ_NEXT	62	16-bit data out	Increment X by 2 (X = X + 2), then read word X points to.
READ_PC	63	16-bit data out	Read program counter.
READ_D	64	16-bit data out	Read D accumulator.
READ_X	65	16-bit data out	Read X index register.
READ_Y	66	16-bit data out	Read Y index register.
READ_SP	67	16-bit data out	Read stack pointer.
WRITE_NEXT	42	16-bit data in	Increment X by 2 (X = X + 2), then write word to location pointed to by X.
WRITE_PC	43	16-bit data in	Write program counter.
WRITE_D	44	16-bit data in	Write D accumulator.
WRITE_X	45	16-bit data in	Write X index register.
WRITE_Y	46	16-bit data in	Write Y index register.
WRITE_SP	47	16-bit data in	Write stack pointer.
GO	08	None	Go to user program. If enabled, ACK will occur when leaving active background mode.
GO_UNTIL[2]	0C	None	Go to user program. If enabled, ACK will occur upon returning to active background mode.
TRACE1	10	None	Execute one user instruction then return to active BDM. If enabled, ACK will occur upon returning to active background mode.
TAGGO	18	None	Enable tagging and go to user program. There is no ACK pulse related to this command.

1 If enabled, ACK will occur when data is ready for transmission for all BDM READ commands and will occur after the write is complete for all BDM WRITE commands.

2 Both WAIT (with clocks to the S12 CPU core disabled) and STOP disable the ACK function. The GO_UNTIL command will not get an Acknowledge if one of these two CPU instructions occurs before the “UNTIL” instruction. This can be a problem for any instruction that uses ACK, but GO_UNTIL is a lot more difficult for the development tool to time-out.

18.4.5 BDM Command Structure

Hardware and firmware BDM commands start with an 8-bit opcode followed by a 16-bit address and/or a 16-bit data word depending on the command. All the read commands return 16 bits of data despite the byte or word implication in the command name.

NOTE

8-bit reads return 16-bits of data, of which, only one byte will contain valid data. If reading an even address, the valid data will appear in the MSB. If reading an odd address, the valid data will appear in the LSB.

NOTE

16-bit misaligned reads and writes are not allowed. If attempted, the BDM will ignore the least significant bit of the address and will assume an even address from the remaining bits.

For hardware data read commands, the external host must wait 150 bus clock cycles after sending the address before attempting to obtain the read data. This is to be certain that valid data is available in the BDM shift register, ready to be shifted out. For hardware write commands, the external host must wait 150 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed. The 150 bus clock cycle delay in both cases includes the maximum 128 cycle delay that can be incurred as the BDM waits for a free cycle before stealing a cycle.

For firmware read commands, the external host should wait 44 bus clock cycles after sending the command opcode and before attempting to obtain the read data. This includes the potential of an extra 7 cycles when the access is external with a narrow bus access (+1 cycle) and / or a stretch (+1, 2, or 3 cycles), (7 cycles could be needed if both occur). The 44 cycle wait allows enough time for the requested data to be made available in the BDM shift register, ready to be shifted out.

NOTE

This timing has increased from previous BDM modules due to the new capability in which the BDM serial interface can potentially run faster than the bus. On previous BDM modules this extra time could be hidden within the serial time.

For firmware write commands, the external host must wait 32 bus clock cycles after sending the data to be written before attempting to send a new command. This is to avoid disturbing the BDM shift register before the write has been completed.

The external host should wait 64 bus clock cycles after a TRACE1 or GO command before starting any new serial command. This is to allow the CPU to exit gracefully from the standard BDM firmware lookup table and resume execution of the user code. Disturbing the BDM shift register prematurely may adversely affect the exit from the standard BDM firmware lookup table.

NOTE

If the bus rate of the target processor is unknown or could be changing, it is recommended that the ACK (acknowledge function) be used to indicate when an operation is complete. When using ACK, the delay times are automated.

Figure 18-6 represents the BDM command structure. The command blocks illustrate a series of eight bit times starting with a falling edge. The bar across the top of the blocks indicates that the BKGD line idles in the high state. The time for an 8-bit command is 8×16 target clock cycles.[1]

1. Target clock cycles are cycles measured using the target MCU's serial clock rate. See Section 18.4.6, "BDM Serial Interface," and Section 18.3.2.1, "BDM Status Register (BDMSTS)," for information on how serial clock rate is selected.

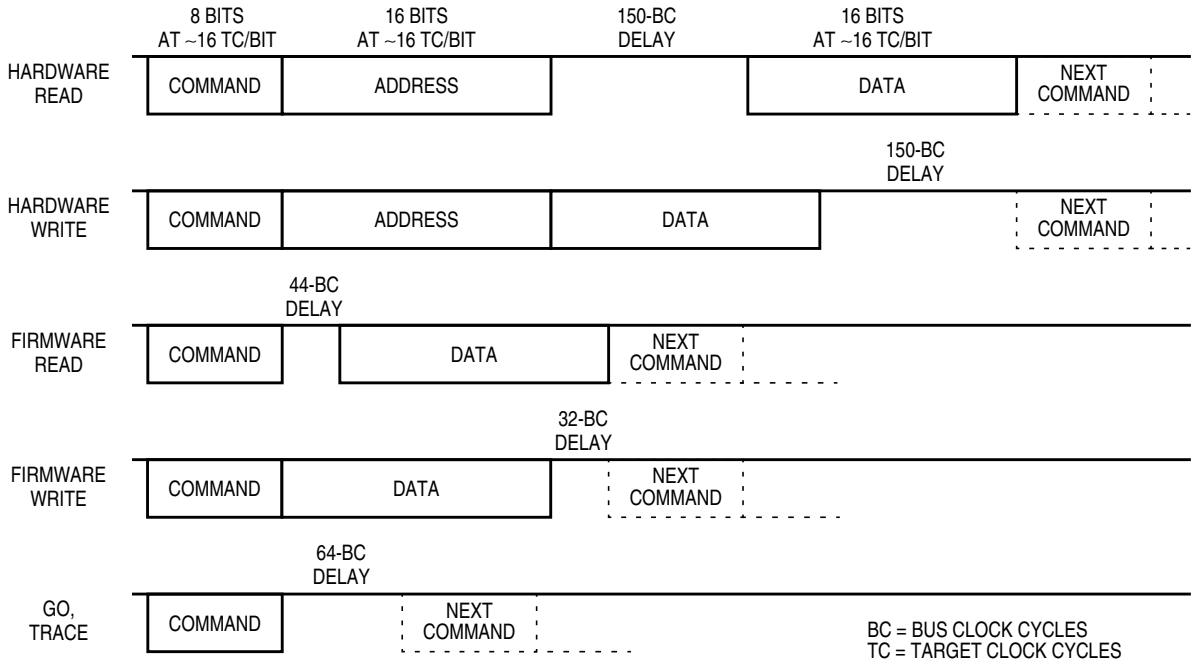


Figure 18-6. BDM Command Structure

18.4.6 BDM Serial Interface

The BDM communicates with external devices serially via the BKGD pin. During reset, this pin is a mode select input which selects between normal and special modes of operation. After reset, this pin becomes the dedicated serial interface pin for the BDM.

The BDM serial interface is timed using the clock selected by the CLKSW bit in the status register see Section 18.3.2.1, “BDM Status Register (BDMSTS).” This clock will be referred to as the target clock in the following explanation.

The BDM serial interface uses a clocking scheme in which the external host generates a falling edge on the BKGD pin to indicate the start of each bit time. This falling edge is sent for every bit whether data is transmitted or received. Data is transferred most significant bit (MSB) first at 16 target clock cycles per bit. The interface times out if 512 clock cycles occur between falling edges from the host.

The BKGD pin is a pseudo open-drain pin and has an weak on-chip active pull-up that is enabled at all times. It is assumed that there is an external pull-up and that drivers connected to BKGD do not typically drive the high level. Because R-C rise time could be unacceptably long, the target system and host provide brief driven-high (speedup) pulses to drive BKGD to a logic 1. The source of this speedup pulse is the host for transmit cases and the target for receive cases.

The timing for host-to-target is shown in Figure 18-7 and that of target-to-host in Figure 18-8 and Figure 18-9. All four cases begin when the host drives the BKGD pin low to generate a falling edge. Because the host and target are operating from separate clocks, it can take the target system up to one full clock cycle to recognize this edge. The target measures delays from this perceived start of the bit time while the host measures delays from the point it actually drove BKGD low to start the bit up to one target

clock cycle earlier. Synchronization between the host and target is established in this manner at the start of every bit time.

Figure 18-7 shows an external host transmitting a logic 1 and transmitting a logic 0 to the BKGD pin of a target system. The host is asynchronous to the target, so there is up to a one clock-cycle delay from the host-generated falling edge to where the target recognizes this edge as the beginning of the bit time. Ten target clock cycles later, the target senses the bit level on the BKGD pin. Internal glitch detect logic requires the pin be driven high no later that eight target clock cycles after the falling edge for a logic 1 transmission.

Because the host drives the high speedup pulses in these two cases, the rising edges look like digitally driven signals.

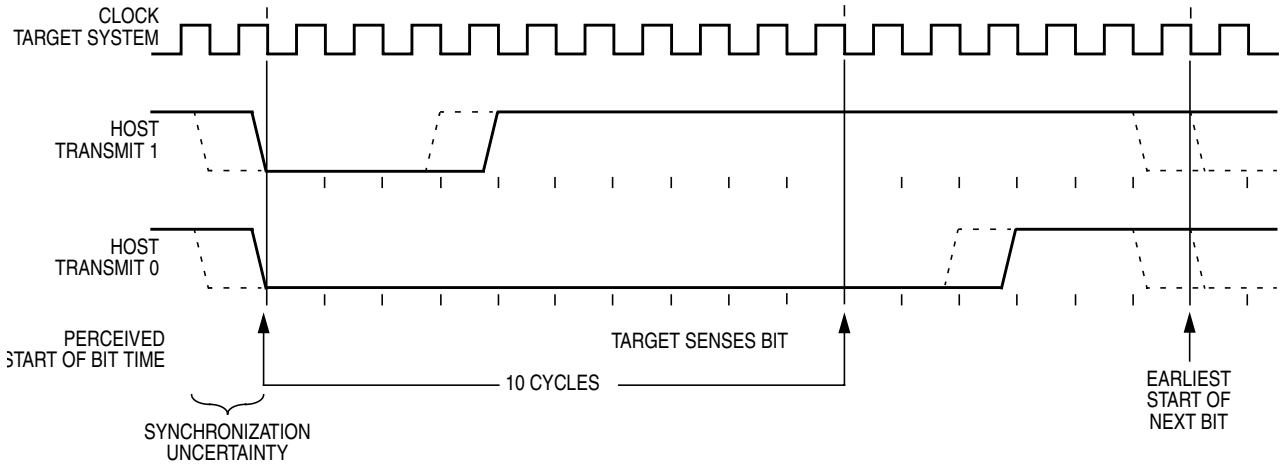


Figure 18-7. BDM Host-to-Target Serial Bit Timing

The receive cases are more complicated. Figure 18-8 shows the host receiving a logic 1 from the target system. Because the host is asynchronous to the target, there is up to one clock-cycle delay from the host-generated falling edge on BKGD to the perceived start of the bit time in the target. The host holds the BKGD pin low long enough for the target to recognize it (at least two target clock cycles). The host must release the low drive before the target drives a brief high speedup pulse seven target clock cycles after the perceived start of the bit time. The host should sample the bit level about 10 target clock cycles after it started the bit time.

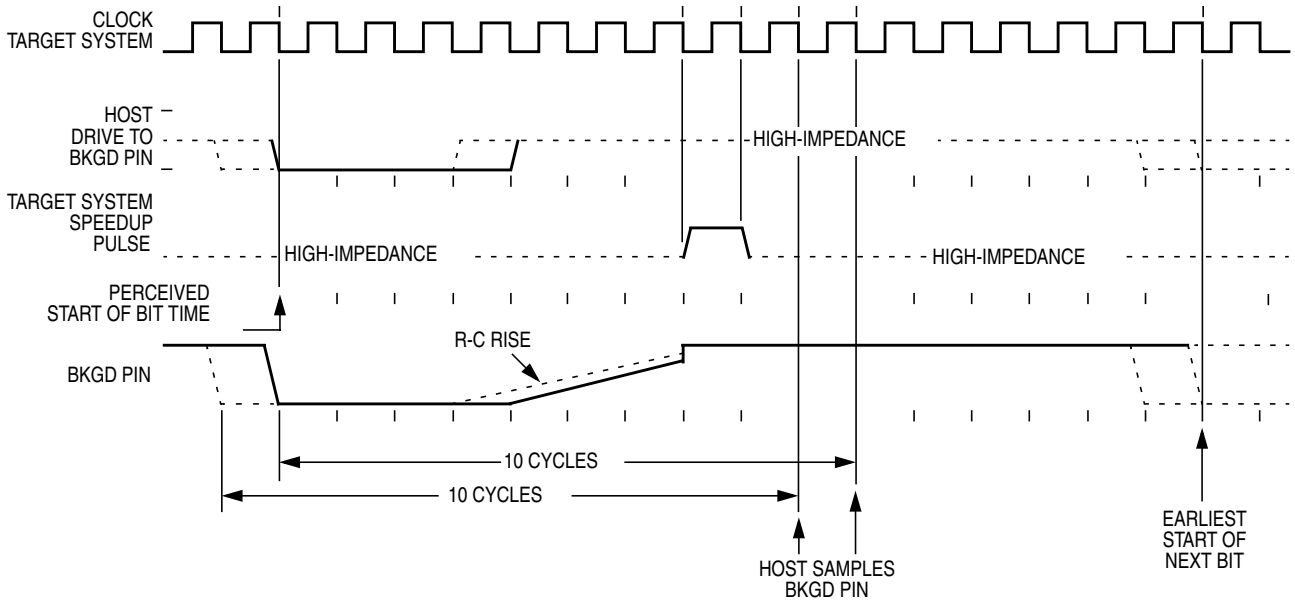


Figure 18-8. BDM Target-to-Host Serial Bit Timing (Logic 1)

Figure 18-9 shows the host receiving a logic 0 from the target. Because the host is asynchronous to the target, there is up to a one clock-cycle delay from the host-generated falling edge on BKGD to the start of the bit time as perceived by the target. The host initiates the bit time but the target finishes it. Because the target wants the host to receive a logic 0, it drives the BKGD pin low for 13 target clock cycles then briefly drives it high to speed up the rising edge. The host samples the bit level about 10 target clock cycles after starting the bit time.

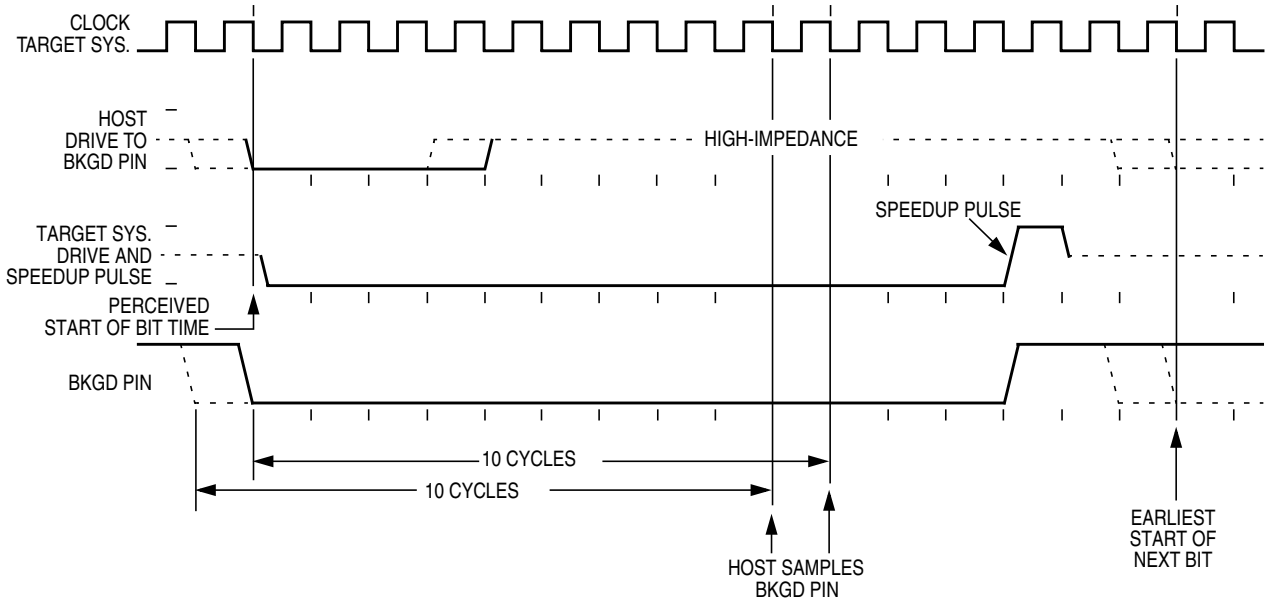


Figure 18-9. BDM Target-to-Host Serial Bit Timing (Logic 0)

18.4.7 Serial Interface Hardware Handshake Protocol

BDM commands that require CPU execution are ultimately treated at the MCU bus rate. Because the BDM clock source can be asynchronously related to the bus frequency, when CLKSW = 0, it is very helpful to provide a handshake protocol in which the host could determine when an issued command is executed by the CPU. The alternative is to always wait the amount of time equal to the appropriate number of cycles at the slowest possible rate the clock could be running. This sub-section will describe the hardware handshake protocol.

The hardware handshake protocol signals to the host controller when an issued command was successfully executed by the target. This protocol is implemented by a 16 serial clock cycle low pulse followed by a brief speedup pulse in the BKGD pin. This pulse is generated by the target MCU when a command, issued by the host, has been successfully executed (see Figure 18-10). This pulse is referred to as the ACK pulse. After the ACK pulse has finished: the host can start the bit retrieval if the last issued command was a read command, or start a new command if the last command was a write command or a control command (BACKGROUND, GO, GO_UNTIL, or TRACE1). The ACK pulse is not issued earlier than 32 serial clock cycles after the BDM command was issued. The end of the BDM command is assumed to be the 16th tick of the last bit. This minimum delay assures enough time for the host to perceive the ACK pulse. Note also that, there is no upper limit for the delay between the command and the related ACK pulse, because the command execution depends upon the CPU bus frequency, which in some cases could be very slow compared to the serial communication rate. This protocol allows a great flexibility for the POD designers, because it does not rely on any accurate time measurement or short response time to any event in the serial communication.

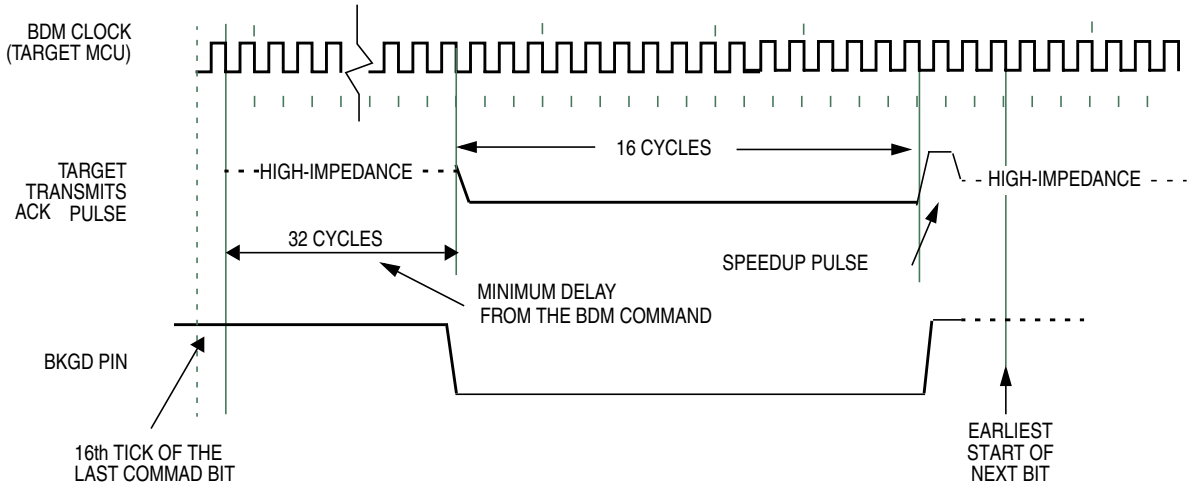


Figure 18-10. Target Acknowledge Pulse (ACK)

NOTE

If the ACK pulse was issued by the target, the host assumes the previous command was executed. If the CPU enters WAIT or STOP prior to executing a hardware command, the ACK pulse will not be issued meaning that the BDM command was not executed. After entering wait or stop mode, the BDM command is no longer pending.

Figure 18-11 shows the ACK handshake protocol in a command level timing diagram. The READ_BYTE instruction is used as an example. First, the 8-bit instruction opcode is sent by the host, followed by the address of the memory location to be read. The target BDM decodes the instruction. A bus cycle is grabbed (free or stolen) by the BDM and it executes the READ_BYTE operation. Having retrieved the data, the BDM issues an ACK pulse to the host controller, indicating that the addressed byte is ready to be retrieved. After detecting the ACK pulse, the host initiates the byte retrieval process. Note that data is sent in the form of a word and the host needs to determine which is the appropriate byte based on whether the address was odd or even.

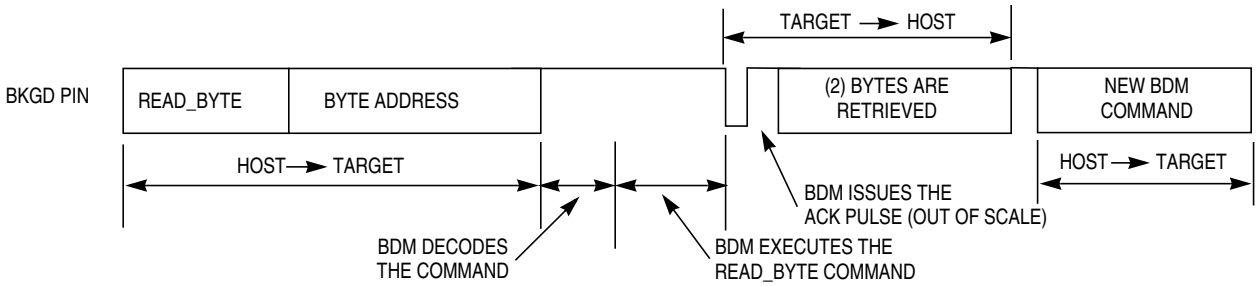


Figure 18-11. Handshake Protocol at Command Level

Differently from the normal bit transfer (where the host initiates the transmission), the serial interface ACK handshake pulse is initiated by the target MCU by issuing a falling edge in the BKGD pin. The hardware handshake protocol in Figure 18-10 specifies the timing when the BKGD pin is being driven, so the host should follow this timing constraint in order to avoid the risk of an electrical conflict in the BKGD pin.

NOTE

The only place the BKGD pin can have an electrical conflict is when one side is driving low and the other side is issuing a speedup pulse (high). Other "highs" are pulled rather than driven. However, at low rates the time of the speedup pulse can become lengthy and so the potential conflict time becomes longer as well.

The ACK handshake protocol does not support nested ACK pulses. If a BDM command is not acknowledge by an ACK pulse, the host needs to abort the pending command first in order to be able to issue a new BDM command. When the CPU enters WAIT or STOP while the host issues a command that requires CPU execution (e.g., WRITE_BYTE), the target discards the incoming command due to the WAIT or STOP being detected. Therefore, the command is not acknowledged by the target, which means that the ACK pulse will not be issued in this case. After a certain time the host should decide to abort the ACK sequence in order to be free to issue a new command. Therefore, the protocol should provide a mechanism in which a command, and therefore a pending ACK, could be aborted.

NOTE

Differently from a regular BDM command, the ACK pulse does not provide a time out. This means that in the case of a WAIT or STOP instruction being executed, the ACK would be prevented from being issued. If not aborted, the ACK would remain pending indefinitely. See the handshake abort procedure described in Section 18.4.8, "Hardware Handshake Abort Procedure."

18.4.8 Hardware Handshake Abort Procedure

The abort procedure is based on the SYNC command. In order to abort a command, which had not issued the corresponding ACK pulse, the host controller should generate a low pulse in the BKGD pin by driving it low for at least 128 serial clock cycles and then driving it high for one serial clock cycle, providing a speedup pulse. By detecting this long low pulse in the BKGD pin, the target executes the SYNC protocol, see Section 18.4.9, “SYNC — Request Timed Reference Pulse,” and assumes that the pending command and therefore the related ACK pulse, are being aborted. Therefore, after the SYNC protocol has been completed the host is free to issue new BDM commands.

Although it is not recommended, the host could abort a pending BDM command by issuing a low pulse in the BKGD pin shorter than 128 serial clock cycles, which will not be interpreted as the SYNC command. The ACK is actually aborted when a falling edge is perceived by the target in the BKGD pin. The short abort pulse should have at least 4 clock cycles keeping the BKGD pin low, in order to allow the falling edge to be detected by the target. In this case, the target will not execute the SYNC protocol but the pending command will be aborted along with the ACK pulse. The potential problem with this abort procedure is when there is a conflict between the ACK pulse and the short abort pulse. In this case, the target may not perceive the abort pulse. The worst case is when the pending command is a read command (i.e., READ_BYTE). If the abort pulse is not perceived by the target the host will attempt to send a new command after the abort pulse was issued, while the target expects the host to retrieve the accessed memory byte. In this case, host and target will run out of synchronism. However, if the command to be aborted is not a read command the short abort pulse could be used. After a command is aborted the target assumes the next falling edge, after the abort pulse, is the first bit of a new BDM command.

NOTE

The details about the short abort pulse are being provided only as a reference for the reader to better understand the BDM internal behavior. It is not recommended that this procedure be used in a real application.

Because the host knows the target serial clock frequency, the SYNC command (used to abort a command) does not need to consider the lower possible target frequency. In this case, the host could issue a SYNC very close to the 128 serial clock cycles length. Providing a small overhead on the pulse length in order to assure the SYNC pulse will not be misinterpreted by the target. See Section 18.4.9, “SYNC — Request Timed Reference Pulse.”

Figure 18-12 shows a SYNC command being issued after a READ_BYTE, which aborts the READ_BYTE command. Note that, after the command is aborted a new command could be issued by the host computer.

NOTE

Figure 18-12 does not represent the signals in a true timing scale

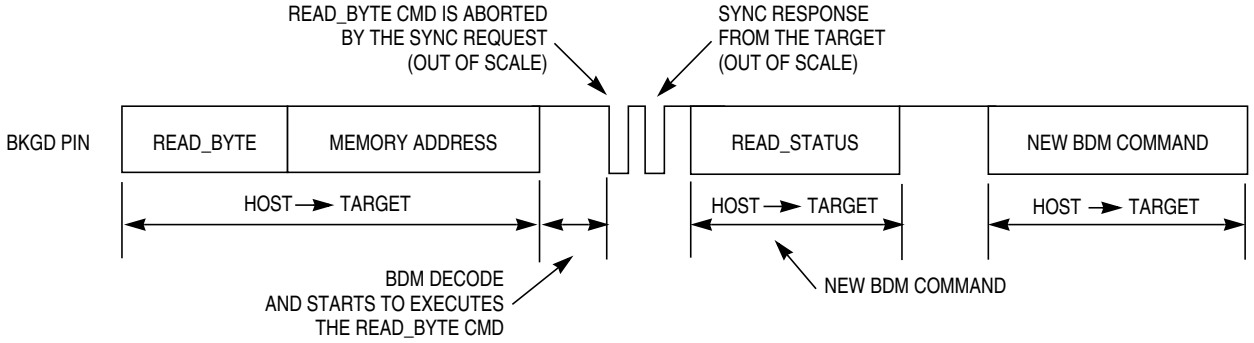


Figure 18-12. ACK Abort Procedure at the Command Level

Figure 18-13 shows a conflict between the ACK pulse and the SYNC request pulse. This conflict could occur if a POD device is connected to the target BKGD pin and the target is already in debug active mode. Consider that the target CPU is executing a pending BDM command at the exact moment the POD is being connected to the BKGD pin. In this case, an ACK pulse is issued along with the SYNC command. In this case, there is an electrical conflict between the ACK speedup pulse and the SYNC pulse. Because this is not a probable situation, the protocol does not prevent this conflict from happening.

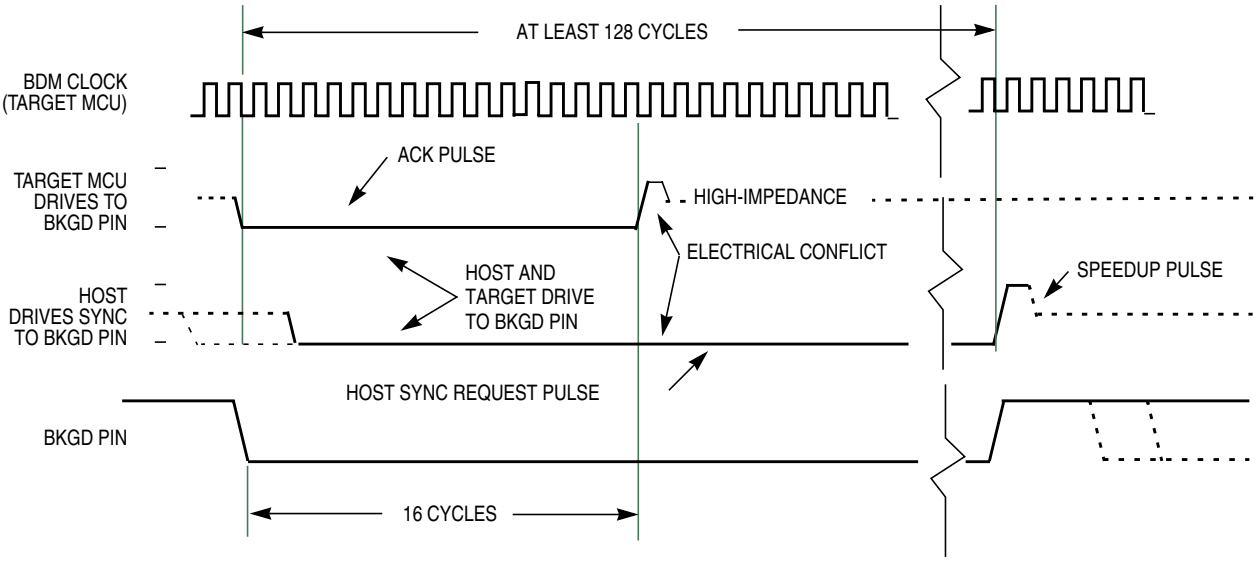


Figure 18-13. ACK Pulse and SYNC Request Conflict

NOTE

This information is being provided so that the MCU integrator will be aware that such a conflict could eventually occur.

The hardware handshake protocol is enabled by the ACK_ENABLE and disabled by the ACK_DISABLE BDM commands. This provides backwards compatibility with the existing POD devices which are not able to execute the hardware handshake protocol. It also allows for new POD devices, that support the hardware handshake protocol, to freely communicate with the target device. If desired, without the need for waiting for the ACK pulse.

The commands are described as follows:

- ACK_ENABLE — enables the hardware handshake protocol. The target will issue the ACK pulse when a CPU command is executed by the CPU. The ACK_ENABLE command itself also has the ACK pulse as a response.
- ACK_DISABLE — disables the ACK pulse protocol. In this case, the host needs to use the worst case delay time at the appropriate places in the protocol.

The default state of the BDM after reset is hardware handshake protocol disabled.

All the read commands will ACK (if enabled) when the data bus cycle has completed and the data is then ready for reading out by the BKGD serial pin. All the write commands will ACK (if enabled) after the data has been received by the BDM through the BKGD serial pin and when the data bus cycle is complete. See Section 18.4.3, “BDM Hardware Commands,” and Section 18.4.4, “Standard BDM Firmware Commands,” for more information on the BDM commands.

The ACK_ENABLE sends an ACK pulse when the command has been completed. This feature could be used by the host to evaluate if the target supports the hardware handshake protocol. If an ACK pulse is issued in response to this command, the host knows that the target supports the hardware handshake protocol. If the target does not support the hardware handshake protocol the ACK pulse is not issued. In this case, the ACK_ENABLE command is ignored by the target because it is not recognized as a valid command.

The BACKGROUND command will issue an ACK pulse when the CPU changes from normal to background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO command will issue an ACK pulse when the CPU exits from background mode. The ACK pulse related to this command could be aborted using the SYNC command.

The GO_UNTIL command is equivalent to a GO command with exception that the ACK pulse, in this case, is issued when the CPU enters into background mode. This command is an alternative to the GO command and should be used when the host wants to trace if a breakpoint match occurs and causes the CPU to enter active background mode. Note that the ACK is issued whenever the CPU enters BDM, which could be caused by a breakpoint match or by a BGND instruction being executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TRACE1 command has the related ACK pulse issued when the CPU enters background active mode after one instruction of the application program is executed. The ACK pulse related to this command could be aborted using the SYNC command.

The TAGGO command will not issue an ACK pulse because this would interfere with the tagging function shared on the same pin.

18.4.9 SYNC — Request Timed Reference Pulse

The SYNC command is unlike other BDM commands because the host does not necessarily know the correct communication speed to use for BDM communications until after it has analyzed the response to the SYNC command. To issue a SYNC command, the host should perform the following steps:

1. Drive the BKGD pin low for at least 128 cycles at the lowest possible BDM serial communication frequency (the lowest serial communication frequency is determined by the crystal oscillator or the clock chosen by CLKSW.)
2. Drive BKGD high for a brief speedup pulse to get a fast rise time (this speedup pulse is typically one cycle of the host clock.)
3. Remove all drive to the BKGD pin so it reverts to high impedance.
4. Listen to the BKGD pin for the sync response pulse.

Upon detecting the SYNC request from the host, the target performs the following steps:

1. Discards any incomplete command received or bit retrieved.
2. Waits for BKGD to return to a logic 1.
3. Delays 16 cycles to allow the host to stop driving the high speedup pulse.
4. Drives BKGD low for 128 cycles at the current BDM serial communication frequency.
5. Drives a one-cycle high speedup pulse to force a fast rise time on BKGD.
6. Removes all drive to the BKGD pin so it reverts to high impedance.

The host measures the low time of this 128 cycle SYNC response pulse and determines the correct speed for subsequent BDM communications. Typically, the host can determine the correct communication speed within a few percent of the actual target speed and the communication protocol can easily tolerate speed errors of several percent.

As soon as the SYNC request is detected by the target, any partially received command or bit retrieved is discarded. This is referred to as a soft-reset, equivalent to a time-out in the serial communication. After the SYNC response, the target will consider the next falling edge (issued by the host) as the start of a new BDM command or the start of new SYNC request.

Another use of the SYNC command pulse is to abort a pending ACK pulse. The behavior is exactly the same as in a regular SYNC command. Note that one of the possible causes for a command to not be acknowledged by the target is a host-target synchronization problem. In this case, the command may not have been understood by the target and so an ACK response pulse will not be issued.

18.4.10 Instruction Tracing

When a TRACE1 command is issued to the BDM in active BDM, the CPU exits the standard BDM firmware and executes a single instruction in the user code. As soon as this has occurred, the CPU is forced to return to the standard BDM firmware and the BDM is active and ready to receive a new command. If the TRACE1 command is issued again, the next user instruction will be executed. This facilitates stepping or tracing through the user code one instruction at a time.

If an interrupt is pending when a TRACE1 command is issued, the interrupt stacking operation occurs but no user instruction is executed. Upon return to standard BDM firmware execution, the program counter points to the first instruction in the interrupt service routine.

18.4.11 Instruction Tagging

The instruction queue and cycle-by-cycle CPU activity are reconstructible in real time or from trace history that is captured by a logic analyzer. However, the reconstructed queue cannot be used to stop the CPU at a specific instruction. This is because execution already has begun by the time an operation is visible outside the system. A separate instruction tagging mechanism is provided for this purpose.

The tag follows program information as it advances through the instruction queue. When a tagged instruction reaches the head of the queue, the CPU enters active BDM rather than executing the instruction.

NOTE

Tagging is disabled when BDM becomes active and BDM serial commands are not processed while tagging is active.

Executing the BDM TAGGO command configures two system pins for tagging. The $\overline{\text{TAGLO}}$ signal shares a pin with the $\overline{\text{LSTRB}}$ signal, and the $\overline{\text{TAGHI}}$ signal shares a pin with the BKGD signal.

Table 18-7 shows the functions of the two tagging pins. The pins operate independently, that is the state of one pin does not affect the function of the other. The presence of logic level 0 on either pin at the fall of the external clock (ECLK) performs the indicated function. High tagging is allowed in all modes. Low tagging is allowed only when low strobe is enabled (LSTRB is allowed only in wide expanded modes and emulation expanded narrow mode).

Table 18-7. Tag Pin Function

$\overline{\text{TAGHI}}$	$\overline{\text{TAGLO}}$	Tag
1	1	No tag
1	0	Low byte
0	1	High byte
0	0	Both bytes

18.4.12 Serial Communication Time-Out

The host initiates a host-to-target serial transmission by generating a falling edge on the BKGD pin. If BKGD is kept low for more than 128 target clock cycles, the target understands that a SYNC command was issued. In this case, the target will keep waiting for a rising edge on BKGD in order to answer the SYNC request pulse. If the rising edge is not detected, the target will keep waiting forever without any time-out limit.

Consider now the case where the host returns BKGD to logic one before 128 cycles. This is interpreted as a valid bit transmission, and not as a SYNC request. The target will keep waiting for another falling edge marking the start of a new bit. If, however, a new falling edge is not detected by the target within 512 clock cycles since the last falling edge, a time-out occurs and the current command is discarded without affecting memory or the operating mode of the MCU. This is referred to as a soft-reset.

If a read command is issued but the data is not retrieved within 512 serial clock cycles, a soft-reset will occur causing the command to be disregarded. The data is not available for retrieval after the time-out has occurred. This is the expected behavior if the handshake protocol is not enabled. However, consider the behavior where the BDC is running in a frequency much greater than the CPU frequency. In this case, the command could time out before the data is ready to be retrieved. In order to allow the data to be retrieved even with a large clock frequency mismatch (between BDC and CPU) when the hardware handshake protocol is enabled, the time out between a read command and the data retrieval is disabled. Therefore, the host could wait for more then 512 serial clock cycles and continue to be able to retrieve the data from an issued read command. However, as soon as the handshake pulse (ACK pulse) is issued, the time-out feature is re-activated, meaning that the target will time out after 512 clock cycles. Therefore, the host needs to retrieve the data within a 512 serial clock cycles time frame after the ACK pulse had been issued. After that period, the read command is discarded and the data is no longer available for retrieval. Any falling edge of the BKGD pin after the time-out period is considered to be a new command or a SYNC request.

Note that whenever a partially issued command, or partially retrieved data, has occurred the time out in the serial communication is active. This means that if a time frame higher than 512 serial clock cycles is observed between two consecutive negative edges and the command being issued or data being retrieved is not complete, a soft-reset will occur causing the partially received command or data retrieved to be disregarded. The next falling edge of the BKGD pin, after a soft-reset has occurred, is considered by the target as the start of a new BDM command, or the start of a SYNC request pulse.

18.4.13 Operation in Wait Mode

The BDM cannot be used in wait mode if the system disables the clocks to the BDM.

There is a clearing mechanism associated with the WAIT instruction when the clocks to the BDM (CPU core platform) are disabled. As the clocks restart from wait mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.

18.4.14 Operation in Stop Mode

The BDM is completely shutdown in stop mode.

There is a clearing mechanism associated with the STOP instruction. STOP must be enabled and the part must go into stop mode for this to occur. As the clocks restart from stop mode, the BDM receives a soft reset (clearing any command in progress) and the ACK function will be disabled. This is a change from previous BDM modules.

Chapter 19
Debug Module (DBGV1)

19.1 Introduction

This section describes the functionality of the debug (DBG) sub-block of the HCS12 core platform.

The DBG module is designed to be fully compatible with the existing BKP_HCS12_A module (BKP mode) and furthermore provides an on-chip trace buffer with flexible triggering capability (DBG mode). The DBG module provides for non-intrusive debug of application software. The DBG module is optimized for the HCS12 16-bit architecture.

19.1.1 Features

The DBG module in BKP mode includes these distinctive features:

- Full or dual breakpoint mode
  - Compare on address and data (full)
  - Compare on either of two addresses (dual)
- BDM or SWI breakpoint
  - Enter BDM on breakpoint (BDM)
  - Execute SWI on breakpoint (SWI)
- Tagged or forced breakpoint
  - Break just before a specific instruction will begin execution (TAG)
  - Break on the first instruction boundary after a match occurs (Force)
- Single, range, or page address compares
  - Compare on address (single)
  - Compare on address 256 byte (range)
  - Compare on any 16K page (page)
- At forced breakpoints compare address on read or write
- High and/or low byte data compares
- Comparator C can provide an additional tag or force breakpoint (enhancement for BKP mode)

The DBG in DBG mode includes these distinctive features:

- Three comparators (A, B, and C)
  - — Dual mode, comparators A and B used to compare addresses
  - — Full mode, comparator A compares address and comparator B compares data
  - — Can be used as trigger and/or breakpoint
  - — Comparator C used in LOOP1 capture mode or as additional breakpoint
- Four capture modes
  - — Normal mode, change-of-flow information is captured based on trigger specification
  - — Loop1 mode, comparator C is dynamically updated to prevent redundant change-of-flow storage.
  - — Detail mode, address and data for all cycles except program fetch (P) and free (f) cycles are stored in trace buffer
  - — Profile mode, last instruction address executed by CPU is returned when trace buffer address is read
- Two types of breakpoint or debug triggers
  - — Break just before a specific instruction will begin execution (tag)
  - — Break on the first instruction boundary after a match occurs (force)
- BDM or SWI breakpoint
  - — Enter BDM on breakpoint (BDM)
  - — Execute SWI on breakpoint (SWI)
- Nine trigger modes for comparators A and B
  - — A
  - — A or B
  - — A then B
  - — A and B, where B is data (full mode)
  - — A and not B, where B is data (full mode)
  - — Event only B, store data
  - — A then event only B, store data
  - — Inside range, $A \leq address \leq B$
  - — Outside range, $address < A$ or $address > B$
- Comparator C provides an additional tag or force breakpoint when capture mode is not configured in LOOP1 mode.
- Sixty-four word (16 bits wide) trace buffer for storing change-of-flow information, event only data and other bus information.
  - — Source address of taken conditional branches (long, short, bit-conditional, and loop constructs)
  - — Destination address of indexed JMP, JSR, and CALL instruction.
  - — Destination address of RTI, RTS, and RTC instructions
  - — Vector address of interrupts, except for SWI and BDM vectors

— Data associated with event B trigger modes
— Detail report mode stores address and data for all cycles except program (P) and free (f) cycles
— Current instruction address when in profiling mode
— BGND is not considered a change-of-flow (cof) by the debugger

19.1.2 Modes of Operation

There are two main modes of operation: breakpoint mode and debug mode. Each one is mutually exclusive of the other and selected via a software programmable control bit.

In the breakpoint mode there are two sub-modes of operation:

- Dual address mode, where a match on either of two addresses will cause the system to enter background debug mode (BDM) or initiate a software interrupt (SWI).
- Full breakpoint mode, where a match on address and data will cause the system to enter background debug mode (BDM) or initiate a software interrupt (SWI).

In debug mode, there are several sub-modes of operation.

- Trigger modes

  There are many ways to create a logical trigger. The trigger can be used to capture bus information either starting from the trigger or ending at the trigger. Types of triggers (A and B are registers):

  — A only
  — A or B
  — A then B
  — Event only B (data capture)
  — A then event only B (data capture)
  — A and B, full mode
  — A and not B, full mode
  — Inside range
  — Outside range

- Capture modes

  There are several capture modes. These determine which bus information is saved and which is ignored.

  — Normal: save change-of-flow program fetches
  — Loop1: save change-of-flow program fetches, ignoring duplicates
  — Detail: save all bus operations except program and free cycles
  — Profile: poll target from external device

19.1.3 Block Diagram

Figure 19-1 is a block diagram of this module in breakpoint mode. Figure 19-2 is a block diagram of this module in debug mode.

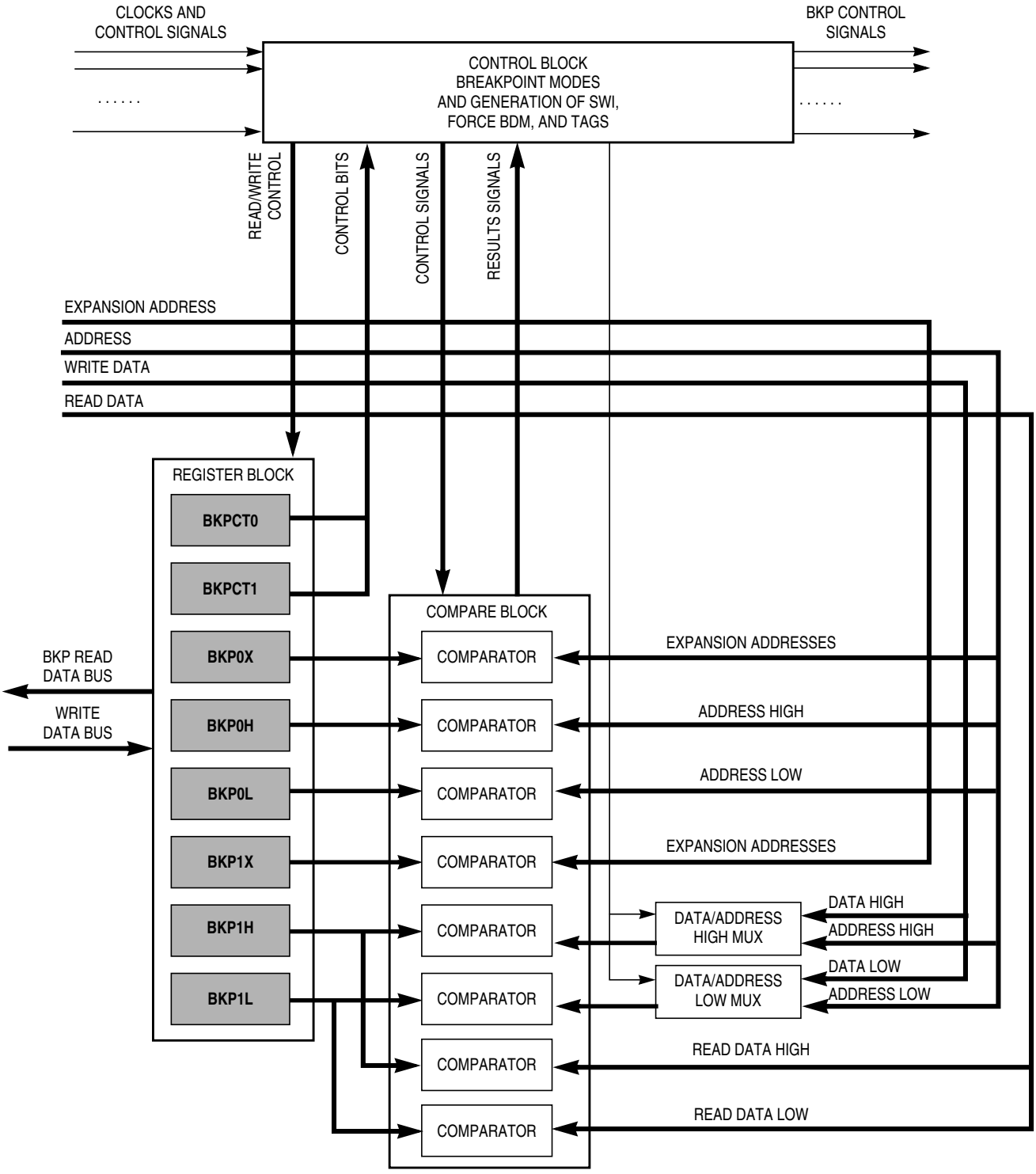


Figure 19-1. DBG Block Diagram in BKP Mode

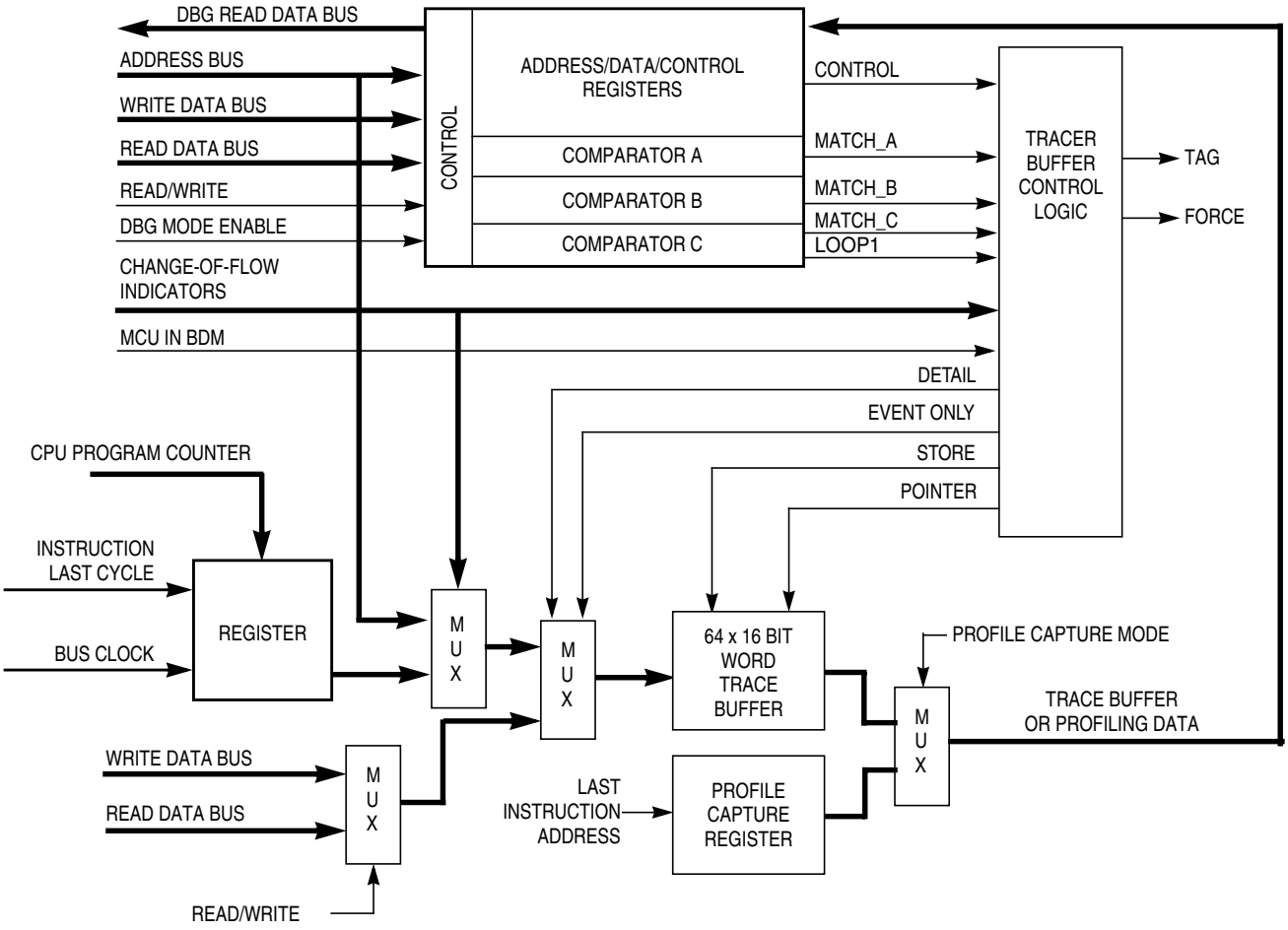


Figure 19-2. DBG Block Diagram in DBG Mode

19.2 External Signal Description

The DBG sub-module relies on the external bus interface (generally the MEBI) when the DBG is matching on the external bus.

The tag pins in Table 19-1 (part of the MEBI) may also be a part of the breakpoint operation.

Table 19-1. External System Pins Associated with DBG and MEBI

Pin Name	Pin Functions	Description
BKGD/MODC/ $\overline{\text{TAGHI}}$	$\overline{\text{TAGHI}}$	When instruction tagging is on, a 0 at the falling edge of E tags the high half of the instruction word being read into the instruction queue.
PE3/$\overline{\text{LSTRB}}$/ $\overline{\text{TAGLO}}$	$\overline{\text{TAGLO}}$	In expanded wide mode or emulation narrow modes, when instruction tagging is on and low strobe is enabled, a 0 at the falling edge of E tags the low half of the instruction word being read into the instruction queue.

19.3 Memory Map and Register Definition

A summary of the registers associated with the DBG sub-block is shown in Figure 19-3. Detailed descriptions of the registers and bits are given in the subsections that follow.

19.3.1 Module Memory Map

Table 19-2. DBG Memory Map

Address Offset	Use	Access
	Debug Control Register (DBGC1)	R/W
	Debug Status and Control Register (DBGSC)	R/W
	Debug Trace Buffer Register High (DBGTBH)	R
	Debug Trace Buffer Register Low (DBGTBL)	R
4	Debug Count Register (DBGCNT)	R
5	Debug Comparator C Extended Register (DBGCCX)	R/W
6	Debug Comparator C Register High (DBGCCH)	R/W
	Debug Comparator C Register Low (DBGCCL)	R/W
8	Debug Control Register 2 (DBGC2) / (BKPCT0)	R/W
9	Debug Control Register 3 (DBGC3) / (BKPCT1)	R/W
A	Debug Comparator A Extended Register (DBGCAX) / (/BKP0X)	R/W
B	Debug Comparator A Register High (DBGCAH) / (BKP0H)	R/W
	Debug Comparator A Register Low (DBGCAL) / (BKP0L)	R/W
	Debug Comparator B Extended Register (DBGCBX) / (BKP1X)	R/W
E	Debug Comparator B Register High (DBGCBH) / (BKP1H)	R/W
F	Debug Comparator B Register Low (DBGCBL) / (BKP1L)	R/W

19.3.2 Register Descriptions

This section consists of the DBG register descriptions in address order. Most of the register bits can be written to in either BKP or DBG mode, although they may not have any effect in one of the modes. However, the only bits in the DBG module that can be written while the debugger is armed (ARM = 1) are DBGEN and ARM

Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
DBGC1	R	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
	W								
DBGSC	R	AF	BF	CF	0	TRG			
	W								

= Unimplemented or Reserved

Figure 19-3. DBG Register Summary

Name[1]		Bit 7	6	5	4	3	2	1	Bit 0
DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
	W								
DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	W								
DBGCNT	R	TBF	0	CNT					
	W								
DBGCCX[(2)]	R	PAGSEL		EXTCMP					
	W								
DBGCCH[(2)]	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
DBGCCL[(2)]	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
DBGC2 BKPCT0	R	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
	W								
DBGC3 BKPCT1	R	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
	W								
DBGCAX BKP0X	R	PAGSEL		EXTCMP					
	W								
DBGCAH BKP0H	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
DBGCAL BKP0L	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
DBGCBX BKP1X	R	PAGSEL		EXTCMP					
	W								
DBGCBH BKP1H	R	Bit 15	14	13	12	11	10	9	Bit 8
	W								
DBGCBL BKP1L	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								

= Unimplemented or Reserved

Figure 19-3. DBG Register Summary (continued)

1 The DBG module is designed for backwards compatibility to existing BKP modules. Register and bit names have changed from the BKP module. This column shows the DBG register name, as well as the BKP register name for reference.

2 Comparator C can be used to enhance the BKP mode by providing a third breakpoint.

19.3.2.1 Debug Control Register 1 (DBGC1)

NOTE

All bits are used in DBG mode only.

	7	6	5	4	3	2	1	0
R	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-4. Debug Control Register (DBGC1)

NOTE

This register cannot be written if BKP mode is enabled (BKABEN in DBGC2 is set).

Table 19-3. DBGC1 Field Descriptions

Field	Description
7 DBGEN	**DBG Mode Enable Bit** — The DBGEN bit enables the DBG module for use in DBG mode. This bit cannot be set if the MCU is in secure mode. 0 DBG mode disabled 1 DBG mode enabled
6 ARM	**Arm Bit** — The ARM bit controls whether the debugger is comparing and storing data in the trace buffer. See Section 19.4.2.4, “Arming the DBG Module,” for more information. 0 Debugger unarmed 1 Debugger armed **Note:** This bit cannot be set if the DBGEN bit is not also being set at the same time. For example, a write of 01 to DBGEN[7:6] will be interpreted as a write of 00.
5 TRGSEL	**Trigger Selection Bit** — The TRGSEL bit controls the triggering condition for comparators A and B in DBG mode. It serves essentially the same function as the TAGAB bit in the DBGC2 register does in BKP mode. See Section 19.4.2.1.2, “Trigger Selection,” for more information. TRGSEL may also determine the type of breakpoint based on comparator A and B if enabled in DBG mode (DBGBRK = 1). Please refer to Section 19.4.3.1, “Breakpoint Based on Comparator A and B.” 0 Trigger on any compare address match 1 Trigger before opcode at compare address gets executed (tagged-type)
4 BEGIN	**Begin/End Trigger Bit** — The BEGIN bit controls whether the trigger begins or ends storing of data in the trace buffer. See Section 19.4.2.8.1, “Storing with Begin-Trigger,” and Section 19.4.2.8.2, “Storing with End-Trigger,” for more details. 0 Trigger at end of stored data 1 Trigger before storing data

Table 19-3. DBGC1 Field Descriptions (continued)

Field	Description
3 DBGBRK	**DBG Breakpoint Enable Bit** — The DBGBRK bit controls whether the debugger will request a breakpoint based on comparator A and B to the CPU upon completion of a tracing session. Please refer to Section 19.4.3, “Breakpoints,” for further details. 0 CPU break request not enabled 1 CPU break request enabled
1:0 CAPMOD	**Capture Mode Field** — See Table 19-4 for capture mode field definitions. In LOOP1 mode, the debugger will automatically inhibit redundant entries into capture memory. In detail mode, the debugger is storing address and data for all cycles except program fetch (P) and free (f) cycles. In profile mode, the debugger is returning the address of the last instruction executed by the CPU on each access of trace buffer address. Refer to Section 19.4.2.6, “Capture Modes,” for more information.

Table 19-4. CAPMOD Encoding

CAPMOD	Description
00	Normal
01	LOOP1
10	DETAIL
11	PROFILE

19.3.2.2 Debug Status and Control Register (DBGSC)

	7	6	5	4	3	2	1	0
R	AF	BF	CF	0	TRG			
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 19-5. Debug Status and Control Register (DBGSC)

Table 19-5. DBGSC Field Descriptions

Field	Description
7 AF	**Trigger A Match Flag** — The AF bit indicates if trigger A match condition was met since arming. This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger A did not match 1 Trigger A match
6 BF	**Trigger B Match Flag** — The BF bit indicates if trigger B match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Trigger B did not match 1 Trigger B match
5 CF	**Comparator C Match Flag** — The CF bit indicates if comparator C match condition was met since arming.This bit is cleared when ARM in DBGC1 is written to a 1 or on any write to this register. 0 Comparator C did not match 1 Comparator C match
3:0 TRG	**Trigger Mode Bits** — The TRG bits select the trigger mode of the DBG module as shown Table 19-6. See Section 19.4.2.5, “Trigger Modes,” for more detail.

Table 19-6. Trigger Mode Encoding

TRG Value	Meaning
0000	A only
0001	A or B
0010	A then B
0011	Event only B
0100	A then event only B
0101	A and B (full mode)
0110	A and Not B (full mode)
0111	Inside range
1000	Outside range
1001 ↓ 1111	Reserved (Defaults to A only)

19.3.2.3 Debug Trace Buffer Register (DBGTB)

	15	14	13	12	11	10	9	8
R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
W								
Reset	u	u	u	u	u	u	u	u

= Unimplemented or Reserved

Figure 19-6. Debug Trace Buffer Register High (DBGTBH)

	7	6	5	4	3	2	1	0
R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
W								
Reset	u	u	u	u	u	u	u	u

= Unimplemented or Reserved

Figure 19-7. Debug Trace Buffer Register Low (DBGTBL)

Table 19-7. DBGTB Field Descriptions

Field	Description
15:0	**Trace Buffer Data Bits** — The trace buffer data bits contain the data of the trace buffer. This register can be read only as a word read. Any byte reads or misaligned access of these registers will return 0 and will not cause the trace buffer pointer to increment to the next trace buffer address. The same is true for word reads while the debugger is armed. In addition, this register may appear to contain incorrect data if it is not read with the same capture mode bit settings as when the trace buffer data was recorded (See Section 19.4.2.9, “Reading Data from Trace Buffer”). Because reads will reflect the contents of the trace buffer RAM, the reset state is undefined.

19.3.2.4 Debug Count Register (DBGCNT)

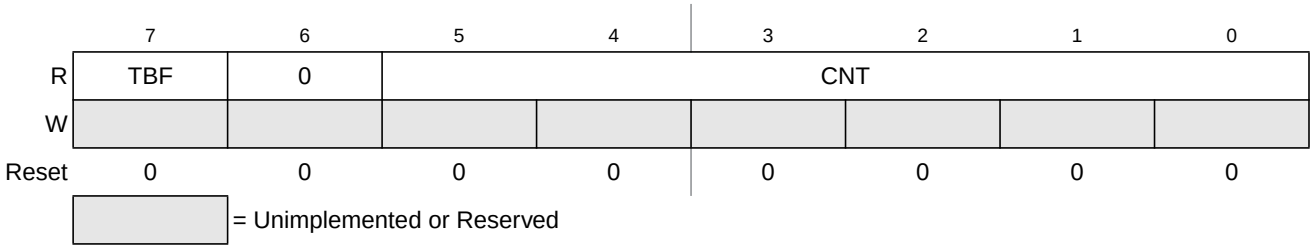


Figure 19-8. Debug Count Register (DBGCNT)

Table 19-8. DBGCNT Field Descriptions

Field	Description
7 TBF	**Trace Buffer Full** — The TBF bit indicates that the trace buffer has stored 64 or more words of data since it was last armed. If this bit is set, then all 64 words will be valid data, regardless of the value in CNT[5:0]. The TBF bit is cleared when ARM in DBGC1 is written to a 1.
5:0 CNT	**Count Value** — The CNT bits indicate the number of valid data words stored in the trace buffer. Table 19-9 shows the correlation between the CNT bits and the number of valid data words in the trace buffer. When the CNT rolls over to 0, the TBF bit will be set and incrementing of CNT will continue if DBG is in end-trigger mode. The DBGCNT register is cleared when ARM in DBGC1 is written to a 1.

Table 19-9. CNT Decoding Table

TBF	CNT	Description
0	000000	No data valid
0	000001	1 word valid
0	000010 111110	2 words valid .. .. 62 words valid
0	111111	63 words valid
1	000000	64 words valid; if BEGIN = 1, the ARM bit will be cleared. A breakpoint will be generated if DBGBRK = 1
1	000001 111111	64 words valid, oldest data has been overwritten by most recent data

19.3.2.5 Debug Comparator C Extended Register (DBGCCX)

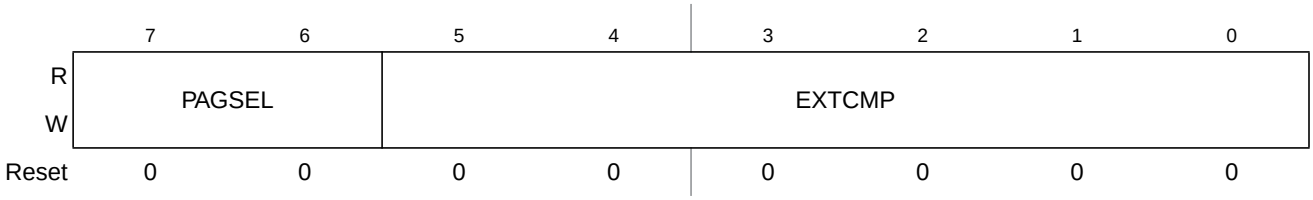


Figure 19-9. Debug Comparator C Extended Register (DBGCCX)

Table 19-10. DBGCCX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — In both BKP and DBG mode, PAGSEL selects the type of paging as shown in Table 19-11. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively).
5:0 EXTCMP	**Comparator C Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 19-11 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core. **Note:** Comparator C can be used when the DBG module is configured for BKP mode. Extended addressing comparisons for comparator C use PAGSEL and will operate differently to the way that comparator A and B operate in BKP mode.

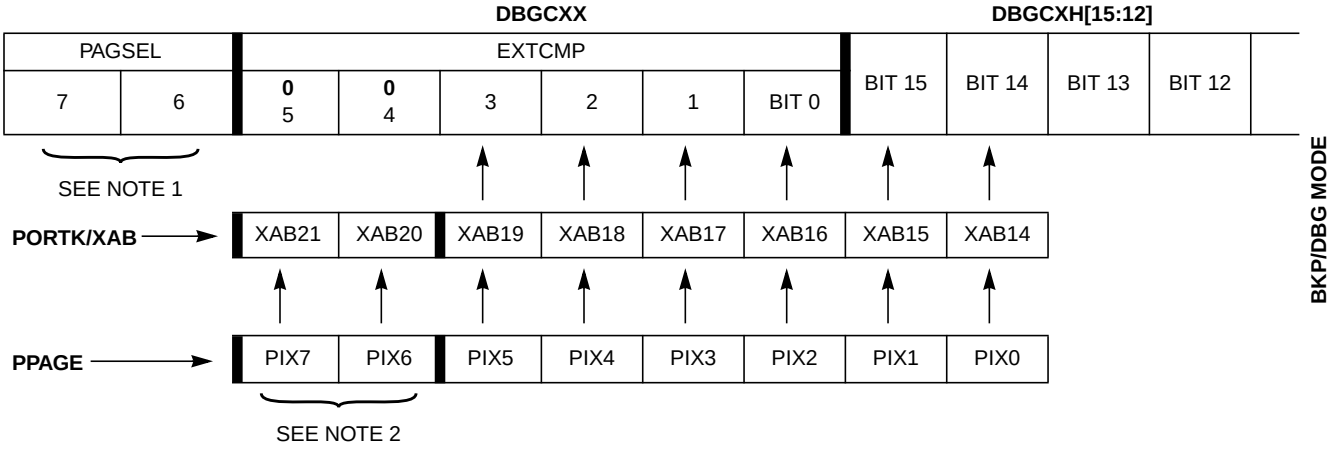
Table 19-11. PAGSEL Decoding[1]

PAGSEL	Description	EXTCMP	Comment
00	Normal (64k)	Not used	No paged memory
01	PPAGE (256 — 16K pages)	EXTCMP[5:0] is compared to address bits [21:16][2]	PPAGE[7:0] / XAB[21:14] becomes address bits [21:14][1]
10[3]	DPAGE (reserved) (256 — 4K pages)	EXTCMP[3:0] is compared to address bits [19:16]	DPAGE / XAB[21:14] becomes address bits [19:12]
11[2]	EPAGE (reserved) (256 — 1K pages)	EXTCMP[1:0] is compared to address bits [17:16]	EPAGE / XAB[21:14] becomes address bits [17:10]

1 See Figure 19-10.

2 Current HCS12 implementations have PPAGE limited to 6 bits. Therefore, EXTCMP[5:4] should be set to 00.

3 Data page (DPAGE) and Extra page (EPAGE) are reserved for implementation on devices that support paged data and extra space.



NOTES:
1. In BKP and DBG mode, PAGSEL selects the type of paging as shown in Table 19-11.
2. Current HCS12 implementations are limited to six PPAGE bits, PIX[5:0]. Therefore, EXTCMP[5:4] = 00.

Figure 19-10. Comparator C Extended Comparison in BKP/DBG Mode

19.3.2.6 Debug Comparator C Register (DBGCC)

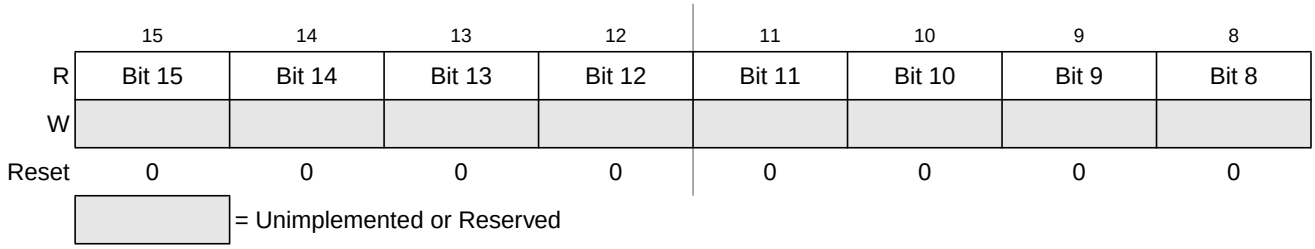


Figure 19-11. Debug Comparator C Register High (DBGCCH)

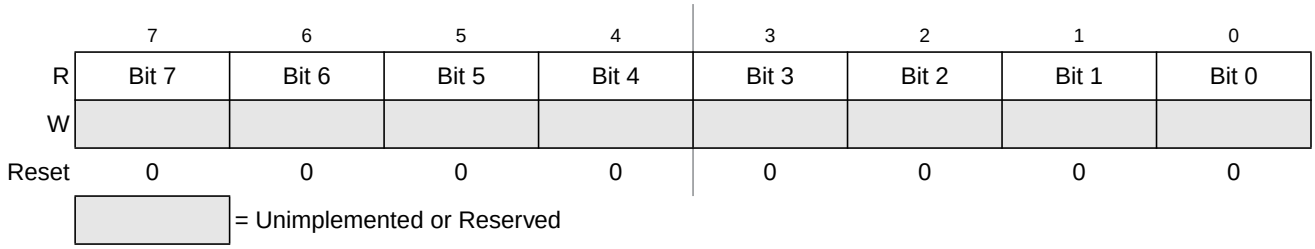


Figure 19-12. Debug Comparator C Register Low (DBGCCL)

Table 19-12. DBGCC Field Descriptions

Field	Description
15:0	**Comparator C Compare Bits** — The comparator C compare bits control whether comparator C will compare the address bus bits [15:0] to a logic 1 or logic 0. See Table 19-13. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1 **Note:** This register will be cleared automatically when the DBG module is armed in LOOP1 mode.

Table 19-13. Comparator C Compares

PAGSEL	EXTCMP Compare	High-Byte Compare
x0	No compare	DBGCCH[7:0] = AB[15:8]
x1	EXTCMP[5:0] = XAB[21:16]	DBGCCH[7:0] = XAB[15:14],AB[13:8]

19.3.2.7 Debug Control Register 2 (DBGC2)

	7	6	5	4	3	2	1	0
R W	BKABEN[1]	FULL	BDM	TAGAB	BKCEN[2]	TAGC[2]	RWCEN[2]	RWC[2]
Reset	0	0	0	0	0	0	0	0

1 When BKABEN is set (BKP mode), all bits in DBGC2 are available. When BKABEN is cleared and DBG is used in DBG mode, bits FULL and TAGAB have no meaning.

2 These bits can be used in BKP mode and DBG mode (when capture mode is not set in LOOP1) to provide a third breakpoint.

Figure 19-13. Debug Control Register 2 (DBGC2)

Table 19-14. DBGC2 Field Descriptions

Field	Description
7 BKABEN	**Breakpoint Using Comparator A and B Enable** — This bit enables the breakpoint capability using comparator A and B, when set (BKP mode) the DBGEN bit in DBGC1 cannot be set. 0 Breakpoint module off 1 Breakpoint module on
6 FULL	**Full Breakpoint Mode Enable** — This bit controls whether the breakpoint module is in dual mode or full mode. In full mode, comparator A is used to match address and comparator B is used to match data. See Section 19.4.1.2, “Full Breakpoint Mode,” for more details. 0 Dual address mode enabled 1 Full breakpoint mode enabled
5 BDM	**Background Debug Mode Enable** — This bit determines if the breakpoint causes the system to enter background debug mode (BDM) or initiate a software interrupt (SWI). 0 Go to software interrupt on a break request 1 Go to BDM on a break request
4 TAGAB	**Comparator A/B Tag Select** — This bit controls whether the breakpoint will cause a break on the next instruction boundary (force) or on a match that will be an executable opcode (tagged). Non-executed opcodes cannot cause a tagged breakpoint. 0 On match, break at the next instruction boundary (force) 1 On match, break if/when the instruction is about to be executed (tagged)
3 BKCEN	**Breakpoint Comparator C Enable Bit** — This bit enables the breakpoint capability using comparator C. 0 Comparator C disabled for breakpoint 1 Comparator C enabled for breakpoint **Note:** This bit will be cleared automatically when the DBG module is armed in loop1 mode.
2 TAGC	**Comparator C Tag Select** — This bit controls whether the breakpoint will cause a break on the next instruction boundary (force) or on a match that will be an executable opcode (tagged). Non-executed opcodes cannot cause a tagged breakpoint. 0 On match, break at the next instruction boundary (force) 1 On match, break if/when the instruction is about to be executed (tagged)

Table 19-14. DBGC2 Field Descriptions (continued)

Field	Description
1 RWCEN	**Read/Write Comparator C Enable Bit** — The RWCEN bit controls whether read or write comparison is enabled for comparator C. RWCEN is not useful for tagged breakpoints. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 RWC	**Read/Write Comparator C Value Bit** — The RWC bit controls whether read or write is used in compare for comparator C. The RWC bit is not used if RWCEN = 0. 0 Write cycle will be matched 1 Read cycle will be matched

19.3.2.8 Debug Control Register 3 (DBGC3)

	7	6	5	4	3	2	1	0
R W	BKAMBH[1]	BKAMBL[1]	BKBMBH[2]	BKBMBL[2]	RWAEN	RWA	RWBEN	RWB
Reset	0	0	0	0	0	0	0	0

1 In DBG mode, BKAMBH:BKAMBL has no meaning and are forced to 0's.

2 In DBG mode, BKBMBH:BKBMBL are used in full mode to qualify data.

Figure 19-14. Debug Control Register 3 (DBGC3)

Table 19-15. DBGC3 Field Descriptions

Field	Description
7:6 BKAMB[H:L]	**Breakpoint Mask High Byte for First Address** — In dual or full mode, these bits may be used to mask (disable) the comparison of the high and/or low bytes of the first address breakpoint. The functionality is as given in Table 19-16. The x:0 case is for a full address compare. When a program page is selected, the full address compare will be based on bits for a 20-bit compare. The registers used for the compare are {DBGCAX[5:0], DBGCAH[5:0], DBGCAL[7:0]}, where DBGAX[5:0] corresponds to PPAGE[5:0] or extended address bits [19:14] and CPU address [13:0]. When a program page is not selected, the full address compare will be based on bits for a 16-bit compare. The registers used for the compare are {DBGCAH[7:0], DBGCAL[7:0]} which corresponds to CPU address [15:0]. **Note:** This extended address compare scheme causes an aliasing problem in BKP mode in which several physical addresses may match with a single logical address. This problem may be avoided by using DBG mode to generate breakpoints. The 1:0 case is not sensible because it would ignore the high order address and compare the low order and expansion addresses. Logic forces this case to compare all address lines (effectively ignoring the BKAMBH control bit). The 1:1 case is useful for triggering a breakpoint on any access to a particular expansion page. This only makes sense if a program page is being accessed so that the breakpoint trigger will occur only if DBGCAX compares.

Table 19-15. DBGC3 Field Descriptions (continued)

Field	Description
5:4 BKBMB[H:L]	**Breakpoint Mask High Byte and Low Byte of Data (Second Address)** — In dual mode, these bits may be used to mask (disable) the comparison of the high and/or low bytes of the second address breakpoint. The functionality is as given in Table 19-17. The x:0 case is for a full address compare. When a program page is selected, the full address compare will be based on bits for a 20-bit compare. The registers used for the compare are {DBGCBX[5:0], DBGCBH[5:0], DBGCBL[7:0]} where DBGCBX[5:0] corresponds to PPAGE[5:0] or extended address bits [19:14] and CPU address [13:0]. When a program page is not selected, the full address compare will be based on bits for a 16-bit compare. The registers used for the compare are {DBGCBH[7:0], DBGCBL[7:0]} which corresponds to CPU address [15:0]. **Note:** This extended address compare scheme causes an aliasing problem in BKP mode in which several physical addresses may match with a single logical address. This problem may be avoided by using DBG mode to generate breakpoints. The 1:0 case is not sensible because it would ignore the high order address and compare the low order and expansion addresses. Logic forces this case to compare all address lines (effectively ignoring the BKBMBH control bit). The 1:1 case is useful for triggering a breakpoint on any access to a particular expansion page. This only makes sense if a program page is being accessed so that the breakpoint trigger will occur only if DBGCBX compares. In full mode, these bits may be used to mask (disable) the comparison of the high and/or low bytes of the data breakpoint. The functionality is as given in Table 19-18.
3 RWAEN	**Read/Write Comparator A Enable Bit** — The RWAEN bit controls whether read or write comparison is enabled for comparator A. See Section 19.4.2.1.1, “Read or Write Comparison,” for more information. This bit is not useful for tagged operations. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
2 RWA	**Read/Write Comparator A Value Bit** — The RWA bit controls whether read or write is used in compare for comparator A. The RWA bit is not used if RWAEN = 0. 0 Write cycle will be matched 1 Read cycle will be matched
1 RWBEN	**Read/Write Comparator B Enable Bit** — The RWBEN bit controls whether read or write comparison is enabled for comparator B. See Section 19.4.2.1.1, “Read or Write Comparison,” for more information. This bit is not useful for tagged operations. 0 Read/Write is not used in comparison 1 Read/Write is used in comparison
0 RWB	**Read/Write Comparator B Value Bit** — The RWB bit controls whether read or write is used in compare for comparator B. The RWB bit is not used if RWBEN = 0. 0 Write cycle will be matched 1 Read cycle will be matched **Note:** RWB and RWBEN are not used in full mode.

Table 19-16. Breakpoint Mask Bits for First Address

BKAMBH:BKAMBL	Address Compare	DBGCAX	DBGCAH	DBGCAL
x:0	Full address compare	Yes[1]	Yes	Yes
0:1	256 byte address range	Yes[1]	Yes	No
1:1	16K byte address range	Yes[1]	No	No

[1] If PPAGE is selected.

Table 19-17. Breakpoint Mask Bits for Second Address (Dual Mode)

BKBMBH:BKBMBL	Address Compare	DBGCBX	DBGCBH	DBGCBL
x:0	Full address compare	Yes[1]	Yes	Yes
0:1	256 byte address range	Yes[1]	Yes	No
1:1	16K byte address range	Yes[1]	No	No

1 If PPAGE is selected.

Table 19-18. Breakpoint Mask Bits for Data Breakpoints (Full Mode)

BKBMBH:BKBMBL	Data Compare	DBGCBX	DBGCBH	DBGCBL
0:0	High and low byte compare	No[1]	Yes	Yes
0:1	High byte	No[1]	Yes	No
1:0	Low byte	No[1]	No	Yes
1:1	No compare	No[1]	No	No

1 Expansion addresses for breakpoint B are not applicable in this mode.

19.3.2.9 Debug Comparator A Extended Register (DBGCAX)

	7	6	5	4	3	2	1	0
R W	PAGSEL		EXTCMP					
Reset	0	0	0	0	0	0	0	0

Figure 19-15. Debug Comparator A Extended Register (DBGCAX)

Table 19-19. DBGCAX Field Descriptions

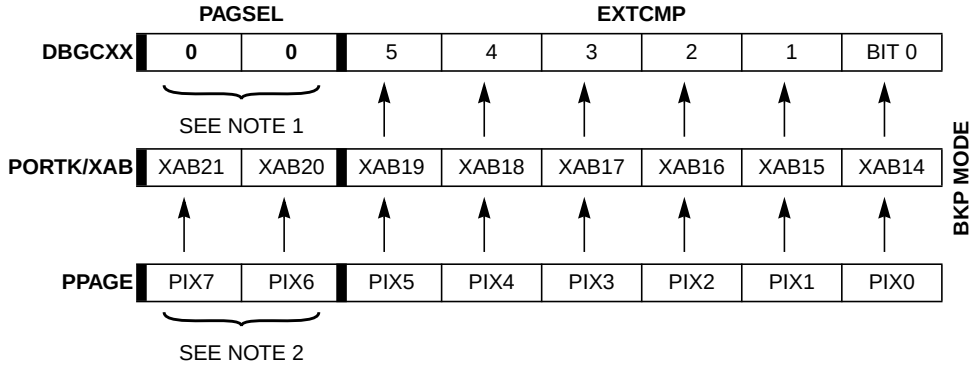
Field	Description
7:6 PAGSEL	**Page Selector Field** — If DBGEN is set in DBGC1, then PAGSEL selects the type of paging as shown in Table 19-20. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively). In BKP mode, PAGSEL has no meaning and EXTCMP[5:0] are compared to address bits [19:14] if the address is in the FLASH/ROM memory space.
5:0 EXTCMP	**Comparator A Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 19-20 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core.

Table 19-20. Comparator A or B Compares

Mode		EXTCMP Compare	High-Byte Compare
BKP[1]	Not FLASH/ROM access	No compare	DBGCxH[7:0] = AB[15:8]
	FLASH/ROM access	EXTCMP[5:0] = XAB[19:14]	DBGCxH[5:0] = AB[13:8]
DBG[2]	PAGSEL = 00	No compare	DBGCxH[7:0] = AB[15:8]
	PAGSEL = 01	EXTCMP[5:0] = XAB[21:16]	DBGCxH[7:0] = XAB[15:14], AB[13:8]

1 See Figure 19-16.

2 See Figure 19-10 (note that while this figure provides extended comparisons for comparator C, the figure also pertains to comparators A and B in DBG mode only).



NOTES:
1. In BKP mode, PAGSEL has no functionality. Therefore, set PAGSEL to 00 (reset state).
2. Current HCS12 implementations are limited to six PPAGE bits, PIX[5:0].

Figure 19-16. Comparators A and B Extended Comparison in BKP Mode

19.3.2.10 Debug Comparator A Register (DBGCA)

	15	14	13	12	11	10	9	8
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 19-17. Debug Comparator A Register High (DBGCAH)

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 19-18. Debug Comparator A Register Low (DBGCAL)

Table 19-21. DBGCA Field Descriptions

Field	Description
15:0 15:0	**Comparator A Compare Bits** — The comparator A compare bits control whether comparator A compares the address bus bits [15:0] to a logic 1 or logic 0. See Table 19-20. 0 Compare corresponding address bit to a logic 0 1 Compare corresponding address bit to a logic 1

19.3.2.11 Debug Comparator B Extended Register (DBGCBX)

	7	6	5	4	3	2	1	0
R W	PAGSEL		EXTCMP					
Reset	0	0	0	0	0	0	0	0

Figure 19-19. Debug Comparator B Extended Register (DBGCBX)

Table 19-22. DBGCBX Field Descriptions

Field	Description
7:6 PAGSEL	**Page Selector Field** — If DBGEN is set in DBGC1, then PAGSEL selects the type of paging as shown in Table 19-11. DPAGE and EPAGE are not yet implemented so the value in bit 7 will be ignored (i.e., PAGSEL values of 10 and 11 will be interpreted as values of 00 and 01, respectively.) In BKP mode, PAGSEL has no meaning and EXTCMP[5:0] are compared to address bits [19:14] if the address is in the FLASH/ROM memory space.
5:0 EXTCMP	**Comparator B Extended Compare Bits** — The EXTCMP bits are used as comparison address bits as shown in Table 19-11 along with the appropriate PPAGE, DPAGE, or EPAGE signal from the core. Also see Table 19-20.

19.3.2.12 Debug Comparator B Register (DBGCB)

	15	14	13	12	11	10	9	8
R W	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Reset	0	0	0	0	0	0	0	0

Figure 19-20. Debug Comparator B Register High (DBGCBH)

	7	6	5	4	3	2	1	0
R W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 19-21. Debug Comparator B Register Low (DBGCBL)

Table 19-23. DBGCB Field Descriptions

Field	Description
15:0 15:0	**Comparator B Compare Bits** — The comparator B compare bits control whether comparator B compares the address bus bits [15:0] or data bus bits [15:0] to a logic 1 or logic 0. See Table 19-20. 0 Compare corresponding address bit to a logic 0, compares to data if in Full mode 1 Compare corresponding address bit to a logic 1, compares to data if in Full mode

19.4 Functional Description

This section provides a complete functional description of the DBG module. The DBG module can be configured to run in either of two modes, BKP or DBG. BKP mode is enabled by setting BKABEN in DBGC2. DBG mode is enabled by setting DBGEN in DBGC1. Setting BKABEN in DBGC2 overrides the DBGEN in DBGC1 and prevents DBG mode. If the part is in secure mode, DBG mode cannot be enabled.

19.4.1 DBG Operating in BKP Mode

In BKP mode, the DBG will be fully backwards compatible with the existing BKP_ST12_A module. The DBGC2 register has four additional bits that were not available on existing BKP_ST12_A modules. As long as these bits are written to either all 1s or all 0s, they should be transparent to the user. All 1s would enable comparator C to be used as a breakpoint, but tagging would be enabled. The match address register would be all 0s if not modified by the user. Therefore, code executing at address 0x0000 would have to occur before a breakpoint based on comparator C would happen.

The DBG module in BKP mode supports two modes of operation: dual address mode and full breakpoint mode. Within each of these modes, forced or tagged breakpoint types can be used. Forced breakpoints occur at the next instruction boundary if a match occurs and tagged breakpoints allow for breaking just before the tagged instruction executes. The action taken upon a successful match can be to either place the CPU in background debug mode or to initiate a software interrupt.

The breakpoint can operate in dual address mode or full breakpoint mode. Each of these modes is discussed in the subsections below.

19.4.1.1 Dual Address Mode

When dual address mode is enabled, two address breakpoints can be set. Each breakpoint can cause the system to enter background debug mode or to initiate a software interrupt based upon the state of BDM in DBGC2 being logic 1 or logic 0, respectively. BDM requests have a higher priority than SWI requests. No data breakpoints are allowed in this mode.

TAGAB in DBGC2 selects whether the breakpoint mode is forced or tagged. The BKxMBH:L bits in DBGC3 select whether or not the breakpoint is matched exactly or is a range breakpoint. They also select whether the address is matched on the high byte, low byte, both bytes, and/or memory expansion. The RWx and RWxEN bits in DBGC3 select whether the type of bus cycle to match is a read, write, or read/write when performing forced breakpoints.

19.4.1.2 Full Breakpoint Mode

Full breakpoint mode requires a match on address and data for a breakpoint to occur. Upon a successful match, the system will enter background debug mode or initiate a software interrupt based upon the state of BDM in DBGC2 being logic 1 or logic 0, respectively. BDM requests have a higher priority than SWI requests. R/W matches are also allowed in this mode.

TAGAB in DBGC2 selects whether the breakpoint mode is forced or tagged. When TAGAB is set in DBGC2, only addresses are compared and data is ignored. The BKAMBH:L bits in DBGC3 select whether or not the breakpoint is matched exactly, is a range breakpoint, or is in page space. The BKBMBH:L bits in DBGC3 select whether the data is matched on the high byte, low byte, or both bytes. RWA and RWAEN bits in DBGC2 select whether the type of bus cycle to match is a read or a write when performing forced breakpoints. RWB and RWBEN bits in DBGC2 are not used in full breakpoint mode.

NOTE

The full trigger mode is designed to be used for either a word access or a byte access, but not both at the same time. Confusing trigger operation (seemingly false triggers or no trigger) can occur if the trigger address occurs in the user program as both byte and word accesses.

19.4.1.3 Breakpoint Priority

Breakpoint operation is first determined by the state of the BDM module. If the BDM module is already active, meaning the CPU is executing out of BDM firmware, breakpoints are not allowed. In addition, while executing a BDM TRACE command, tagging into BDM is not allowed. If BDM is not active, the breakpoint will give priority to BDM requests over SWI requests. This condition applies to both forced and tagged breakpoints.

In all cases, BDM related breakpoints will have priority over those generated by the Breakpoint sub-block. This priority includes breakpoints enabled by the $\overline{\text{TAGLO}}$ and $\overline{\text{TAGHI}}$ external pins of the system that interface with the BDM directly and whose signal information passes through and is used by the breakpoint sub-block.

NOTE

BDM should not be entered from a breakpoint unless the ENABLE bit is set in the BDM. Even if the ENABLE bit in the BDM is cleared, the CPU actually executes the BDM firmware code. It checks the ENABLE and returns if ENABLE is not set. If the BDM is not serviced by the monitor then the breakpoint would be re-asserted when the BDM returns to normal CPU flow.

There is no hardware to enforce restriction of breakpoint operation if the BDM is not enabled.

When program control returns from a tagged breakpoint through an RTI or a BDM GO command, it will return to the instruction whose tag generated the breakpoint. Unless breakpoints are disabled or modified in the service routine or active BDM session, the instruction will be tagged again and the breakpoint will be repeated. In the case of BDM breakpoints, this situation can also be avoided by executing a TRACE1 command before the GO to increment the program flow past the tagged instruction.

19.4.1.4 Using Comparator C in BKP Mode

The original BKP_ST12_A module supports two breakpoints. The DBG_ST12_A module can be used in BKP mode and allow a third breakpoint using comparator C. Four additional bits, BKCEN, TAGC, RWCEN, and RWC in DBGC2 in conjunction with additional comparator C address registers, DBGCCX, DBGCCH, and DBGCCL allow the user to set up a third breakpoint. Using PAGSEL in DBGCCX for expanded memory will work differently than the way paged memory is done using comparator A and B in BKP mode. See Section 19.3.2.5, “Debug Comparator C Extended Register (DBGCCX),” for more information on using comparator C.

19.4.2 DBG Operating in DBG Mode

Enabling the DBG module in DBG mode, allows the arming, triggering, and storing of data in the trace buffer and can be used to cause CPU breakpoints. The DBG module is made up of three main blocks, the comparators, trace buffer control logic, and the trace buffer.

NOTE

In general, there is a latency between the triggering event appearing on the bus and being detected by the DBG circuitry. In general, tagged triggers will be more predictable than forced triggers.

19.4.2.1 Comparators

The DBG contains three comparators, A, B, and C. Comparator A compares the core address bus with the address stored in DBGCAH and DBGCAL. Comparator B compares the core address bus with the address stored in DBGCBH and DBGCBL except in full mode, where it compares the data buses to the data stored in DBGCBH and DBGCBL. Comparator C can be used as a breakpoint generator or as the address comparison unit in the loop1 mode. Matches on comparator A, B, and C are signaled to the trace buffer

control (TBC) block. When PAGSEL = 01, registers DBGCAX, DBGCBX, and DBGCCX are used to match the upper addresses as shown in Table 19-11.

NOTE

If a tagged-type C breakpoint is set at the same address as an A/B tagged-type trigger (including the initial entry in an inside or outside range trigger), the C breakpoint will have priority and the trigger will not be recognized.

19.4.2.1.1 Read or Write Comparison

Read or write comparisons are useful only with TRGSEL = 0, because only opcodes should be tagged as they are “read” from memory. RWAEN and RWBEN are ignored when TRGSEL = 1.

In full modes (“A and B” and “A and not B”) RWAEN and RWA are used to select read or write comparisons for both comparators A and B. Table 19-24 shows the effect for RWAEN, RWA, and RW on the DBGCB comparison conditions. The RWBEN and RWB bits are not used and are ignored in full modes.

Table 19-24. Read or Write Comparison Logic Table

RWAEN bit	RWA bit	RW signal	Comment
0	x	0	Write data bus
0	x	1	Read data bus
1	0	0	Write data bus
1	0	1	No data bus compare since RW=1
1	1	0	No data bus compare since RW=0
1	1	1	Read data bus

19.4.2.1.2 Trigger Selection

The TRGSEL bit in DBGC1 is used to determine the triggering condition in DBG mode. TRGSEL applies to both trigger A and B except in the event only trigger modes. By setting TRGSEL, the comparators A and B will qualify a match with the output of opcode tracking logic and a trigger occurs before the tagged instruction executes (tagged-type trigger). With the TRGSEL bit cleared, a comparator match forces a trigger when the matching condition occurs (force-type trigger).

NOTE

If the TRGSEL is set, the address stored in the comparator match address registers must be an opcode address for the trigger to occur.

19.4.2.2 Trace Buffer Control (TBC)

The TBC is the main controller for the DBG module. Its function is to decide whether data should be stored in the trace buffer based on the trigger mode and the match signals from the comparator. The TBC also determines whether a request to break the CPU should occur.

19.4.2.3 Begin- and End-Trigger

The definitions of begin- and end-trigger as used in the DBG module are as follows:

- Begin-trigger: Storage in trace buffer occurs after the trigger and continues until 64 locations are filled.
- End-trigger: Storage in trace buffer occurs until the trigger, with the least recent data falling out of the trace buffer if more than 64 words are collected.

19.4.2.4 Arming the DBG Module

In DBG mode, arming occurs by setting DBGEN and ARM in DBGC1. The ARM bit in DBGC1 is cleared when the trigger condition is met in end-trigger mode or when the Trace Buffer is filled in begin-trigger mode. The TBC logic determines whether a trigger condition has been met based on the trigger mode and the trigger selection.

19.4.2.5 Trigger Modes

The DBG module supports nine trigger modes. The trigger modes are encoded as shown in Table 19-6. The trigger mode is used as a qualifier for either starting or ending the storing of data in the trace buffer. When the match condition is met, the appropriate flag A or B is set in DBGSC. Arming the DBG module clears the A, B, and C flags in DBGSC. In all trigger modes except for the event-only modes and DETAIL capture mode, change-of-flow addresses are stored in the trace buffer. In the event-only modes only the value on the data bus at the trigger event B will be stored. In DETAIL capture mode address and data for all cycles except program fetch (P) and free (f) cycles are stored in trace buffer.

19.4.2.5.1 A Only

In the A only trigger mode, if the match condition for A is met, the A flag in DBGSC is set and a trigger occurs.

19.4.2.5.2 A or B

In the A or B trigger mode, if the match condition for A or B is met, the corresponding flag in DBGSC is set and a trigger occurs.

19.4.2.5.3 A then B

In the A then B trigger mode, the match condition for A must be met before the match condition for B is compared. When the match condition for A or B is met, the corresponding flag in DBGSC is set. The trigger occurs only after A then B have matched.

NOTE

When tagging and using A then B, if addresses A and B are close together, then B may not complete the trigger sequence. This occurs when A and B are in the instruction queue at the same time. Basically the A trigger has not yet occurred, so the B instruction is not tagged. Generally, if address B is at

least six addresses higher than address A (or B is lower than A) and there are not changes of flow to put these in the queue at the same time, then this operation should trigger properly.

19.4.2.5.4 Event-Only B (Store Data)

In the event-only B trigger mode, if the match condition for B is met, the B flag in DBGSC is set and a trigger occurs. The event-only B trigger mode is considered a begin-trigger type and the BEGIN bit in DBGC1 is ignored. Event-only B is incompatible with instruction tagging (TRGSEL = 1), and thus the value of TRGSEL is ignored. Please refer to Section 19.4.2.7, “Storage Memory,” for more information.

This trigger mode is incompatible with the detail capture mode so the detail capture mode will have priority. TRGSEL and BEGIN will not be ignored and this trigger mode will behave as if it were “B only”.

19.4.2.5.5 A then Event-Only B (Store Data)

In the A then event-only B trigger mode, the match condition for A must be met before the match condition for B is compared, after the A match has occurred, a trigger occurs each time B matches. When the match condition for A or B is met, the corresponding flag in DBGSC is set. The A then event-only B trigger mode is considered a begin-trigger type and BEGIN in DBGC1 is ignored. TRGSEL in DBGC1 applies only to the match condition for A. Please refer to Section 19.4.2.7, “Storage Memory,” for more information.

This trigger mode is incompatible with the detail capture mode so the detail capture mode will have priority. TRGSEL and BEGIN will not be ignored and this trigger mode will be the same as A then B.

19.4.2.5.6 A and B (Full Mode)

In the A and B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and B trigger mode, if the match condition for A and B happen on the same bus cycle, both the A and B flags in the DBGSC register are set and a trigger occurs.

If TRGSEL = 1, only matches from comparator A are used to determine if the trigger condition is met and comparator B matches are ignored. If TRGSEL = 0, full-word data matches on an odd address boundary (misaligned access) do not work unless the access is to a RAM that manages misaligned accesses in a single clock cycle (which is typical of RAM modules used in HCS12 MCUs).

19.4.2.5.7 A and Not B (Full Mode)

In the A and not B trigger mode, comparator A compares to the address bus and comparator B compares to the data bus. In the A and not B trigger mode, if the match condition for A and not B happen on the same bus cycle, both the A and B flags in DBGSC are set and a trigger occurs.

If TRGSEL = 1, only matches from comparator A are used to determine if the trigger condition is met and comparator B matches are ignored. As described in Section 19.4.2.5.6, “A and B (Full Mode),” full-word data compares on misaligned accesses will not match expected data (and thus will cause a trigger in this mode) unless the access is to a RAM that manages misaligned accesses in a single clock cycle.

19.4.2.5.8 Inside Range (A ≤ address ≤ B)

In the inside range trigger mode, if the match condition for A and B happen on the same bus cycle, both the A and B flags in DBGSC are set and a trigger occurs. If a match condition on only A or only B occurs no flags are set. If TRGSEL = 1, the inside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is within the range.

19.4.2.5.9 Outside Range (address < A or address > B)

In the outside range trigger mode, if the match condition for A or B is met, the corresponding flag in DBGSC is set and a trigger occurs. If TRGSEL = 1, the outside range is accurate only to word boundaries. If TRGSEL = 0, an aligned word access which straddles the range boundary will cause a trigger only if the aligned address is outside the range.

19.4.2.5.10 Control Bit Priorities

The definitions of some of the control bits are incompatible with each other. Table 19-25 and the notes associated with it summarize how these incompatibilities are managed:

- Read/write comparisons are not compatible with TRGSEL = 1. Therefore, RWAEN and RWBEN are ignored.
- Event-only trigger modes are always considered a begin-type trigger. See Section 19.4.2.8.1, “Storing with Begin-Trigger,” and Section 19.4.2.8.2, “Storing with End-Trigger.”
- Detail capture mode has priority over the event-only trigger/capture modes. Therefore, event-only modes have no meaning in detail mode and their functions default to similar trigger modes.

Table 19-25. Resolution of Mode Conflicts

Mode	Normal / Loop1		Detail	
	Tag	Force	Tag	Force
A only				
A or B				
A then B				
Event-only B	1		1, 3	3
A then event-only B	2		4	4
A and B (full mode)	5		5	
A and not B (full mode)	5		5	
Inside range	6		6	
Outside range	6		6	

1 — Ignored — same as force
2 — Ignored for comparator B
3 — Reduces to effectively “B only”
4 — Works same as A then B
5 — Reduces to effectively “A only” — B not compared
6 — Only accurate to word boundaries

19.4.2.6 Capture Modes

The DBG in DBG mode can operate in four capture modes. These modes are described in the following subsections.

19.4.2.6.1 Normal Mode

In normal mode, the DBG module uses comparator A and B as triggering devices. Change-of-flow information or data will be stored depending on TRG in DBGSC.

19.4.2.6.2 Loop1 Mode

The intent of loop1 mode is to prevent the trace buffer from being filled entirely with duplicate information from a looping construct such as delays using the DBNE instruction or polling loops using BRSET/BRCLR instructions. Immediately after address information is placed in the trace buffer, the DBG module writes this value into the C comparator and the C comparator is placed in ignore address mode. This will prevent duplicate address entries in the trace buffer resulting from repeated bit-conditional branches. Comparator C will be cleared when the ARM bit is set in loop1 mode to prevent the previous contents of the register from interfering with loop1 mode operation. Breakpoints based on comparator C are disabled.

Loop1 mode only inhibits duplicate source address entries that would typically be stored in most tight looping constructs. It will not inhibit repeated entries of destination addresses or vector addresses, because repeated entries of these would most likely indicate a bug in the user's code that the DBG module is designed to help find.

NOTE

In certain very tight loops, the source address will have already been fetched again before the C comparator is updated. This results in the source address being stored twice before further duplicate entries are suppressed. This condition occurs with branch-on-bit instructions when the branch is fetched by the first P-cycle of the branch or with loop-construct instructions in which the branch is fetched with the first or second P cycle. See examples below:

```
LOOP  INCX                    ; 1-byte instruction fetched by 1st P-cycle of BRCLR
      BRCLR CMPTMP,#$0c,LOOP  ; the BRCLR instruction also will be fetched by 1st P-cycle of BRCLR

LOOP2 BRN   *                 ; 2-byte instruction fetched by 1st P-cycle of DBNE
      NOP                     ; 1-byte instruction fetched by 2nd P-cycle of DBNE
      DBNE  A,LOOP2           ; this instruction also fetched by 2nd P-cycle of DBNE
```

NOTE

Loop1 mode does not support paged memory, and inhibits duplicate entries in the trace buffer based solely on the CPU address. There is a remote possibility of an erroneous address match if program flow alternates between paged and unpaged memory space.

19.4.2.6.3 Detail Mode

In the detail mode, address and data for all cycles except program fetch (P) and free (f) cycles are stored in trace buffer. This mode is intended to supply additional information on indexed, indirect addressing modes where storing only the destination address would not provide all information required for a user to determine where his code was in error.

19.4.2.6.4 Profile Mode

This mode is intended to allow a host computer to poll a running target and provide a histogram of program execution. Each read of the trace buffer address will return the address of the last instruction executed. The DBGCNT register is not incremented and the trace buffer does not get filled. The ARM bit is not used and all breakpoints and all other debug functions will be disabled.

19.4.2.7 Storage Memory

The storage memory is a 64 words deep by 16-bits wide dual port RAM array. The CPU accesses the RAM array through a single memory location window (DBGTBH:DBGTBL). The DBG module stores trace information in the RAM array in a circular buffer format. As data is read via the CPU, a pointer into the RAM will increment so that the next CPU read will receive fresh information. In all trigger modes except for event-only and detail capture mode, the data stored in the trace buffer will be change-of-flow addresses. change-of-flow addresses are defined as follows:

- Source address of conditional branches (long, short, BRSET, and loop constructs) taken
- Destination address of indexed JMP, JSR, and CALL instruction
- Destination address of RTI, RTS, and RTC instructions
- Vector address of interrupts except for SWI and BDM vectors

In the event-only trigger modes only the 16-bit data bus value corresponding to the event is stored. In the detail capture mode, address and then data are stored for all cycles except program fetch (P) and free (f) cycles.

19.4.2.8 Storing Data in Memory Storage Buffer

19.4.2.8.1 Storing with Begin-Trigger

Storing with begin-trigger can be used in all trigger modes. When DBG mode is enabled and armed in the begin-trigger mode, data is not stored in the trace buffer until the trigger condition is met. As soon as the trigger condition is met, the DBG module will remain armed until 64 words are stored in the trace buffer. If the trigger is at the address of the change-of-flow instruction the change-of-flow associated with the trigger event will be stored in the trace buffer.

19.4.2.8.2 Storing with End-Trigger

Storing with end-trigger cannot be used in event-only trigger modes. When DBG mode is enabled and armed in the end-trigger mode, data is stored in the trace buffer until the trigger condition is met. When the trigger condition is met, the DBG module will become de-armed and no more data will be stored. If

the trigger is at the address of a change-of-flow address the trigger event will not be stored in the trace buffer.

19.4.2.9 Reading Data from Trace Buffer

The data stored in the trace buffer can be read using either the background debug module (BDM) module or the CPU provided the DBG module is enabled and not armed. The trace buffer data is read out first-in first-out. By reading CNT in DBGCNT the number of valid words can be determined. CNT will not decrement as data is read from DBGTBH:DBGTBL. The trace buffer data is read by reading DBGTBH:DBGTBL with a 16-bit read. Each time DBGTBH:DBGTBL is read, a pointer in the DBG will be incremented to allow reading of the next word.

Reading the trace buffer while the DBG module is armed will return invalid data and no shifting of the RAM pointer will occur.

NOTE

The trace buffer should be read with the DBG module enabled and in the same capture mode that the data was recorded. The contents of the trace buffer counter register (DBGCNT) are resolved differently in detail mode verses the other modes and may lead to incorrect interpretation of the trace buffer data.

19.4.3 Breakpoints

There are two ways of getting a breakpoint in DBG mode. One is based on the trigger condition of the trigger mode using comparator A and/or B, and the other is using comparator C. External breakpoints generated using the $\overline{\text{TAGHI}}$ and $\overline{\text{TAGLO}}$ external pins are disabled in DBG mode.

19.4.3.1 Breakpoint Based on Comparator A and B

A breakpoint request to the CPU can be enabled by setting DBGBRK in DBGC1. The value of BEGIN in DBGC1 determines when the breakpoint request to the CPU will occur. When BEGIN in DBGC1 is set, begin-trigger is selected and the breakpoint request will not occur until the trace buffer is filled with 64 words. When BEGIN in DBGC1 is cleared, end-trigger is selected and the breakpoint request will occur immediately at the trigger cycle.

There are two types of breakpoint requests supported by the DBG module, tagged and forced. Tagged breakpoints are associated with opcode addresses and allow breaking just before a specific instruction executes. Forced breakpoints are not associated with opcode addresses and allow breaking at the next instruction boundary. The type of breakpoint based on comparators A and B is determined by TRGSEL in the DBGC1 register (TRGSEL = 1 for tagged breakpoint, TRGSEL = 0 for forced breakpoint). Table 19-26 illustrates the type of breakpoint that will occur based on the debug run.

Table 19-26. Breakpoint Setup

BEGIN	TRGSEL	DBGBRK	Type of Debug Run
0	0	0	Fill trace buffer until trigger address (no CPU breakpoint — keep running)
0	0	1	Fill trace buffer until trigger address, then a forced breakpoint request occurs
0	1	0	Fill trace buffer until trigger opcode is about to execute (no CPU breakpoint — keep running)
0	1	1	Fill trace buffer until trigger opcode about to execute, then a tagged breakpoint request occurs
1	0	0	Start trace buffer at trigger address (no CPU breakpoint — keep running)
1	0	1	Start trace buffer at trigger address, a forced breakpoint request occurs when trace buffer is full
1	1	0	Start trace buffer at trigger opcode (no CPU breakpoint — keep running)
1	1	1	Start trace buffer at trigger opcode, a forced breakpoint request occurs when trace buffer is full

19.4.3.2 Breakpoint Based on Comparator C

A breakpoint request to the CPU can be created if BKCEN in DBGC2 is set. Breakpoints based on a successful comparator C match can be accomplished regardless of the mode of operation for comparator A or B, and do not affect the status of the ARM bit. TAGC in DBGC2 is used to select either tagged or forced breakpoint requests for comparator C. Breakpoints based on comparator C are disabled in LOOP1 mode.

NOTE

Because breakpoints cannot be disabled when the DBG is armed, one must be careful to avoid an “infinite breakpoint loop” when using tagged-type C breakpoints while the DBG is armed. If BDM breakpoints are selected, executing a TRACE1 instruction before the GO instruction is the recommended way to avoid re-triggering a breakpoint if one does not wish to de-arm the DBG. If SWI breakpoints are selected, disarming the DBG in the SWI interrupt service routine is the recommended way to avoid re-triggering a breakpoint.

19.5 Resets

The DBG module is disabled after reset.

The DBG module cannot cause a MCU reset.

19.6 Interrupts

The DBG contains one interrupt source. If a breakpoint is requested and BDM in DBGC2 is cleared, an SWI interrupt will be generated.

Chapter 20
Interrupt (INTV1)

20.1 Introduction

This section describes the functionality of the interrupt (INT) sub-block of the S12 core platform.

A block diagram of the interrupt sub-block is shown in Figure 20-1.

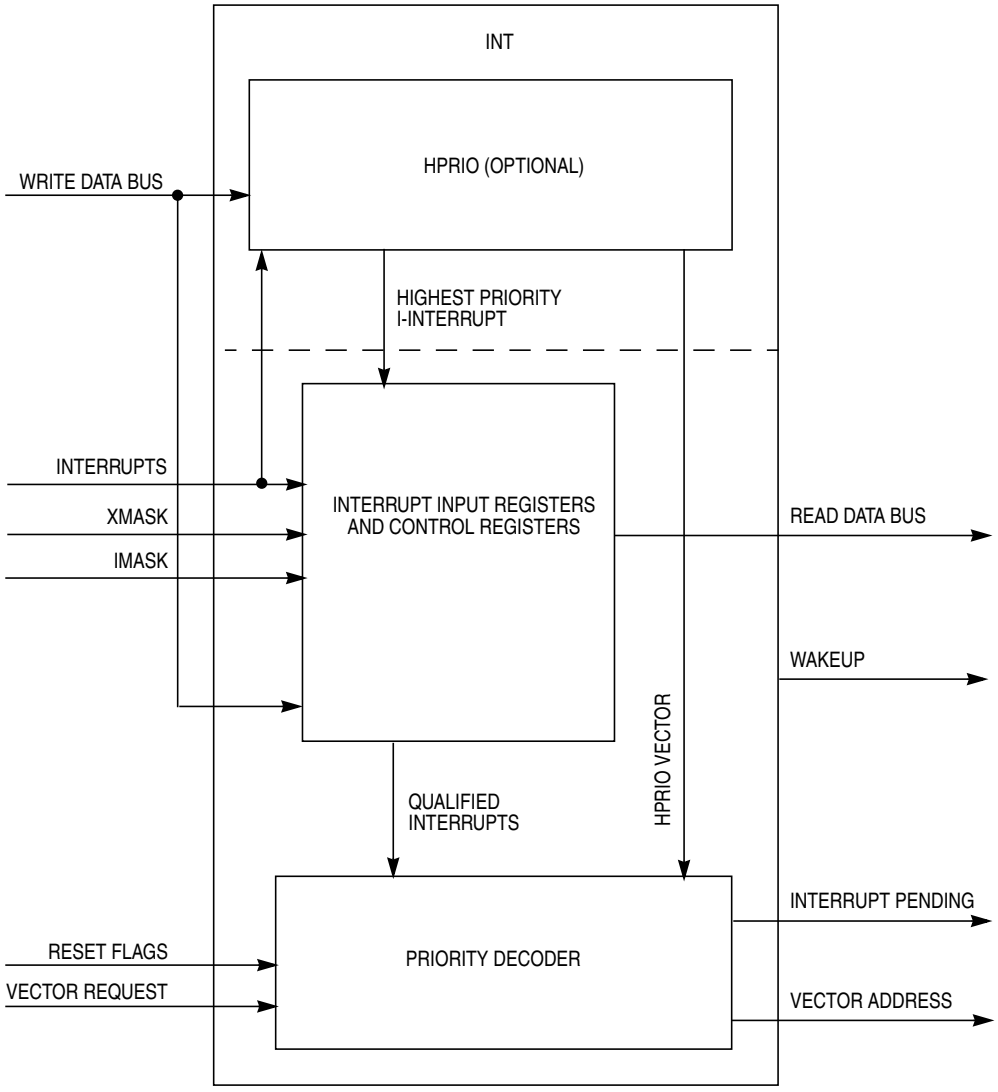


Figure 20-1. INT Block Diagram

The interrupt sub-block decodes the priority of all system exception requests and provides the applicable vector for processing the exception. The INT supports I-bit maskable and X-bit maskable interrupts, a non-maskable unimplemented opcode trap, a non-maskable software interrupt (SWI) or background debug mode request, and three system reset vector requests. All interrupt related exception requests are managed by the interrupt sub-block (INT).

20.1.1 Features

The INT includes these features:

- Provides two to 122 I-bit maskable interrupt vectors (0xFF00–0xFFF2)
- Provides one X-bit maskable interrupt vector (0xFFF4)
- Provides a non-maskable software interrupt (SWI) or background debug mode request vector (0xFFF6)
- Provides a non-maskable unimplemented opcode trap (TRAP) vector (0xFFF8)
- Provides three system reset vectors (0xFFFA–0xFFFE) (reset, CMR, and COP)
- Determines the appropriate vector and drives it onto the address bus at the appropriate time
- Signals the CPU that interrupts are pending
- Provides control registers which allow testing of interrupts
- Provides additional input signals which prevents requests for servicing I and X interrupts
- Wakes the system from stop or wait mode when an appropriate interrupt occurs or whenever $\overline{\text{XIRQ}}$ is active, even if $\overline{\text{XIRQ}}$ is masked
- Provides asynchronous path for all I and X interrupts, (0xFF00–0xFFF4)
- (Optional) selects and stores the highest priority I interrupt based on the value written into the HPRIO register

20.1.2 Modes of Operation

The functionality of the INT sub-block in various modes of operation is discussed in the subsections that follow.

- **Normal operation**

  The INT operates the same in all normal modes of operation.
- **Special operation**

  Interrupts may be tested in special modes through the use of the interrupt test registers.
- **Emulation modes**

  The INT operates the same in emulation modes as in normal modes.
- **Low power modes**

  See Section 20.4.1, “Low-Power Modes,” for details

20.2 External Signal Description

Most interfacing with the interrupt sub-block is done within the core. However, the interrupt does receive direct input from the multiplexed external bus interface (MEBI) sub-block of the core for the $\overline{IRQ}$ and $\overline{XIRQ}$ pin data.

20.3 Memory Map and Register Definition

Detailed descriptions of the registers and associated bits are given in the subsections that follow.

20.3.1 Module Memory Map

Table 20-1. INT Memory Map

Address Offset	Use	Access
0x0015	Interrupt Test Control Register (ITCR)	R/W
0x0016	Interrupt Test Registers (ITEST)	R/W
0x001F	Highest Priority Interrupt (Optional) (HPRIO)	R/W

20.3.2 Register Descriptions

20.3.2.1 Interrupt Test Control Register

	7	6	5	4	3	2	1	0
R	0	0	0	WRTINT	ADR3	ADR2	ADR1	ADR0
W								
Reset	0	0	0	0	1	1	1	1

= Unimplemented or Reserved

Figure 20-2. Interrupt Test Control Register (ITCR)

Read: See individual bit descriptions

Write: See individual bit descriptions

Table 20-2. ITCR Field Descriptions

Field	Description
4 WRTINT	**Write to the Interrupt Test Registers** Read: anytime Write: only in special modes and with I-bit mask and X-bit mask set. 0 Disables writes to the test registers; reads of the test registers will return the state of the interrupt inputs. 1 Disconnect the interrupt inputs from the priority decoder and use the values written into the ITEST registers instead. **Note:** Any interrupts which are pending at the time that WRTINT is set will remain until they are overwritten.
3:0 ADR[3:0]	**Test Register Select Bits** Read: anytime Write: anytime These bits determine which test register is selected on a read or write. The hexadecimal value written here will be the same as the upper nibble of the lower byte of the vector selects. That is, an “F” written into ADR[3:0] will select vectors 0xFFFE–0xFFF0 while a “7” written to ADR[3:0] will select vectors 0xFF7E–0xFF70.

20.3.2.2 Interrupt Test Registers

	7	6	5	4	3	2	1	0
R W	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 20-3. Interrupt TEST Registers (ITEST)

Read: Only in special modes. Reads will return either the state of the interrupt inputs of the interrupt sub-block (WRTINT = 0) or the values written into the TEST registers (WRTINT = 1). Reads will always return 0s in normal modes.

Write: Only in special modes and with WRTINT = 1 and CCR I mask = 1.

Table 20-3. ITEST Field Descriptions

Field	Description
7:0 INT[E:0]	**Interrupt TEST Bits** — These registers are used in special modes for testing the interrupt logic and priority independent of the system configuration. Each bit is used to force a specific interrupt vector by writing it to a logic 1 state. Bits are named INTE through INT0 to indicate vectors 0xFFxE through 0xFFx0. These bits can be written only in special modes and only with the WRTINT bit set (logic 1) in the interrupt test control register (ITCR). In addition, I interrupts must be masked using the I bit in the CCR. In this state, the interrupt input lines to the interrupt sub-block will be disconnected and interrupt requests will be generated only by this register. These bits can also be read in special modes to view that an interrupt requested by a system block (such as a peripheral block) has reached the INT module. There is a test register implemented for every eight interrupts in the overall system. All of the test registers share the same address and are individually selected using the value stored in the ADR[3:0] bits of the interrupt test control register (ITCR). **Note:** When ADR[3:0] have the value of 0x000F, only bits 2:0 in the ITEST register will be accessible. That is, vectors higher than 0xFFF4 cannot be tested using the test registers and bits 7:3 will always read as a logic 0. If ADR[3:0] point to an unimplemented test register, writes will have no effect and reads will always return a logic 0 value.

20.3.2.3 Highest Priority I Interrupt (Optional)

	7	6	5	4	3	2	1	0
R	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
W								
Reset	1	1	1	1	0	0	1	0

= Unimplemented or Reserved

Figure 20-4. Highest Priority I Interrupt Register (HPRIO)

Read: Anytime

Write: Only if I mask in CCR = 1

Table 20-4. HPRIO Field Descriptions

Field	Description
7:1 PSEL[7:1]	**Highest Priority I Interrupt Select Bits** — The state of these bits determines which I-bit maskable interrupt will be promoted to highest priority (of the I-bit maskable interrupts). To promote an interrupt, the user writes the least significant byte of the associated interrupt vector address to this register. If an unimplemented vector address or a non I-bit masked vector address (value higher than 0x00F2) is written, IRQ (0xFFF2) will be the default highest priority interrupt.

20.4 Functional Description

The interrupt sub-block processes all exception requests made by the CPU. These exceptions include interrupt vector requests and reset vector requests. Each of these exception types and their overall priority level is discussed in the subsections below.

20.4.1 Low-Power Modes

The INT does not contain any user-controlled options for reducing power consumption. The operation of the INT in low-power modes is discussed in the following subsections.

20.4.1.1 Operation in Run Mode

The INT does not contain any options for reducing power in run mode.

20.4.1.2 Operation in Wait Mode

Clocks to the INT can be shut off during system wait mode and the asynchronous interrupt path will be used to generate the wake-up signal upon recognition of a valid interrupt or any $\overline{\text{XIRQ}}$ request.

20.4.1.3 Operation in Stop Mode

Clocks to the INT can be shut off during system stop mode and the asynchronous interrupt path will be used to generate the wake-up signal upon recognition of a valid interrupt or any $\overline{\text{XIRQ}}$ request.

20.5 Resets

The INT supports three system reset exception request types: normal system reset or power-on-reset request, crystal monitor reset request, and COP watchdog reset request. The type of reset exception request must be decoded by the system and the proper request made to the core. The INT will then provide the service routine address for the type of reset requested.

20.6 Interrupts

As shown in the block diagram in Figure 20-1, the INT contains a register block to provide interrupt status and control, an optional highest priority I interrupt (HPRIO) block, and a priority decoder to evaluate whether pending interrupts are valid and assess their priority.

20.6.1 Interrupt Registers

The INT registers are accessible only in special modes of operation and function as described in Section 20.3.2.1, “Interrupt Test Control Register,” and Section 20.3.2.2, “Interrupt Test Registers,” previously.

20.6.2 Highest Priority I-Bit Maskable Interrupt

When the optional HPRIO block is implemented, the user is allowed to promote a single I-bit maskable interrupt to be the highest priority I interrupt. The HPRIO evaluates all interrupt exception requests and passes the HPRIO vector to the priority decoder if the highest priority I interrupt is active. RTI replaces the promoted interrupt source.

20.6.3 Interrupt Priority Decoder

The priority decoder evaluates all interrupts pending and determines their validity and priority. When the CPU requests an interrupt vector, the decoder will provide the vector for the highest priority interrupt request. Because the vector is not supplied until the CPU requests it, it is possible that a higher priority interrupt request could override the original exception that caused the CPU to request the vector. In this case, the CPU will receive the highest priority vector and the system will process this exception instead of the original request.

NOTE

Care must be taken to ensure that all exception requests remain active until the system begins execution of the applicable service routine; otherwise, the exception request may not be processed.

If for any reason the interrupt source is unknown (e.g., an interrupt request becomes inactive after the interrupt has been recognized but prior to the vector request), the vector address will default to that of the last valid interrupt that existed during the particular interrupt sequence. If the CPU requests an interrupt vector when there has never been a pending interrupt request, the INT will provide the software interrupt (SWI) vector address.

20.7 Exception Priority

The priority (from highest to lowest) and address of all exception vectors issued by the INT upon request by the CPU is shown in Table 20-5.

Table 20-5. Exception Vector Map and Priority

Vector Address	Source
0xFFFE–0xFFFF	System reset
0xFFFC–0xFFFD	Crystal monitor reset
0xFFFA–0xFFFB	COP reset
0xFFF8–0xFFF9	Unimplemented opcode trap
0xFFF6–0xFFF7	Software interrupt instruction (SWI) or BDM vector request
0xFFF4–0xFFF5	$\overline{\text{XIRQ}}$ signal
0xFFF2–0xFFF3	$\overline{\text{IRQ}}$ signal
0xFFF0–0xFF00	Device-specific I-bit maskable interrupt sources (priority in descending order)

Chapter 21
Multiplexed External Bus Interface (MEBIV3)

21.1 Introduction

This section describes the functionality of the multiplexed external bus interface (MEBI) sub-block of the S12 core platform. The functionality of the module is closely coupled with the S12 CPU and the memory map controller (MMC) sub-blocks.

Figure 21-1 is a block diagram of the MEBI. In Figure 21-1, the signals on the right hand side represent pins that are accessible externally. On some chips, these may not all be bonded out.

The MEBI sub-block of the core serves to provide access and/or visibility to internal core data manipulation operations including timing reference information at the external boundary of the core and/or system. Depending upon the system operating mode and the state of bits within the control registers of the MEBI, the internal 16-bit read and write data operations will be represented in 8-bit or 16-bit accesses externally. Using control information from other blocks within the system, the MEBI will determine the appropriate type of data access to be generated.

21.1.1 Features

The block name includes these distinctive features:

- External bus controller with four 8-bit ports A,B, E, and K
- Data and data direction registers for ports A, B, E, and K when used as general-purpose I/O
- Control register to enable/disable alternate functions on ports E and K
- Mode control register
- Control register to enable/disable pull resistors on ports A, B, E, and K
- Control register to enable/disable reduced output drive on ports A, B, E, and K
- Control register to configure external clock behavior
- Control register to configure $\overline{\text{IRQ}}$ pin operation
- Logic to capture and synchronize external interrupt pin inputs

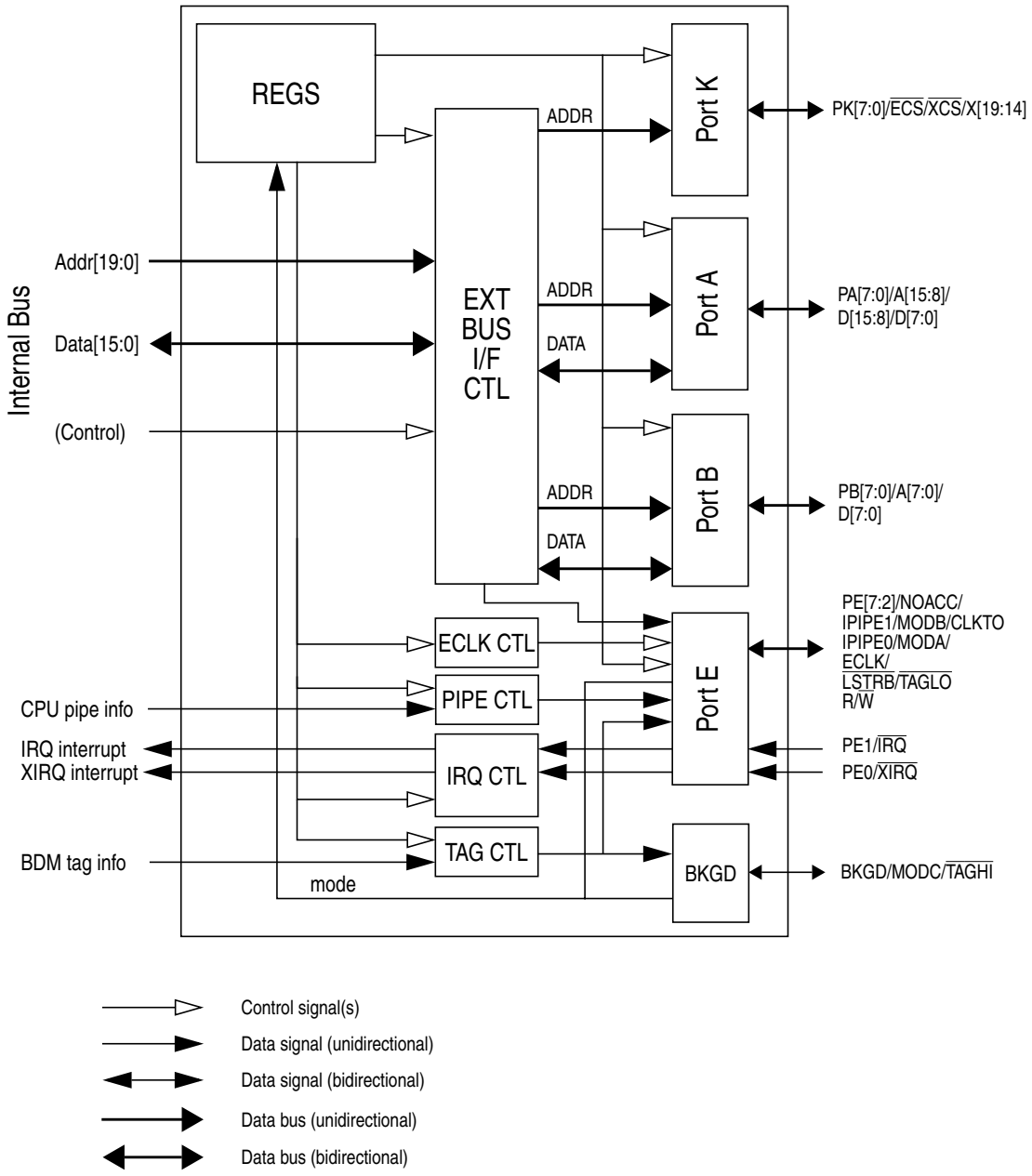


Figure 21-1. MEBI Block Diagram

21.1.2 Modes of Operation

- Normal expanded wide mode

  Ports A and B are configured as a 16-bit multiplexed address and data bus and port E provides bus control and status signals. This mode allows 16-bit external memory and peripheral devices to be interfaced to the system.
- Normal expanded narrow mode

  Ports A and B are configured as a 16-bit address bus and port A is multiplexed with 8-bit data. Port E provides bus control and status signals. This mode allows 8-bit external memory and peripheral devices to be interfaced to the system.
- Normal single-chip mode

  There is no external expansion bus in this mode. The processor program is executed from internal memory. Ports A, B, K, and most of E are available as general-purpose I/O.
- Special single-chip mode

  This mode is generally used for debugging single-chip operation, boot-strapping, or security related operations. The active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. There is no external expansion bus after reset in this mode.
- Emulation expanded wide mode

  Developers use this mode for emulation systems in which the users target application is normal expanded wide mode.
- Emulation expanded narrow mode

  Developers use this mode for emulation systems in which the users target application is normal expanded narrow mode.
- Special test mode

  Ports A and B are configured as a 16-bit multiplexed address and data bus and port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.
- Special peripheral mode

  This mode is intended for Freescale Semiconductor factory testing of the system. The CPU is inactive and an external (tester) bus master drives address, data, and bus control signals.

21.2 External Signal Description

In typical implementations, the MEBI sub-block of the core interfaces directly with external system pins. Some pins may not be bonded out in all implementations.

Table 21-1 outlines the pin names and functions and gives a brief description of their operation reset state of these pins and associated pull-ups or pull-downs is dependent on the mode of operation and on the integration of this block at the chip level (chip dependent).

Table 21-1. External System Pins Associated With MEBI

Pin Name	Pin Functions	Description
BKGD/MODC/ $\overline{\text{TAGHI}}$	MODC	At the rising edge on $\overline{\text{RESET}}$, the state of this pin is registered into the MODC bit to set the mode. (This pin always has an internal pullup.)
	BKGD	Pseudo open-drain communication pin for the single-wire background debug mode. There is an internal pull-up resistor on this pin.
	$\overline{\text{TAGHI}}$	When instruction tagging is on, a 0 at the falling edge of E tags the high half of the instruction word being read into the instruction queue.
PA7/A15/D15/D7 thru PA0/A8/D8/D0	PA7–PA0	General-purpose I/O pins, see PORTA and DDRA registers.
	A15–A8	High-order address lines multiplexed during ECLK low. Outputs except in special peripheral mode where they are inputs from an external tester system.
	D15–D8	High-order bidirectional data lines multiplexed during ECLK high in expanded wide modes, special peripheral mode, and visible internal accesses (IVIS = 1) in emulation expanded narrow mode. Direction of data transfer is generally indicated by R/$\overline{\text{W}}$.
	D15/D7 thru D8/D0	Alternate high-order and low-order bytes of the bidirectional data lines multiplexed during ECLK high in expanded narrow modes and narrow accesses in wide modes. Direction of data transfer is generally indicated by R/$\overline{\text{W}}$.
PB7/A7/D7 thru PB0/A0/D0	PB7–PB0	General-purpose I/O pins, see PORTB and DDRB registers.
	A7–A0	Low-order address lines multiplexed during ECLK low. Outputs except in special peripheral mode where they are inputs from an external tester system.
	D7–D0	Low-order bidirectional data lines multiplexed during ECLK high in expanded wide modes, special peripheral mode, and visible internal accesses (with IVIS = 1) in emulation expanded narrow mode. Direction of data transfer is generally indicated by R/$\overline{\text{W}}$.
PE7/NOACC	PE7	General-purpose I/O pin, see PORTE and DDRE registers.
	NOACC	CPU No Access output. Indicates whether the current cycle is a free cycle. Only available in expanded modes.
PE6/IPIPE1/ MODB/CLKTO	MODB	At the rising edge of $\overline{\text{RESET}}$, the state of this pin is registered into the MODB bit to set the mode.
	PE6	General-purpose I/O pin, see PORTE and DDRE registers.
	IPIPE1	Instruction pipe status bit 1, enabled by PIPOE bit in PEAR.
	CLKTO	System clock test output. Only available in special modes. PIPOE = 1 overrides this function. The enable for this function is in the clock module.
PE5/IPIPE0/MODA	MODA	At the rising edge on $\overline{\text{RESET}}$, the state of this pin is registered into the MODA bit to set the mode.
	PE5	General-purpose I/O pin, see PORTE and DDRE registers.
	IPIPE0	Instruction pipe status bit 0, enabled by PIPOE bit in PEAR.

Table 21-1. External System Pins Associated With MEBI (continued)

Pin Name	Pin Functions	Description
PE4/ECLK	PE4	General-purpose I/O pin, see PORTE and DDRE registers.
	ECLK	Bus timing reference clock, can operate as a free-running clock at the system clock rate or to produce one low-high clock per visible access, with the high period stretched for slow accesses. ECLK is controlled by the NECLK bit in PEAR, the IVIS bit in MODE, and the ESTR bit in EBICTL.
PE3/$\overline{\text{LSTRB}}$/ $\overline{\text{TAGLO}}$	PE3	General-purpose I/O pin, see PORTE and DDRE registers.
	$\overline{\text{LSTRB}}$	Low strobe bar, 0 indicates valid data on D7–D0.
	SZ8	In special peripheral mode, this pin is an input indicating the size of the data transfer (0 = 16-bit; 1 = 8-bit).
	$\overline{\text{TAGLO}}$	In expanded wide mode or emulation narrow modes, when instruction tagging is on and low strobe is enabled, a 0 at the falling edge of E tags the low half of the instruction word being read into the instruction queue.
PE2/R/$\overline{\text{W}}$	PE2	General-purpose I/O pin, see PORTE and DDRE registers.
	R/$\overline{\text{W}}$	Read/write, indicates the direction of internal data transfers. This is an output except in special peripheral mode where it is an input.
PE1/$\overline{\text{IRQ}}$	PE1	General-purpose input-only pin, can be read even if $\overline{\text{IRQ}}$ enabled.
	$\overline{\text{IRQ}}$	Maskable interrupt request, can be level sensitive or edge sensitive.
PE0/$\overline{\text{XIRQ}}$	PE0	General-purpose input-only pin.
	$\overline{\text{XIRQ}}$	Non-maskable interrupt input.
PK7/$\overline{\text{ECS}}$	PK7	General-purpose I/O pin, see PORTK and DDRK registers.
	$\overline{\text{ECS}}$	Emulation chip select
PK6/$\overline{\text{XCS}}$	PK6	General-purpose I/O pin, see PORTK and DDRK registers.
	$\overline{\text{XCS}}$	External data chip select
PK5/X19 thru PK0/X14	PK5–PK0	General-purpose I/O pins, see PORTK and DDRK registers.
	X19–X14	Memory expansion addresses

Detailed descriptions of these pins can be found in the device overview chapter.

21.3 Memory Map and Register Definition

A summary of the registers associated with the MEBI sub-block is shown in Table 21-2. Detailed descriptions of the registers and bits are given in the subsections that follow. On most chips the registers are mappable. Therefore, the upper bits may not be all 0s as shown in the table and descriptions.

21.3.1 Module Memory Map

Table 21-2. MEBI Memory Map

Address Offset	Use	Access
0x0000	Port A Data Register (PORTA)	R/W
0x0001	Port B Data Register (PORTB)	R/W
0x0002	Data Direction Register A (DDRA)	R/W
0x0003	Data Direction Register B (DDRB)	R/W
0x0004	Reserved	R
0x0005	Reserved	R
0x0006	Reserved	R
0x0007	Reserved	R
0x0008	Port E Data Register (PORTE)	R/W
0x0009	Data Direction Register E (DDRE)	R/W
0x000A	Port E Assignment Register (PEAR)	R/W
0x000B	Mode Register (MODE)	R/W
0x000C	Pull Control Register (PUCR)	R/W
0x000D	Reduced Drive Register (RDRIV)	R/W
0x000E	External Bus Interface Control Register (EBICTL)	R/W
0x000F	Reserved	R
0x001E	IRQ Control Register (IRQCR)	R/W
0x00032	Port K Data Register (PORTK)	R/W
0x00033	Data Direction Register K (DDRK)	R/W

21.3.2 Register Descriptions

21.3.2.1 Port A Data Register (PORTA)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0
Single Chip	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Expanded Wide, Emulation Narrow with IVIS, and Peripheral	AB/DB15	AB/DB14	AB/DB13	AB/DB12	AB/DB11	AB/DB10	AB/DB9	AB/DB8
Expanded Narrow	AB15 and DB15/DB7	AB14 and DB14/DB6	AB13 and DB13/DB5	AB12 and DB12/DB4	AB11 and DB11/DB3	AB10 and DB10/DB2	AB9 and DB9/DB1	AB8 and DB8/DB0

Figure 21-2. Port A Data Register (PORTA)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Port A bits 7 through 0 are associated with address lines A15 through A8 respectively and data lines D15/D7 through D8/D0 respectively. When this port is not used for external addresses such as in single-chip mode, these pins can be used as general-purpose I/O. Data direction register A (DDRA) determines the primary direction of each pin. DDRA also determines the source of data for a read of PORTA.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

NOTE

To ensure that you read the value present on the PORTA pins, always wait at least one cycle after writing to the DDRA register before reading from the PORTA register.

21.3.2.2 Port B Data Register (PORTB)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0
Single Chip	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Expanded Wide, Emulation Narrow with IVIS, and Peripheral	AB/DB7	AB/DB6	AB/DB5	AB/DB4	AB/DB3	AB/DB2	AB/DB1	AB/DB0
Expanded Narrow	AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0

Figure 21-3. Port A Data Register (PORTB)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Port B bits 7 through 0 are associated with address lines A7 through A0 respectively and data lines D7 through D0 respectively. When this port is not used for external addresses, such as in single-chip mode, these pins can be used as general-purpose I/O. Data direction register B (DDRB) determines the primary direction of each pin. DDRB also determines the source of data for a read of PORTB.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

NOTE

To ensure that you read the value present on the PORTB pins, always wait at least one cycle after writing to the DDRB register before reading from the PORTB register.

21.3.2.3 Data Direction Register A (DDRA)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 21-4. Data Direction Register A (DDRA)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

This register controls the data direction for port A. When port A is operating as a general-purpose I/O port, DDRA determines the primary direction for each port A pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTA register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. It is reset to 0x00 so the DDR does not override the three-state control signals.

Table 21-3. DDRA Field Descriptions

Field	Description
7:0 DDRA	**Data Direction Port A** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output

21.3.2.4 Data Direction Register B (DDRB)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 21-5. Data Direction Register B (DDRB)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

This register controls the data direction for port B. When port B is operating as a general-purpose I/O port, DDRB determines the primary direction for each port B pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTB register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. It is reset to 0x00 so the DDR does not override the three-state control signals.

Table 21-4. DDRB Field Descriptions

Field	Description
7:0 DDRB	**Data Direction Port B** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output

21.3.2.5 Reserved Registers

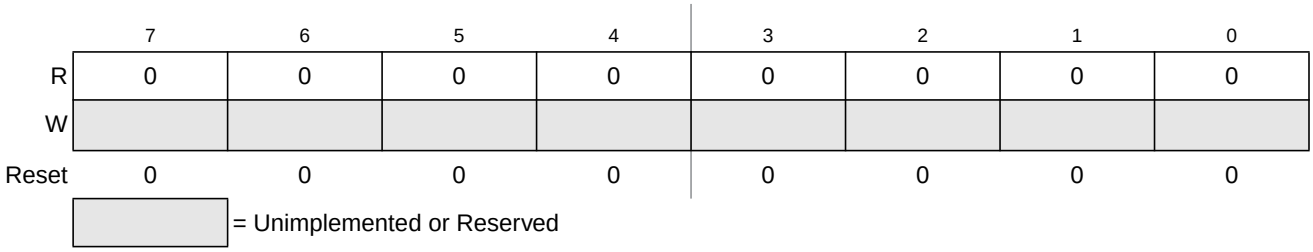


Figure 21-6. Reserved Register

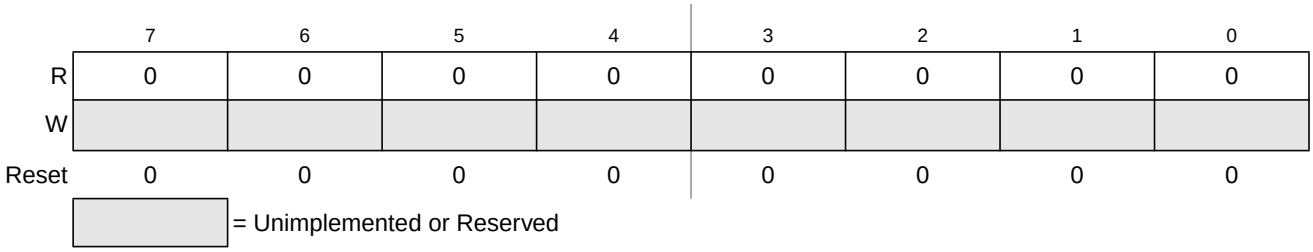


Figure 21-7. Reserved Register

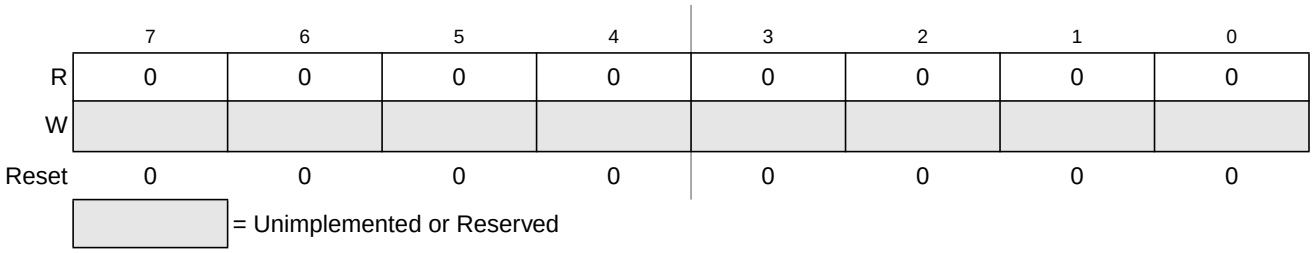


Figure 21-8. Reserved Register

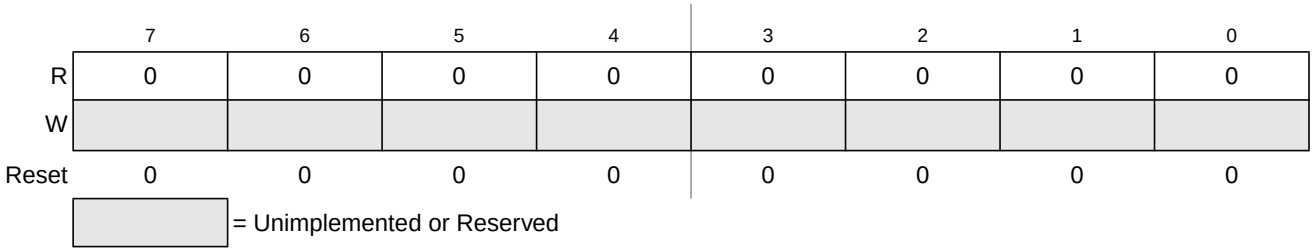


Figure 21-9. Reserved Register

These register locations are not used (reserved). All unused registers and bits in this block return logic 0s when read. Writes to these registers have no effect.

These registers are not in the on-chip map in special peripheral mode.

21.3.2.6 Port E Data Register (PORTE)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	2	Bit 1	Bit 0
W								
Reset	0	0	0	0	0	0	u	u
Alternate Pin Function	NOACC	MODB or IPIPE1 or CLKTO	MODA or IPIPE0	ECLK	$\overline{\text{LSTRB}}$ or $\overline{\text{TAGLO}}$	R/$\overline{\text{W}}$	$\overline{\text{IRQ}}$	$\overline{\text{XIRQ}}$

= Unimplemented or Reserved u = Unaffected by reset

Figure 21-10. Port E Data Register (PORTE)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Port E is associated with external bus control signals and interrupt inputs. These include mode select (MODB/IPIPE1, MODA/IPIPE0), E clock, size ($\overline{\text{LSTRB}}$/$\overline{\text{TAGLO}}$), read/write (R/$\overline{\text{W}}$), $\overline{\text{IRQ}}$, and $\overline{\text{XIRQ}}$. When not used for one of these specific functions, port E pins 7:2 can be used as general-purpose I/O and pins 1:0 can be used as general-purpose input. The port E assignment register (PEAR) selects the function of each pin and DDRE determines whether each pin is an input or output when it is configured to be general-purpose I/O. DDRE also determines the source of data for a read of PORTE.

Some of these pins have software selectable pull resistors. $\overline{\text{IRQ}}$ and $\overline{\text{XIRQ}}$ can only be pulled up whereas the polarity of the PE7, PE4, PE3, and PE2 pull resistors are determined by chip integration. Please refer to the device overview chapter (Signal Property Summary) to determine the polarity of these resistors. A single control bit enables the pull devices for all of these pins when they are configured as inputs.

This register is not in the on-chip map in special peripheral mode or in expanded modes when the EME bit is set. Therefore, these accesses will be echoed externally.

NOTE

It is unwise to write PORTE and DDRE as a word access. If you are changing port E pins from being inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTE before enabling as outputs.

NOTE

To ensure that you read the value present on the PORTE pins, always wait at least one cycle after writing to the DDRE register before reading from the PORTE register.

21.3.2.7 Data Direction Register E (DDRE)

	7	6	5	4	3	2	1	0
R	Bit 7	6	5	4	3	Bit 2	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-11. Data Direction Register E (DDRE)

Read: Anytime when register is in the map

Write: Anytime when register is in the map

Data direction register E is associated with port E. For bits in port E that are configured as general-purpose I/O lines, DDRE determines the primary direction of each of these pins. A 1 causes the associated bit to be an output and a 0 causes the associated bit to be an input. Port E bit 1 (associated with $\overline{\text{IRQ}}$) and bit 0 (associated with $\overline{\text{XIRQ}}$) cannot be configured as outputs. Port E, bits 1 and 0, can be read regardless of whether the alternate interrupt function is enabled. The value in a DDR bit also affects the source of data for reads of the corresponding PORTE register. If the DDR bit is 0 (input) the buffered pin input state is read. If the DDR bit is 1 (output) the associated port data register bit state is read.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally. Also, it is not in the map in expanded modes while the EME control bit is set.

Table 21-5. DDRE Field Descriptions

Field	Description
7:2 DDRE	**Data Direction Port E** 0 Configure the corresponding I/O pin as an input 1 Configure the corresponding I/O pin as an output **Note:** It is unwise to write PORTE and DDRE as a word access. If you are changing port E pins from inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTE before enabling as outputs.

21.3.2.8 Port E Assignment Register (PEAR)

	7	6	5	4	3	2	1	0
R	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
W								
Reset								
Special Single Chip	0	0	0	0	0	0	0	0
Special Test	0	0	1	0	1	1	0	0
Peripheral	0	0	0	0	0	0	0	0
Emulation Expanded Narrow	1	0	1	0	1	1	0	0
Emulation Expanded Wide	1	0	1	0	1	1	0	0
Normal Single Chip	0	0	0	1	0	0	0	0
Normal Expanded Narrow	0	0	0	0	0	0	0	0
Normal Expanded Wide	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-12. Port E Assignment Register (PEAR)

Read: Anytime (provided this register is in the map).

Write: Each bit has specific write conditions. Please refer to the descriptions of each bit on the following pages.

Port E serves as general-purpose I/O or as system and bus control signals. The PEAR register is used to choose between the general-purpose I/O function and the alternate control functions. When an alternate control function is selected, the associated DDRE bits are overridden.

The reset condition of this register depends on the mode of operation because bus control signals are needed immediately after reset in some modes. In normal single-chip mode, no external bus control signals are needed so all of port E is configured for general-purpose I/O. In normal expanded modes, only the E clock is configured for its alternate bus control function and the other bits of port E are configured for general-purpose I/O. As the reset vector is located in external memory, the E clock is required for this access. R/$\overline{W}$ is only needed by the system when there are external writable resources. If the normal expanded system needs any other bus control signals, PEAR would need to be written before any access that needed the additional signals. In special test and emulation modes, IPIPE1, IPIPE0, E, $\overline{LSTRB}$, and R/$\overline{W}$ are configured out of reset as bus control signals.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

Table 21-6. PEAR Field Descriptions

Field	Description
7 NOACCE	**CPU No Access Output Enable** Normal: write once Emulation: write never Special: write anytime 1 The associated pin (port E, bit 7) is general-purpose I/O. 0 The associated pin (port E, bit 7) is output and indicates whether the cycle is a CPU free cycle. This bit has no effect in single-chip or special peripheral modes.
5 PIPOE	**Pipe Status Signal Output Enable** Normal: write once Emulation: write never Special: write anytime. 0 The associated pins (port E, bits 6:5) are general-purpose I/O. 1 The associated pins (port E, bits 6:5) are outputs and indicate the state of the instruction queue This bit has no effect in single-chip or special peripheral modes.
4 NECLK	**No External E Clock** Normal and special: write anytime Emulation: write never 0 The associated pin (port E, bit 4) is the external E clock pin. External E clock is free-running if ESTR = 0 1 The associated pin (port E, bit 4) is a general-purpose I/O pin. External E clock is available as an output in all modes.
3 LSTRE	**Low Strobe ($\overline{\text{LSTRB}}$) Enable** Normal: write once Emulation: write never Special: write anytime. 0 The associated pin (port E, bit 3) is a general-purpose I/O pin. 1 The associated pin (port E, bit 3) is configured as the $\overline{\text{LSTRB}}$ bus control output. If BDM tagging is enabled, $\overline{\text{TAGLO}}$ is multiplexed in on the rising edge of ECLK and $\overline{\text{LSTRB}}$ is driven out on the falling edge of ECLK. This bit has no effect in single-chip, peripheral, or normal expanded narrow modes. **Note:** $\overline{\text{LSTRB}}$ is used during external writes. After reset in normal expanded mode, $\overline{\text{LSTRB}}$ is disabled to provide an extra I/O pin. If $\overline{\text{LSTRB}}$ is needed, it should be enabled before any external writes. External reads do not normally need $\overline{\text{LSTRB}}$ because all 16 data bits can be driven even if the system only needs 8 bits of data.
2 RDWE	**Read/Write Enable** Normal: write once Emulation: write never Special: write anytime 0 The associated pin (port E, bit 2) is a general-purpose I/O pin. 1 The associated pin (port E, bit 2) is configured as the R/$\overline{\text{W}}$ pin This bit has no effect in single-chip or special peripheral modes. **Note:** R/$\overline{\text{W}}$ is used for external writes. After reset in normal expanded mode, R/$\overline{\text{W}}$ is disabled to provide an extra I/O pin. If R/$\overline{\text{W}}$ is needed it should be enabled before any external writes.

21.3.2.9 Mode Register (MODE)

	7	6	5	4	3	2	1	0
R	MODC	MODB	MODA	0	IVIS	0	EMK	EME
W								
Reset								
Special Single Chip	0	0	0	0	0	0	0	0
Emulation Expanded Narrow	0	0	1	0	1	0	1	1
Special Test	0	1	0	0	1	0	0	0
Emulation Expanded Wide	0	1	1	0	1	0	1	1
Normal Single Chip	1	0	0	0	0	0	0	0
Normal Expanded Narrow	1	0	1	0	0	0	0	0
Peripheral	1	1	0	0	0	0	0	0
Normal Expanded Wide	1	1	1	0	0	0	0	0

= Unimplemented or Reserved

Figure 21-13. Mode Register (MODE)

Read: Anytime (provided this register is in the map).

Write: Each bit has specific write conditions. Please refer to the descriptions of each bit on the following pages.

The MODE register is used to establish the operating mode and other miscellaneous functions (i.e., internal visibility and emulation of port E and K).

In special peripheral mode, this register is not accessible but it is reset as shown to system configuration features. Changes to bits in the MODE register are delayed one cycle after the write.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

Table 21-7. MODE Field Descriptions

Field	Description
7:5 MOD[C:A]	**Mode Select Bits** — These bits indicate the current operating mode. If MODA = 1, then MODC, MODB, and MODA are write never. If MODC = MODA = 0, then MODC, MODB, and MODA are writable with the exception that you cannot change to or from special peripheral mode If MODC = 1, MODB = 0, and MODA = 0, then MODC is write never. MODB and MODA are write once, except that you cannot change to special peripheral mode. From normal single-chip, only normal expanded narrow and normal expanded wide modes are available. See Table 21-8 and Table 21-16.
3 IVIS	**Internal Visibility (for both read and write accesses)** — This bit determines whether internal accesses generate a bus cycle that is visible on the external bus. Normal: write once Emulation: write never Special: write anytime 0 No visibility of internal bus operations on external bus. 1 Internal bus operations are visible on external bus.
1 EMK	**Emulate Port K** Normal: write once Emulation: write never Special: write anytime 0 PORTK and DDRK are in the memory map so port K can be used for general-purpose I/O. 1 If in any expanded mode, PORTK and DDRK are removed from the memory map. In single-chip modes, PORTK and DDRK are always in the map regardless of the state of this bit. In special peripheral mode, PORTK and DDRK are never in the map regardless of the state of this bit.
0 EME	**Emulate Port E** Normal and Emulation: write never Special: write anytime 0 PORTE and DDRE are in the memory map so port E can be used for general-purpose I/O. 1 If in any expanded mode or special peripheral mode, PORTE and DDRE are removed from the memory map. Removing the registers from the map allows the user to emulate the function of these registers externally. In single-chip modes, PORTE and DDRE are always in the map regardless of the state of this bit.

Table 21-8. MODC, MODB, and MODA Write Capability[1]

MODC	MODB	MODA	Mode	MODx Write Capability
0	0	0	Special single chip	MODC, MODB, and MODA write anytime but not to 110[2]
0	0	1	Emulation narrow	No write
0	1	0	Special test	MODC, MODB, and MODA write anytime but not to 110(2)
0	1	1	Emulation wide	No write
1	0	0	Normal single chip	MODC write never, MODB and MODA write once but not to 110
1	0	1	Normal expanded narrow	No write
1	1	0	Special peripheral	No write
1	1	1	Normal expanded wide	No write

1 No writes to the MOD bits are allowed while operating in a secure mode. For more details, refer to the device overview chapter.

2 If you are in a special single-chip or special test mode and you write to this register, changing to normal single-chip mode, then one allowed write to this register remains. If you write to normal expanded or emulation mode, then no writes remain.

21.3.2.10 Pull Control Register (PUCR)

	7	6	5	4	3	2	1	0
R	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
W								
Reset[1]	1	0	0	1	0	0	0	0

NOTES:
1. The default value of this parameter is shown. Please refer to the device overview chapter to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 21-14. Pull Control Register (PUCR)

Read: Anytime (provided this register is in the map).

Write: Anytime (provided this register is in the map).

This register is used to select pull resistors for the pins associated with the core ports. Pull resistors are assigned on a per-port basis and apply to any pin in the corresponding port that is currently configured as an input. The polarity of these pull resistors is determined by chip integration. Please refer to the device overview chapter to determine the polarity of these resistors.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

NOTE

These bits have no effect when the associated pin(s) are outputs. (The pull resistors are inactive.)

Table 21-9. PUCR Field Descriptions

Field	Description
7 PUPKE	**Pull resistors Port K Enable** 0 Port K pull resistors are disabled. 1 Enable pull resistors for port K input pins.
4 PUPEE	**Pull resistors Port E Enable** 0 Port E pull resistors on bits 7, 4:0 are disabled. 1 Enable pull resistors for port E input pins bits 7, 4:0. **Note:** Pins 5 and 6 of port E have pull resistors which are only enabled during reset. This bit has no effect on these pins.
1 PUPBE	**Pull resistors Port B Enable** 0 Port B pull resistors are disabled. 1 Enable pull resistors for all port B input pins.
0 PUPAE	**Pull resistors Port A Enable** 0 Port A pull resistors are disabled. 1 Enable pull resistors for all port A input pins.

21.3.2.11 Reduced Drive Register (RDRIV)

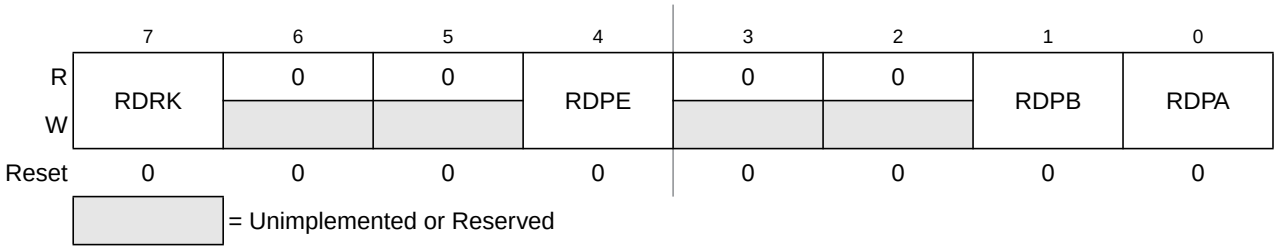


Figure 21-15. Reduced Drive Register (RDRIV)

Read: Anytime (provided this register is in the map)

Write: Anytime (provided this register is in the map)

This register is used to select reduced drive for the pins associated with the core ports. This gives reduced power consumption and reduced RFI with a slight increase in transition time (depending on loading). This feature would be used on ports which have a light loading. The reduced drive function is independent of which function is being used on a particular port.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

Table 21-10. RDRIV Field Descriptions

Field	Description
7 RDRK	**Reduced Drive of Port K** 0 All port K output pins have full drive enabled. 1 All port K output pins have reduced drive enabled.
4 RDPE	**Reduced Drive of Port E** 0 All port E output pins have full drive enabled. 1 All port E output pins have reduced drive enabled.
1 RDPB	**Reduced Drive of Port B** 0 All port B output pins have full drive enabled. 1 All port B output pins have reduced drive enabled.
0 RDPA	**Reduced Drive of Ports A** 0 All port A output pins have full drive enabled. 1 All port A output pins have reduced drive enabled.

21.3.2.12 External Bus Interface Control Register (EBICTL)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	ESTR
W								
Reset:								
Peripheral	0	0	0	0	0	0	0	0
All other modes	0	0	0	0	0	0	0	1

= Unimplemented or Reserved

Figure 21-16. External Bus Interface Control Register (EBICTL)

Read: Anytime (provided this register is in the map)

Write: Refer to individual bit descriptions below

The EBICTL register is used to control miscellaneous functions (i.e., stretching of external E clock).

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

Table 21-11. EBICTL Field Descriptions

Field	Description
0 ESTR	**E Clock Stretches** — This control bit determines whether the E clock behaves as a simple free-running clock or as a bus control signal that is active only for external bus cycles. Normal and Emulation: write once Special: write anytime 0 E never stretches (always free running). 1 E stretches high during stretched external accesses and remains low during non-visible internal accesses. This bit has no effect in single-chip modes.

21.3.2.13 Reserved Register

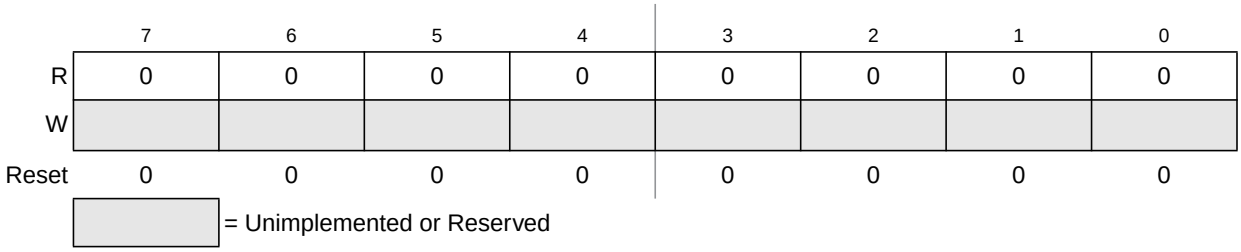


Figure 21-17. Reserved Register

This register location is not used (reserved). All bits in this register return logic 0s when read. Writes to this register have no effect.

This register is not in the on-chip memory map in expanded and special peripheral modes. Therefore, these accesses will be echoed externally.

21.3.2.14 IRQ Control Register (IRQCR)

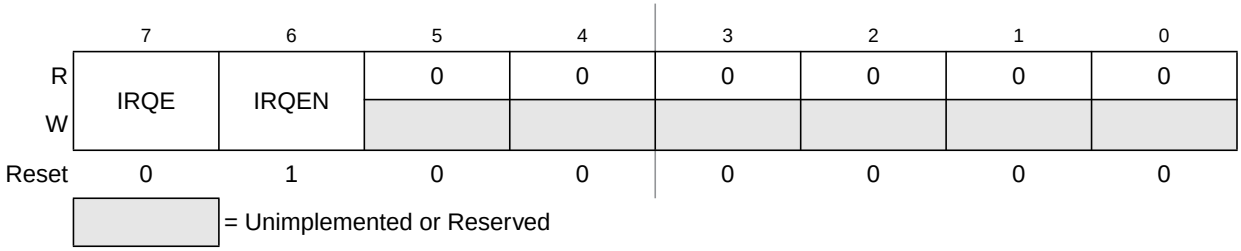


Figure 21-18. IRQ Control Register (IRQCR)

Read: See individual bit descriptions below

Write: See individual bit descriptions below

Table 21-12. IRQCR Field Descriptions

Field	Description
7 IRQE	**IRQ Select Edge Sensitive Only** Special modes: read or write anytime Normal and Emulation modes: read anytime, write once 0 IRQ configured for low level recognition. 1 IRQ configured to respond only to falling edges. Falling edges on the IRQ pin will be detected anytime IRQE = 1 and will be cleared only upon a reset or the servicing of the IRQ interrupt.
6 IRQEN	**External IRQ Enable** Normal, emulation, and special modes: read or write anytime 0 External IRQ pin is disconnected from interrupt logic. 1 External IRQ pin is connected to interrupt logic. **Note:** When IRQEN = 0, the edge detect latch is disabled.

21.3.2.15 Port K Data Register (PORTK)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0
Alternate Pin Function	$\overline{ECS}$	$\overline{XCS}$	XAB19	XAB18	XAB17	XAB16	XAB15	XAB14

Figure 21-19. Port K Data Register (PORTK)

Read: Anytime

Write: Anytime

This port is associated with the internal memory expansion emulation pins. When the port is not enabled to emulate the internal memory expansion, the port pins are used as general-purpose I/O. When port K is operating as a general-purpose I/O port, DDRK determines the primary direction for each port K pin. A 1 causes the associated port pin to be an output and a 0 causes the associated pin to be a high-impedance input. The value in a DDR bit also affects the source of data for reads of the corresponding PORTK register. If the DDR bit is 0 (input) the buffered pin input is read. If the DDR bit is 1 (output) the output of the port data register is read.

This register is not in the map in peripheral or expanded modes while the EMK control bit in MODE register is set. Therefore, these accesses will be echoed externally.

When inputs, these pins can be selected to be high impedance or pulled up, based upon the state of the PUPKE bit in the PUCR register.

Table 21-13. PORTK Field Descriptions

Field	Description
7 Port K, Bit 7	**Port K, Bit 7** — This bit is used as an emulation chip select signal for the emulation of the internal memory expansion, or as general-purpose I/O, depending upon the state of the EMK bit in the MODE register. While this bit is used as a chip select, the external bit will return to its de-asserted state (V_{DD}) for approximately 1/4 cycle just after the negative edge of ECLK, unless the external access is stretched and ECLK is free-running (ESTR bit in EBICTL = 0). See the MMC block description chapter for additional details on when this signal will be active.
6 Port K, Bit 6	**Port K, Bit 6** — This bit is used as an external chip select signal for most external accesses that are not selected by $\overline{ECS}$ (see the MMC block description chapter for more details), depending upon the state the of the EMK bit in the MODE register. While this bit is used as a chip select, the external pin will return to its de-asserted state (V_{DD}) for approximately 1/4 cycle just after the negative edge of ECLK, unless the external access is stretched and ECLK is free-running (ESTR bit in EBICTL = 0).
5:0 Port K, Bits 5:0	**Port K, Bits 5:0** — These six bits are used to determine which FLASH/ROM or external memory array page is being accessed. They can be viewed as expanded addresses XAB19–XAB14 of the 20-bit address used to access up to1M byte internal FLASH/ROM or external memory array. Alternatively, these bits can be used for general-purpose I/O depending upon the state of the EMK bit in the MODE register.

21.3.2.16 Port K Data Direction Register (DDRK)

	7	6	5	4	3	2	1	0
R W	Bit 7	6	5	4	3	2	1	Bit 0
Reset	0	0	0	0	0	0	0	0

Figure 21-20. Port K Data Direction Register (DDRK)

Read: Anytime

Write: Anytime

This register determines the primary direction for each port K pin configured as general-purpose I/O. This register is not in the map in peripheral or expanded modes while the EMK control bit in MODE register is set. Therefore, these accesses will be echoed externally.

Table 21-14. EBICTL Field Descriptions

Field	Description
7:0 DDRK	**Data Direction Port K Bits** 0 Associated pin is a high-impedance input 1 Associated pin is an output **Note:** It is unwise to write PORTK and DDRK as a word access. If you are changing port K pins from inputs to outputs, the data may have extra transitions during the write. It is best to initialize PORTK before enabling as outputs. **Note:** To ensure that you read the correct value from the PORTK pins, always wait at least one cycle after writing to the DDRK register before reading from the PORTK register.

21.4 Functional Description

21.4.1 Detecting Access Type from External Signals

The external signals $\overline{\text{LSTRB}}$, R/$\overline{\text{W}}$, and AB0 indicate the type of bus access that is taking place. Accesses to the internal RAM module are the only type of access that would produce $\overline{\text{LSTRB}}$ = AB0 = 1, because the internal RAM is specifically designed to allow misaligned 16-bit accesses in a single cycle. In these cases the data for the address that was accessed is on the low half of the data bus and the data for address + 1 is on the high half of the data bus. This is summarized in Table 21-15.

Table 21-15. Access Type vs. Bus Control Pins

$\overline{\text{LSTRB}}$	AB0	R/$\overline{\text{W}}$	Type of Access
1	0	1	8-bit read of an even address
0	1	1	8-bit read of an odd address
1	0	0	8-bit write of an even address
0	1	0	8-bit write of an odd address
0	0	1	16-bit read of an even address

Table 21-15. Access Type vs. Bus Control Pins

$\overline{\text{LSTRB}}$	AB0	R/$\overline{\text{W}}$	Type of Access
1	1	1	16-bit read of an odd address (low/high data swapped)
0	0	0	16-bit write to an even address
1	1	0	16-bit write to an odd address (low/high data swapped)

21.4.2 Stretched Bus Cycles

In order to allow fast internal bus cycles to coexist in a system with slower external memory resources, the HCS12 supports the concept of stretched bus cycles (module timing reference clocks for timers and baud rate generators are not affected by this stretching). Control bits in the MISC register in the MMC sub-block of the core specify the amount of stretch (0, 1, 2, or 3 periods of the internal bus-rate clock). While stretching, the CPU state machines are all held in their current state. At this point in the CPU bus cycle, write data would already be driven onto the data bus so the length of time write data is valid is extended in the case of a stretched bus cycle. Read data would not be captured by the system until the E clock falling edge. In the case of a stretched bus cycle, read data is not required until the specified setup time before the falling edge of the stretched E clock. The chip selects, and R/$\overline{\text{W}}$ signals remain valid during the period of stretching (throughout the stretched E high time).

NOTE

The address portion of the bus cycle is not stretched.

21.4.3 Modes of Operation

The operating mode out of reset is determined by the states of the MODC, MODB, and MODA pins during reset (Table 21-16). The MODC, MODB, and MODA bits in the MODE register show the current operating mode and provide limited mode switching during operation. The states of the MODC, MODB, and MODA pins are latched into these bits on the rising edge of the reset signal.

Table 21-16. Mode Selection

MODC	MODB	MODA	Mode Description
0	0	0	Special Single Chip, BDM allowed and ACTIVE. BDM is allowed in all other modes but a serial command is required to make BDM active.
0	0	1	Emulation Expanded Narrow, BDM allowed
0	1	0	Special Test (Expanded Wide), BDM allowed
0	1	1	Emulation Expanded Wide, BDM allowed
1	0	0	Normal Single Chip, BDM allowed
1	0	1	Normal Expanded Narrow, BDM allowed
1	1	0	Peripheral; BDM allowed but bus operations would cause bus conflicts (must not be used)
1	1	1	Normal Expanded Wide, BDM allowed

There are two basic types of operating modes:

1. Normal modes: Some registers and bits are protected against accidental changes.
2. Special modes: Allow greater access to protected control registers and bits for special purposes such as testing.

A system development and debug feature, background debug mode (BDM), is available in all modes. In special single-chip mode, BDM is active immediately after reset.

Some aspects of Port E are not mode dependent. Bit 1 of Port E is a general purpose input or the $\overline{\text{IRQ}}$ interrupt input. $\overline{\text{IRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. Bit 0 of Port E is a general purpose input or the $\overline{\text{XIRQ}}$ interrupt input. $\overline{\text{XIRQ}}$ can be enabled by bits in the CPU's condition codes register but it is inhibited at reset so this pin is initially configured as a simple input with a pull-up. The ESTR bit in the EBICTL register is set to one by reset in any user mode. This assures that the reset vector can be fetched even if it is located in an external slow memory device. The PE6/MODB/IPIPE1 and PE5/MODA/IPIPE0 pins act as high-impedance mode select inputs during reset.

The following paragraphs discuss the default bus setup and describe which aspects of the bus can be changed after reset on a per mode basis.

21.4.3.1 Normal Operating Modes

These modes provide three operating configurations. Background debug is available in all three modes, but must first be enabled for some operations by means of a BDM background command, then activated.

21.4.3.1.1 Normal Single-Chip Mode

There is no external expansion bus in this mode. All pins of Ports A, B and E are configured as general purpose I/O pins Port E bits 1 and 0 are available as general purpose input only pins with internal pull resistors enabled. All other pins of Port E are bidirectional I/O pins that are initially configured as high-impedance inputs with internal pull resistors enabled. Ports A and B are configured as high-impedance inputs with their internal pull resistors disabled.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE, and RDWE are reset to zero. Writing the opposite state into them in single chip mode does not change the operation of the associated Port E pins.

In normal single chip mode, the MODE register is writable one time. This allows a user program to change the bus mode to narrow or wide expanded mode and/or turn on visibility of internal accesses.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

21.4.3.1.2 Normal Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E bit 4 is configured as the E clock output signal. These signals allow external memory and peripheral devices to be interfaced to the MCU.

Port E pins other than PE4/ECLK are configured as general purpose I/O pins (initially high-impedance inputs with internal pull resistors enabled). Control bits PIPOE, NECLK, LSTRE, and RDWE in the PEAR register can be used to configure Port E pins to act as bus control outputs instead of general purpose I/O pins.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. Development systems where pipe status signals are monitored would typically use the special variation of this mode.

The Port E bit 2 pin can be reconfigured as the R/$\overline{W}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded system includes external devices that can be written, such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

The Port E bit 3 pin can be reconfigured as the $\overline{\text{LSTRB}}$ bus control signal by writing “1” to the LSTRE bit in PEAR. The default condition of this pin is a general purpose input because the $\overline{\text{LSTRB}}$ function is not needed in all expanded wide applications.

The Port E bit 4 pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. The E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

21.4.3.1.3 Normal Expanded Narrow Mode

This mode is used for lower cost production systems that use 8-bit wide external EPROMs or RAMs. Such systems take extra bus cycles to access 16-bit locations but this may be preferred over the extra cost of additional external memory devices.

Ports A and B are configured as a 16-bit address bus and Port A is multiplexed with data. Internal visibility is not available in this mode because the internal cycles would need to be split into two 8-bit cycles.

Since the PEAR register can only be written one time in this mode, use care to set all bits to the desired states during the single allowed write.

The PE3/$\overline{\text{LSTRB}}$ pin is always a general purpose I/O pin in normal expanded narrow mode. Although it is possible to write the LSTRE bit in PEAR to “1” in this mode, the state of LSTRE is overridden and Port E bit 3 cannot be reconfigured as the $\overline{\text{LSTRB}}$ output.

It is possible to enable the pipe status signals on Port E bits 6 and 5 by setting the PIPOE bit in PEAR, but it would be unusual to do so in this mode. LSTRB would also be needed to fully understand system activity. Development systems where pipe status signals are monitored would typically use special expanded wide mode or occasionally special expanded narrow mode.

The PE4/ECLK pin is initially configured as ECLK output with stretch. The E clock output function depends upon the settings of the NECLK bit in the PEAR register, the IVIS bit in the MODE register and the ESTR bit in the EBICTL register. In normal expanded narrow mode, the E clock is available for use in external select decode logic or as a constant speed clock for use in the external application system.

The PE2/R/W pin is initially configured as a general purpose input with an internal pull resistor enabled but this pin can be reconfigured as the R/$\overline{W}$ bus control signal by writing “1” to the RDWE bit in PEAR. If the expanded narrow system includes external devices that can be written such as RAM, the RDWE bit would need to be set before any attempt to write to an external location. If there are no writable resources in the external system, PE2 can be left as a general purpose I/O pin.

21.4.3.1.4 Emulation Expanded Wide Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. These signals allow external memory and peripheral devices to be interfaced to the MCU. These signals can also be used by a logic analyzer to monitor the progress of application programs.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in emulation mode are restricted.

21.4.3.1.5 Emulation Expanded Narrow Mode

Expanded narrow modes are intended to allow connection of single 8-bit external memory devices for lower cost systems that do not need the performance of a full 16-bit external data bus. Accesses to internal resources that have been mapped external (i.e. PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, PUCR, RDRIV) will be accessed with a 16-bit data bus on Ports A and B. Accesses of 16-bit external words to addresses which are normally mapped external will be broken into two separate 8-bit accesses using Port A as an 8-bit data bus. Internal operations continue to use full 16-bit data paths. They are only visible externally as 16-bit information if IVIS=1.

Ports A and B are configured as multiplexed address and data output ports. During external accesses, address A15, data D15 and D7 are associated with PA7, address A0 is associated with PB0 and data D8 and D0 are associated with PA0. During internal visible accesses and accesses to internal resources that have been mapped external, address A15 and data D15 is associated with PA7 and address A0 and data D0 is associated with PB0.

The bus control related pins in Port E (PE7/NOACC, PE6/MODB/IPIPE1, PE5/MODA/IPIPE0, PE4/ECLK, PE3/$\overline{LSTRB}$/$\overline{TAGLO}$, and PE2/R/$\overline{W}$) are all configured to serve their bus control output functions rather than general purpose I/O. Notice that writes to the bus control enable bits in the PEAR register in emulation mode are restricted.

The main difference between special modes and normal modes is that some of the bus control and system control signals cannot be written in emulation modes.

21.4.3.2 Special Operating Modes

There are two special operating modes that correspond to normal operating modes. These operating modes are commonly used in factory testing and system development.

21.4.3.2.1 Special Single-Chip Mode

When the MCU is reset in this mode, the background debug mode is enabled and active. The MCU does not fetch the reset vector and execute application code as it would in other modes. Instead the active background mode is in control of CPU execution and BDM firmware is waiting for additional serial commands through the BKGD pin. When a serial command instructs the MCU to return to normal execution, the system will be configured as described below unless the reset states of internal control registers have been changed through background commands after the MCU was reset.

There is no external expansion bus after reset in this mode. Ports A and B are initially simple bidirectional I/O pins that are configured as high-impedance inputs with internal pull resistors disabled; however, writing to the mode select bits in the MODE register (which is allowed in special modes) can change this after reset. All of the Port E pins (except PE4/ECLK) are initially configured as general purpose high-impedance inputs with internal pull resistors enabled. PE4/ECLK is configured as the E clock output in this mode.

The pins associated with Port E bits 6, 5, 3, and 2 cannot be configured for their alternate functions IPIPE1, IPIPE0, $\overline{\text{LSTRB}}$, and R/$\overline{\text{W}}$ while the MCU is in single chip modes. In single chip modes, the associated control bits PIPOE, LSTRE and RDWE are reset to zero. Writing the opposite value into these bits in single chip mode does not change the operation of the associated Port E pins.

Port E, bit 4 can be configured for a free-running E clock output by clearing NECLK=0. Typically the only use for an E clock output while the MCU is in single chip modes would be to get a constant speed clock for use in the external application system.

21.4.3.2.2 Special Test Mode

In expanded wide modes, Ports A and B are configured as a 16-bit multiplexed address and data bus and Port E provides bus control and status signals. In special test mode, the write protection of many control bits is lifted so that they can be thoroughly tested without needing to go through reset.

21.4.3.3 Test Operating Mode

There is a test operating mode in which an external master, such as an I.C. tester, can control the on-chip peripherals.

21.4.3.3.1 Peripheral Mode

This mode is intended for factory testing of the MCU. In this mode, the CPU is inactive and an external (tester) bus master drives address, data and bus control signals in through Ports A, B and E. In effect, the whole MCU acts as if it was a peripheral under control of an external CPU. This allows faster testing of on-chip memory and peripherals than previous testing methods. Since the mode control register is not accessible in peripheral mode, the only way to change to another mode is to reset the MCU into a different

mode. Background debugging should not be used while the MCU is in special peripheral mode as internal bus conflicts between BDM and the external master can cause improper operation of both functions.

21.4.4 Internal Visibility

Internal visibility is available when the MCU is operating in expanded wide modes or emulation narrow mode. It is not available in single-chip, peripheral or normal expanded narrow modes. Internal visibility is enabled by setting the IVIS bit in the MODE register.

If an internal access is made while E, R/$\overline{W}$, and $\overline{LSTRB}$ are configured as bus control outputs and internal visibility is off (IVIS=0), E will remain low for the cycle, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

When internal visibility is enabled (IVIS=1), certain internal cycles will be blocked from going external. During cycles when the BDM is selected, R/$\overline{W}$ will remain high, data will maintain its previous state, and address and $\overline{LSTRB}$ pins will be updated with the internal value. During CPU no access cycles when the BDM is not driving, R/$\overline{W}$ will remain high, and address, data and the $\overline{LSTRB}$ pins will remain at their previous state.

NOTE

When the system is operating in a secure mode, internal visibility is not available (i.e., IVIS = 1 has no effect). Also, the IPIPE signals will not be visible, regardless of operating mode. IPIPE1–IPIPE0 will display 0es if they are enabled. In addition, the MOD bits in the MODE control register cannot be written.

21.4.5 Low-Power Options

The MEBI does not contain any user-controlled options for reducing power consumption. The operation of the MEBI in low-power modes is discussed in the following subsections.

21.4.5.1 Operation in Run Mode

The MEBI does not contain any options for reducing power in run mode; however, the external addresses are conditioned to reduce power in single-chip modes. Expanded bus modes will increase power consumption.

21.4.5.2 Operation in Wait Mode

The MEBI does not contain any options for reducing power in wait mode.

21.4.5.3 Operation in Stop Mode

The MEBI will cease to function after execution of a CPU STOP instruction.

Chapter 22
Module Mapping Control (MMCV4)

22.1 Introduction

This section describes the functionality of the module mapping control (MMC) sub-block of the S12 core platform.

The block diagram of the MMC is shown in Figure 22-1.

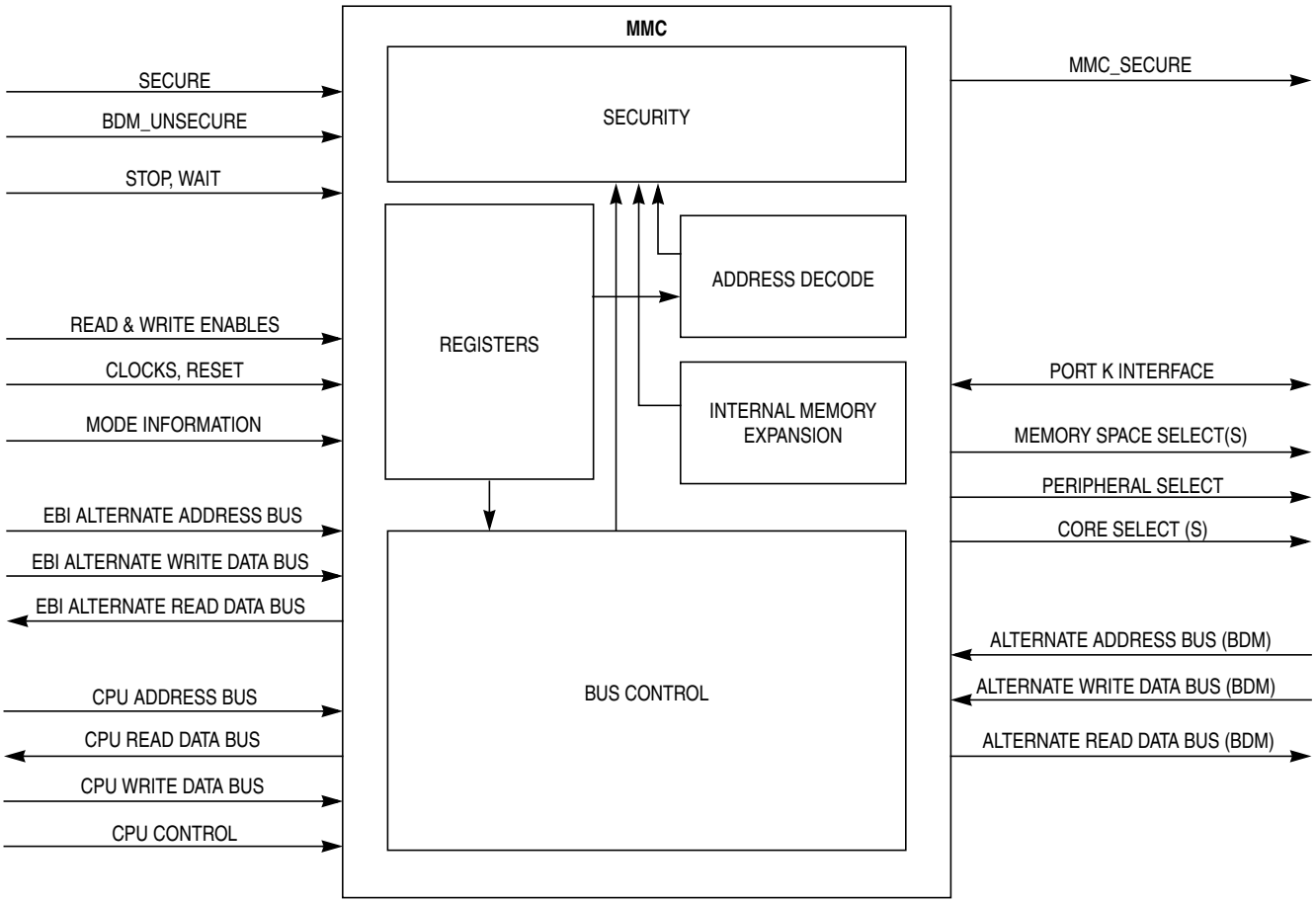


Figure 22-1. MMC Block Diagram

The MMC is the sub-module which controls memory map assignment and selection of internal resources and external space. Internal buses between the core and memories and between the core and peripherals is controlled in this module. The memory expansion is generated in this module.

22.1.1 Features

- Registers for mapping of address space for on-chip RAM, EEPROM, and FLASH (or ROM) memory blocks and associated registers
- Memory mapping control and selection based upon address decode and system operating mode
- Core address bus control
- Core data bus control and multiplexing
- Core security state decoding
- Emulation chip select signal generation ($\overline{ECS}$)
- External chip select signal generation ($\overline{XCS}$)
- Internal memory expansion
- External stretch and ROM mapping control functions via the MISC register
- Reserved registers for test purposes
- Configurable system memory options defined at integration of core into the system-on-a-chip (SoC).

22.1.2 Modes of Operation

Some of the registers operate differently depending on the mode of operation (i.e., normal expanded wide, special single chip, etc.). This is best understood from the register descriptions.

22.2 External Signal Description

All interfacing with the MMC sub-block is done within the core, it has no external signals.

22.3 Memory Map and Register Definition

A summary of the registers associated with the MMC sub-block is shown in Figure 22-2. Detailed descriptions of the registers and bits are given in the subsections that follow.

22.3.1 Module Memory Map

Table 22-1. MMC Memory Map

Address Offset	Register	Access
	Initialization of Internal RAM Position Register (INITRM)	R/W
	Initialization of Internal Registers Position Register (INITRG)	R/W
	Initialization of Internal EEPROM Position Register (INITEE)	R/W
	Miscellaneous System Control Register (MISC)	R/W
	Reserved	—
. .	. .	—

Table 22-1. MMC Memory Map (continued)

Address Offset	Register	Access
	Reserved	—
. .	. .	—
	Memory Size Register 0 (MEMSIZ0)	R
	Memory Size Register 1 (MEMSIZ1)	R
. .	. .	
	Program Page Index Register (PPAGE)	R/W
	Reserved	—

22.3.2 Register Descriptions

Name		Bit 7	6	5	4	3	2	1	Bit 0
INITRM	R	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
	W								
INITRG	R	0	REG14	REG13	REG12	REG11	0	0	0
	W								
INITEE	R	EE15	EE14	EE13	EE12	EE11	0	0	EEON
	W								
MISC	R	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
	W								
MTSTO	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
MTST1	R	Bit 7	6	5	4	3	2	1	Bit 0
	W								
MEMSIZ0	R	REG_SW0	0	EEP_SW1	EEP_SW0	0	RAM_SW2	RAM_SW1	RAM_SW0
	W								
MEMSIZ1	R	ROM_SW1	ROM_SW0	0	0	0	0	PAG_SW1	PAG_SW0
	W								
PPAGE	R	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
	W								
Reserved	R	0	0	0	0	0	0	0	0
	W								

= Unimplemented

Figure 22-2. MMC Register Summary

22.3.2.1 Initialization of Internal RAM Position Register (INITRM)

	7	6	5	4	3	2	1	0
R	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
W								
Reset	0	0	0	0	1	0	0	1

= Unimplemented or Reserved

Figure 22-3. Initialization of Internal RAM Position Register (INITRM)

Read: Anytime

Write: Once in normal and emulation modes, anytime in special modes

NOTE

Writes to this register take one cycle to go into effect.

This register initializes the position of the internal RAM within the on-chip system memory map.

Table 22-2. INITRM Field Descriptions

Field	Description
7:3 RAM[15:11]	**Internal RAM Map Position** — These bits determine the upper five bits of the base address for the system's internal RAM array.
0 RAMHAL	**RAM High-Align** — RAMHAL specifies the alignment of the internal RAM array. 0 Aligns the RAM to the lowest address (0x0000) of the mappable space 1 Aligns the RAM to the higher address (0xFFFF) of the mappable space

22.3.2.2 Initialization of Internal Registers Position Register (INITRG)

	7	6	5	4	3	2	1	0
R	0	REG14	REG13	REG12	REG11	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-4. Initialization of Internal Registers Position Register (INITRG)

Read: Anytime

Write: Once in normal and emulation modes and anytime in special modes

This register initializes the position of the internal registers within the on-chip system memory map. The registers occupy either a 1K byte or 2K byte space and can be mapped to any 2K byte space within the first 32K bytes of the system's address space.

Table 22-3. INITRG Field Descriptions

Field	Description
6:3 REG[14:11]	**Internal Register Map Position** — These four bits in combination with the leading zero supplied by bit 7 of INITRG determine the upper five bits of the base address for the system's internal registers (i.e., the minimum base address is 0x0000 and the maximum is 0x7FFF).

22.3.2.3 Initialization of Internal EEPROM Position Register (INITEE)

	7	6	5	4	3	2	1	0
R	EE15	EE14	EE13	EE12	EE11	0	0	EEON
W								
Reset[1]	—	—	—	—	—	—	—	—

1. The reset state of this register is controlled at chip integration. Please refer to the device overview section to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 22-5. Initialization of Internal EEPROM Position Register (INITEE)

Read: Anytime

Write: The EEON bit can be written to any time on all devices. Bits E[11:15] are “write anytime in all modes” on most devices. On some devices, bits E[11:15] are “write once in normal and emulation modes and write anytime in special modes”. See device overview chapter to determine the actual write access rights.

NOTE

Writes to this register take one cycle to go into effect.

This register initializes the position of the internal EEPROM within the on-chip system memory map.

Table 22-4. INITEE Field Descriptions

Field	Description
7:3 EE[15:11]	**Internal EEPROM Map Position** — These bits determine the upper five bits of the base address for the system’s internal EEPROM array.
0 EEON	**Enable EEPROM** — This bit is used to enable the EEPROM memory in the memory map. 0 Disables the EEPROM from the memory map. 1 Enables the EEPROM in the memory map at the address selected by EE[15:11].

22.3.2.4 Miscellaneous System Control Register (MISC)

	7	6	5	4	3	2	1	0
R	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
W								
Reset: Expanded or Emulation	0	0	0	0	1	1	0	—[1]
Reset: Peripheral or Single Chip	0	0	0	0	1	1	0	1
Reset: Special Test	0	0	0	0	1	1	0	0

1. The reset state of this bit is determined at the chip integration level.

= Unimplemented or Reserved

Figure 22-6. Miscellaneous System Control Register (MISC)

Read: Anytime

Write: As stated in each bit description

NOTE

Writes to this register take one cycle to go into effect.

This register initializes miscellaneous control functions.

Table 22-5. INITEE Field Descriptions

Field	Description
3:2 EXSTR[1:0]	**External Access Stretch Bits 1 and 0** Write: once in normal and emulation modes and anytime in special modes This two-bit field determines the amount of clock stretch on accesses to the external address space as shown in Table 22-6. In single chip and peripheral modes these bits have no meaning or effect.
1 ROMHM	**FLASH EEPROM or ROM Only in Second Half of Memory Map** Write: once in normal and emulation modes and anytime in special modes 0 The fixed page(s) of FLASH EEPROM or ROM in the lower half of the memory map can be accessed. 1 Disables direct access to the FLASH EEPROM or ROM in the lower half of the memory map. These physical locations of the FLASH EEPROM or ROM remain accessible through the program page window.
0 ROMON	**ROMON — Enable FLASH EEPROM or ROM** Write: once in normal and emulation modes and anytime in special modes This bit is used to enable the FLASH EEPROM or ROM memory in the memory map. 0 Disables the FLASH EEPROM or ROM from the memory map. 1 Enables the FLASH EEPROM or ROM in the memory map.

Table 22-6. External Stretch Bit Definition

Stretch Bit EXSTR1	Stretch Bit EXSTR0	Number of E Clocks Stretched
0	0	0
0	1	1
1	0	2
1	1	3

22.3.2.5 Reserved Test Register 0 (MTST0)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	0	0	0	0	0

= Unimplemented or Reserved

Figure 22-7. Reserved Test Register 0 (MTST0)

Read: Anytime

Write: No effect — this register location is used for internal test purposes.

22.3.2.6 Reserved Test Register 1 (MTST1)

	7	6	5	4	3	2	1	0
R	0	0	0	0	0	0	0	0
W								
Reset	0	0	0	1	0	0	0	0

= Unimplemented or Reserved

Figure 22-8. Reserved Test Register 1 (MTST1)

Read: Anytime

Write: No effect — this register location is used for internal test purposes.

22.3.2.7 Memory Size Register 0 (MEMSIZ0)

	7	6	5	4	3	2	1	0
R	REG_SW0	0	EEP_SW1	EEP_SW0	0	RAM_SW2	RAM_SW1	RAM_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 22-9. Memory Size Register 0 (MEMSIZ0)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ0 register reflects the state of the register, EEPROM and RAM memory space configuration switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

Table 22-7. MEMSIZ0 Field Descriptions

Field	Description
7 REG_SW0	**Allocated System Register Space** 0 Allocated system register space size is 1K byte 1 Allocated system register space size is 2K byte
5:4 EEP_SW[1:0]	**Allocated System EEPROM Memory Space** — The allocated system EEPROM memory space size is as given in Table 22-8.
2 RAM_SW[2:0]	**Allocated System RAM Memory Space** — The allocated system RAM memory space size is as given in Table 22-9.

Table 22-8. Allocated EEPROM Memory Space

eep_sw1:eep_sw0	Allocated EEPROM Space
00	0K byte
01	2K bytes
10	4K bytes
11	8K bytes

Table 22-9. Allocated RAM Memory Space

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address[1]
000	2K bytes	2K bytes	RAM[15:11]	0x0800
001	4K bytes	4K bytes	RAM[15:12]	0x0000
010	6K bytes	8K bytes[2]	RAM[15:13]	0x0800
011	8K bytes	8K bytes	RAM[15:13]	0x0000
100	10K bytes	16K bytes [2]	RAM[15:14]	0x1800

Table 22-9. Allocated RAM Memory Space (continued)

ram_sw2:ram_sw0	Allocated RAM Space	RAM Mappable Region	INITRM Bits Used	RAM Reset Base Address[1]
101	12K bytes	16K bytes [2]	RAM[15:14]	0x1000
110	14K bytes	16K bytes [2]	RAM[15:14]	0x0800
111	16K bytes	16K bytes	RAM[15:14]	0x0000

1 The RAM Reset BASE Address is based on the reset value of the INITRM register, 0x0009.

2 Alignment of the Allocated RAM space within the RAM mappable region is dependent on the value of RAMHAL.

NOTE

As stated, the bits in this register provide read visibility to the system physical memory space allocations defined at system integration. The actual array size for any given type of memory block may differ from the allocated size. Please refer to the device overview chapter for actual sizes.

22.3.2.8 Memory Size Register 1 (MEMSIZ1)

	7	6	5	4	3	2	1	0
R	ROM_SW1	ROM_SW0	0	0	0	0	PAG_SW1	PAG_SW0
W								
Reset	—	—	—	—	—	—	—	—

= Unimplemented or Reserved

Figure 22-10. Memory Size Register 1 (MEMSIZ1)

Read: Anytime

Write: Writes have no effect

Reset: Defined at chip integration, see device overview section.

The MEMSIZ1 register reflects the state of the FLASH or ROM physical memory space and paging switches at the core boundary which are configured at system integration. This register allows read visibility to the state of these switches.

Table 22-10. MEMSIZ0 Field Descriptions

Field	Description
7:6 ROM_SW[1:0]	**Allocated System FLASH or ROM Physical Memory Space** — The allocated system FLASH or ROM physical memory space is as given in Table 22-11.
1:0 PAG_SW[1:0]	**Allocated Off-Chip FLASH or ROM Memory Space** — The allocated off-chip FLASH or ROM memory space size is as given in Table 22-12.

Table 22-11. Allocated FLASH/ROM Physical Memory Space

rom_sw1:rom_sw0	Allocated FLASH or ROM Space
00	0K byte
01	16K bytes
10	48K bytes(1)
11	64K bytes(1)

NOTES:

1. The ROMHM software bit in the MISC register determines the accessibility of the FLASH/ROM memory space. Please refer to Section 22.3.2.8, "Memory Size Register 1 (MEMSIZ1)," for a detailed functional description of the ROMHM bit.

Table 22-12. Allocated Off-Chip Memory Options

pag_sw1:pag_sw0	Off-Chip Space	On-Chip Space
00	876K bytes	128K bytes
01	768K bytes	256K bytes
10	512K bytes	512K bytes
11	0K byte	1M byte

NOTE

As stated, the bits in this register provide read visibility to the system memory space and on-chip/off-chip partitioning allocations defined at system integration. The actual array size for any given type of memory block may differ from the allocated size. Please refer to the device overview chapter for actual sizes.

22.3.2.9 Program Page Index Register (PPAGE)

	7	6	5	4	3	2	1	0
R	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
W								
Reset[1]	—	—	—	—	—	—	—	—

1. The reset state of this register is controlled at chip integration. Please refer to the device overview section to determine the actual reset state of this register.

= Unimplemented or Reserved

Figure 22-11. Program Page Index Register (PPAGE)

Read: Anytime

Write: Determined at chip integration. Generally it's: "write anytime in all modes;" on some devices it will be: "write only in special modes." Check specific device documentation to determine which applies.

Reset: Defined at chip integration as either 0x00 (paired with write in any mode) or 0x3C (paired with write only in special modes), see device overview chapter.

The HCS12 core architecture limits the physical address space available to 64K bytes. The program page index register allows for integrating up to 1M byte of FLASH or ROM into the system by using the six page index bits to page 16K byte blocks into the program page window located from 0x8000 to 0xBFFF as defined in Table 22-14. CALL and RTC instructions have special access to read and write this register without using the address bus.

NOTE

Normal writes to this register take one cycle to go into effect. Writes to this register using the special access of the CALL and RTC instructions will be complete before the end of the associated instruction.

Table 22-13. MEMSIZ0 Field Descriptions

Field	Description
5:0 PIX[5:0]	**Program Page Index Bits 5:0** — These page index bits are used to select which of the 64 FLASH or ROM array pages is to be accessed in the program page window as shown in Table 22-14.

Table 22-14. Program Page Index Register Bits

PIX5	PIX4	PIX3	PIX2	PIX1	PIX0	Program Space Selected
0	0	0	0	0	0	16K page 0
0	0	0	0	0	1	16K page 1
0	0	0	0	1	0	16K page 2
0	0	0	0	1	1	16K page 3
. . . . .	. . . . .	. . . .	. . . . .	. . . . .	. . . . .	. . . . .
1	1	1	1	0	0	16K page 60
1	1	1	1	0	1	16K page 61
1	1	1	1	1	0	16K page 62
1	1	1	1	1	1	16K page 63

22.4 Functional Description

The MMC sub-block performs four basic functions of the core operation: bus control, address decoding and select signal generation, memory expansion, and security decoding for the system. Each aspect is described in the following subsections.

22.4.1 Bus Control

The MMC controls the address bus and data buses that interface the core with the rest of the system. This includes the multiplexing of the input data buses to the core onto the main CPU read data bus and control

of data flow from the CPU to the output address and data buses of the core. In addition, the MMC manages all CPU read data bus swapping operations.

22.4.2 Address Decoding

As data flows on the core address bus, the MMC decodes the address information, determines whether the internal core register or firmware space, the peripheral space or a memory register or array space is being addressed and generates the correct select signal. This decoding operation also interprets the mode of operation of the system and the state of the mapping control registers in order to generate the proper select. The MMC also generates two external chip select signals, emulation chip select ($\overline{ECS}$) and external chip select ($\overline{XCS}$).

22.4.2.1 Select Priority and Mode Considerations

Although internal resources such as control registers and on-chip memory have default addresses, each can be relocated by changing the default values in control registers. Normally, I/O addresses, control registers, vector spaces, expansion windows, and on-chip memory are mapped so that their address ranges do not overlap. The MMC will make only one select signal active at any given time. This activation is based upon the priority outlined in Table 22-15. If two or more blocks share the same address space, only the select signal for the block with the highest priority will become active. An example of this is if the registers and the RAM are mapped to the same space, the registers will have priority over the RAM and the portion of RAM mapped in this shared space will not be accessible. The expansion windows have the lowest priority. This means that registers, vectors, and on-chip memory are always visible to a program regardless of the values in the page select registers.

Table 22-15. Select Signal Priority

Priority	Address Space
Highest	BDM (internal to core) firmware or register space
...	Internal register space
...	RAM memory block
...	EEPROM memory block
...	On-chip FLASH or ROM
Lowest	Remaining external space

In expanded modes, all address space not used by internal resources is by default external memory space. The data registers and data direction registers for ports A and B are removed from the on-chip memory map and become external accesses. If the EME bit in the MODE register (see MEBI block description chapter) is set, the data and data direction registers for port E are also removed from the on-chip memory map and become external accesses.

In special peripheral mode, the first 16 registers associated with bus expansion are removed from the on-chip memory map (PORTA, PORTB, DDRA, DDRB, PORTE, DDRE, PEAR, MODE, PUCR, RDRIV, and the EBI reserved registers).

In emulation modes, if the EMK bit in the MODE register (see MEBI block description chapter) is set, the data and data direction registers for port K are removed from the on-chip memory map and become external accesses.

22.4.2.2 Emulation Chip Select Signal

When the EMK bit in the MODE register (see MEBI block description chapter) is set, port K bit 7 is used as an active-low emulation chip select signal, $\overline{\text{ECS}}$. This signal is active when the system is in emulation mode, the EMK bit is set and the FLASH or ROM space is being addressed subject to the conditions outlined in Section 22.4.3.2, "Extended Address (XAB19:14) and ECS Signal Functionality." When the EMK bit is clear, this pin is used for general purpose I/O.

22.4.2.3 External Chip Select Signal

When the EMK bit in the MODE register (see MEBI block description chapter) is set, port K bit 6 is used as an active-low external chip select signal, $\overline{\text{XCS}}$. This signal is active only when the $\overline{\text{ECS}}$ signal described above is not active and when the system is addressing the external address space. Accesses to unimplemented locations within the register space or to locations that are removed from the map (i.e., ports A and B in expanded modes) will not cause this signal to become active. When the EMK bit is clear, this pin is used for general purpose I/O.

22.4.3 Memory Expansion

The HCS12 core architecture limits the physical address space available to 64K bytes. The program page index register allows for integrating up to 1M byte of FLASH or ROM into the system by using the six page index bits to page 16K byte blocks into the program page window located from 0x8000 to 0xBFFF in the physical memory space. The paged memory space can consist of solely on-chip memory or a combination of on-chip and off-chip memory. This partitioning is configured at system integration through the use of the paging configuration switches (*pag_sw1:pag_sw0*) at the core boundary. The options available to the integrator are as given in Table 22-16 (this table matches Table 22-12 but is repeated here for easy reference).

Table 22-16. Allocated Off-Chip Memory Options

pag_sw1:pag_sw0	Off-Chip Space	On-Chip Space
00	876K bytes	128K bytes
01	768K bytes	256K bytes
10	512K bytes	512K bytes
11	0K byte	1M byte

Based upon the system configuration, the program page window will consider its access to be either internal or external as defined in Table 22-17.

Table 22-17. External/Internal Page Window Access

pag_sw1:pag_sw0	Partitioning	PIX5:0 Value	Page Window Access
00	876K off-Chip, 128K on-Chip	0x0000–0x0037	External
		0x0038–0x003F	Internal
01	768K off-chip, 256K on-chip	0x0000–0x002F	External
		0x0030–0x003F	Internal
10	512K off-chip, 512K on-chip	0x0000–0x001F	External
		0x0020–0x003F	Internal
11	0K off-chip, 1M on-chip	N/A	External
		0x0000–0x003F	Internal

NOTE

The partitioning as defined in Table 22-17 applies only to the allocated memory space and the actual on-chip memory sizes implemented in the system may differ. Please refer to the device overview chapter for actual sizes.

The PPAGE register holds the page select value for the program page window. The value of the PPAGE register can be manipulated by normal read and write (some devices don't allow writes in some modes) instructions as well as the CALL and RTC instructions.

Control registers, vector spaces, and a portion of on-chip memory are located in unpaged portions of the 64K byte physical address space. The stack and I/O addresses should also be in unpaged memory to make them accessible from any page.

The starting address of a service routine must be located in unpaged memory because the 16-bit exception vectors cannot point to addresses in paged memory. However, a service routine can call other routines that are in paged memory. The upper 16K byte block of memory space (0xC000–0xFFFF) is unpaged. It is recommended that all reset and interrupt vectors point to locations in this area.

22.4.3.1 CALL and Return from Call Instructions

CALL and RTC are uninterruptable instructions that automate page switching in the program expansion window. CALL is similar to a JSR instruction, but the subroutine that is called can be located anywhere in the normal 64K byte address space or on any page of program expansion memory. CALL calculates and stacks a return address, stacks the current PPAGE value, and writes a new instruction-supplied value to PPAGE. The PPAGE value controls which of the 64 possible pages is visible through the 16K byte expansion window in the 64K byte memory map. Execution then begins at the address of the called subroutine.

During the execution of a CALL instruction, the CPU:

- Writes the old PPAGE value into an internal temporary register and writes the new instruction-supplied PPAGE value into the PPAGE register.

- Calculates the address of the next instruction after the CALL instruction (the return address), and pushes this 16-bit value onto the stack.
- Pushes the old PPAGE value onto the stack.
- Calculates the effective address of the subroutine, refills the queue, and begins execution at the new address on the selected page of the expansion window.

This sequence is uninterruptable; there is no need to inhibit interrupts during CALL execution. A CALL can be performed from any address in memory to any other address.

The PPAGE value supplied by the instruction is part of the effective address. For all addressing mode variations except indexed-indirect modes, the new page value is provided by an immediate operand in the instruction. In indexed-indirect variations of CALL, a pointer specifies memory locations where the new page value and the address of the called subroutine are stored. Using indirect addressing for both the new page value and the address within the page allows values calculated at run time rather than immediate values that must be known at the time of assembly.

The RTC instruction terminates subroutines invoked by a CALL instruction. RTC unstacks the PPAGE value and the return address and refills the queue. Execution resumes with the next instruction after the CALL.

During the execution of an RTC instruction, the CPU:

- Pulls the old PPAGE value from the stack
- Pulls the 16-bit return address from the stack and loads it into the PC
- Writes the old PPAGE value into the PPAGE register
- Refills the queue and resumes execution at the return address

This sequence is uninterruptable; an RTC can be executed from anywhere in memory, even from a different page of extended memory in the expansion window.

The CALL and RTC instructions behave like JSR and RTS, except they use more execution cycles. Therefore, routinely substituting CALL/RTC for JSR/RTS is not recommended. JSR and RTS can be used to access subroutines that are on the same page in expanded memory. However, a subroutine in expanded memory that can be called from other pages must be terminated with an RTC. And the RTC unstacks a PPAGE value. So any access to the subroutine, even from the same page, must use a CALL instruction so that the correct PPAGE value is in the stack.

22.4.3.2 Extended Address (XAB19:14) and $\overline{\text{ECS}}$ Signal Functionality

If the EMK bit in the MODE register is set (see MEBI block description chapter) the PIX5:0 values will be output on XAB19:14 respectively (port K bits 5:0) when the system is addressing within the physical program page window address space (0x8000–0xBFFF) and is in an expanded mode. When addressing anywhere else within the physical address space (outside of the paging space), the XAB19:14 signals will be assigned a constant value based upon the physical address space selected. In addition, the active-low emulation chip select signal, $\overline{\text{ECS}}$, will likewise function based upon the assigned memory allocation. In the cases of 48K byte and 64K byte allocated physical FLASH/ROM space, the operation of the $\overline{\text{ECS}}$ signal will additionally depend upon the state of the ROMHM bit (see Section 22.3.2.4, “Miscellaneous System Control Register (MISC)”) in the MISC register. Table 22-18, Table 22-19, Table 22-20, and

Table 22-21 summarize the functionality of these signals based upon the allocated memory configuration. Again, this signal information is only available externally when the EMK bit is set and the system is in an expanded mode.

Table 22-18. 0K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	N/A	1	0x3D
0x4000–0x7FFF	N/A	N/A	1	0x3E
0x8000–0xBFFF	N/A	N/A	0	PIX[5:0]
0xC000–0xFFFF	N/A	N/A	0	0x3F

Table 22-19. 16K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	N/A	1	0x3D
0x4000–0x7FFF	N/A	N/A	1	0x3E
0x8000–0xBFFF	N/A	N/A	1	PIX[5:0]
0xC000–0xFFFF	N/A	N/A	0	0x3F

Table 22-20. 48K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	N/A	1	0x3D
0x4000–0x7FFF	N/A	0	0	0x3E
	N/A	1	1	
0x8000–0xBFFF	External	N/A	1	PIX[5:0]
	Internal	N/A	0	
0xC000–0xFFFF	N/A	N/A	0	0x3F

Table 22-21. 64K Byte Physical FLASH/ROM Allocated

Address Space	Page Window Access	ROMHM	ECS	XAB19:14
0x0000–0x3FFF	N/A	0	0	0x3D
	N/A	1	1	
0x4000–0x7FFF	N/A	0	0	0x3E
	N/A	1	1	
0x8000–0xBFFF	External	N/A	1	PIX[5:0]
	Internal	N/A	0	
0xC000–0xFFFF	N/A	N/A	0	0x3F

A graphical example of a memory paging for a system configured as 1M byte on-chip FLASH/ROM with 64K allocated physical space is given in Figure 22-12.

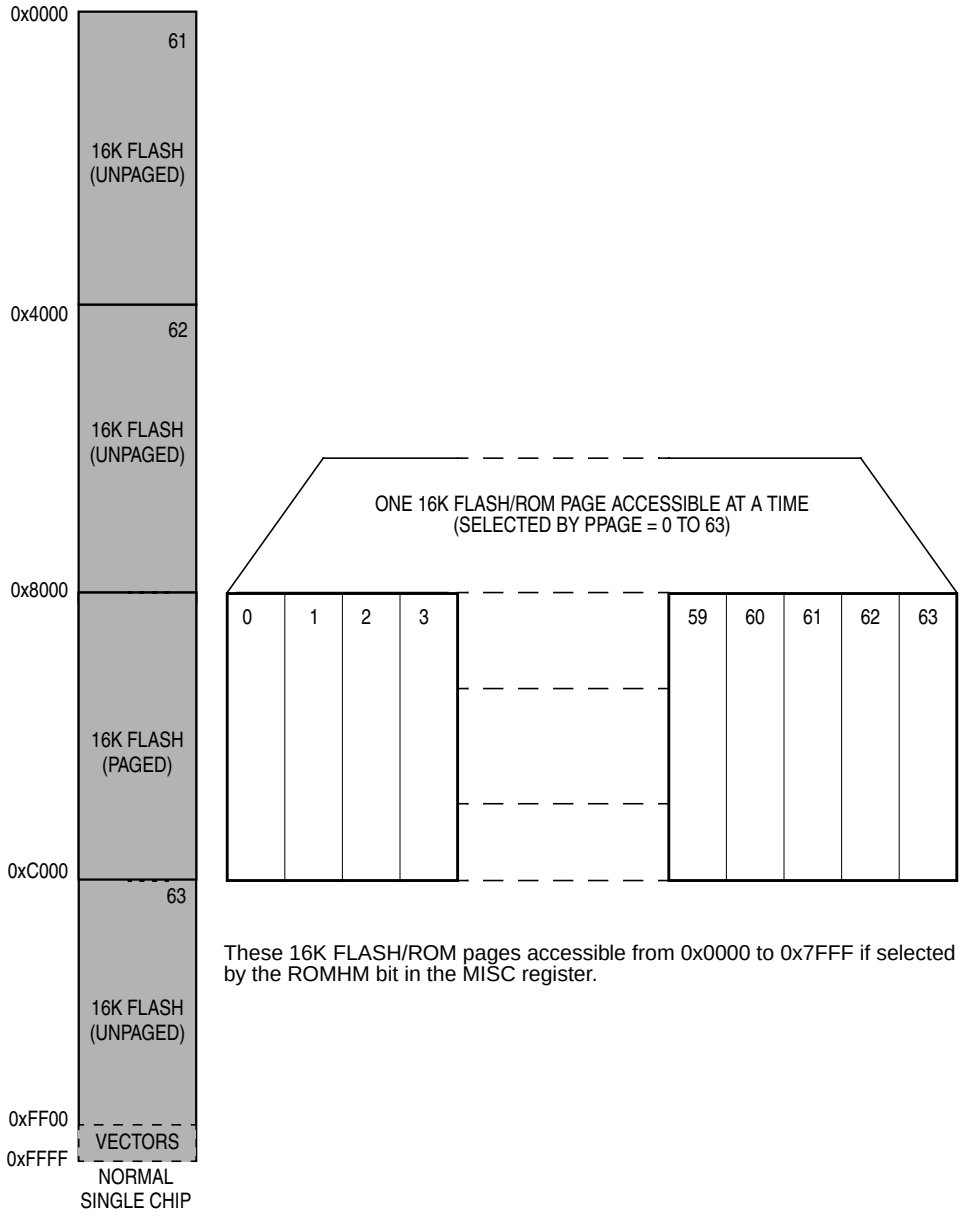


Figure 22-12. Memory Paging Example: 1M Byte On-Chip FLASH/ROM, 64K Allocation

Appendix A
Electrical Characteristics

A.1 General

This supplement contains the most accurate electrical information for the MC9S12HZ256 of microcontrollers available at the time of publication.

This introduction is intended to give an overview on several common topics like power supply, current injection etc.

A.1.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate.

NOTE

This classification is shown in the column labeled “C” in the parameter tables where appropriate.

P: Those parameters are guaranteed during production testing on each individual device.

C: Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.

T: Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.

D: Those parameters are derived mainly from simulations.

A.1.2 Power Supply

The MC9S12HZ256 utilizes several pins to supply power to the I/O ports, A/D converter, oscillator and PLL as well as the digital core.

The VDDA, VSSA pair supplies the A/D converter and the resistor ladder of the internal voltage regulator.

The VDDX1/VSSX1 and VDDX2/VSSX2 pairs supply the I/O pins except PH, PU, PV and PW. VDDR supplies the internal voltage regulator.

VDDM1/VSSM1, VDDM2/VSSM2 and VDDM3/VSSM3 pairs supply the ports PH, PU, PV and PW.

VDD1, VSS1 and VSS2 are the supply pins for the digital logic, VDDPLL, VSSPLL supply the oscillator and the PLL.

VSS1 and VSS2 are internally connected by metal.

VDDA, VDDX1, VDDX2, VDDM as well as VSSA, VSSX1, VSSX2 and VSSM are connected by anti-parallel diodes for ESD protection.

NOTE

In the following context VDD5 is used for either VDDA, VDDM, VDDR and VDDX1/2; VSS5 is used for either VSSA, VSSR and VSSX unless otherwise noted.
IDD5 denotes the sum of the currents flowing into the VDDA, VDDX1/2, VDDM and VDDR pins.
VDD is used for VDD1 and VDDPLL, VSS is used for VSS1, VSS2 and VSSPLL.
IDD is used for the sum of the currents flowing into VDD1 and VDDPLL.

A.1.3 Pins

There are four groups of functional pins.

A.1.3.1 5V I/O pins

Those I/O pins have a nominal level of 5V. This class of pins is comprised of all port I/O pins, the analog inputs, BKGD and the RESET pins.The internal structure of all those pins is identical, however some of the functionality may be disabled. E.g. for the analog inputs the output drivers, pull-up and pull-down resistors are disabled permanently.

A.1.3.2 Analog Reference

This group is made up by the VRH and VRL pins.

A.1.3.3 Oscillator

The pins XFC, EXTAL, XTAL dedicated to the oscillator have a nominal 2.5V level. They are supplied by VDDPLL.

A.1.3.4 TEST

This pin is used for production testing only.

A.1.4 Current Injection

Power supply must maintain regulation within operating V_{DD5} or V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD5}$) is greater than I_{DD5}, the injection current may flow out of VDD5 and could result in external power supply going out of regulation. Ensure external VDD5 load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power; e.g. if no system clock is present, or if clock rate is very low which would reduce overall power consumption.

A.1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only. A functional operation under or outside those maxima is not guaranteed. Stress beyond those limits may affect the reliability or cause permanent damage of the device.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS5} or V_{DD5}).

Table A-1. Absolute Maximum Ratings[1]

Num	Rating	Symbol	Min	Max	Unit
1	I/O, Regulator and Analog Supply Voltage	V_{DD5}	–0.3	6.0	V
2	Digital Logic Supply Voltage [2]	V_{DD}	–0.3	3.0	V
3	PLL Supply Voltage [2]	V_{DDPLL}	–0.3	3.0	V
4	Voltage difference VDDX1 to VDDX2 to VDDM and VDDA	Δ_{VDDX}	–0.3	0.3	V
5	Voltage difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.3	0.3	V
6	Digital I/O Input Voltage	V_{IN}	–0.3	6.0	V
7	Analog Reference	V_{RH}, V_{RL}	–0.3	6.0	V
8	XFC, EXTAL, XTAL inputs	V_{ILV}	–0.3	3.0	V
9	TEST input	V_{TEST}	–0.3	10.0	V
10	Instantaneous Maximum Current Single pin limit for all digital I/O pins except PU and PV [3]	I_D	–25	+25	mA
11	Instantaneous Maximum Current Single pin limit for Port PU and PV [4]	I_D	–55	+55	mA
12	Instantaneous Maximum Current Single pin limit for XFC, EXTAL, XTAL[5]	I_{DL}	–25	+25	mA
13	Instantaneous Maximum Current Single pin limit for TEST [6]	I_{DT}	–0.25	0	mA
14	Storage Temperature Range	T_{stg}	– 65	155	°C

1 Beyond absolute maximum ratings device might be damaged.

2 The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when the device is powered from an external source.

3 All digital I/O pins are internally clamped to $V_{SSX1/2}$ and $V_{DDX1/2}$, V_{SSM} and V_{DDM} or V_{SSA} and V_{DDA}.

4 Ports PU and PV are internally clamped to V_{SSM} and V_{DDM}.

5 Those pins are internally clamped to V_{SSPLL} and V_{DDPLL}.

6 This pin is clamped low to V_{SSPLL}, but not clamped high. This pin must be tied low in applications.

A.1.6 ESD Protection and Latch-up Immunity

All ESD testing is in conformity with CDF-AEC-Q100 Stress test qualification for Automotive Grade Integrated Circuits. During the device qualification ESD stresses were performed for the Human Body Model (HBM), the Machine Model (MM) and the Charge Device Model.

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification. Complete DC parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table A-2. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	W
	Storage Capacitance	C	100	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Machine	Series Resistance	R1	0	W
	Storage Capacitance	C	200	pF
	Number of Pulse per pin positive negative	–	– 3 3	
Latch-up	Minimum input voltage limit		–2.5	V
	Maximum input voltage limit		7.5	V

Table A-3. ESD and Latch-Up Protection Characteristics

Num	C	Rating	Symbol	Min	Max	Unit
1	C	Human Body Model (HBM)	V_{HBM}	2000	–	V
2	C	Machine Model (MM)	V_{MM}	200	–	V
3	C	Charge Device Model (CDM)	V_{CDM}	500	–	V

Table A-3. ESD and Latch-Up Protection Characteristics

4	C	Latch-up Current at T_A = 125°C positive negative	I_{LAT}	 +100 –100	–	mA
5	C	Latch-up Current at T_A = 27°C positive negative	I_{LAT}	 +200 –200	–	mA

A.1.7 Operating Conditions

This chapter describes the operating conditions of the device. Unless otherwise noted those conditions apply to all the following data.

NOTE

Please refer to the temperature rating of the device (C, V, M) with regards to the ambient temperature T_A and the junction temperature T_J. For power dissipation calculations refer to Section A.1.8, "Power Dissipation and Thermal Characteristics."

Table A-4. Operating Conditions

Rating	Symbol	Min	Typ	Max	Unit
I/O, Regulator and Analog Supply Voltage	V_{DD5}	4.5	5	5.5	V
Digital Logic Supply Voltage [1]	V_{DD}	2.35	2.5	2.75	V
PLL Supply Voltage [2]	V_{DDPLL}	2.35	2.5	2.75	V
Voltage Difference VDDX to VDDR and VDDA	Δ_{VDDX}	–0.1	0	0.1	V
Voltage Difference VSSX to VSSR and VSSA	Δ_{VSSX}	–0.1	0	0.1	V
Crystal oscillator (Colpitts)	f_{osc}	0.5	–	16	MHz
Crystal oscillator (Pierce)	f_{osc}	0.5	–	40	MHz
Bus Frequency	f_{bus}	0.5	–	25	MHz
Operating Junction Temperature Range **C parts** **V parts** **M parts**	T_J	–40	–	 100 120 140	°C
Operating Ambient Temperature Range[2] **C parts** **V parts** **M parts**	T_A	–40	27	 85 105 125	°C

1 The device contains an internal voltage regulator to generate the logic and PLL supply out of the I/O supply. The absolute maximum ratings apply when this regulator is disabled and the device is powered from an external source.

2 Please refer to Section A.1.8, "Power Dissipation and Thermal Characteristics," for more details about the relation between ambient temperature T_A and device junction temperature T_J.

A.1.8 Power Dissipation and Thermal Characteristics

Power dissipation and thermal characteristics are closely related. The user must assure that the maximum operating junction temperature is not exceeded. The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \Theta_{JA})$$

T_J = Junction Temperature, [°C]

T_A = Ambient Temperature, [°C]

P_D = Total Chip Power Dissipation, [W]

Θ_{JA} = Package Thermal Resistance, [°C/W]

The total power dissipation can be calculated from:

$$P_D = P_{INT} + P_{IO}$$

P_{INT} = Chip Internal Power Dissipation, [W]

$$P_{INT} = I_{DDR} \cdot V_{DDR} + I_{DDA} \cdot V_{DDA}$$

$$P_{IO} = \sum_i R_{DSON} \cdot I_{IO_i}^2$$

P_{IO} is the sum of all output currents on I/O ports associated with VDDX1,2 and VDDM1,2,3.

Table A-5. Thermal Package Characteristics[1]

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	T	Thermal Resistance LQFP112, single sided PCB[2]	θ_{JA}	–	–	54	°C/W
2	T	Thermal Resistance LQFP112, double sided PCB with 2 internal planes[3]	θ_{JA}	–	–	41	°C/W
3	T	Junction to Board LQFP112	θ_{JB}	—	—	31	°C/W
4	T	Junction to Case LQFP112	θ_{JC}	—	—	11	°C/W
5	T	Junction to Package Top LQFP112	Ψ_{JT}	—	—	2	°C/W
6	T	Thermal Resistance QFP 80, single sided PCB	θ_{JA}	—	—	51	°C/W
7	T	Thermal Resistance QFP 80, double sided PCB with 2 internal planes	θ_{JA}	—	—	41	°C/W
8	T	Junction to Board QFP80	θ_{JB}	—	—	27	°C/W
9	T	Junction to Case QFP80	θ_{JC}	—	—	14	°C/W
10	T	Junction to Package Top QFP80	Ψ_{JT}	—	—	3	°C/W

1 The values for thermal resistance are achieved by package simulations

[2] PC Board according to EIA/JEDEC Standard 51-2
[3] PC Board according to EIA/JEDEC Standard 51-7

A.1.9 I/O Characteristics

This section describes the characteristics of all 5V I/O pins. All parameters are not always applicable, e.g. not all pins feature pull up/down resistances.

Table A-6. 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Input High Voltage	V_{IH}	0.65*V_{DD5}	–	V_{DD5} + 0.3	V
2	P	Input Low Voltage	V_{IL}	V_{SS5} – 0.3	–	0.35*V_{DD5}	V
3	C	Input Hysteresis	V_{HYS}		250		mV
4	P	Input Leakage Current except PU, PV (pins in high impedance input mode)[1] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–1.0	–	1.0	µA
5	P	Input Leakage Current PU, PV (pins in high impedance input mode)[2] V_{in} = V_{DD5} or V_{SS5}	I_{in}	–2.5	–	2.5	µA
6	P	Output High Voltage (pins in output mode, except PU and PV) Partial Drive I_{OH} = –1.0mA Full Drive I_{OH} = –10mA	V_{OH}	V_{DD5} – 0.8	–	–	V
7	P	Output Low Voltage (pins in output mode except PU and PV) Partial Drive I_{OL} = +1.0mA Full Drive I_{OL} = +10mA	V_{OL}	–	–	0.8	V
8	P	Output High Voltage (pins PU and PV in output mode) I_{OH} = –20mA (typical value at 25°C)	V_{OH}	V_{DD5} – 0.32	V_{DD5} – 0.2	–	V
9	P	Output Low Voltage (pins PU and PV in output mode) I_{OL} = +20mA (typical value at 25°C)	V_{OL}	–	.2	0.32	V
10	C	Output Rise Time (pins PU and PV in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH}	t_r	60	100	130	ns
11	C	Output Fall Time (pins PU and PV in output mode with slew control enabled) V_{DD5}=5V, R_{load}=1KΩ, 10% to 90% of V_{OH}	t_f	60	100	130	ns
12	P	Internal Pull Up Device Current, tested at V_{IL} Max.	I_{PUL}	–	–	–130	µA
13	P	Internal Pull Up Device Current, tested at V_{IH} Min.	I_{PUH}	–10	–	–	µA
14	P	Internal Pull Down Device Current, tested at V_{IH} Min.	I_{PDH}	–	–	130	µA

Table A-6. 5V I/O Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
15	P	Internal Pull Down Device Current, tested at V_{IL} Max.	I_{PDL}	10	–	–	µA
16	D	Input Capacitance	C_{in}		6	–	pF
17	T	Injection current[3] Single Pin limit Total Device Limit. Sum of all injected currents	 I_{ICS} I_{ICP}	 –2.5 –25	–	 2.5 25	mA
18	P	Port AD Interrupt Input Pulse filtered[4]	t_{PULSE}			3	µs
19	P	Port AD Interrupt Input Pulse passed[4]	t_{PULSE}	10			µs

1 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C

2 Maximum leakage current occurs at maximum operating temperature. Current decreases by approximately one-half for each 8 C to 12 C in the temperature range from 50 C to 125 C

3 Refer to Section A.1.4, “Current Injection,” for more details

4 Parameter only applies in STOP or Pseudo STOP mode.

A.1.10 Supply Currents

This section describes the current consumption characteristics of the device as well as the conditions for the measurements.

A.1.10.1 Measurement Conditions

All measurements are without output loads. Unless otherwise noted the currents are measured in single chip mode, internal voltage regulator enabled and at 16MHz bus frequency using a 4MHz oscillator in Colpitts mode. Production testing is performed using a square wave signal at the EXTAL input.

A.1.10.2 Additional Remarks

In expanded modes the currents flowing in the system are highly dependent on the load at the address, data and control signals as well as on the duty cycle of those signals. No generally applicable numbers can be given. A very good estimate is to take the single chip currents and add the currents due to the external loads.

Table A-7. Supply Current Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Run supply currents Single Chip, Internal regulator enabled	I_{DD5}			65	mA
2		Wait Supply current	I_{DDW}				mA
	P	All modules enabled, PLL on				40	
	P	only RTI enabled [1]				5	
3		Pseudo Stop Current (RTI and COP disabled) [1, 2]	I_{DDPS}				µA
	C	–40°C			360		
	P	27°C			420	520	
	C	70°C			760		
	C	85°C			800		
	P	C Temp Option 100°C			950	2000	
	C	105°C			1000		
	P	V Temp Option 120°C			1500	3300	
	C	125°C			1700		
	P	M Temp Option 140° C			2500	4800	
4		Pseudo Stop Current (RTI and COP enabled) [1, 2]	I_{DDPS}				µA
	C	–40°C			420		
	C	27°C			480		
	C	70°C			820		
	C	85°C			860		
	C	105°C			1050		
	C	125°C			1700		
	C	140°C			2500		
5		Stop Current [2]	I_{DDS}				µA
	C	–40°C			20		
	P	27°C			40	100	
	C	70°C			200		
	C	85°C			300		
	P	C Temp Option 100°C			550	1500	
	C	105°C			700		
	P	V Temp Option 120°C			1200	2900	
	C	125°C			1400		
	P	M Temp Option 140°C			2200	4500	

1 PLL off

2 At those low power dissipation levels $T_J = T_A$ can be assumed

A.2 ATD

This section describes the characteristics of the analog to digital converter.

A.2.1 ATD Operating Characteristics

The Table A-8 shows conditions under which the ATD operates.

The following constraints exist to obtain full-scale, full range results:
$V_{SSA} \le V_{RL} \le V_{IN} \le V_{RH} \le V_{DDA}$. This constraint exists since the sample buffer amplifier can not drive beyond the power supply levels that it ties to. If the input level goes outside of this range it will effectively be clipped.

Table A-8. ATD Operating Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	Reference Potential Low High	 V_{RL} V_{RH}	 V_{SSA} $V_{DDA}/2$		 $V_{DDA}/2$ V_{DDA}	 V V
2	C	Differential Reference Voltage[1]	$V_{RH}-V_{RL}$	4.50	5.00	5.25	V
3	D	ATD Clock Frequency	f_{ATDCLK}	0.5		2.0	MHz
4	D	ATD 10-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV10} T_{CONV10}	 14 7		 28 14	 Cycles µs
5	D	ATD 8-Bit Conversion Period Clock Cycles[2] Conv, Time at 2.0MHz ATD Clock f_{ATDCLK}	 N_{CONV8} T_{CONV8}	 12 6		 26 13	 Cycles µs
6	D	Stop Recovery Time (V_{DDA}=5.0 Volts)	t_{SR}			20	µs
7	P	Reference Supply current	I_{REF}			0.375	mA

1 Full accuracy is not guaranteed when differential voltage is less than 4.50V

2 The minimum time assumes a final sample period of 2 ATD clocks cycles while the maximum time assumes a final sample period of 16 ATD clocks.

A.2.2 Factors influencing accuracy

Three factors – source resistance, source capacitance and current injection – have an influence on the accuracy of the ATD.

A.2.2.1 Source Resistance:

Due to the input pin leakage current as specified in Table A-6 in conjunction with the source resistance there will be a voltage drop from the signal source to the ATD input. The maximum source resistance R_S specifies results in an error of less than 1/2 LSB (2.5mV) at the maximum leakage current. If device or operating conditions are less than worst case or leakage-induced error is acceptable, larger values of source resistance is allowed.

A.2.2.2 Source Capacitance

When sampling an additional internal capacitor is switched to the input. This can cause a voltage drop due to charge sharing with the external and the pin capacitance. For a maximum sampling error of the input voltage ≤ 1LSB, then the external filter capacitor, $C_f \geq 1024 * (C_{INS} - C_{INN})$.

A.2.2.3 Current Injection

There are two cases to consider.

1. A current is injected into the channel being converted. The channel being stressed has conversion values of $3FF ($FF in 8-bit mode) for analog inputs greater than V_{RH} and $000 for values less than V_{RL} unless the current is higher than specified as disruptive condition.
2. Current is injected into pins in the neighborhood of the channel being converted. A portion of this current is picked up by the channel (coupling ratio K), This additional current impacts the accuracy of the conversion depending on the source resistance.
   The additional input voltage error on the converted channel can be calculated as $V_{ERR} = K * R_S * I_{INJ}$, with I_{INJ} being the sum of the currents injected into the two pins adjacent to the converted channel.

Table A-9. ATD Electrical Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Max input Source Resistance	R_S	–	–	1	KΩ
2	T	Total Input Capacitance Non Sampling Sampling	 C_{INN} C_{INS}			 10 22	pF
3	C	Disruptive Analog Input Current	I_{NA}	–2.5		2.5	mA
4	C	Coupling Ratio positive current injection	K_p			10^{-4}	A/A
5	C	Coupling Ratio negative current injection	K_n			10^{-2}	A/A

A.2.3 ATD accuracy

Table A-10 specifies the ATD conversion performance excluding any errors due to current injection, input capacitance and source resistance.

Table A-10. ATD Conversion Performance

Conditions are shown in Table A-4 unless otherwise noted
$V_{REF} = V_{RH} – V_{RL}$ = 5.12V. Resulting to one 8 bit count = 20mV and one 10 bit count = 5mV
f_{ATDCLK} = 2.0MHz

Num	C	Rating	Symbol	Min	Typ	Max	Unit
1	P	10-Bit Resolution	LSB		5		mV
2	P	10-Bit Differential Nonlinearity	DNL	–1		1	Counts
3	P	10-Bit Integral Nonlinearity	INL	–2.5	±1.5	2.5	Counts
4	P	10-Bit Absolute Error (Port AD)[1]	AE	–3	±2.0	3	Counts
5	P	10-Bit Absolute Error (Port L)[1]	AE	–4	±3.0	4	Counts
6	P	8-Bit Resolution	LSB		20		mV
7	P	8-Bit Differential Nonlinearity	DNL	–0.5		0.5	Counts
8	P	8-Bit Integral Nonlinearity	INL	–1.0	±0.5	1.0	Counts
9	P	8-Bit Absolute Error (Port AD)[1]	AE	–1.5	±1.0	1.5	Counts
10	P	8-Bit Absolute Error (Port L)[1]	AE	–2.0	±1.5	2.0	Counts

[1] These values include the quantization error which is inherently 1/2 count for any A/D converter.

For the following definitions see also Figure A-1.

Differential Non-Linearity (DNL) is defined as the difference between two adjacent switching steps.

$$DNL(i) = \frac{V_i - V_{i-1}}{1LSB} - 1$$

The Integral Non-Linearity (INL) is defined as the sum of all DNLs:

$$INL(n) = \sum_{i=1}^{n} DNL(i) = \frac{V_n - V_0}{1LSB} - n$$

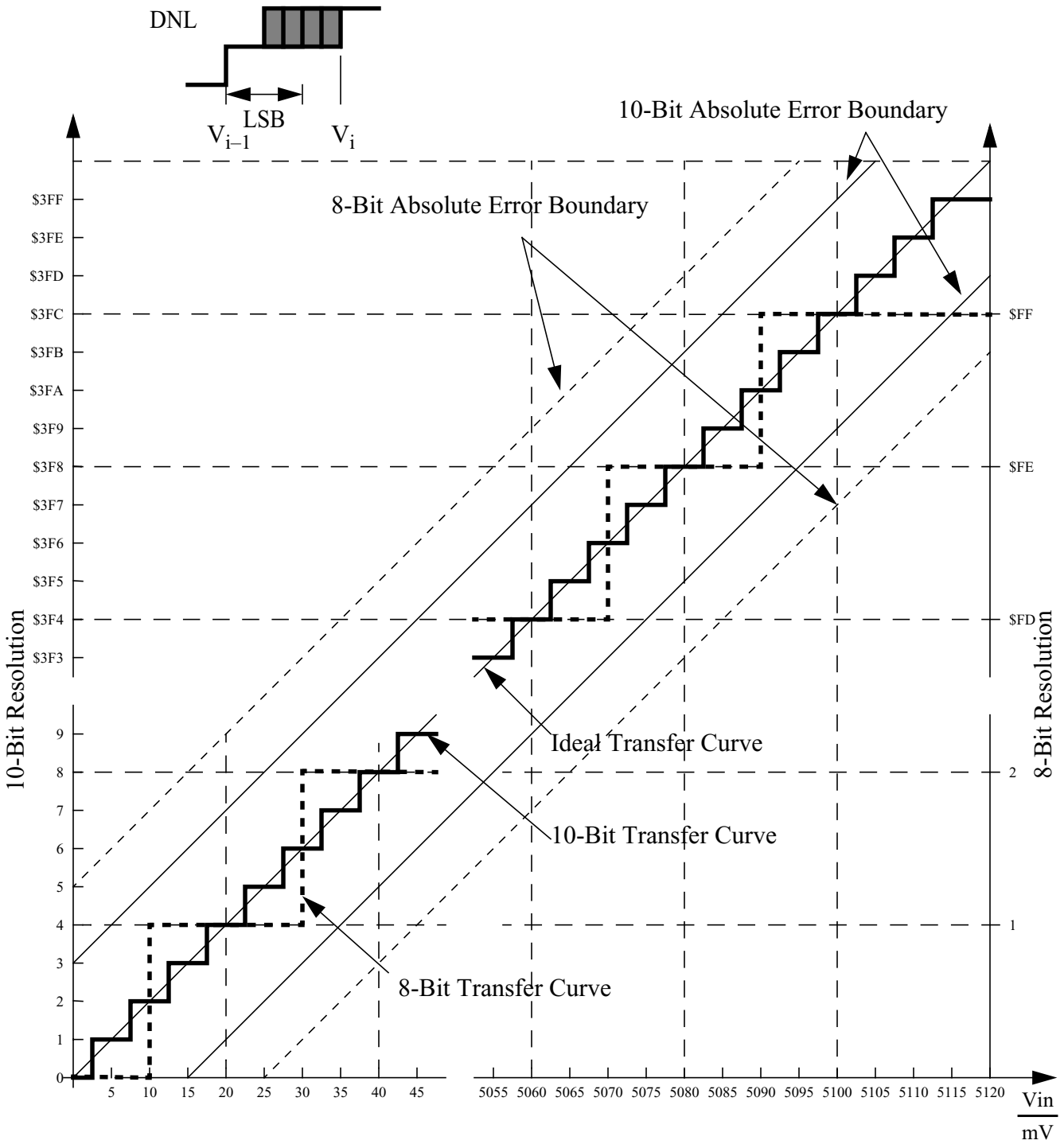


Figure A-1. ATD Accuracy Definitions

A.3 NVM, Flash and EEPROM

NOTE

Unless otherwise noted the abbreviation NVM (Non Volatile Memory) is used for both Flash and EEPROM.

A.3.1 NVM timing

The time base for all NVM program or erase operations is derived from the oscillator. A minimum oscillator frequency f_{NVMOSC} is required for performing program or erase operations. The NVM modules do not have any means to monitor the frequency and will not prevent program or erase operation at frequencies above or below the specified minimum. Attempting to program or erase the NVM modules at a lower frequency a full program or erase transition is not assured.

The Flash and EEPROM program and erase operations are timed using a clock derived from the oscillator using the FCLKDIV and ECLKDIV registers respectively. The frequency of this clock must be set within the limits specified as f_{NVMOP}.

The minimum program and erase times shown in Table A-11 are calculated for maximum f_{NVMOP} and maximum f_{bus}. The maximum times are calculated for minimum f_{NVMOP} and a f_{bus} of 2MHz.

A.3.1.1 Single Word Programming

The programming time for single word programming is dependant on the bus frequency as a well as on the frequency f_{NVMOP} and can be calculated according to the following formula.

$$t_{swpgm} = 9 \cdot \frac{1}{f_{NVMOP}} + 25 \cdot \frac{1}{f_{bus}}$$

A.3.1.2 Row Programming

Flash programming where up to 32 words in a row can be programmed consecutively by keeping the command pipeline filled. The time to program a consecutive word can be calculated as:

$$t_{bwpgm} = 4 \cdot \frac{1}{f_{NVMOP}} + 9 \cdot \frac{1}{f_{bus}}$$

The time to program a whole row is:

$$t_{brpgm} = t_{swpgm} + 31 \cdot t_{bwpgm}$$

Row programming is more than 2 times faster than single word programming.

A.3.1.3 Sector Erase

Erasing a 512 byte Flash sector or a 4 byte EEPROM sector takes:

$$t_{era} \approx 4000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.4 Mass Erase

Erasing a NVM block takes:

$$t_{mass} \approx 20000 \cdot \frac{1}{f_{NVMOP}}$$

The setup time can be ignored for this operation.

A.3.1.5 Blank Check

The time it takes to perform a blank check on the Flash or EEPROM is dependant on the location of the first non-blank word starting at relative address zero. It takes one bus cycle per word to verify plus a setup of the command.

$$t_{check} \approx location \cdot t_{cyc} + 10 \cdot t_{cyc}$$

Table A-11. NVM Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	D	External Oscillator Clock	f_{NVMOSC}	0.5		50 [1]	MHz
2	D	Bus frequency for Programming or Erase Operations	f_{NVMBUS}	1			MHz
3	D	Operating Frequency	f_{NVMOP}	150		200	kHz
4	P	Single Word Programming Time	t_{swpgm}	46 [2]		74.5 [3]	µs
5	D	Flash Burst Programming consecutive word [4]	t_{bwpgm}	20.4 [2]		31 [3]	µs
6	D	Flash Burst Programming Time for 32 Words [4]	t_{brpgm}	678.4 [2]		1035.5 [3]	µs
7	P	Sector Erase Time	t_{era}	20 [5]		26.7 [3]	ms
8	P	Mass Erase Time	t_{mass}	100 [5]		133 [3]	ms
9	D	Blank Check Time Flash per block	t_{check}	11 [6]		32778 [7]	t_{cyc}
10	D	Blank Check Time EEPROM per block	t_{check}	11 [6]		2058[7]	t_{cyc}

1 Restrictions for oscillator in crystal mode apply!

2 Minimum Programming times are achieved under maximum NVM operating frequency f_{NVMOP} and maximum bus frequency f_{bus}.

3 Maximum Erase and Programming times are achieved under particular combinations of f_{NVMOP} and bus frequency f_{bus}. Refer to formulae in Sections Section A.3.1.1, “Single Word Programming,” through Section A.3.1.4, “Mass Erase,” for guidance.

4 urst Programming operations are not applicable to EEPROM

5 Minimum Erase times are achieved under maximum NVM operating frequency f_{NVMOP}

6 Minimum time, if first word in the array is not blank

7 Maximum time to complete check on an erased block

A.3.2 NVM Reliability

The reliability of the NVM blocks is guaranteed by stress test during qualification, constant process monitors and burn-in to screen early life failures.

The failure rates for data retention and program/erase cycling are specified at the operating conditions noted.

The program/erase cycle count on the sector is incremented every time a sector or mass erase event is executed.

NOTE

All values shown in Table A-12 are target values and subject to further extensive characterization.

Table A-12. NVM Reliability Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	C	Data Retention at an average junction temperature of T_{Javg} = 70°C	t_{NVMRET}	15			Years
2	C	Flash number of Program/Erase cycles	n_{FLPE}	1000	10,000		Cycles
3	C	EEPROM number of Program/Erase cycles (–40°C ≤ T_J ≤ 0°C)	n_{EEPE}	10,000			Cycles
4	C	EEPROM number of Program/Erase cycles (0°C < T_J ≤ 140°C)	n_{EEPE}	100,000			Cycles

A.4 Voltage Regulator

A.4.1 Operating Conditions

Table A-13. Voltage Regulator - Operating Conditions

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Characteristic**	**Symbol**	**Min**	**Typical**	**Max**	**Unit**
1	P	Input Voltages	$V_{VDDR,A}$	4.5	—	5.5	V
2	P	Regulator Current Shutdown Mode	I_{REG}	—	12	40	µA
3	P	Output Voltage Core Full Performance Mode Shutdown Mode	V_{DD}	2.35 —	2.5 —[1]	2.75 —	V V
4	P	Output Voltage PLL Full Performance Mode Shutdown Mode	V_{DDPLL}	2.35 —	2.5 —[2]	2.75 —	V V
7	P	Low Voltage Interrupt[3] Assert Level Deassert Level	 V_{LVIA} V_{LVID}	 4.0 4.15	 4.37 4.52	 4.66 4.77	 V V
8	P	Low Voltage Reset[4] Assert Level	V_{LVRA}	2.25	—	—	V
9	C	Power-on Reset[5] Assert Level Deassert Level	 V_{PORA} V_{PORD}	 0.97 —	 — —	 — 2.05	 V V

1 High Impedance Output

2 High Impedance Output

3 Monitors V_{DDA}, active only in Full Performance Mode. Indicates I/O & ADC performance degradation due to low supply voltage.

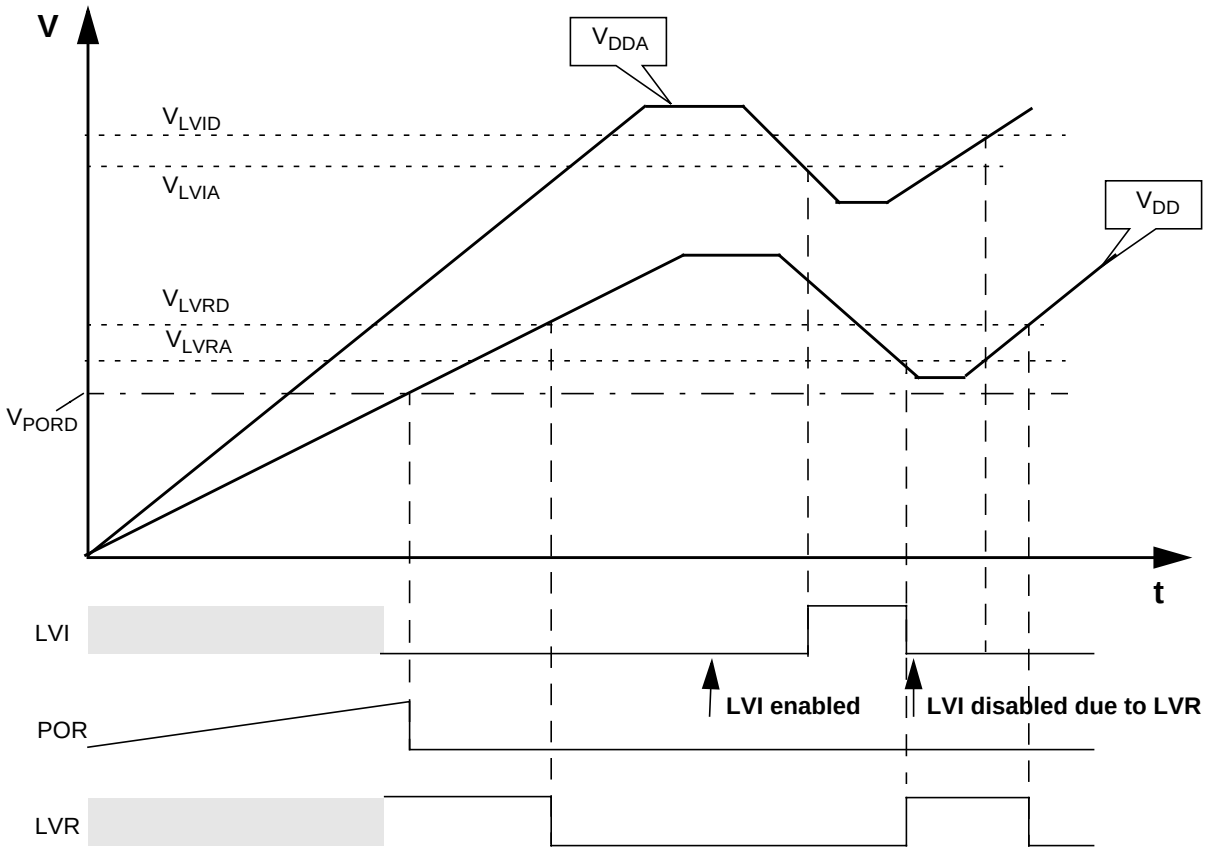
4 Monitors V_{DD}, active only in Full Performance Mode. MCU is monitored by the POR in RPM (see Figure A-2)

5 Monitors V_{DD}. Active in all modes.

A.4.2 Chip Power-up and Voltage Drops

The voltage regulator sub modules LVI (low voltage interrupt), POR (power-on reset) and LVR (low voltage reset) handle chip power-up or drops of the supply voltage. Their function is described in Figure A-2.

Figure A-2. Voltage Regulator - Chip Power-up and Voltage Drops (not scaled)



A.4.3 Output Loads

A.4.3.1 Resistive Loads

On-chip voltage regulator intended to supply the internal logic and oscillator circuits allows no external DC loads.

A.4.3.2 Capacitive Loads

The capacitive loads are specified in Table A-14. Ceramic capacitors with X7R dielectricum are required.

Table A-14. Voltage Regulator - Capacitive Loads

Num	Characteristic	Symbol	Min	Typical	Max	Unit
1	VDD external capacitive load	C_{DDext}	200	440	12000	nF
3	VDDPLL external capacitive load	$C_{DDPLLext}$	90	220	5000	nF

A.5 Reset, Oscillator and PLL

This section summarizes the electrical characteristics of the various startup scenarios for Oscillator and Phase-Locked-Loop (PLL).

A.5.1 Startup

Table A-15 summarizes several startup characteristics explained in this section. Detailed description of the startup behavior can be found in the Clock and Reset Generator (CRG) Block User Guide.

Table A-15. Startup Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	T	POR release level	V_{PORR}			2.07	V
2	T	POR assert level	V_{PORA}	0.97			V
3	D	Reset input pulse width, minimum input time	PW_{RSTL}	2			t_{osc}
4	D	Startup from Reset	n_{RST}	192		196	n_{osc}
5	D	Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	PW_{IRQ}	20			ns
6	D	Wait recovery startup time	t_{WRS}			14	t_{cyc}

A.5.1.1 POR

The release level V_{PORR} and the assert level V_{PORA} are derived from the VDD supply. They are also valid if the device is powered externally. After releasing the POR reset the oscillator and the clock quality check are started. If after a time t_{CQOUT} no valid oscillation is detected, the MCU will start using the internal self clock. The fastest startup time possible is given by n_{uposc}.

A.5.1.2 SRAM Data Retention

Provided an appropriate external reset signal is applied to the MCU, preventing the CPU from executing code when VDD5 is out of specification limits, the SRAM contents integrity is guaranteed if after the reset the PORF bit in the CRG Flags Register has not been set.

A.5.1.3 External Reset

When external reset is asserted for a time greater than PW_{RSTL} the CRG module generates an internal reset, and the CPU starts fetching the reset vector without doing a clock quality check, if there was an oscillation before reset.

A.5.1.4 Stop Recovery

Out of STOP the controller can be woken up by an external interrupt. A clock quality check as after POR is performed before releasing the clocks to the system.

A.5.1.5 Pseudo Stop and Wait Recovery

The recovery from Pseudo STOP and Wait are essentially the same since the oscillator was not stopped in both modes. The controller can be woken up by internal or external interrupts. After t_{wrs} the CPU starts fetching the interrupt vector.

A.5.2 Oscillator

The device features an internal Colpitts and Pierce oscillator. The selection of Colpitts oscillator or Pierce oscillator/external clock depends on the XCLKS signal which is sampled during reset. Pierce oscillator/external clock mode allows the input of a square wave. Before asserting the oscillator to the internal system clocks the quality of the oscillation is checked for each start from either power-on, STOP or oscillator fail. t_{CQOUT} specifies the maximum time before switching to the internal self clock mode after POR or STOP if a proper oscillation is not detected. The quality check also determines the minimum oscillator start-up time t_{UPOSC}. The device also features a clock monitor. A Clock Monitor Failure is asserted if the frequency of the incoming clock signal is below the Assert Frequency $f_{CMFA.}$

Table A-16. Oscillator Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1a	C	Crystal oscillator range (Colpitts)	f_{OSC}	0.5		16	MHz
1b	C	Crystal oscillator range (Pierce) [1]	f_{OSC}	0.5		40	MHz
2	P	Startup Current	i_{OSC}	100			µA
3	C	Oscillator start-up time (Colpitts)	t_{UPOSC}		8[2]	100[3]	ms
4	D	Clock Quality check time-out	t_{CQOUT}	0.45		2.5	s
5	P	Clock Monitor Failure Assert Frequency	f_{CMFA}	50	100	200	KHz
6	P	External square wave input frequency [4]	f_{EXT}	0.5		50	MHz
7	D	External square wave pulse width low[4]	t_{EXTL}	9.5			ns
8	D	External square wave pulse width high[4]	t_{EXTH}	9.5			ns
9	D	External square wave rise time[4]	t_{EXTR}			1	ns
10	D	External square wave fall time[4]	t_{EXTF}			1	ns
11	D	Input Capacitance (EXTAL, XTAL pins)	C_{IN}		7		pF
12	C	DC Operating Bias in Colpitts Configuration on EXTAL Pin	V_{DCBIAS}		1.1		V
13	P	EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$	0.75*V_{DDPLL}			V
	T	EXTAL Pin Input High Voltage[4]	$V_{IH,EXTAL}$			V_{DDPLL} + 0.3	V
14	P	EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$			0.25*V_{DDPLL}	V
	T	EXTAL Pin Input Low Voltage[4]	$V_{IL,EXTAL}$	V_{SSPLL} - 0.3			V
15	C	EXTAL Pin Input Hysteresis[4]	$V_{HYS,EXTAL}$		250		mV

1 Depending on the crystal a damping series resistor might be necessary

2 f_{osc} = 4MHz, C = 22pF.

3 Maximum value is for extreme cases using high Q, low frequency crystals

4 Only valid if Pierce oscillator/external clock mode is selected

A.5.3 Phase Locked Loop

The oscillator provides the reference clock for the PLL. The PLL´s Voltage Controlled Oscillator (VCO) is also the system clock source in self clock mode.

A.5.3.1 XFC Component Selection

This section describes the selection of the XFC components to achieve a good filter characteristics.

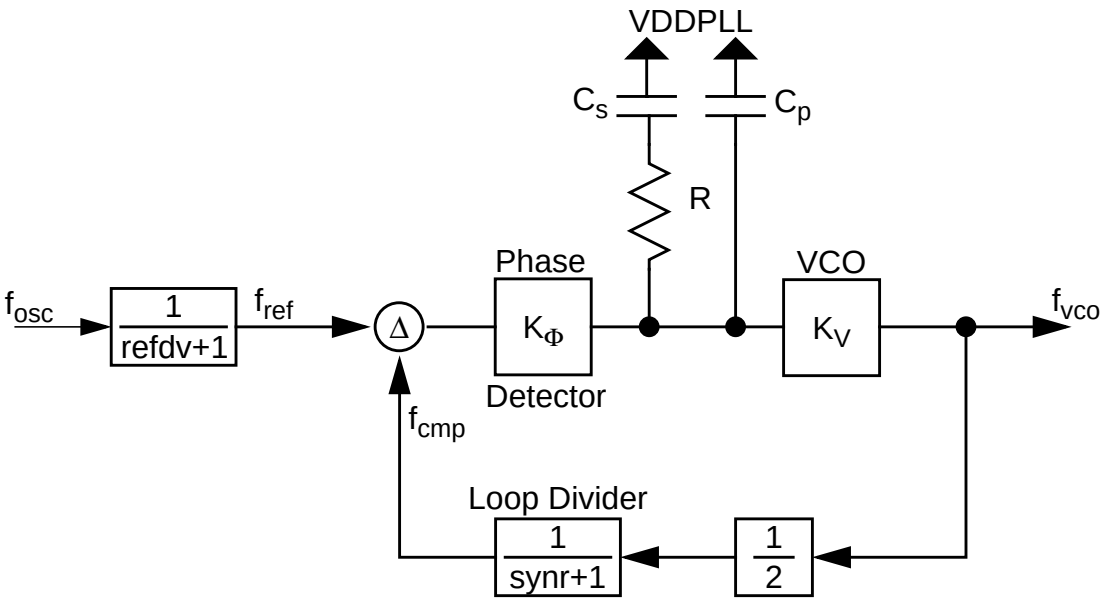


Figure A-3. Basic PLL Functional Diagram

The following procedure can be used to calculate the resistance and capacitance values using typical values for K_1, f_1 and i_{ch} from Table A-17.

The VCO Gain at the desired VCO output frequency is approximated by:

$$K_V = K_1 \cdot e^{\frac{(f_1 - f_{vco})}{K_1 \cdot 1V}}$$

The phase detector relationship is given by:

$$K_\Phi = i_{ch} \cdot K_V$$

i_{ch} is the current in tracking mode.

The loop bandwidth f_C should be chosen to fulfill the Gardner's stability criteria by at least a factor of 10, typical values are 50. $\zeta = 0.9$ ensures a good transient response.

$$f_C < \frac{2 \cdot \zeta \cdot f_{ref}}{\pi \cdot \left(\zeta + \sqrt{1 + \zeta^2}\right)} \quad \frac{1}{50} \rightarrow f_C < \frac{f_{ref}}{4 \cdot 50}; (\zeta = 0.9)$$

And finally the frequency relationship is defined as

$$n = \frac{f_{VCO}}{f_{ref}} = 2 \cdot (synr + 1)$$

With the above inputs the resistance can be calculated as:

$$R = \frac{2 \cdot \pi \cdot n \cdot f_C}{K_\Phi}$$

The capacitance C_s can now be calculated as:

$$C_s = \frac{2 \cdot \zeta^2}{\pi \cdot f_C \cdot R} \approx \frac{0.516}{f_C \cdot R}; (\zeta = 0.9)$$

The capacitance C_p should be chosen in the range of:

$$C_s / 20 \leq C_p \leq C_s / 10$$

The stabilization delays shown in Table A-17 are dependant on PLL operational settings and external component selection (e.g. crystal, XFC filter).

A.5.3.2 Jitter Information

The basic functionality of the PLL is shown in Figure A-3. With each transition of the clock f_{cmp}, the deviation from the reference clock f_{ref} is measured and input voltage to the VCO is adjusted accordingly.The adjustment is done continuously with no abrupt changes in the clock output frequency. Noise, voltage, temperature and other factors cause slight variations in the control loop resulting in a clock jitter. This jitter affects the real minimum and maximum clock periods as illustrated in Figure A-4.

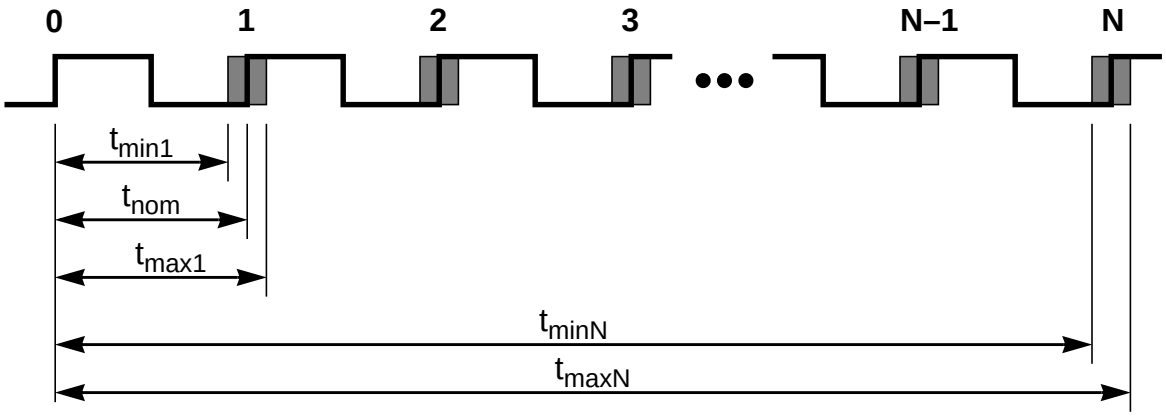


Figure A-4. Jitter Definitions

The relative deviation of t_{nom} is at its maximum for one clock period, and decreases towards zero for larger number of clock periods (N).

Defining the jitter as:

$$J(N) = \max\left(\left|1 - \frac{t_{max}(N)}{N \cdot t_{nom}}\right|, \left|1 - \frac{t_{min}(N)}{N \cdot t_{nom}}\right|\right)$$

For N < 100, the following equation is a good fit for the maximum jitter:

$$J(N) = \frac{j_1}{\sqrt{N}} + j_2$$

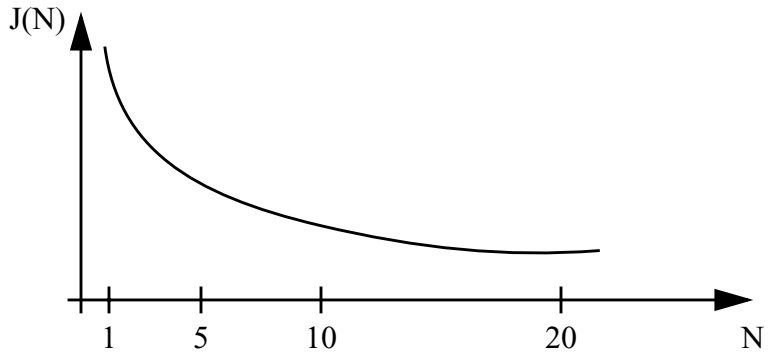


Figure A-5. Maximum bus clock jitter approximation

This is very important to notice with respect to timers, serial modules where a pre-scaler will eliminate the effect of the jitter to a large extent.

Table A-17. PLL Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Self Clock Mode frequency	f_{SCM}	1		5.5	MHz
2	D	VCO locking range	f_{VCO}	8		50	MHz
3	D	Lock Detector transition from Acquisition to Tracking mode	$\|\Delta_{trk}\|$	3		4	%[1]
4	D	Lock Detection	$\|\Delta_{Lock}\|$	0		1.5	%[1]
5	D	Un-Lock Detection	$\|\Delta_{unl}\|$	0.5		2.5	%[1]
6	D	Lock Detector transition from Tracking to Acquisition mode	$\|\Delta_{unt}\|$	6		8	%[1]
7	C	PLLON Total Stabilization delay (Auto Mode) [2]	t_{stab}		0.5		ms
8	D	PLLON Acquisition mode stabilization delay [2]	t_{acq}		0.3		ms
9	D	PLLON Tracking mode stabilization delay [2]	t_{al}		0.2		ms
10	D	Fitting parameter VCO loop gain	K_1		–100		MHz/V
11	D	Fitting parameter VCO loop frequency	f_1		60		MHz
12	D	Charge pump current acquisition mode	$\| i_{ch} \|$		38.5		µA
13	D	Charge pump current tracking mode	$\| i_{ch} \|$		3.5		µA
14	C	Jitter fit parameter 1 [2]	j_1			1.1	%
15	C	Jitter fit parameter 2 [2]	j_2			0.13	%

1 % deviation from target frequency

2 f_{REF} = 4MHz, f_{BUS} = 25MHz equivalent f_{VCO} = 50MHz: REFDV = #$03, SYNR = #$18, Cs = 4.7nF, Cp = 470pF, Rs = 10KΩ.

A.6 MSCAN

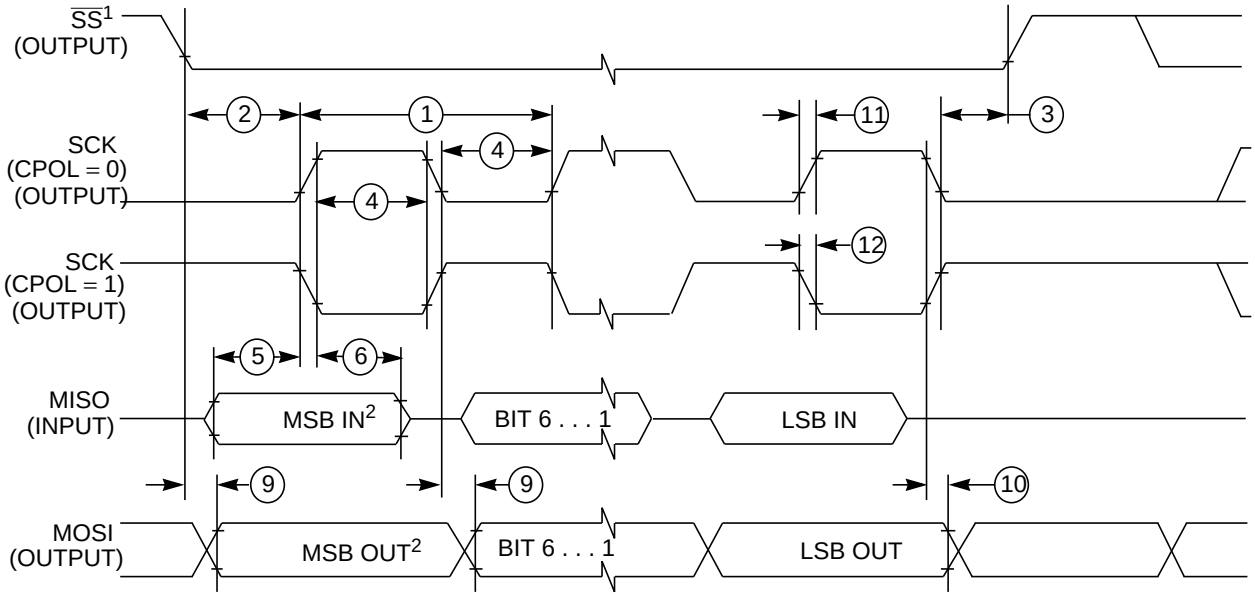
Table A-18. MSCAN Wake-up Pulse Characteristics

Conditions are shown in Table A-4 unless otherwise noted							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	MSCAN Wake-up dominant pulse filtered	t_{WUP}			2	µs
2	P	MSCAN Wake-up dominant pulse pass	t_{WUP}	5			µs

A.7 SPI

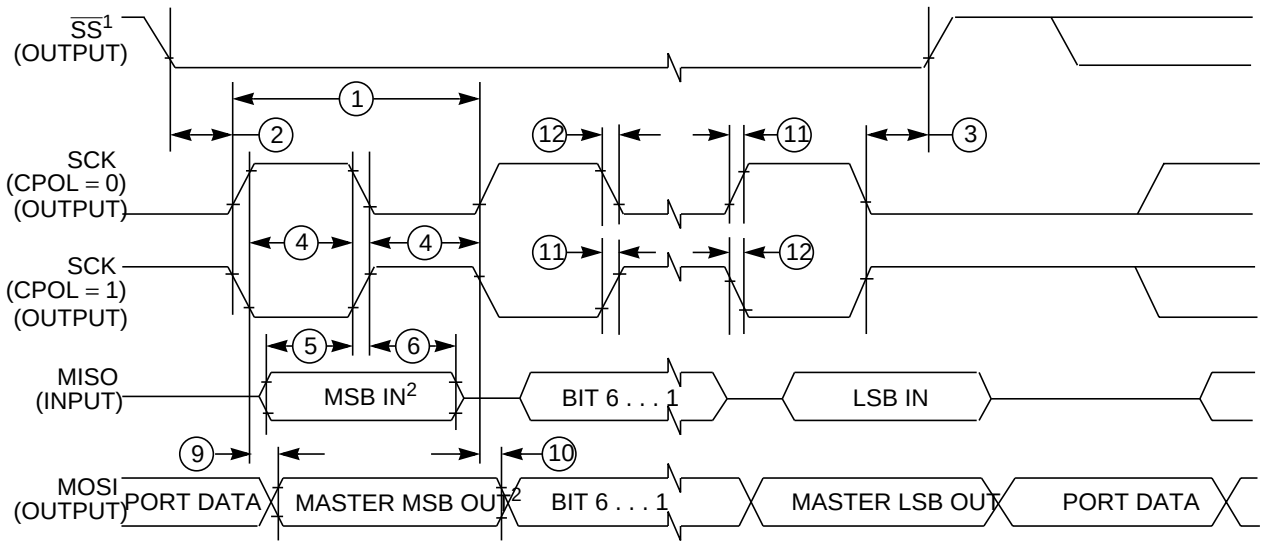
A.7.1 Master Mode

Figure A-6 and Figure A-7 illustrate the master mode timing. Timing values are shown in Table A-19.



1. If configured as output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6. SPI Master Timing (CPHA = 0)



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7. SPI Master Timing (CPHA =1)

Table A-19. SPI Master Mode Timing Characteristics[1]

Conditions are shown in Table A-4 unless otherwise noted, C_{LOAD} = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1/2		—	t_{sck}
3	D	Enable Lag Time	t_{lag}	1/2			t_{sck}
4	D	Clock (SCK) High or Low Time	t_{wsck}	t_{bus} – 30		1024 t_{bus}	ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	0			ns
9	D	Data Valid (after SCK Edge)	t_{v}			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_{r}			25	ns
12	D	Fall Time Inputs and Outputs	t_{f}			25	ns

1 The numbers 7, 8 in the column labeled “Num” are missing. This has been done on purpose to be consistent between the Master and the Slave timing shown in Table A-20.

A.7.2 Slave Mode

Figure A-8 and Figure A-9 illustrate the slave mode timing. Timing values are shown in Figure A-20.

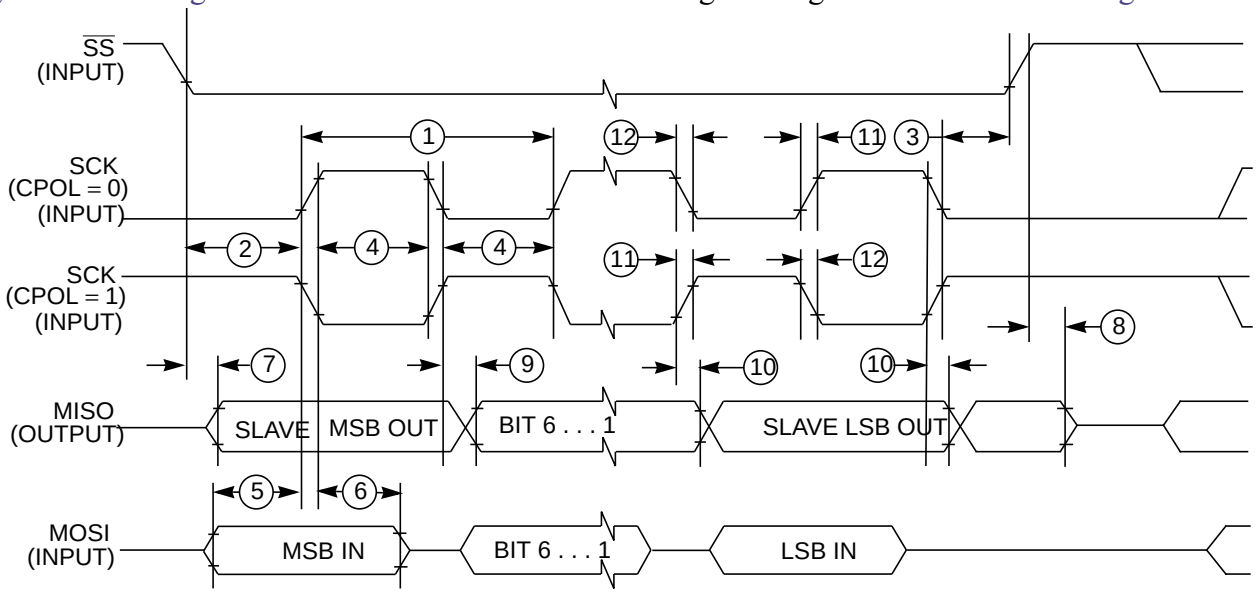


Figure A-8. SPI Slave Timing (CPHA = 0)

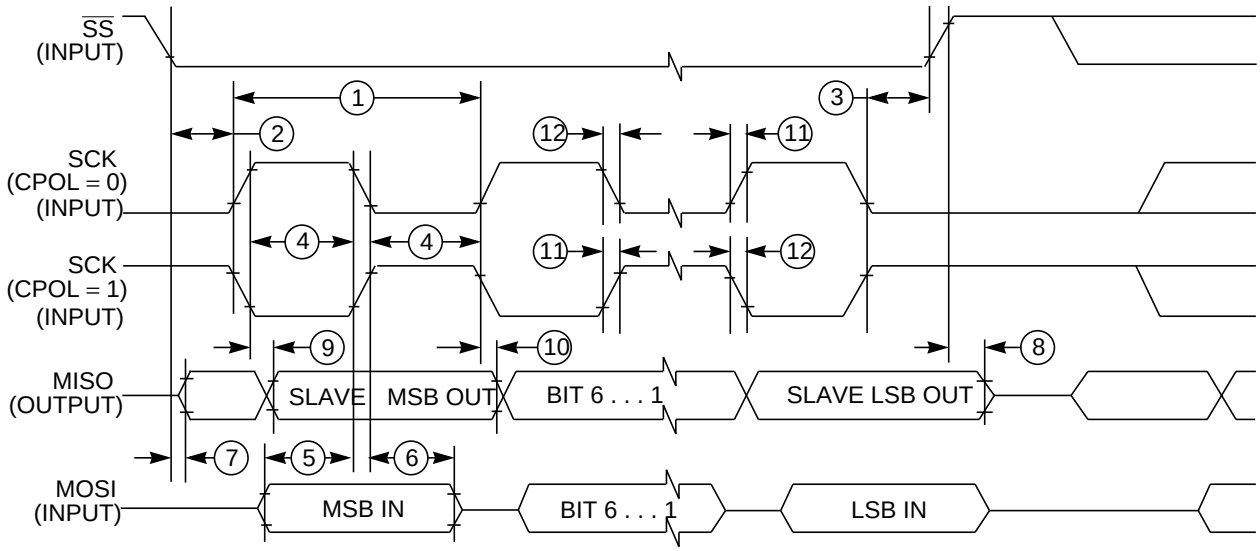


Figure A-9. SPI Slave Timing (CPHA =1)

Table A-20. SPI Slave Mode Timing Characteristics

Conditions are shown in Table A-4 unless otherwise noted, CLOAD = 200pF on all outputs							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Operating Frequency	f_{op}	DC		1/4	f_{bus}
1	P	SCK Period $t_{sck} = 1./f_{op}$	t_{sck}	4		2048	t_{bus}
2	D	Enable Lead Time	t_{lead}	1			t_{cyc}
3	D	Enable Lag Time	t_{lag}	1			t_{cyc}
4	D	Clock (SCK) High or Low Time	t_{wsck}	$t_{cyc} - 30$			ns
5	D	Data Setup Time (Inputs)	t_{su}	25			ns
6	D	Data Hold Time (Inputs)	t_{hi}	25			ns
7	D	Slave Access Time	t_a			1	t_{cyc}
8	D	Slave MISO Disable Time	t_{dis}			1	t_{cyc}
9	D	Data Valid (after SCK Edge)	t_v			25	ns
10	D	Data Hold Time (Outputs)	t_{ho}	0			ns
11	D	Rise Time Inputs and Outputs	t_r			25	ns
12	D	Fall Time Inputs and Outputs	t_f			25	ns

A.8 LCD_32F4B

Table A-21. LCD_32F4B Driver Electrical Characteristics

Characteristic	Symbol	Min.	Typ.	Max.	Unit
LCD Supply Voltage	VLCD	-0.25	-	VDDX + 0.25	V
LCD Output Impedance(BP[3:0],FP[31:0]) for outputs to charge to higher voltage level or to GND [1]	$Z_{BP/FP}$	-	-	5.0	kΩ
LCD Output Current (BP[3:0],FP[31:0]) for outputs to discharge to lower voltage level except GND [2]	$I_{BP/FP}$	50	-	-	uA

[1] Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.

[2] Outputs measured one at a time, low impedance voltage source connected to the VLCD pin.

A.9 External Bus Timing

A timing diagram of the external multiplexed-bus is illustrated in Figure A-10 with the actual timing values shown on table Table A-22. All major bus signals are included in the diagram. While both a data write and data read cycle are shown, only one or the other would occur on a particular bus cycle.

The expanded bus timings are highly dependent on the load conditions. The timing parameters shown assume a balanced load across all outputs.

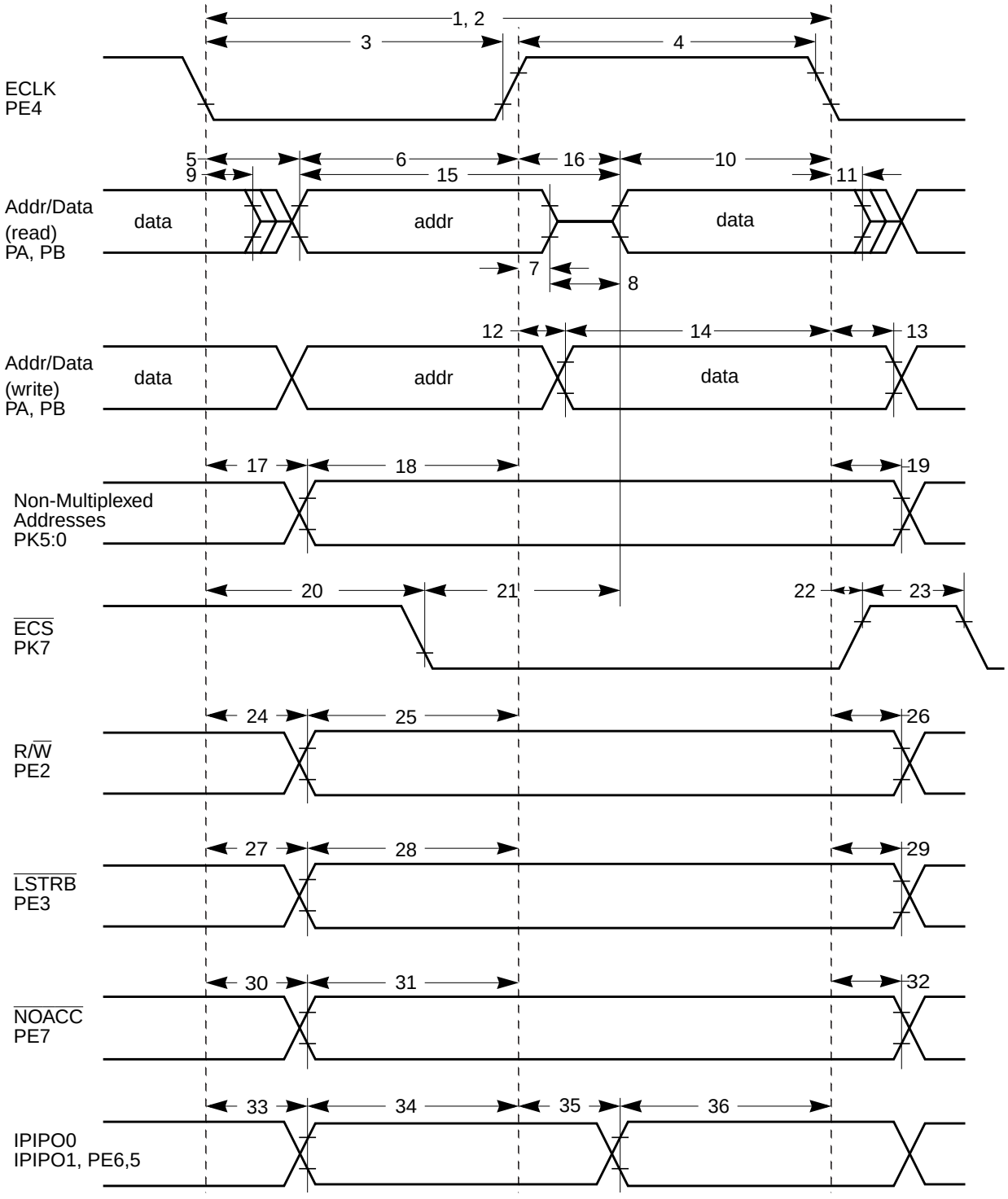


Figure A-10. General External Bus Timing

Table A-22. Expanded Bus Timing Characteristics (5V Range)

Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40˚C to +140˚C, C_{LOAD} = 50pF							
Num	**C**	**Rating**	**Symbol**	**Min**	**Typ**	**Max**	**Unit**
1	P	Frequency of operation (E-clock)	f_o	0		25.0	MHz
2	P	Cycle time	t_{cyc}	40			ns
3	D	Pulse width, E low	PW_{EL}	19			ns
4	D	Pulse width, E high[1]	PW_{EH}	19			ns
5	D	Address delay time	t_{AD}			8	ns
6	D	Address valid time to E rise (PW_{EL}–t_{AD})	t_{AV}	11			ns
7	D	Muxed address hold time	t_{MAH}	2			ns
8	D	Address hold to data valid	t_{AHDS}	7			ns
9	D	Data hold to address	t_{DHA}	2			ns
10	D	Read data setup time	t_{DSR}	13			ns
11	D	Read data hold time	t_{DHR}	0			ns
12	D	Write data delay time	t_{DDW}			7	ns
13	D	Write data hold time	t_{DHW}	2			ns
14	D	Write data setup time[1] (PW_{EH}–t_{DDW})	t_{DSW}	12			ns
15	D	Address access time[1] (t_{cyc}–t_{AD}–t_{DSR})	t_{ACCA}	19			ns
16	D	E high access time[1] (PW_{EH}–t_{DSR})	t_{ACCE}	6			ns
17	D	Non-multiplexed address delay time	t_{NAD}			6	ns
18	D	Non-muxed address valid to E rise (PW_{EL}–t_{NAD})	t_{NAV}	14			ns
19	D	Non-multiplexed address hold time	t_{NAH}	2			ns
20	D	Chip select delay time	t_{CSD}			16	ns
21	D	Chip select access time[1] (t_{cyc}–t_{CSD}–t_{DSR})	t_{ACCS}	11			ns
22	D	Chip select hold time	t_{CSH}	2			ns
23	D	Chip select negated time	t_{CSN}	8			ns
24	D	Read/write delay time	t_{RWD}			7	ns
25	D	Read/write valid time to E rise (PW_{EL}–t_{RWD})	t_{RWV}	14			ns
26	D	Read/write hold time	t_{RWH}	2			ns
27	D	Low strobe delay time	t_{LSD}			7	ns
28	D	Low strobe valid time to E rise (PW_{EL}–t_{LSD})	t_{LSV}	14			ns
29	D	Low strobe hold time	t_{LSH}	2			ns
30	D	NOACC strobe delay time	t_{NOD}			7	ns
31	D	NOACC valid time to E rise (PW_{EL}–t_{NOD})	t_{NOV}	14			ns
32	D	NOACC hold time	t_{NOH}	2			ns
33	D	IPIPO[1:0] delay time	t_{P0D}	2		7	ns
34	D	IPIPO[1:0] valid time to E rise (PW_{EL}–t_{P0D})	t_{P0V}	11			ns

Table A-22. Expanded Bus Timing Characteristics (5V Range)

Conditions are 4.75V < VDDX < 5.25V, Junction Temperature -40˚C to +140˚C, C_{LOAD} = 50pF							
35	D	IPIPO[1:0] delay time[1] (PW_{EH}-t_{P1V})	t_{P1D}	2		25	ns
36	D	IPIPO[1:0] valid time to E fall	t_{P1V}	11			ns

[1] Affected by clock stretch: add N x t_{cyc} where N=0,1,2 or 3, depending on the number of clock stretches.

Appendix B
PCB Layout Guidelines

The PCB must be carefully laid out to ensure proper operation of the voltage regulator as well as of the MCU itself. The following rules must be observed:

- Every supply pair must be decoupled by a ceramic/tantalum capacitor connected as near as possible to the corresponding pins (C1–C9).
- Central point of the ground star should be the V_{SS1} pin.
- Use low ohmic low inductance connections between V_{SS1}, V_{SS2}, V_{SSA}, $V_{SSX1,2}$ and $V_{SSM1,2,3}$.
- V_{SSPLL} must be directly connected to V_{SS1}.
- Keep traces of V_{SSPLL}, EXTAL and XTAL as short as possible and occupied board area for C10, C11, C14 and Q1 as small as possible.
- Do not place other signals or supplies underneath area occupied by C10, C11, C14 and Q1 and the connection area to the MCU.
- Central power input should be fed in at the V_{DDA}/V_{SSA} pins.

Table B-1. Recommended Components

Component	Purpose	Type	Value
C1	V_{DD1} filter cap	ceramic X7R	100 .. 220 nF
C2	V_{DDA} filter cap	X7R/tantalum	>=100 nF
C3	V_{DDX2} filter cap	X7R/tantalum	>=100 nF
C4	V_{DDR} filter cap	X7R/tantalum	>=100 nF
C5	V_{DDM3} filter cap	X7R/tantalum	>=100 nF
C6	V_{DDM2} filter cap	X7R/tantalum	>=100 nF
C7	V_{DDM1} filter cap	X7R/tantalum	>=100 nF
C8	V_{DDX1} filter cap	X7R/tantalum	>=100 nF
C9	V_{DDPLL} filter cap	ceramic X7R	100 nF .. 220 nF
C10	OSC load cap	See CRG block description chapter	
C11	OSC load cap		
C12	PLL loop filter cap		
C13	PLL loop filter cap		
C14	DC cutoff cap		
R1	PLL loop filter res		
Q1	Quartz/Resonator		

Example layouts are illustrated on Figure B-1 and Figure B-2.

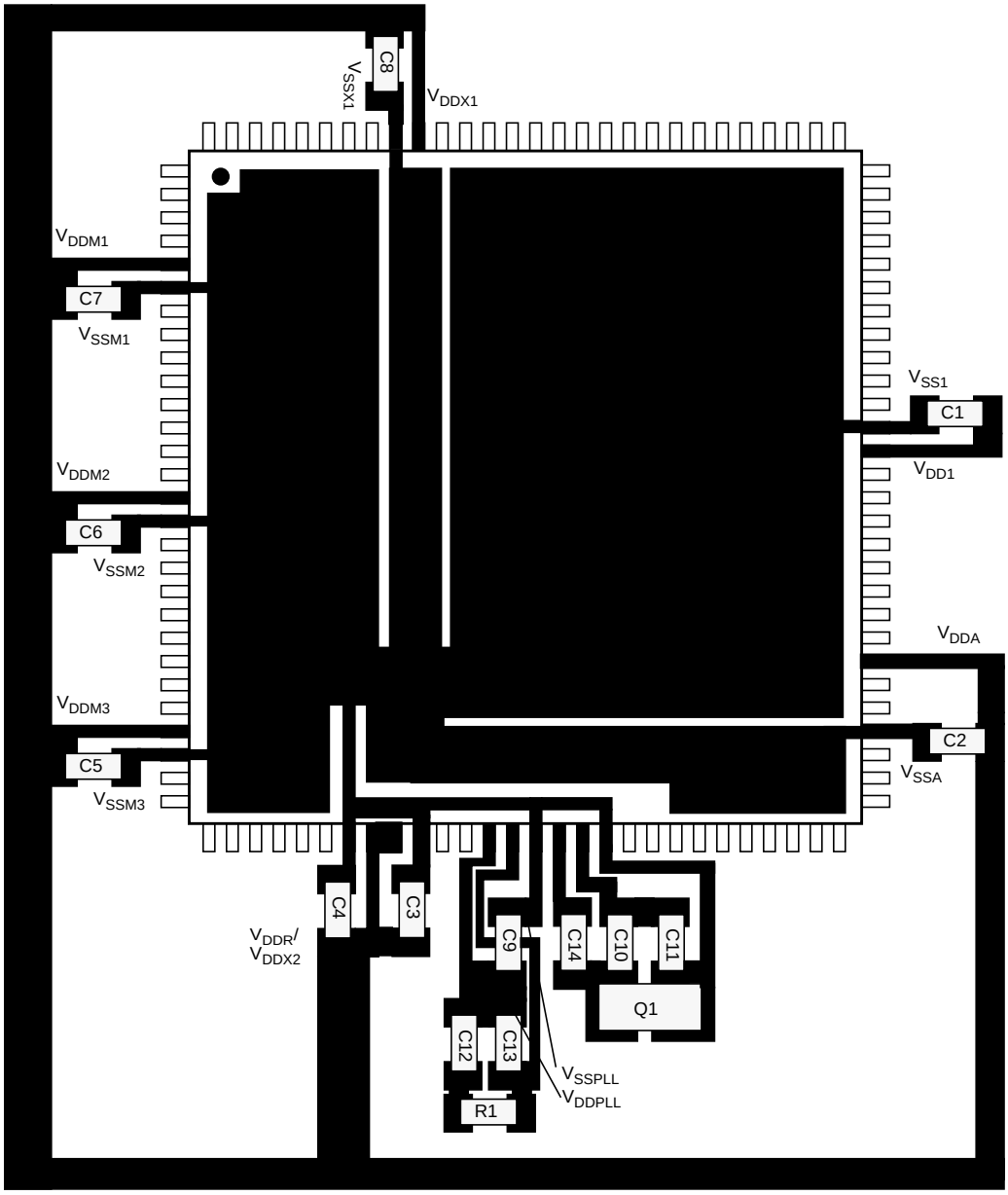


Figure B-1. Recommended PCB Layout for 112-pin LQFP

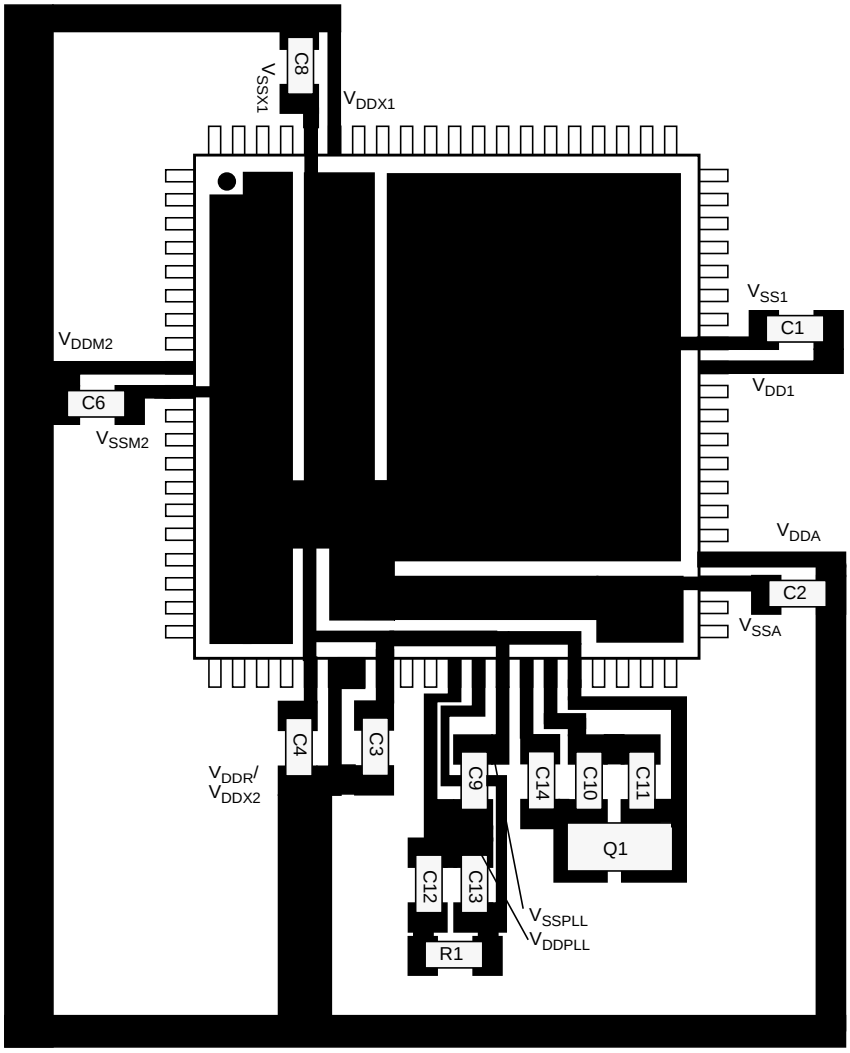
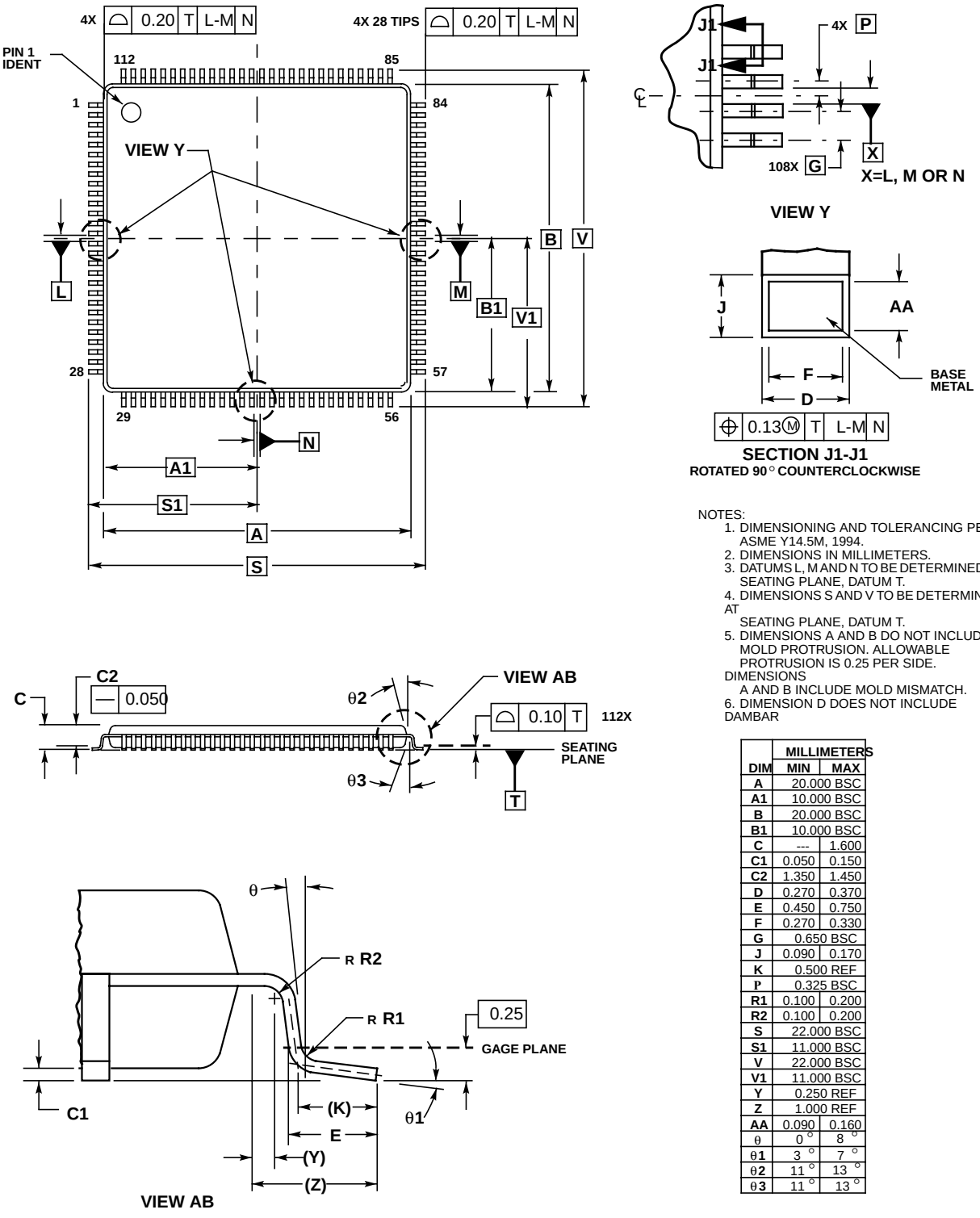


Figure B-2. Recommended PCB Layout for 80-pin QFP

Appendix C
Package Information

This section provides the physical dimensions of the MC9S12HZ256 packages.

C.1 112-Pin LQFP Package

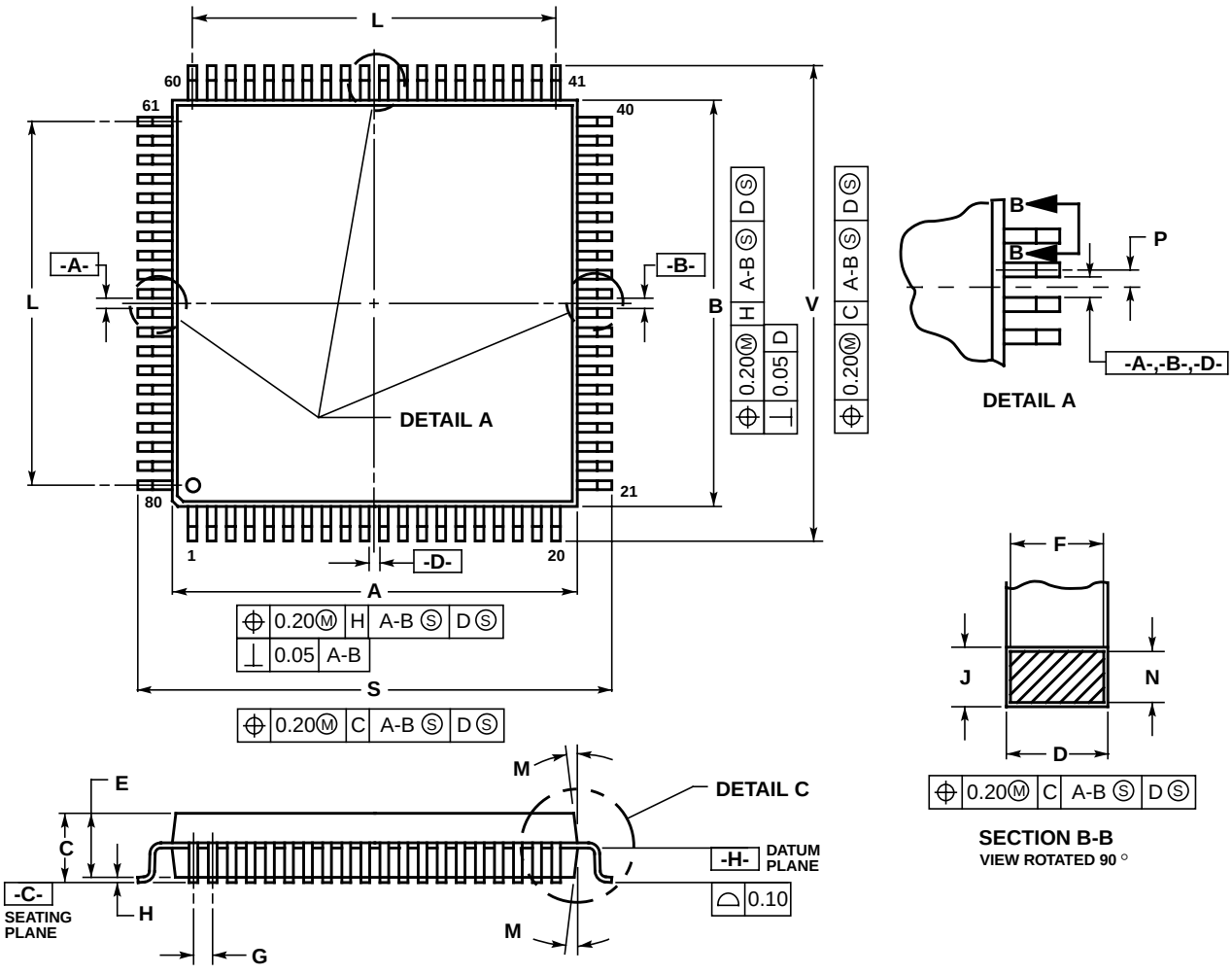


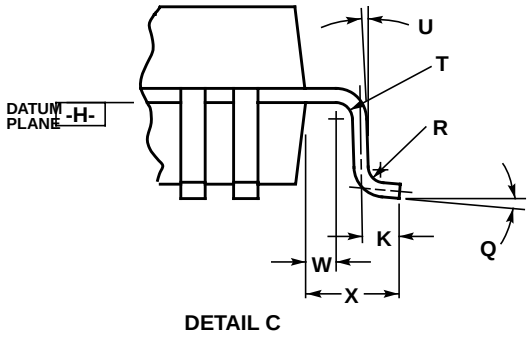
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. DATUMS L, M AND N TO BE DETERMINED AT SEATING PLANE, DATUM T.
4. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE, DATUM T.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B INCLUDE MOLD MISMATCH.
6. DIMENSION D DOES NOT INCLUDE DAMBAR

	MILLIMETERS	
DIM	MIN	MAX
A	20.000 BSC	
A1	10.000 BSC	
B	20.000 BSC	
B1	10.000 BSC	
C	---	1.600
C1	0.050	0.150
C2	1.350	1.450
D	0.270	0.370
E	0.450	0.750
F	0.270	0.330
G	0.650 BSC	
J	0.090	0.170
K	0.500 REF	
P	0.325 BSC	
R1	0.100	0.200
R2	0.100	0.200
S	22.000 BSC	
S1	11.000 BSC	
V	22.000 BSC	
V1	11.000 BSC	
Y	0.250 REF	
Z	1.000 REF	
AA	0.090	0.160
θ	0°	8°
θ1	3°	7°
θ2	11°	13°
θ3	11°	13°

Figure C-1. 112-Pin LQFP Mechanical Dimensions (case no. 987)

C.2 80-Pin QFP Package





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS	
DIM	MIN	MAX
A	13.90	14.10
B	13.90	14.10
C	2.15	2.45
D	0.22	0.38
E	2.00	2.40
F	0.22	0.33
G	0.65 BSC	
H	---	0.25
J	0.13	0.23
K	0.65	0.95
L	12.35 REF	
M	5 °	10 °
N	0.13	0.17
P	0.325 BSC	
Q	0 °	7 °
R	0.13	0.30
S	16.95	17.45
T	0.13	---
U	0 °	---
V	16.95	17.45
W	0.35	0.45
X	1.6 REF	

Figure C-2. 80-Pin QFP Mechanical Dimensions (case no. 841B)

Appendix D
Derivative Differences

Table D-1 shows the different options for the MC9S12HZ256 members.

Table D-1. Package, Memory and Peripheral Options for MC9S12HZ256 members

Device	Package	Flash	ROM	RAM	EEPROM	CAN	SCI	SPI	IIC	SSD	LCD	Motor	A/D	PWM	TIM	I/O
MC9S12HZ256	112 LQFP	256K	0	12K	2K	2	2	1	1	4	32x4	16/4	1/16	6-ch	8-ch	85
MC9S12HZ128	112 LQFP	128K	0	6K	2K	2	2	1	1	4	32x4	16/4	1/16	6-ch	8-ch	85
MC9S12HZ64	112 LQFP	64K	0	4K	1K	1	1	1	0	4	24x4	16/4	1/8	4-ch	8-ch	69
	80 QFP					1	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59
MC9S12HN64	112 LQFP	64K	0	4K	1K	0	1	1	0	4	24x4	16/4	1/8	4-ch	8-ch	69
	80 QFP					0	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59
MC3S12HZ256	112 LQFP	0	256K	12K	0	2	2	1	1	4	32x4	16/4	1/16	6-ch	8-ch	85
MC3S12HZ128	112 LQFP	0	128K	6K	0	1	2	1	1	4	32x4	16/4	1/16	6-ch	8-ch	85
MC3S12HZ64	112 LQFP	0	64K	4K	0	1	1	1	0	4	24x4	16/4	1/8	4-ch	8-ch	69
	80 QFP					1	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59
MC3S12HN64	112 LQFP	0	64K	4K	0	0	1	1	0	4	24x4	16/4	1/8	4-ch	8-ch	69
	80 QFP					0	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59
MC3S12HZ32	80 QFP	0	32K	2K	0	1	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59
MC3S12HN32	80 QFP	0	32K	2K	0	0	1	0	0	4	20x4	16/4	1/7	4-ch	4-ch	59

Appendix E
ROM Description

E.1 Memory Map and Register Definition

ROM control registers are located in the same place as the 16-byte memory space for Flash control registers 0x0100-0x010F. There are no EEPROM control registers in a ROM device and register locations 0x0110-0x011F are reserved.

Table E-1. ROM Memory Map

Address	Use	Access
0x0100	Reserved	Read
0x0101	ROM Options Register (ROPT)	Read
0x0102	Reserved	Read
0x0103	ROM Configuration Register (RCNFG)	Read/Write
0x0104-0x010B	Reserved	Read
0x010C	Device SC number byte0 (DSC0)	Read
0x010D	Device SC number byte1 (DSC1)	Read
0x010E	Device SC number byte2 (DSC2)	Read
0x010F	Reserved	Read

E.1.1 ROM Options Register (ROPT)

Upon reset the contents of the non-volatile location NVOPT are copied from ROM into ROPT. This register may be read at any time, but writes have no meaning or effect.

	7	6	5	4	3	2	1	0
R	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0
W								
Reset	R	R	R	R	R	R	R	R

= Unimplemented or Reserved

R = Read from ROM

Figure E-1. ROM Options Register (ROPT)

Table E-2. ROPT Field Descriptions

Field	Description
7:6 KEYEN[1:0]	**Backdoor Key Mechanism Enable** — Determines the state of the ROM backdoor key access. If the backdoor key mechanism is enabled, user firmware can write a 4-words value that matches the non-volatile backdoor key (NVBACKKEY through NVBACKKEY+7 in that order) to temporarily disengage security until the next reset. The backdoor key mechanism is accessible only from user (secured) firmware. BDM commands cannot be used to write key comparison values that would unlock the backdoor key. If disabled, no backdoor key access is allowed. The backdoor keywords 0x0000 and 0xFFFF are invalid and will effectively disable the backdoor key access when used. 00 Disabled 01 Disabled (preferred KEYEN state to disable backdoor key access) 10 Enabled 11 Enabled
5:2 NV[5:2]	**Non-volatile flag bits —** This bits are available to the user.
1:0 SEC[1:0]	**Security State Code —** Determines the security state of the MCU. 00 Secured 01 Secured 10 Unsecured 11 Secured

E.1.2 ROM Configuration Register (RCNFG)

	7	6	5	4	3	2	1	0
R	0	0	KEYACC	0	0	0	0	0
W								
Reset	R	R	R	R	R	R	R	R

= Unimplemented or Reserved

Figure E-2. ROM Configuration Register (RCNFG)

Table E-3. RCNFG Field Descriptions

Field	Description
5 KEYACC	**Security Access Key Write Enable** — Enables writes to the backdoor comparison key to disable security. This bit can not be set unless the KEYEN1:KEYEN0 bits are 10. This bit can not be written through BDM. 0 Backdoor key access enabled 1 Backdoor key access disabled

E.1.3 Device SC Number Registers

This register contains a copy of the Device SC number which is stored in the non-volatile registers at addresses 0xFF0C, 0xFF0D and 0xFF0E.

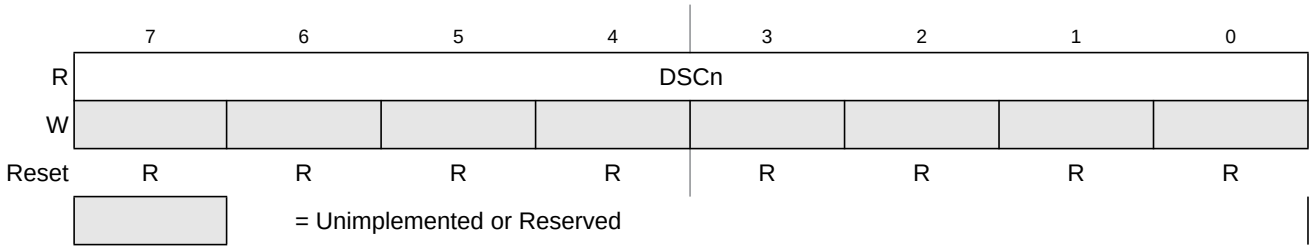


Figure E-3. Device SC Number (DSCn)

Table E-4. DSCn Field Descriptions

Field	Description
7:0 DSCn	**Device SC Number byte n (n= 0,1 or 2)** — Reads Device SC number

E.1.4 Non-volatile Registers

A range of addresses in the ROM is reserved for the security bits and backdoor key. In addition, some locations are reserved for the ROM device SC number and for the 32 bit CRC value used by the BIST control.

Table E-5. Non-volatile Register Summary

Address	Register Name	7	6	5	4	3	2	1	0
0xFF00 – 0xFF07	NVBACKKEY	8-Byte Comparison Key							
0xFF08	NVCRC0	CRC value byte0							
0xFF09	NVCRC1	CRC value byte1							
0xFF0A	NVCRC2	CRC value byte2							
0xFF0B	NVCRC3	CRC value byte3							
0xFF0C	NVSC0	Device SC number byte0							
0xFF0D	NVSC1	Device SC number byte1							
0xFF0E	NVSC2	Device SC number byte2							
0xFF0F	NVOPT	KEYEN1	KEYEN0	NV5	NV4	NV3	NV2	SEC1	SEC0

NOTE

Please note that backdoor keywords 0x0000 or 0xFFFF are invalid and will effectively disable backdoor key access when used.

E.2 ROM Security

The ROM module provides the necessary security information to the rest of the chip. After each reset, the ROM module determines the security state of the microcontroller as defined in section Section E.1.1, “ROM Options Register (ROPT)”.

If the NVM Options byte at 0xFF0F in the NVM Options Field is in secure state, any reset will cause the microcontroller to return to the secure operating mode

E.2.1 Security and Backdoor Key Access definition

Security is engaged or disengaged based on the state of two non-volatile register bits (SEC1:SEC0) in the ROPT register. During reset, the contents of the non-volatile location NVOPT are copied from ROM into the working ROPT register in high-page register space.

A user engages security by defining the security bits in the NVOPT location to select security enabled. This data is included along with the ROM program and data file which is delivered when ordering a ROM device. The SEC1=1:SEC0=0 state disengages security while the other three combinations engage security.

In a similar manner the user can choose to allow or disallow a security unlocking mechanism through an 8-byte backdoor security key. There is no way to disable security unless the non-volatile KEYEN1:KEYEN0 bits in NVOPT/ROPT are set to 1:0.

NOTE

The backdoor key is also used to protect access to internal product analysis features. No product analysis will be possible on a secured ROM if backdoor key access is disabled or keywords are invalid.

E.2.2 Unsecuring the MCU using the Backdoor Key Access

Provided that the key access is permitted, security can be disabled by the backdoor access sequence described below:

1. Writing 1 to KEYACC in the RCNFG register. This causes the ROM control logic to interpret writes to the backdoor comparison key locations (NVBACKKEY through NVBACKKEY+7) as values to be compared against the key rather than as writes to ROM locations.
2. Writing the correct four 16-bit key values to addresses NVBACKKEY through NVBACKKEY+7 locations. These writes must be done in order starting with the value for NVBACKKEY and ending with NVBACKKEY+7. User software normally would get the key codes from outside the MCU system through a communication interface such as a serial I/O.
3. Writing 0 to KEYACC in the RCNFG register. If the 8-byte key that was just written matches the key stored in the backdoor comparison key locations, SEC1:SEC0 in the ROPT register are automatically changed to 10 and security will be disengaged until the next POR.

The security key can be written only from a secure memory, so it cannot be entered through background commands without the cooperation of a secure user program.

Appendix F
Ordering Information

Figure F-1 provides an ordering example for the MC9S12HZ256.

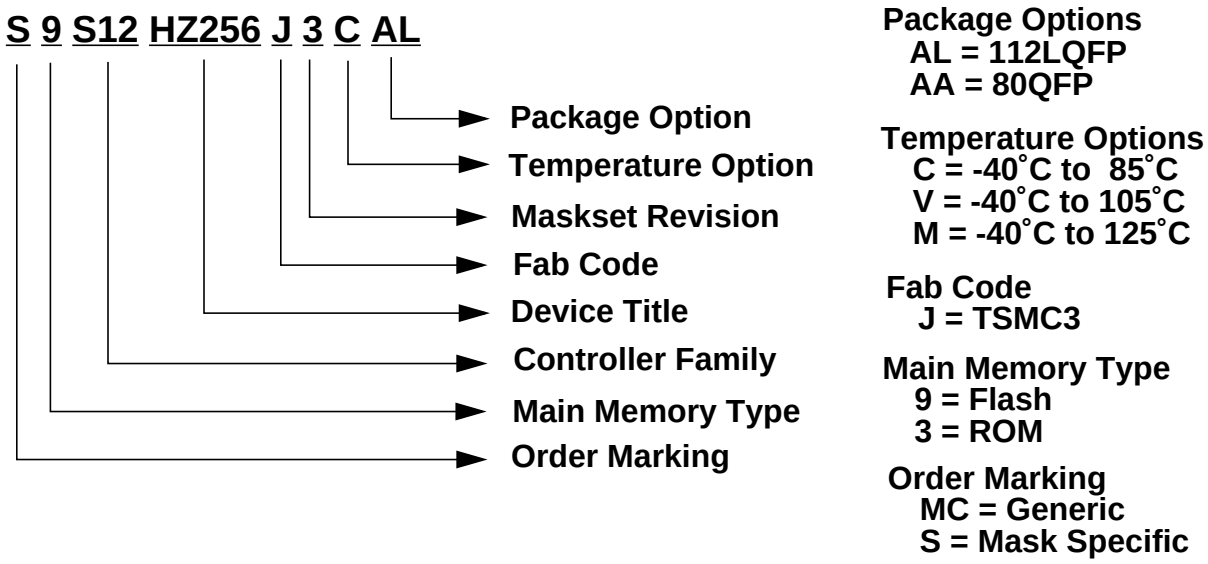


Figure F-1. Order Part Number Coding

Customers who place orders using the generic MC part numbers which are constructed using the above rules will automatically receive the preferred maskset. If the product is updated in the future and a newer maskset is put into production, then the newer maskset may automatically ship against these generic MC part numbers.

If required, a customer can specify a particular maskset when ordering product. Orders placed against a "S" part number will only receive one specific maskset. If a new maskset is made available, customers will be notified by PCN (Process Change Notification) but will have to order against a different "S" part number in order to receive the new maskset.

Appendix G
Detailed Register Map

The following tables show the detailed register map of the MC9S12HZ256.

0x0000–0x000F MEBI Map 1 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		7	6	5	4	3	2	1	0
0x0000	PORTA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0001	PORTB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0002	DDRA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0003	DDRB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0004–0x0007	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0008	PORTE	R	Bit 7	6	5	4	3	2	Bit 1	Bit 0
		W								
0x0009	DDRE	R	Bit 7	6	5	4	3	Bit 2	0	0
		W								
0x000A	PEAR	R	NOACCE	0	PIPOE	NECLK	LSTRE	RDWE	0	0
		W								
0x000B	MODE	R	MODC	MODB	MODA	0	IVIS	0	EMK	EME
		W								
0x000C	PUCR	R	PUPKE	0	0	PUPEE	0	0	PUPBE	PUPAE
		W								
0x000D	RDRIV	R	RDPK	0	0	RDPE	0	0	RDPB	RDPA
		W								
0x000E	EBICTL	R	0	0	0	0	0	0	0	ESTR
		W								
0x000F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0010–0x0014 MMC Map 1 of 4 (HCS12 Module Mapping Control)

Address	Name		7	6	5	4	3	2	1	0
0x0010	INITRM	R	RAM15	RAM14	RAM13	RAM12	RAM11	0	0	RAMHAL
		W								
0x0011	INITRG	R	0	REG14	REG13	REG12	REG11	0	0	0
		W								
0x0012	INITEE	R	EE15	EE14	EE13	EE12	EE11	0	0	EEON
		W								
0x0013	MISC	R	0	0	0	0	EXSTR1	EXSTR0	ROMHM	ROMON
		W								
0x0014	MTST0 Test Only	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0015–0x0016 INT Map 1 of 2 (HCS12 Interrupt)

Address	Name		7	6	5	4	3	2	1	0
0x0015	ITCR	R	0	0	0	WRINT	ADR3	ADR2	ADR1	ADR0
		W								
0x0016	ITEST	R	INTE	INTC	INTA	INT8	INT6	INT4	INT2	INT0
		W								

0x0017–0x0017 MMC Map 2 of 4 (HCS12 Module Mapping Control)

Address	Name		7	6	5	4	3	2	1	0
0x0017	MTST1 Test Only	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0018–0x0018 Miscellaneous Peripherals

Address	Name		7	6	5	4	3	2	1	0
0x0018	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0019–0x0019 VREG3V3 (Voltage Regulator)

Address	Name		7	6	5	4	3	2	1	0
0x0019	VREGCTRL	R	0	0	0	0	0	LVDS	LVIE	LVIF
		W								

0x001A–0x001B Miscellaneous Peripherals

Address	Name		7	6	5	4	3	2	1	0
0x001A	PARTIDH	R	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
		W								
0x001B	PARTIDL	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
		W								

0x001C–0x001D MMC Map 3 of 4 (HCS12 Module Mapping Control)

Address	Name		7	6	5	4	3	2	1	0
0x001C	MEMSIZ0	R	reg_sw0	0	eep_sw1	eep_sw0	0	ram_sw2	ram_sw1	ram_sw0
		W								
0x001D	MEMSIZ1	R	rom_sw1	rom_sw0	0	0	0	0	pag_sw1	pag_sw0
		W								

0x001E–0x001E MEBI map 2 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		7	6	5	4	3	2	1	0
0x001E	INTCR	R	IRQE	IRQEN	0	0	0	0	0	0
		W								

0x001F–0x001F INT map 2 of 2 (HCS12 Interrupt)

Address	Name		7	6	5	4	3	2	1	0
0x001F	HPRIO	R	PSEL7	PSEL6	PSEL5	PSEL4	PSEL3	PSEL2	PSEL1	0
		W								

0x0020–0x002F DBG (including BKP) map 1of 1 (HCS12 Debug)

Address	Name		7	6	5	4	3	2	1	0
0x0020	DBGC1	R	DBGEN	ARM	TRGSEL	BEGIN	DBGBRK	0	CAPMOD	
		W								
0x0021	DBGSC	R	AF	BF	CF	0	TRG			
		W								
0x0022	DBGTBH	R	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		W								
0x0023	DBGTBL	R	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		W								
0x0024	DBGCNT	R	TBF	0	CNT					
		W								
0x0025	DBGCCX	R	PAGSEL		EXTCMP					
		W								
0x0026	DBGCCH	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0027	DBGCCL	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0028	DBGC2 BKPCT0	R	BKABEN	FULL	BDM	TAGAB	BKCEN	TAGC	RWCEN	RWC
		W								
0x0029	DBGC3 BKPCT1	R	BKAMBH	BKAMBL	BKBMBH	BKBMBL	RWAEN	RWA	RWBEN	RWB
		W								
0x002A	DBGCAX BKP0X	R	PAGSEL		EXTCMP					
		W								
0x002B	DBGCAH BKP0H	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002C	DBGCAL BKP0L	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x002D	DBGCBX BKP1X	R	PAGSEL		EXTCMP					
		W								
0x002E	DBGCBH BKP1H	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x002F	DBGCBL BKP1L	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0030–0x0031 MMC map 4 of 4 (HCS12 Module Mapping Control)

Address	Name		7	6	5	4	3	2	1	0
0x0030	PPAGE	R	0	0	PIX5	PIX4	PIX3	PIX2	PIX1	PIX0
		W								
0x0031	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0032–0x0033 MEBI map 3 of 3 (HCS12 Multiplexed External Bus Interface)

Address	Name		7	6	5	4	3	2	1	0
0x0032	PORTK	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0033	DDRK	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0034–0x003F CRG (Clock and Reset Generator)

Address	Name		7	6	5	4	3	2	1	0
0x0034	SYNR	R	0	0	SYN5	SYN4	SYN3	SYN2	SYN1	SYN0
		W								
0x0035	REFDV	R	0	0	0	0	REFDV3	REFDV2	REFDV1	REFDV0
		W								
0x0036	CTFLG TEST ONLY	R	0	0	0	0	0	0	0	0
		W								
0x0037	CRGFLG	R	RTIF	PORF	LVRF	LOCKIF	LOCK	TRACK	SCMIF	SCM
		W								
0x0038	CRGINT	R	RTIE	0	0	LOCKIE	0	0	SCMIE	0
		W								
0x0039	CLKSEL	R	PLLSEL	PSTP	SYSWAI	ROAWAI	PLLWAI	CWAI	RTIWAI	COPWAI
		W								
0x003A	PLLCTL	R	CME	PLLON	AUTO	ACQ	0	PRE	PCE	SCME
		W								
0x003B	RTICTL	R	0	RTR6	RTR5	RTR4	RTR3	RTR2	RTR1	RTR0
		W								
0x003C	COPCTL	R	WCOP	RSBCK	0	0	0	CR2	CR1	CR0
		W								
0x003D	FORBYP TEST ONLY	R	0	0	0	0	0	0	0	0
		W								
0x003E	CTCTL TEST ONLY	R	0	0	0	0	0	0	0	0
		W								
0x003F	ARMCOP	R	0	0	0	0	0	0	0	0
		W	Bit 7	6	5	4	3	2	1	Bit 0

0x0040–0x006F TIM (Timer 16 Bit 8 Channels) (Sheet 1 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x0040	TIOS	R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
		W								
0x0041	CFORC	R	0	0	0	0	0	0	0	0
		W	FOC7	FOC6	FOC5	FOC4	FOC3	FOC2	FOC1	FOC0
0x0042	OC7M	R	OC7M7	OC7M6	OC7M5	OC7M4	OC7M3	OC7M2	OC7M1	OC7M0
		W								
0x0043	OC7D	R	OC7D7	OC7D6	OC7D5	OC7D4	OC7D3	OC7D2	OC7D1	OC7D0
		W								
0x0044	TCNT (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								

0x0040–0x006F TIM (Timer 16 Bit 8 Channels) (Sheet 2 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x0045	TCNT (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0046	TSCR1	R	TEN	TSWAI	TSFRZ	TFFCA	0	0	0	0
		W								
0x0047	TTOV	R	TOV7	TOV6	TOV5	TOV4	TOV3	TOV2	TOV1	TOV0
		W								
0x0048	TCTL1	R	OM7	OL7	OM6	OL6	OM5	OL5	OM4	OL4
		W								
0x0049	TCTL2	R	OM3	OL3	OM2	OL2	OM1	OL1	OM0	OL0
		W								
0x004A	TCTL3	R	EDG7B	EDG7A	EDG6B	EDG6A	EDG5B	EDG5A	EDG4B	EDG4A
		W								
0x004B	TCTL4	R	EDG3B	EDG3A	EDG2B	EDG2A	EDG1B	EDG1A	EDG0B	EDG0A
		W								
0x004C	TIE	R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
		W								
0x004D	TSCR2	R	TOI	0	0	0	TCRE	PR2	PR1	PR0
		W								
0x004E	TFLG1	R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
		W								
0x004F	TFLG2	R	TOF	0	0	0	0	0	0	0
		W								
0x0050	TC0 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0051	TC0 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0052	TC1 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0053	TC1 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0054	TC2 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0055	TC2 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0056	TC3 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0057	TC3 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0058	TC4 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x0059	TC4 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x005A	TC5 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x005B	TC5 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x0040–0x006F TIM (Timer 16 Bit 8 Channels) (Sheet 3 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x005C	TC6 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x005D	TC6 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x005E	TC7 (hi)	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x005F	TC7 (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0060	PACTL	R	0	PAEN	PAMOD	PEDGE	CLK1	CLK0	PAOVI	PAI
		W								
0x0061	PAFLG	R	0	0	0	0	0	0	PAOVF	PAIF
		W								
0x0062	PACNT (hi)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0063	PACNT (lo)	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x0064–0x006C	Reserved	R								
		W								
0x006D	TIMTST Test Only	R	0	0	0	0	0	0	TCBYP	PCBYP
		W								
0x006E–0x006F	Reserved	R								
		W								

0x0070–0x007F Reserved

Address	Name		7	6	5	4	3	2	1	0
0x0070–0x007F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0080–0x00AF ATD (Analog-to-Digital Converter 10 Bit 16 Channel) (Sheet 1 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x0080	ATDCTL0	R	0	0	0	0	WRAP3	WRAP2	WRAP1	WRAP0
		W								
0x0081	ATDCTL1	R	0	0	0	0	ETRIGCH3	ETRIGCH2	ETRIGCH1	ETRIGCH0
		W								
0x0082	ATDCTL2	R	ADPU	AFFC	AWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF
		W								
0x0083	ATDCTL3	R	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0
		W								
0x0084	ATDCTL4	R	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0
		W								
0x0085	ATDCTL5	R	DJM	DSGN	SCAN	MULT	CD	CC	CB	CA
		W								
0x0086	ATDSTAT0	R	SCF	0	ETORF	FIFOR	CC3	CC2	CC1	CC0
		W								

0x0080–0x00AF ATD (Analog-to-Digital Converter 10 Bit 16 Channel) (Sheet 2 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x0087	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0088	ATDTEST0	R	SAR9	SAR8	SAR7	SAR6	SAR5	SAR4	SAR3	SAR2
		W								
0x0089	ATDTEST1	R	SAR1	SAR0	0	0	0	RST	ATDCLK	SC
		W								
0x008A	ATDSTAT2	R	CCF15	CCF14	CCF13	CCF12	CCF11	CCF10	CCF9	CCF8
		W								
0x008B	ATDSTAT1	R	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0
		W								
0x008C	ATDDIEN0	R	Bit 15	14	13	12	11	10	9	Bit 8
		W								
0x008D	ATDDIEN1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x008E	PORTAD0	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x008F	PORTAD1	R	Bit7	6	5	4	3	2	1	BIT 0
		W								
0x0090	ATDDR0H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0091	ATDDR0L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x0092	ATDDR1H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0093	ATDDR1L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x0094	ATDDR2H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0095	ATDDR2L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x0096	ATDDR3H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0097	ATDDR3L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x0098	ATDDR4H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x0099	ATDDR4L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x009A	ATDDR5H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009B	ATDDR5L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x009C	ATDDR6H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009D	ATDDR6L	R	Bit7	6	5	4	3	2	1	Bit0
		W								

0x0080–0x00AF ATD (Analog-to-Digital Converter 10 Bit 16 Channel) (Sheet 3 of 3)

Address	Name		7	6	5	4	3	2	1	0
0x009E	ATDDR7H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x009F	ATDDR7L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00A0	ATDDR8H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A1	ATDDR8L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00A2	ATDDR9H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A3	ATDDR9L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00A4	ATDDR10H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A5	ATDDR10L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00A6	ATDDR11H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A7	ATDDR11L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00A8	ATDDR12H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00A9	ATDDR12L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00AA	ATDDR13H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AB	ATDDR13L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00AC	ATDDR14H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AD	ATDDR14L	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0X00AE	ATDDR15H	R	Bit15	14	13	12	11	10	9	Bit8
		W								
0x00AF	ATDDR15L	R	Bit7	6	5	4	3	2	1	Bit0
		W								

0x00B0–0x00BF Reserved

Address	Name		7	6	5	4	3	2	1	0
0x00B0–0x00BF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00C0–0x00C7 IIC (Inter IC Bus)

Address	Name		7	6	5	4	3	2	1	0
0x00C0	IBAD	R	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	0
		W								
0x00C1	IBFD	R	IBC7	IBC6	IBC5	IBC4	IBC3	IBC2	IBC1	IBC0
		W								
0x00C2	IBCR	R	IBEN	IBIE	MS/SL	Tx/Rx	TXAK	0	0	IBSWAI
		W						RSTA		
0x00C3	IBSR	R	TCF	IAAS	IBB	IBAL	0	SRW	IBIF	RXAK
		W								
0x00C4	IBDR	R	D7	D6	D5	D4	D3	D2	D1	D 0
		W								
0x00C5–0x00C7	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00C8–0x00CF SCI0 (Asynchronous Serial Interface)

Address	Name		7	6	5	4	3	2	1	0
0x00C8	SCI0BDH	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x00C9	SCI0BDL	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x00CA	SCI0CR1	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x00CB	SCI0CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x00CC	SCI0SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								
0x00CD	SCI0SR2	R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x00CE	SCI0DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x00CF	SCI0DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

0x00D0–0x00D7 SCI1 (Asynchronous Serial Interface)

Address	Name		7	6	5	4	3	2	1	0
0x00D0	SCI1BDH	R	IREN	TNP1	TNP0	SBR12	SBR11	SBR10	SBR9	SBR8
		W								
0x00D1	SCI1BDL	R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
		W								
0x00D2	SCI1CR1	R	LOOPS	SCISWAI	RSRC	M	WAKE	ILT	PE	PT
		W								
0x00D3	SCI1CR2	R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
		W								
0x00D4	SCI1SR1	R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
		W								

0x00D0–0x00D7 SCI1 (Asynchronous Serial Interface) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x00D5	SCI1SR2	R	0	0	0	TXPOL	RXPOL	BRK13	TXDIR	RAF
		W								
0x00D6	SCI1DRH	R	R8	T8	0	0	0	0	0	0
		W								
0x00D7	SCI1DRL	R	R7	R6	R5	R4	R3	R2	R1	R0
		W	T7	T6	T5	T4	T3	T2	T1	T0

0x00D8–0x00DF SPI (Serial Peripheral Interface)

Address	Name		7	6	5	4	3	2	1	0
0x00D8	SPICR1	R	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBFE
		W								
0x00D9	SPICR2	R	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0
		W								
0x00DA	SPIBR	R	0	SPPR2	SPPR1	SPPR0	0	SPR2	SPR1	SPR0
		W								
0x00DB	SPISR	R	SPIF	0	SPTEF	MODF	0	0	0	0
		W								
0x00DC	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x00DD	SPIDR	R	Bit7	6	5	4	3	2	1	Bit0
		W								
0x00DE–0x00DF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x00E0–0x00FF PWM (Pulse Width Modulator 8 Bit 6 Channel) (Sheet 1 of 2)

Address	Name		7	6	5	4	3	2	1	0
0x00E0	PWME	R	0	0	PWME5	PWME4	PWME3	PWME2	PWME1	PWME0
		W								
0x00E1	PWMPOL	R	0	0	PPOL5	PPOL4	PPOL3	PPOL2	PPOL1	PPOL0
		W								
0x00E2	PWMCLK	R	0	0	PCLK5	PCLK4	PCLK3	PCLK2	PCLK1	PCLK0
		W								
0x00E3	PWMPRCLK	R	0	PCKB2	PCKB1	PCKB0	0	PCKA2	PCKA1	PCKA0
		W								
0x00E4	PWMCAE	R	0	0	CAE5	CAE4	CAE3	CAE2	CAE1	CAE0
		W								
0x00E5	PWMCTL	R	0	CON45	CON23	CON01	PSWAI	PFRZ	0	0
		W								
0x00E6	PWMTST Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E7	PWMPRSC Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00E8	PWMSCLA	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								

0x00E0–0x00FF PWM (Pulse Width Modulator 8 Bit 6 Channel) (Sheet 2 of 2)

Address	Name		7	6	5	4	3	2	1	0
0x00E9	PWMSCLB	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00EA	PWMSCNTA Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00EB	PWMSCNTB Test Only	R	0	0	0	0	0	0	0	0
		W								
0x00EC	PWMCNT0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00ED	PWMCNT1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00EE	PWMCNT2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00EF	PWMCNT3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00F0	PWMCNT4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00F1	PWMCNT5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W	0	0	0	0	0	0	0	0
0x00F2	PWMPER0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F3	PWMPER1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F4	PWMPER2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F5	PWMPER3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F6	PWMPER4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F7	PWMPER5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F8	PWMDTY0	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00F9	PWMDTY1	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FA	PWMDTY2	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FB	PWMDTY3	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FC	PWMDTY4	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FD	PWMDTY5	R	Bit 7	6	5	4	3	2	1	Bit 0
		W								
0x00FE	PWMSDN	R	PWMIF	PWMIE	PWM-RSTRT	PWMLVL	0	PWM5IN	PWM5INL	PWM-5ENA
		W								
0x00FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0100–0x010F Flash Control Register (fts256k2)

Address	Name		7	6	5	4	3	2	1	0
0x0100	FCLKDIV	R	FDIVLD	PRDIV8	FDIV5	FDIV4	FDIV3	FDIV2	FDIV1	FDIV0
		W								
0x0101	FSEC	R	KEYEN		RNV5	RNV4	RNV3	RNV2	SEC	
		W								
0x0102	Reserved	R	0	0	0	WRALL	0	0	0	0
		W								
0x0103	FCNFG	R	CBEIE	CCIE	KEYACC	0	0	0	0	BKSEL
		W								
0x0104	FPROT	R	FPOPEN	RNV6	FPHDIS	FPHS		FPLDIS	FPLS	
		W								
0x0105	FSTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		W								
0x0106	FCMD	R	0	CMDB						
		W								
0x0107	FCTL	R	NV7	NV6	NV5	NV4	NV3	NV2	NV1	NV0
		W								
0x0108	FADDRHI	R	FADDRHI							
		W								
0x0109	FADDRLO	R	FADDRLO							
		W								
0x010A	FDATAHI	R	FDATAHI							
		W								
0x010B	FDATALO	R	FDATALO							
		W								
0x010C–0x010F	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0110–0x011B EEPROM Control Register (eets2k)

Address	Name		7	6	5	4	3	2	1	0
0x0110	ECLKDIV	R	EDIVLD	PRDIV8	EDIV5	EDIV4	EDIV3	EDIV2	EDIV1	EDIV0
		W								
0x0111–0x0112	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0113	ECNFG	R	CBEIE	CCIE	0	0	0	0	0	0
		W								
0x0114	EPROT	R	EPOPEN	NV6	NV5	NV4	EPDIS	EP2	EP1	EP0
		W								
0x0115	ESTAT	R	CBEIF	CCIF	PVIOL	ACCERR	0	BLANK	0	0
		W								
0x0116	ECMD	R	0	CMDB6	CMDB5	0	0	CMDB2	0	CMDB0
		W								
0x0117	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0118	EADDRHI	R	0	0	0	0	0	0	EABHI	
		W								

0x0110–0x011B EEPROM Control Register (eets2k) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0119	EADDRLO	R W	EABLO							
0x011A	EDATAHI	R W	EDHI							
0x011B	EDATALO	R W	EDLO							

0x011C–0x011F Reserved Space

Address	Name		7	6	5	4	3	2	1	0
0x011C– 0x011F	Reserved	R W	0	0	0	0	0	0	0	0

0x0120–0x0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes)

Address	Name		7	6	5	4	3	2	1	0
0x0120	LCDCR0	R W	LCDEN	0	LCLK2	LCLK1	LCLK0	BIAS	DUTY1	DUTY0
0x0121	LCDCR1	R W	0	0	0	0	0	0	LCDSWAI	LCDRPSTP
0x0122	FPENR0	R W	FPEN7	FPEN6	FPEN5	FPEN4	FPEN3	FPEN2	FPEN1	FPEN0
0x0123	FPENR1	R W	FPEN15	FPEN14	FPEN13	FPEN12	FPEN11	FPEN10	FPEN9	FPEN8
0x0124	FPENR2	R W	FPEN23	FPEN22	FPEN21	FPEN20	FPEN19	FPEN18	FPEN17	FPEN16
0x0125	FPENR3	R W	FPEN31	FPEN30	FPEN29	FPEN28	FPEN27	FPEN26	FPEN25	FPEN24
0x0126– 0x0127	Reserved	R W	0	0	0	0	0	0	0	0
0x0128	LCDRAM0	R W	FP1BP3	FP1BP2	FP1BP1	FP1BP0	FP0BP3	FP0BP2	FP0BP1	FP0BP0
0x0129	LCDRAM1	R W	FP3BP3	FP3BP2	FP3BP1	FP3BP0	FP2BP3	FP2BP2	FP2BP1	FP2BP0
0x012A	LCDRAM2	R W	FP5BP3	FP5BP2	FP5BP1	FP5BP0	FP4BP3	FP4BP2	FP4BP1	FP4BP0
0x012B	LCDRAM3	R W	FP7BP3	FP7BP2	FP7BP1	FP7BP0	FP6BP3	FP6BP2	FP6BP1	FP6BP0
0x012C	LCDRAM4	R W	FP9BP3	FP9BP2	FP9BP1	FP9BP0	FP8BP3	FP8BP2	FP8BP1	FP8BP0
0x012D	LCDRAM5	R W	FP11BP3	FP11BP2	FP11BP1	FP11BP0	FP10BP3	FP10BP2	FP10BP1	FP10BP0
0x012E	LCDRAM6	R W	FP13BP3	FP13BP2	FP13BP1	FP13BP0	FP12BP3	FP12BP2	FP12BP1	FP12BP0
0x012F	LCDRAM7	R W	FP15BP3	FP15BP2	FP15BP1	FP15BP0	FP14BP3	FP14BP2	FP14BP1	FP14BP0

0x0120–0x0137 LCD (Liquid Crystal Display 32 frontplanes, 4 backplanes) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0130	LCDRAM8	R	FP17BP3	FP17BP2	FP17BP1	FP17BP0	FP16BP3	FP16BP2	FP16BP1	FP16BP0
		W								
0x0131	LCDRAM9	R	FP19BP3	FP19BP2	FP19BP1	FP19BP0	FP18BP3	FP18BP2	FP18BP1	FP18BP0
		W								
0x0132	LCDRAM10	R	FP21BP3	FP21BP2	FP21BP1	FP21BP0	FP20BP3	FP20BP2	FP20BP1	FP20BP0
		W								
0x0133	LCDRAM11	R	FP23BP3	FP23BP2	FP23BP1	FP23BP0	FP22BP3	FP22BP2	FP22BP1	FP22BP0
		W								
0x0134	LCDRAM12	R	FP25BP3	FP25BP2	FP25BP1	FP25BP0	FP24BP3	FP24BP2	FP24BP1	FP24BP0
		W								
0x0135	LCDRAM13	R	FP27BP3	FP27BP2	FP27BP1	FP27BP0	FP26BP3	FP26BP2	FP26BP1	FP26BP0
		W								
0x0136	LCDRAM14	R	FP29BP3	FP29BP2	FP29BP1	FP29BP0	FP28BP3	FP28BP2	FP28BP1	FP28BP0
		W								
0x0137	LCDRAM15	R	FP31BP3	FP31BP2	FP31BP1	FP31BP0	FP30BP3	FP30BP2	FP30BP1	FP30BP0
		W								

0x0140–0x017F CAN0 (Scalable CAN–MSCAN)

Address	Name		7	6	5	4	3	2	1	0
0x0140	CAN0CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0141	CAN0CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		W								
0x0142	CAN0BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0143	CAN0BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0144	CAN0RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0145	CAN0RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0146	CAN0TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0147	CAN0TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0148	CAN0TARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0149	CAN0TAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								
0x014A	CAN0TBSEL	R	0	0	0	0	0	TX2	TX1	TX0
		W								
0x014B	CAN0IDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		W								
0x014C–0x014D	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0140–0x017F CAN0 (Scalable CAN–MSCAN) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x014E	CAN0RXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x014F	CAN0TXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0150–0x0153	CAN0IDAR0–CAN0IDAR3	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x0154–0x0157	CAN0IDMR0–CAN0IDMR3	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x0158–0x015B	CAN0IDAR4–CAN0IDAR7	R W	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
0x015C–0x015F	CAN0IDMR4–CAN0IDMR7	R W	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
0x0160–0x016F	CAN0RXFG	R	FOREGROUND RECEIVE BUFFER see Table 22-22							
		W								
0x0170–0x017F	CAN0TXFG	R W	FOREGROUND TRANSMIT BUFFER see Table 22-22							

Table 22-22. Detailed MSCAN Foreground Receive and Transmit Buffer Layout

Address	Name		7	6	5	4	3	2	1	0
	Extended ID	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
0x0160	Standard ID	R	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN0RIDR0	W								
	Extended ID	R	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
0x0161	Standard ID	R	ID2	ID1	ID0	RTR	IDE=0			
	CAN0RIDR1	W								
	Extended ID	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
0x0162	Standard ID	R								
	CAN0RIDR2	W								
	Extended ID	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
0x0163	Standard ID	R								
	CAN0RIDR3	W								
0x0164–0x016B	CAN0RDSR0–CAN0RDSR7	R W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x016C	CAN0RDLR	R					DLC3	DLC2	DLC1	DLC0
		W								
0x016D	Reserved	R W								
0x016E	CAN0RTSRH	R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		W								
0x016F	CAN0RTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								
0x0170	Extended ID CAN0TIDR0	R W	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
	Standard ID	R W	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3

Table 22-22. Detailed MSCAN Foreground Receive and Transmit Buffer Layout (continued)

Address	Name		7	6	5	4	3	2	1	0
0x0171	Extended ID CAN0TIDR1	R	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		W								
	Standard ID	R	ID2	ID1	ID0	RTR	IDE=0			
		W								
0x0172	Extended ID CAN0TIDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		W								
	Standard ID	R								
		W								
0x0173	Extended ID CAN0TIDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		W								
	Standard ID	R								
		W								
0x0174–0x017B	CAN0TDSR0–CAN0TDSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		W								
0x017C	CAN0TDLR	R					DLC3	DLC2	DLC1	DLC0
		W								
0x017D	CON0TTBPR	R	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		W								
0x017E	CAN0TTSRH	R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		W								
0x017F	CAN0TTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								

0x0180–0x01BF CAN1 (Freescale's Scalable CAN–MSCAN)

Address	Name		7	6	5	4	3	2	1	0
0x0180	CAN1CTL0	R	RXFRM	RXACT	CSWAI	SYNCH	TIME	WUPE	SLPRQ	INITRQ
		W								
0x0181	CAN1CTL1	R	CANE	CLKSRC	LOOPB	LISTEN	0	WUPM	SLPAK	INITAK
		W								
0x0182	CAN1BTR0	R	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
		W								
0x0183	CAN1BTR1	R	SAMP	TSEG22	TSEG21	TSEG20	TSEG13	TSEG12	TSEG11	TSEG10
		W								
0x0184	CAN1RFLG	R	WUPIF	CSCIF	RSTAT1	RSTAT0	TSTAT1	TSTAT0	OVRIF	RXF
		W								
0x0185	CAN1RIER	R	WUPIE	CSCIE	RSTATE1	RSTATE0	TSTATE1	TSTATE0	OVRIE	RXFIE
		W								
0x0186	CAN1TFLG	R	0	0	0	0	0	TXE2	TXE1	TXE0
		W								
0x0187	CAN1TIER	R	0	0	0	0	0	TXEIE2	TXEIE1	TXEIE0
		W								
0x0188	CAN1TARQ	R	0	0	0	0	0	ABTRQ2	ABTRQ1	ABTRQ0
		W								
0x0189	CAN1TAAK	R	0	0	0	0	0	ABTAK2	ABTAK1	ABTAK0
		W								

0x0180–0x01BF CAN1 (Freescale's Scalable CAN–MSCAN) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x018A	CAN1TBSEL	R	0	0	0	0	0	TX2	TX1	TX0
		W								
0x018B	CAN1IDAC	R	0	0	IDAM1	IDAM0	0	IDHIT2	IDHIT1	IDHIT0
		W								
0x018C–0x018D	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x018E	CAN1RXERR	R	RXERR7	RXERR6	RXERR5	RXERR4	RXERR3	RXERR2	RXERR1	RXERR0
		W								
0x018F	CAN1TXERR	R	TXERR7	TXERR6	TXERR5	TXERR4	TXERR3	TXERR2	TXERR1	TXERR0
		W								
0x0190–0x0193	CAN1IDAR0–CAN1IDAR3	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x0194–0x0197	CAN1IDMR0–CAN1IDMR3	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x0198–0x019B	CAN1IDAR4–CAN1IDAR7	R	AC7	AC6	AC5	AC4	AC3	AC2	AC1	AC0
		W								
0x019C–0x019F	CAN1IDMR4–CAN1IDMR7	R	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
		W								
0x01A0–0x01AF	CAN1RXFG	R	FOREGROUND RECEIVE BUFFER see Table 22-22							
		W								
0x01B0–0x01BF	CAN1TXFG	R	FOREGROUND TRANSMIT BUFFER see Table 22-22							
		W								

Table 22-23. Detailed MSCAN Foreground Receive and Transmit Buffer Layout (Sheet 1 of 2)

Address	Name		7	6	5	4	3	2	1	0
	Extended ID	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
0x01A0	Standard ID	R	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
	CAN1RIDR0	W								
	Extended ID	R	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
0x01A1	Standard ID	R	ID2	ID1	ID0	RTR	IDE=0			
	CAN1RIDR1	W								
	Extended ID	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
0x01A2	Standard ID	R								
	CAN1RIDR2	W								
	Extended ID	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
0x01A3	Standard ID	R								
	CAN1RIDR3	W								
0x01A4–	CAN1RDSR0–	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0x01AB	CAN1RDSR7	W								
0x01AC	CAN1RDLR	R					DLC3	DLC2	DLC1	DLC0
		W								
0x01AD	Reserved	R								
		W								
0x01AE	CAN1RTSRH	R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		W								

Table 22-23. Detailed MSCAN Foreground Receive and Transmit Buffer Layout (Sheet 2 of 2)

Address	Name		7	6	5	4	3	2	1	0
0x01AF	CAN1RTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								
0x01B0	Extended ID CAN1TIDR0	R	ID28	ID27	ID26	ID25	ID24	ID23	ID22	ID21
		W								
	Standard ID	R	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3
		W								
0x01B1	Extended ID CAN1TIDR1	R	ID20	ID19	ID18	SRR=1	IDE=1	ID17	ID16	ID15
		W								
	Standard ID	R	ID2	ID1	ID0	RTR	IDE=0			
		W								
0x01B2	Extended ID CAN1TIDR2	R	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7
		W								
	Standard ID	R								
		W								
0x01B3	Extended ID CAN1TIDR3	R	ID6	ID5	ID4	ID3	ID2	ID1	ID0	RTR
		W								
	Standard ID	R								
		W								
0x01B4– 0x01BB	CAN1TDSR0– CAN1TDSR7	R	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		W								
0x01BC	CAN1TDLR	R					DLC3	DLC2	DLC1	DLC0
		W								
0x01BD	CON1TTBPR	R	PRIO7	PRIO6	PRIO5	PRIO4	PRIO3	PRIO2	PRIO1	PRIO0
		W								
0x01BE	CAN1TTSRH	R	TSR15	TSR14	TSR13	TSR12	TSR11	TSR10	TSR9	TSR8
		W								
0x01BF	CAN1TTSRL	R	TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0
		W								

0x01C0–0x01FF MC (Motor Controller 10bit 8 channels)

Address	Name		7	6	5	4	3	2	1	0
0x01C0	MCCTL0	R	0	MCPRE1	MCPRE0	MCSWAI	FAST	DITH	0	MCTOIF
		W								
0x01C1	MCCTL1	R	RECIRC	0	0	0	0	0	0	MCTOIE
		W								
0x01C2	MCPER (hi)	R	0	0	0	0	0	P10	P9	P8
		W								
0x01C3	MCPER (lo)	R	P7	P6	P5	P4	P3	P2	P1	P0
		W								
0x01C4– 0x01CF	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x01D0– 0x01D7	MCCC0– MCCC7	R	OM1	OM0	AM1	AM0	0	0	CD1	CD0
		W								
0x01D8– 0x01DF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x01C0–0x01FF MC (Motor Controller 10bit 8 channels) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x01E0	MCDC0 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01E1	MCDC0 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01E2	MCDC1 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01E3	MCDC1 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01E4	MCDC2 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01E5	MCDC2 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01E6	MCDC3 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01E7	MCDC3 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01E8	MCDC4 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01E9	MCDC4 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01EA	MCDC5 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01EB	MCDC5 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01EC	MCDC6 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01ED	MCDC6 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01EE	MCDC7 (hi)	R	S	S	S	S	S	D10	D9	D8
		W								
0x01EF	MCDC7 (lo)	R	D7	D6	D5	D4	D3	D2	D1	D0
		W								
0x01F0–0x01FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0200–0x027F PIM (Port Integration Module) (Sheet 1 of 4)

Address	Name		7	6	5	4	3	2	1	0
0x0200	PTT	R	PTT7	PTT6	PTT5	PTT4	PTT3	PTT2	PTT1	PTT0
		W								
0x0201	PTIT	R	PTIT7	PTIT6	PTIT5	PTIT4	PTIT3	PTIT2	PTIT1	PTIT0
		W								
0x0202	DDRT	R	DDRT7	DDRT7	DDRT5	DDRT4	DDRT3	DDRT2	DDRT1	DDRT0
		W								
0x0203	RDRT	R	RDRT7	RDRT6	RDRT5	RDRT4	RDRT3	RDRT2	RDRT1	RDRT0
		W								

0x0200–0x027F PIM (Port Integration Module) (Sheet 2 of 4)

Address	Name		7	6	5	4	3	2	1	0
0x0204	PERT	R	PERT7	PERT6	PERT5	PERT4	PERT3	PERT2	PERT1	PERT0
		W								
0x0205	PPST	R	PPST7	PPST6	PPST5	PPST4	PPST3	PPST2	PPST1	PPST0
		W								
0x0206–0x0207	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0208	PTS	R	PTS7	PTS6	PTS5	PTS4	0	0	PTS1	PTS0
		W								
0x0209	PTIS	R	PTIS7	PTIS6	PTIS5	PTIS4	0	0	PTIS1	PTIS0
		W								
0x020A	DDRS	R	DDRS7	DDRS7	DDRS5	DDRS4	0	0	DDRS1	DDRS0
		W								
0x020B	RDRS	R	RDRS7	RDRS6	RDRS5	RDRS4	0	0	RDRS1	RDRS0
		W								
0x020C	PERS	R	PERS7	PERS6	PERS5	PERS4	0	0	PERS1	PERS0
		W								
0x020D	PPSS	R	PPSS7	PPSS6	PPSS5	PPSS4	0	0	PPSS1	PPSS0
		W								
0x020E	WOMS	R	WOMS7	WOMS6	WOMS5	WOMS4	0	0	WOMS1	WOMS0
		W								
0x020F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0210	PTM	R	0	0	PTM5	PTM4	PTM3	PTM2	0	0
		W								
0x0211	PTIM	R	0	0	PTIM5	PTIM4	PTIM3	PTIM2	0	0
		W								
0x0212	DDRM	R	0	0	DDRM5	DDRM4	DDRM3	DDRM2	0	0
		W								
0x0213	RDRM	R	0	0	RDRM5	RDRM4	RDRM3	RDRM2	0	0
		W								
0x0214	PERM	R	0	0	PERM5	PERM4	PERM3	PERM2	0	0
		W								
0x0215	PPSM	R	0	0	PPSM5	PPSM4	PPSM3	PPSM2	0	0
		W								
0x0216	WOMM	R	0	0	WOMM5	WOMM4	WOMM3	WOMM2	0	0
		W								
0x0217	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0218	PTP	R	0	0	PTP5	PTP4	PTP3	PTP2	PTP1	PTP0
		W								
0x0219	PTIP	R	0	0	PTIP5	PTIP4	PTIP3	PTIP2	PTIP1	PTIP0
		W								
0x021A	DDRP	R	0	0	DDRP5	DDRP4	DDRP3	DDRP2	DDRP1	DDRP0
		W								
0x021B	RDRP	R	0	0	RDRP5	RDRP4	RDRP3	RDRP2	RDRP1	RDRP0
		W								

0x0200–0x027F PIM (Port Integration Module) (Sheet 3 of 4)

Address	Name		7	6	5	4	3	2	1	0
0x021C	PERP	R	0	0	PERP5	PERP4	PERP3	PERP2	PERP1	PERP0
		W								
0x021D	PPSP	R	0	0	PPSP5	PPSP4	PPSP3	PPSP2	PPSP1	PPSS0
		W								
0x021E	WOMP	R	0	0	WOMP5	WOMP4	0	WOMP2	0	WOMP0
		W								
0x021F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0220–0x022F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0230	PTL	R	PTL7	PTL6	PTL5	PTL4	PTL3	PTL2	PTL1	PTL0
		W								
0x0231	PTIL	R	PTIL7	PTIL6	PTIL5	PTIL4	PTIL3	PTIL2	PTIL1	PTIL0
		W								
0x0232	DDRL	R	DDRL7	DDRL7	DDRL5	DDRL4	DDRL3	DDRL2	DDRL1	DDRL0
		W								
0x0233	RDRL	R	RDRL7	RDRL6	RDRL5	RDRL4	RDRL3	RDRL2	RDRL1	RDRL0
		W								
0x0234	PERL	R	PERL7	PERL6	PERL5	PERL4	PERL3	PERL2	PERL1	PERL0
		W								
0x0235	PPSL	R	PPSL7	PPSL6	PPSL5	PPSL4	PPSL3	PPSL2	PPSL1	PPSL0
		W								
0x0236–0x0237	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0238	PTU	R	PTU7	PTU6	PTU5	PTU4	PTU3	PTU2	PTU1	PTU0
		W								
0x0239	PTIU	R	PTIU7	PTIU6	PTIU5	PTIU4	PTIU3	PTIU2	PTIU1	PTIU0
		W								
0x023A	DDRU	R	DDRU7	DDRU7	DDRU5	DDRU4	DDRU3	DDRU2	DDRU1	DDRU0
		W								
0x023B	SRRU	R	SRRU7	SRRU6	SRRU5	SRRU4	SRRU3	SRRU2	SRRU1	SRRU0
		W								
0x023C	PERU	R	PERU7	PERU6	PERU5	PERU4	PERU3	PERU2	PERU1	PERU0
		W								
0x023D	PPSU	R	PPSU7	PPSU6	PPSU5	PPSU4	PPSU3	PPSU2	PPSU1	PPSU0
		W								
0x023E–0x023F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0240	PTV	R	PTV7	PTV6	PTV5	PTV4	PTV3	PTV2	PTV1	PTV0
		W								
0x0241	PTIV	R	PTIV7	PTIV6	PTIV5	PTIV4	PTIV3	PTIV2	PTIV1	PTIV0
		W								
0x0242	DDRV	R	DDRV7	DDRV7	DDRV5	DDRV4	DDRV3	DDRV2	DDRV1	DDRV0
		W								
0x0243	SRRV	R	SRRV7	SRRV6	SRRV5	SRRV4	SRRV3	SRRV2	SRRV1	SRRV0
		W								

0x0200–0x027F PIM (Port Integration Module) (Sheet 4 of 4)

Address	Name		7	6	5	4	3	2	1	0
0x0244	PERV	R	PERV7	PERV6	PERV5	PERV4	PERV3	PERV2	PERV1	PERV0
		W								
0x0245	PPSV	R	PPSV7	PPSV6	PPSV5	PPSV4	PPSV3	PPSV2	PPSV1	PPSV0
		W								
0x0246–0x024F	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0250	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0251	PTAD	R	PTAD7	PTAD6	PTAD5	PTAD4	PTAD3	PTAD2	PTAD1	PTAD0
		W								
0x0252	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0253	PTIAD	R	PTIAD7	PTIAD6	PTIAD5	PTIAD4	PTIAD3	PTIAD2	PTIAD1	PTIAD0
		W								
0x0254	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0255	DDRAD	R	DDRAD7	DDRAD6	DDRAD5	DDRAD4	DDRAD3	DDRAD2	DDRAD1	DDRAD0
		W								
0x0256	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0257	RDRAD	R	RDRAD7	RDRAD6	RDRAD5	RDRAD4	RDRAD3	RDRAD2	RDRAD1	RDRAD0
		W								
0x0258	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x0259	PERAD	R	PERAD7	PERAD6	PERAD5	PERAD4	PERAD3	PERAD2	PERAD1	PERAD0
		W								
0x025A	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025B	PPSAD	R	PPSAD7	PPSAD6	PPSAD5	PPSAD4	PPSAD3	PPSAD2	PPSAD1	PPSAD0
		W								
0x025C	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025D	PIEAD	R	PIEAD7	PIEAD6	PIEAD5	PIEAD4	PIEAD3	PIEAD2	PIEAD1	PIEAD0
		W								
0x025E	Reserved	R	0	0	0	0	0	0	0	0
		W								
0x025F	PIFAD	R	PIFAD7	PIFAD6	PIFAD5	PIFAD4	PIFAD3	PIFAD2	PIFAD1	PIFAD0
		W								

0x0260–0x0287 Reserved

Address	Name		7	6	5	4	3	2	1	0
0x0260–0x0287	Reserved	R	0	0	0	0	0	0	0	0
		W								

0x0288–0x028F SSD0 (Stepper Stall Detector)

Address	Name		7	6	5	4	3	2	1	0
0x0288	RTZ0CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x0289	MDC0CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x028A	SSD0CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x028B	SSD0FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x028C	MDC0CNT(hi)	R	MDCCNT[15:8]							
		W								
0x028D	MDC0CNT(lo)	R	MDCCNT[7:0]							
		W								
0x028E	ITG0ACC(hi)	R	ITGACC[15:8]							
		W								
0x028F	ITG0ACC(lo)	R	ITGACC[7:0]							
		W								

0x0290–0x0297 SSD1 (Stepper Stall Detector)

Address	Name		7	6	5	4	3	2	1	0
0x0290	RTZ1CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x0291	MDC1CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x0292	SSD1CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x0293	SSD1FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x0294	MDC1CNT(hi)	R	MDCCNT[15:8]							
		W								
0x0295	MDC1CNT(lo)	R	MDCCNT[7:0]							
		W								
0x0296	ITG1ACC(hi)	R	ITGACC[15:8]							
		W								
0x0297	ITG1ACC(lo)	R	ITGACC[7:0]							
		W								

0x0298–0x029F SSD2 (Stepper Stall Detector)

Address	Name		7	6	5	4	3	2	1	0
0x0298	RTZ2CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x0299	MDC2CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x029A	SSD2CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								

0x0298–0x029F SSD2 (Stepper Stall Detector) (continued)

Address	Name		7	6	5	4	3	2	1	0
0x029B	SSD2FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x029C	MDC2CNT(hi)	R	MDCCNT[15:8]							
		W								
0x029D	MDC2CNT(lo)	R	MDCCNT[7:0]							
		W								
0x029E	ITG2ACC(hi)	R	ITGACC[15:8]							
		W								
0x029F	ITG2ACC(lo)	R	ITGACC[7:0]							
		W								

0x02A0–0x02A7 SSD3 (Stepper Stall Detector)

Address	Name		7	6	5	4	3	2	1	0
0x02A0	RTZ3CTL	R	ITG	DCOIL	RCIR	POL	0	0	STEP	
		W								
0x02A1	MDC3CTL	R	MCZIE	MODMC	RDMCL	PRE	0	MCEN	0	AOVIE
		W					FLMC			
0x02A2	SSD3CTL	R	RTZE	SDCPU	SSDWAI	FTST	0	0	ACLKS	
		W								
0x02A3	SSD3FLG	R	MCZIF	0	0	0	0	0	0	AOVIF
		W								
0x02A4	MDC3CNT(hi)	R	MDCCNT[15:8]							
		W								
0x02A5	MDC3CNT(lo)	R	MDCCNT[7:0]							
		W								
0x02A6	ITG3ACC(hi)	R	ITGACC[15:8]							
		W								
0x02A7	ITG3ACC(lo)	R	ITGACC[7:0]							
		W								

0x02A8–0x03FF Reserved

Address	Name		7	6	5	4	3	2	1	0
0x02A8–0x03FF	Reserved	R	0	0	0	0	0	0	0	0
		W								

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