MP8799

CMOS
Very Low Power 10-Bit, Analog-to-Digital Converter with 8-Channel Mux

Micro Power Systems

FEATURES

- **10-Bit Resolution**
- **Sampling Rates from <1 kHz to 1 MHz**
- **DNL better than 1/2 LSB (typ) up to 1 MHz**
- **Very Low Power CMOS - 30 mW (typ)**
- **Power Down; Lower Consumption – 3 mW (typ)**
- **Interface to any Input Range between GND and V_{DD}**
- **8-Channel Mux**
- **No S/H Required for Analog Signals less than 100 kHz**
- **No S/H Required for CCD Signals less than 1 MHz**
- **Single Power Supply (4 to 6.5 Volts)**
- **Latch-Up Free**
- **High ESD Protection: 4000 Volts Minimum**
- **44 Pin PQFP Package Available**

BENEFITS

- **Reliable Operation**
- **Reduced Board Space (Small Package)**
- **Reduced External Parts, No Sample/Hold Needed**
- **Suitable for Battery & Power Critical Applications**
- **Designer Can Adapt Input Range & Scaling**

APPLICATIONS

- **µP/DSP Interface and Control Applications**
- **High Resolution Imaging – Scanners, Copiers, Facsimile**
- **Multiplexed Data Acquisition**
- **Radar Pulse Analysis**
- **Low Power A/D Applications**

3

GENERAL DESCRIPTION

The MP8799 is a flexible, easy to use, precision 10-bit A/D Converter with 8-Channel mux that operates over a wide range of input and sampling conditions. The MP8799 can operate with conversion operation or continuous "pipeline" operation for sampling rates up to 1 MHz. The elimination of the S/H requirements, very low power, and small package size offer the designer a low cost solution. No sample and hold is required for charge couple device applications up to 1 MHz, or multiplexed input applications when the signal source bandwidth is limited to 100 kHz. The input architecture of the MP8799 allows <u>direct interface to any analog input range</u> between AGND and AV_{DD} (0 to 2 V, 1 to 4 V, 0 to 5 V, etc.). The user simply sets $V_{REF(+)}$ and $V_{REF(-)}$ to encompass the desired input range.

Scaled reference resistor tap 1/2 R allows for customizing the transfer curve as well as providing a 1/2 span reference voltage. Digital outputs are CMOS and TTL compatible.

The Micro Power Systems' MP8799 uses a two-step flash technique. The first segment converts the 4 MSBs and consists of 15 autobalanced comparators, latches, an encoder, and buffer storage registers. The second segment converts the remaining 6 LSBs.

When the power down input is "high", the data outputs DB9 to DB0 hold the current values and $V_{REF(-)}$ is disconnected from $V_{REF1(-)}$. The power consumption during the power down mode is approximately 3mW.

Specified for operation over the commercial / industrial (–40 to +85°C) temperature range, the MP8799 is available in a Plastic quad flat pack (PQFP) package.
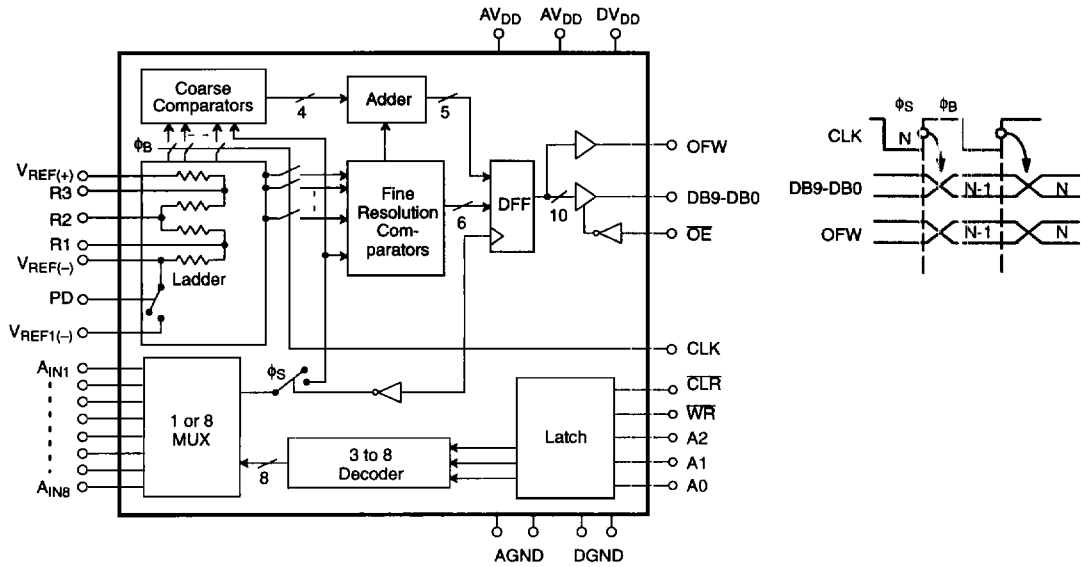
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	DNL (LSB)	INL (LSB)
PQFP	–40 to +85°C	MP8799AE	±1	±1 1/2

MP8799

SIMPLIFIED BLOCK AND TIMING DIAGRAM

PIN CONFIGURATIONS
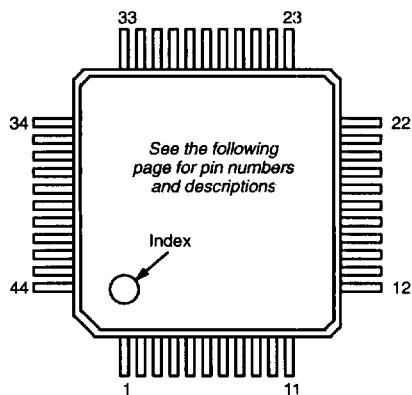
44-Pin PQFP (10 x 10)
QN44

PIN OUT DEFINITIONS

PIN NO.	NAME	DESCRIPTION	PIN NO.	NAME	DESCRIPTION
1	DB6	Data Bit 6 Output	23	R3	Reference Ladder Tap
2	DB7	Data Bit 7 Output	24	N/C	No Connect
3	DGND	Digital Ground	25	A_{IN1}	Analog Signal Input 1
4	DGND	Digital Ground	26	A_{IN2}	Analog Signal Input 2
5	DV_{DD}	Digital V_{DD}	27	A_{IN3}	Analog Signal Input 3
6	$\overline{CLR}$	Clear (Active Low)	28	A_{IN4}	Analog Signal Input 4
7	$\overline{WR}$	Write (Active Low)	29	A_{IN5}	Analog Signal Input 5
8	A2	Address 2	30	AGND	Analog Ground
9	A1	Address 1	31	AV_{DD}	Analog V_{DD}
10	A0	Address 0	32	AV_{DD}	Analog V_{DD}
11	CLK	Clock Input	33	A_{IN6}	Analog Signal Input 6
12	$\overline{OE}$	Output Enable (Active Low)	34	AGND	Analog Ground
13	N/C	No Connect	35	PD	Power Down
14	DB8	Data Bit 8 Output	36	A_{IN7}	Analog Signal Input 7
15	DB9	Data Bit 9 Output (MSB)	37	DB0	Data Bit 0 Output (LSB)
16	OFW	Overflow Output	38	DB1	Data Bit 1 Output
17	$V_{REF(+)}$	Upper Reference Voltage	39	DB2	Data Bit 2 Output
18	$V_{REF(-)}$	Lower Reference Voltage	40	DB3	Data Bit 3 Output
19	$V_{REF1(-)}$	Lower Reference Voltage	41	DB4	Data Bit 4 Output
20	R1	Reference Ladder Tap	42	DB5	Data Bit 5 Output
21	R2	Reference Ladder Tap	43	N/C	No Connect
22	A_{IN8}	Analog Signal Input 8	44	N/C	No Connect

TRUTH TABLE FOR INPUT CHANNEL SELECTION

$\overline{CLR}$	$\overline{WR}$	A2	A1	A0	Selected Analog Input
L	X	X	X	X	A_{IN1}
H	L	L	L	L	A_{IN1}
H	L	L	L	H	A_{IN2}
H	L	L	H	L	A_{IN3}
H	L	L	H	H	A_{IN4}
H	L	H	L	L	A_{IN5}
H	L	H	L	H	A_{IN6}
H	L	H	H	L	A_{IN7}
H	L	H	H	H	A_{IN8}
H	H	X	X	X	Previous Selection

Note: $\overline{CLR}$, $\overline{WR}$, A2, A1, A0 are internally connected to ground through 500kΩ resistance.

MP8799

ELECTRICAL CHARACTERISTICS TABLE

Unless Otherwise Specified: $AV_{DD} = DV_{DD} = 5$ V, $F_S = 1$ MHz (50% Duty Cycle), $V_{REF(+)} = 4.6$, $V_{REF(-)} = AGND$, $T_A = 25°C$

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
KEY FEATURES								
Resolution		10					Bits	
Sampling Rate	F_S	.001		1			MHz	For Rated Performance
ACCURACY (A Grade)[2]								
Differential Non-Linearity	DNL			±1	±1	1/4	LSB	LSB
Integral Non-Linearity	INL		±3/4	±1 1/2		±2	LSB	Best Fit Line (Max INL -- Min INL)/2
Zero Scale Error	EZS		+0.50				LSB	Reference from $V_{REF(+)}$ to $V_{REF(-)}$
Full Scale Error	EFS		−2.5				LSB	
REFERENCE VOLTAGES								
Positive Ref. Voltage	$V_{REF(+)}$			AV_{DD}			V	
Negative Ref. Voltage	$V_{REF(-)}$	AGND					V	
Differential Ref. Voltage[5]	V_{REF}	0.5		AV_{DD}			V	
Ladder Resistance	R_L	525	675	900			Ω	
Ladder Temp. Coefficient[1]	R_{TCO}		2000				ppm/°C	
Ladder Switch Resistance[1]			12				Ω	
Ladder Switch Off Leakage[1]	$I_{ILKG-SW}$		50				nA	
ANALOG INPUT[1]								
Input Bandwidth			100				kHz	
Input Voltage Range[7]	V_{IN}	$V_{REF(-)}$		$V_{REF(+)}$			V	
Input Capacitance[3]	C_{IN}		60				pF	
Aperture Delay	t_{AP}		35				ns	
DIGITAL INPUTS								
Logical "1" Voltage	V_{IH}	2.0					V	
Logical "0" Voltage	V_{IL}			0.8			V	
Leakage Currents	I_{IN}							$V_{IN}=DGND$ to DV_{DD}
CLK				±100			μA	
PD, $\overline{OE}$ (Internal Res to DGND)		−5		30			μA	
Input Capacitance			5				pF	
Clock Timing (*See Figure 1.*)[1]								
Clock Period	t_S	1000					ns	
Rise & Fall Time[4]	t_R, t_F			10			ns	
"High" Time[6]	t_B	250		500,000			ns	
"Low" Time[6]	t_S	150		500,000			ns	

ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

Parameter	Symbol	25°C Min	Typ	Max	Tmin to Tmax Min	Max	Units	Test Conditions/Comments
DIGITAL OUTPUTS								C_{OUT}=15 pF
Logical "1" Voltage	V_{OH}	DV_{DD}-0.5					V	I_{LOAD} = 2 mA
Logical "0" Voltage	V_{OL}			0.4			V	I_{LOAD} = 4 mA
Tristate Leakage	I_{OZ}	0		±5			μA	V_{OUT} = 0 to DV_{DD}
Data Hold Time (See Figure 1.)[1]	t_{HLD}		30				ns	
Data Valid Delay[1]	t_{DL}		70				ns	
Write Pulse Width[1]	t_{WR}	40					ns	
Multiplexer Address Setup Time[1]	t_{AS}	80					ns	
Multiplexer Address Hold Time[1]	t_{AS}	0					ns	
Delay from $\overline{WR}$ to Multiplexer[1] Enable	t_{MUXEN1}			80			ns	
Delay from $\overline{CLR}$ to Multiplexer[1] Enable	t_{MUXEN2}			80			ns	
Power Down Time[1]	t_{PD}			300			ns	
Power Up Time[1]	t_{PU}			200			ns	
POWER SUPPLIES[8]								
Power Down (I_{DD})	I_{PD-DD}		0.6	1.2			mA	
Operating Voltage (AV_{DD}, DV_{DD})	V_{DD}	4	5	6.5			V	
Current (AV_{DD} + DV_{DD})	I_{DD}		6	10			mA	V_{IN} = 2 V

NOTES:
1. Guaranteed. Not tested.
2. Tester measures code transition voltages by dithering the voltage of the analog input (V_{IN}). The difference between the measured code width and the ideal value (V_{REF}/1024) is the DNL error (see Figure 4.). The INL error is the maximum distance (in LSBs) from the best fit line to any transition voltage (See Figure 7.).
3. See V_{IN} input equivalent circuit (see Figure 9.).
4. Clock specification to meet aperture specification (t_{AP}). Actual rise/fall time can be less stringent with no loss of accuracy.
5. Specified values guarantee functional device. Refer to other parameters for accuracy.
6. System can clock MP8799 with any duty cycle as long as all timing conditions are met.
7. Input range where input is converted correctly into binary code. Input voltage outside specified range converts to zero or full scale output.
8. DV_{DD} and AV_{DD} are connected through the silicon substrate. Connect together at the package.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (1, 2, 3) (TA = +25°C unless otherwise noted)

V_{DD} (to GND) .... +7 V
$V_{REF(+)}$, $V_{REF(-)}$, $V_{REF1(-)}$ .... GND –0.5 to V_{DD} +0.5 V
All A_{INs} .... GND –0.5 to V_{DD} +0.5 V
All Inputs .... GND –0.5 to V_{DD} +0.5 V
All Outputs .... GND –0.5 to V_{DD} +0.5 V

Storage Temperature .... –65 to +150°C
Lead Temperature (Soldering 10 seconds) .... +300°C
Package Power Dissipation Rating to 75°C
    PQFP 450mW
    Derates above 75°C .... 14mW/°C

NOTES:
(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 100mA for less than 100μs.
(3) V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.
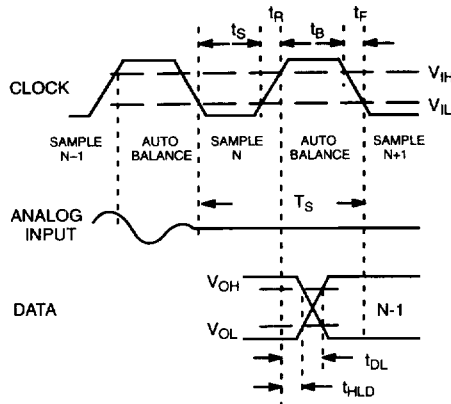
Figure 1. MP8799 Timing Diagram

THEORY OF OPERATION

Analog-to-Digital Conversion

The MP8799 converts analog voltages into 1024 digital codes by encoding the outputs of 15 coarse and 67 fine comparators. Digital logic is used to generate the overflow bit. The conversion is synchronous with the clock and it is accomplished in 2 clock periods.

The reference resistance ladder is a series of 1025 resistors. The first and the last resistor of the ladder are half the value of the others so that the following relations apply:

$$R_{REF} = 1024 * R \quad V_{REF} = V_{REF(+)} - V_{REF(-)} = 1024 * LSB$$

The clock signal generates the two internal phases, ϕ_B (CLK high) and ϕ_S (CLK low = sample) (See Figure 2.). The rising edge of the CLK input marks the end of the sampling phase (ϕ_S). Internal delay of the clock circuitry will delay the actual instant

when ϕ_S disconnects the latches from the comparators. This delay is called aperture delay (t_{AP}).

The coarse comparators make the first pass conversion and selects a ladder range for the fine comparators. The fine comparators are connected to the selected range during the next ϕ_B phase.
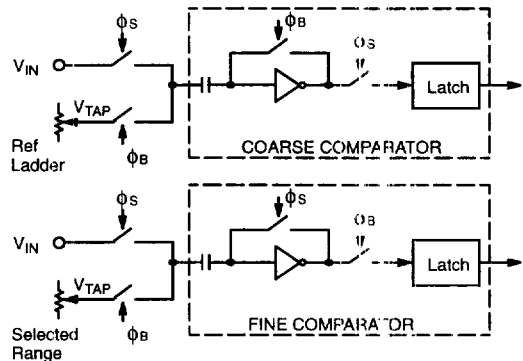
Figure 2. MP8799 Comparators

A_{IN} Sampling, Ladder Sampling, and Conversion Timing

Figure 3. shows this relationship as a timing chart. A_{IN} sampling, ladder sampling and output data relationships are shown for the general case where the levels which drive the ladder need to change for each sampled A_{IN} time point. The ladder is referenced for both last A_{IN} sample and next A_{IN} sample at the same time. If the ladder's levels change by more than 1 LSB, one of the samples must be discarded. Also note that the clock low period for the discarded A_{IN} can be reduced to the minimum t_S time of 150 ns.
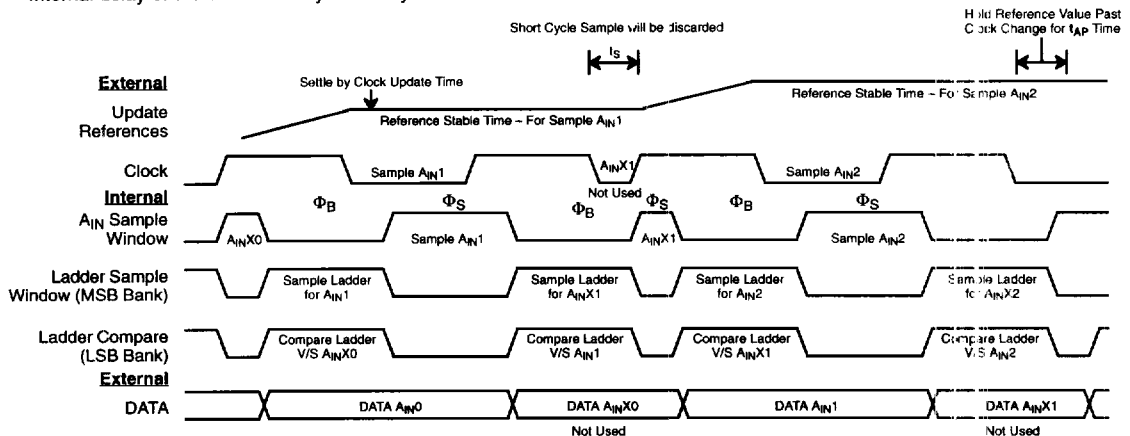
Figure 3. A_{IN} Sampling, Ladder Sampling & Conversion Timing

Accuracy of Conversion: DNL and INL

The transfer function for an ideal A/D converter is shown in *Figure 4.*
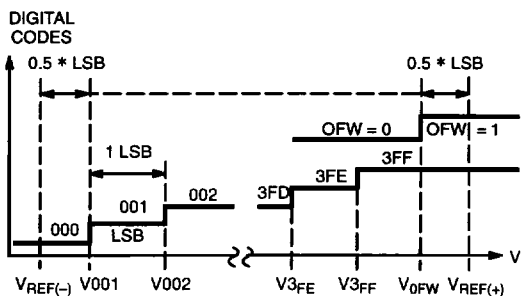
Figure 4. Ideal A/D Transfer Function

The overflow transition (V_{OFW}) takes place at:

$V_{IN} = V_{OFW} = V_{REF(+)} - 0.5 * LSB$

The first and the last transitions for the data bits take place at:

$V_{IN} = V001 = V_{REF(-)} + 0.5 * LSB$

$V_{IN} = V3_{FF} = V_{REF(-)} - 1.5 * LSB$

$LSB = V_{REF} / 1024 = (V3_{FF} - V001) / 1022$

Note that the overflow transition is a flag and has no impact on the data bits.

In a "real" converter the code-to-code transitions don't fall exactly every $V_{REF}/1024$ volts.

A positive DNL (Differential-Non-Linearity) error means that the real width of a particular code is larger than 1 LSB. This error is measured in fractions of LSB's.

A Max DNL specification guarantees that ALL code widths (DNL errors) are within the stated value. A specification of Max DNL = ± 0.5 LSB means that all code widths are within 0.5 and 1.5 LSB. If $V_{REF} = 4.608$ V then 1 LSB = 4.5 mV and every code width is within 2.25 and 6.75 mV.
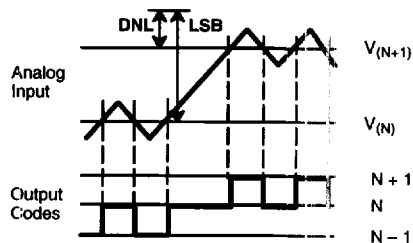
$(N+1)$ Code Width = $V_{(N+1)} - V_{(N)}$
$LSB = [V_{REF(+)} - V_{REF(-)}] / 1024$

$DNL_{(N)} = [V_{(N+1)} - V_{(N)}] - LSB$

**Figure 5. DNL Measurement
On Production Tester**

The formulas for Differential Non-linearity (DNL), Integral Non-Linearity (INL) and zero and full scale errors (E_{ZS}, E_{FS}) are:

$DNL (001) = V002 - V001 - LSB$

: : :

$DNL (3FE) = V3_{FF} - V3_{FE} - LSB$

E_{FS} (full scale error) = $V_{REF(+)} - 1.5 * LSB - V3_{FF}$

E_{ZS} (zero scale error) = $V_{REF(-)} + 0.5 * LSB - V001$
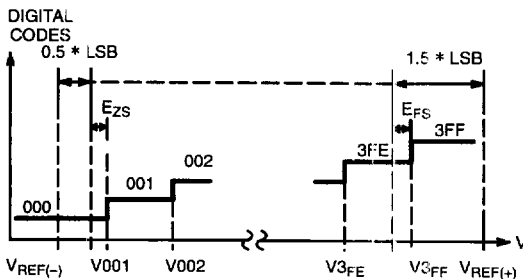
Figure 6. Real A/D Transfer Curve

Figure 8. shows the zero scale and full scale error terms.

Figure 7. gives a visual definition of the INL error. The chart shows a 3 bit converter transfer curve with greatly exaggerated DNL errors to show the deviation of the real transfer curve from the ideal one.

After a tester has measured all the transition voltages, the computer draws a line parallel to the ideal transfer line. By definition the Best Fit Line makes equal the positive and the negative INL errors. For example, an INL error of –1 to +2 LSB's relative to the Ideal Line would be ±1.5 LSB's relative to the Best Fit Line.
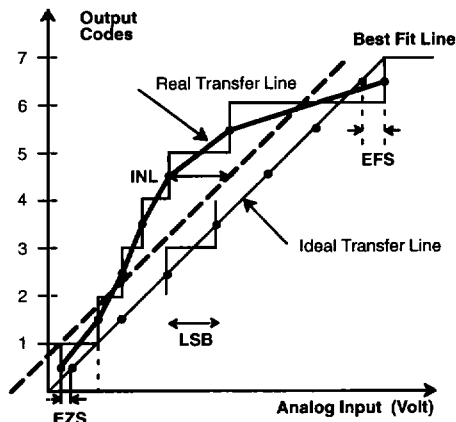
**Figure 7. INL Error Calculation
(Exaggerated for Visualization)**

Clock and Conversion Timing

A system will clock the MP8799 continuously or it will give clock pulses intermittently when a conversion is desired. The timing of *Figure 8a* shows normal operation, while the timing of

Figure 8b keeps the MP8799 in balance and ready to sample the analog input.

a. Continuous sampling

b. Single sampling
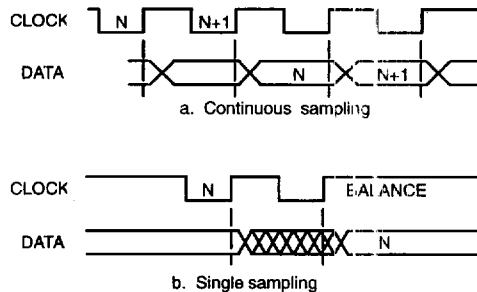
Figure 8. Relationship of Data to Clock

Analog Input

The MP8799 has very flexible input range characteristics. The user may set $V_{REF(+)}$ and $V_{REF(-)}$ to two fixed voltages and then varies the input DC and AC levels to match the V_{REF} range. However, a more common use of this flexibility is to first design the analog circuitry and then to adjust the reference voltages to include the analog input range. One advantage is that this approach may eliminate the need for external gain and offset adjust circuitry which may be required by fixed input range A/Ds. It is good design practice to proceed with these steps:

1) Estimate V_{REF} range.
2) Design analog circuitry.
3) Prototype analog circuitry and debug with ADC clocked.
4) Adjust V_{REF} range.

Good driving capabilities (low resistance, high current) of circuitry driving the flash analog input are guaranteed to optimize the MP8799 performance. *Figure 9.* shows the equivalent circuit for A_{IN}.
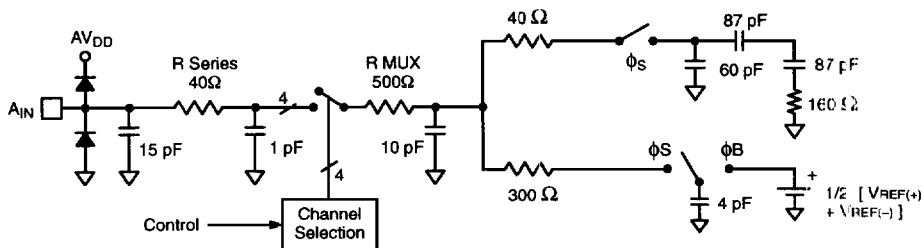
Figure 9. Analog Input Equivalent Circuit

Analog Input Multiplexer

The MP8799 includes a 8-Channel analog input multiplexer. The relationship between the clock, the multiplexer address, the $\overline{WR}$ and the output data is shown in *Figure 10*.
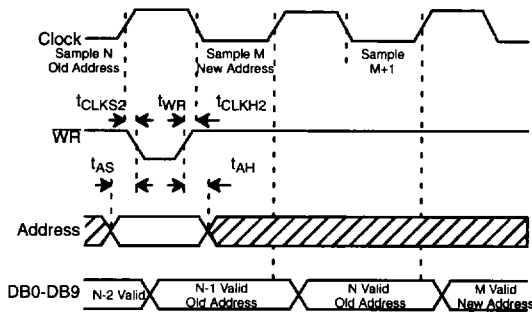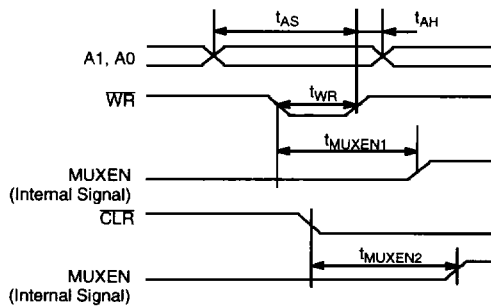

Figure 10. MUX Address Timing

Figure 11. Analog MUX Timing

Reference Voltages

The input/output relationship is a function of V_{REF}:

$$A_{IN} = V_{IN} - V_{REF(-)}$$
$$V_{REF} = V_{REF(+)} - V_{REF(-)}$$
$$DATA = 1023 * (A_{IN}/V_{REF})$$

A system can increase total gain by reducing V_{REF}

Digital Interfaces

The logic encodes the outputs of the comparators into a binary code and latches the data in a D-type flip-flop for output.

The functional equivalent of the MP8799 (*Figure 12*.) is composed of:

1) Delay stage (t_{AP}) from the clock to the sampling phase (ϕ_S).
2) An ideal analog switch which samples V_{IN}.
3) An ideal A/D which tracks and converts VIN with no delay.
4) A series of two DFF's with specified hold (t_{HLD}) and delay (t_{DL}) times.

t_{AP}, t_{HLD} and t_{DL} are specified in the Electrical Characteristics table.
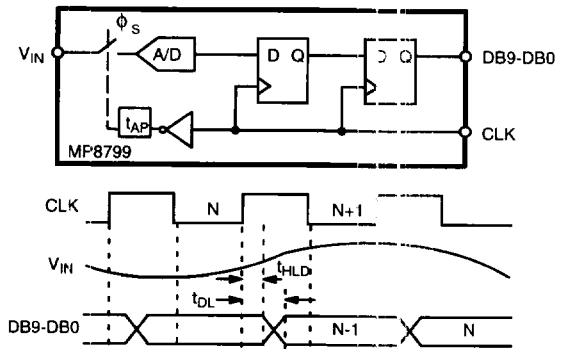
Figure 12. MP8799 Functional Equivalent Circuit and Interface Timing

MP8799

Power Down

Figure 13. shows the relationship between the clock, sampled A_{IN} to output data relationship and the effect of power down.
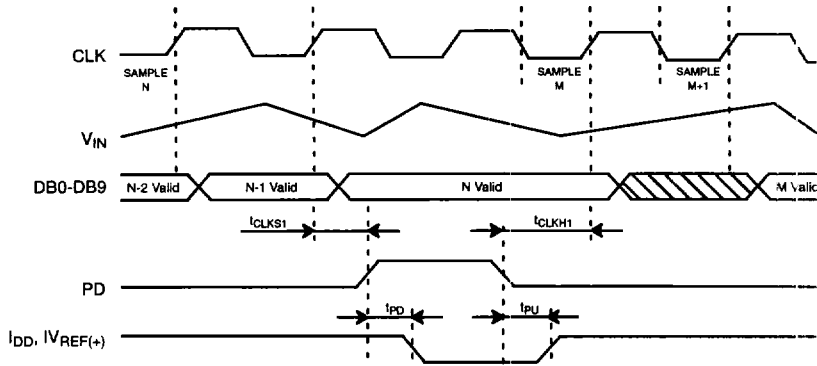
Figure 13. Power Down Timing Diagram

APPLICATION NOTES

C_1 = 4.7 or 10µF Tantalum
C_2 = 0.1µF Chip Cap or low inductance cap
L_1 = 100nH or larger
R_T = Clock Transmission Line Termination
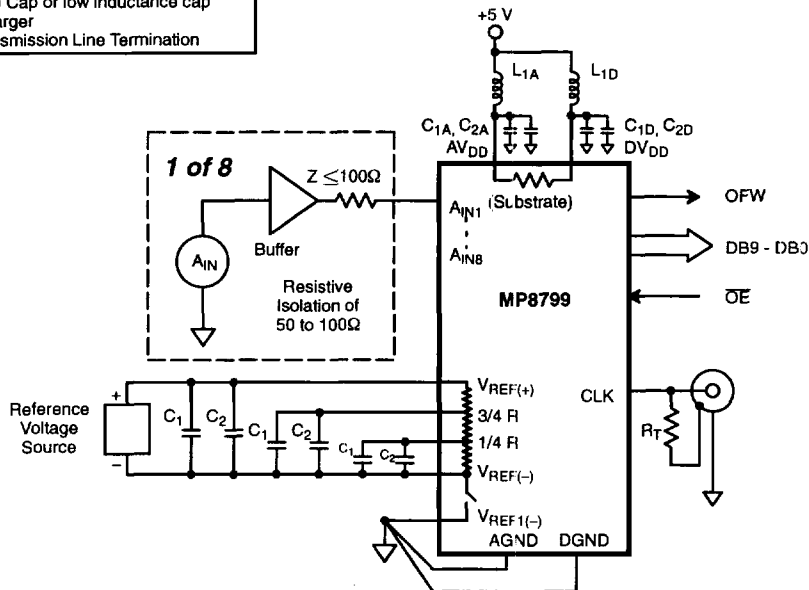
Figure 14. Typical Circuit Connections

The following information will be useful in maximizing the performance of the MP8799.

1. All signals should not exceed AV_{DD} +0.5 V or AGND –0.5 V or DV_{DD} +0.5 V or DGND –0.5 V.

2. Any input pin which can see a value outside the absolute maximum ratings (AV_{DD} or DV_{DD}+0.5 V or AGND –0.5 V) should be protected by diode clamps (HP5082-2835) from input pin to the supplies. All MP7684A inputs have input protection diodes which will protect the device from short transients outside the supply ranges.

3. The design of a PC board will affect the accuracy of MP8799. Use of wire wrap is not recommended.

4. The analog input signal (V_{IN}) is quite sensitive and should be properly routed and terminated. It should be shielded from the clock and digital outputs so as to minimize cross coupling and noise pickup.

5. The analog input should be driven by a low impedance (less than 50Ω).

6. Analog and digital ground planes should be substantial and common at one point only. The ground plane should act as a shield for parasitics and not a return path for signals. To reduce noise levels, use separate low impedance ground paths. *DGND should not be shared with other digital circuitry.* If separate low impedance paths cannot be provided, DGND should be connected to AGND next to the MP8799.

7. *DV$_{DD}$ should not be shared with other digital circuitry* to avoid conversion errors caused by digital supply transients. DV_{DD} for the MP8799 should be connected to AV_{DD} next to the MP8799.

8. DV_{DD} and AV_{DD} are connected inside the MP8799 through the N – doped silicon substrate. Any DC voltage difference between DV_{DD} and AV_{DD} will cause undesirable internal currents.

9. Each power supply and reference voltage pin should be decoupled with a ceramic (0.1µF) and a tantalum (10µF) capacitor as close to the device as possible.

10. The digital output should not drive long wires. The capacitive coupling and reflection will contribute noise to the conversion. When driving distant loads, buffers should be used. 100Ω resistors in series with the digital outputs in some applications reduces the digital output disruption of A_{IN}.
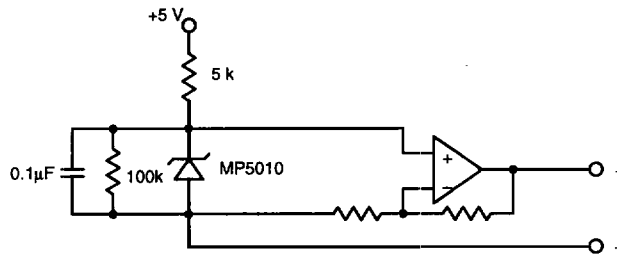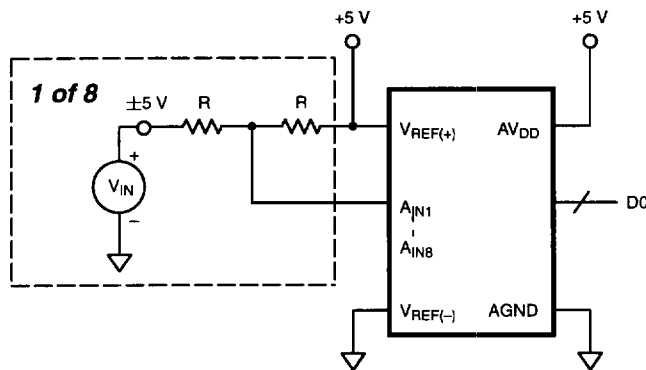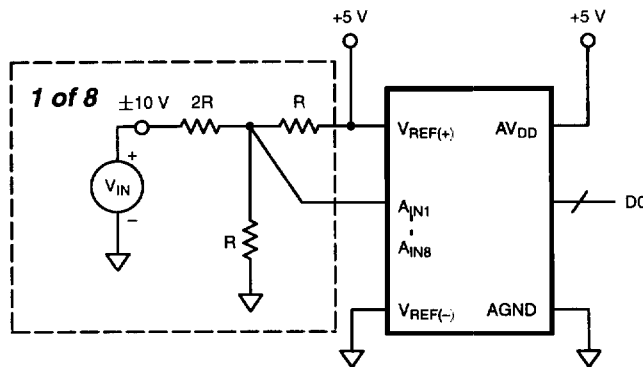
Figure 15. Example of a Reference Voltage Source

For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for differe it applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.
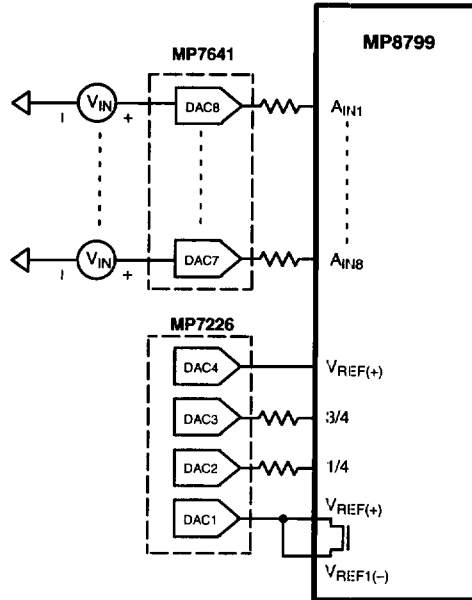
Figure 16. ±5 V Analog Input

For R = 5k use Beckman Instruments #694-3-R10k resistor array or equivalent.

NOTE: High R values affect the input BW of ADC due to the (R * C_{IN} of ADC) time constant. Therefore, for different applications the R value needs to be selected as a tradeoff between A_{IN} settling time and power dissipation.

Figure 17. ±10 V Analog Input

@ Power Down write values to DAC 3, 2, 1 = DAC 4 to minimize power consumption.
Only A_{IN} and Ladder detail shown.

Figure 18. A/D Ladder and A_{IN} with Programmed Control
(of $V_{REF(+)}$, $V_{REF(-)}$, 1/4 and 3/4 TAP.)
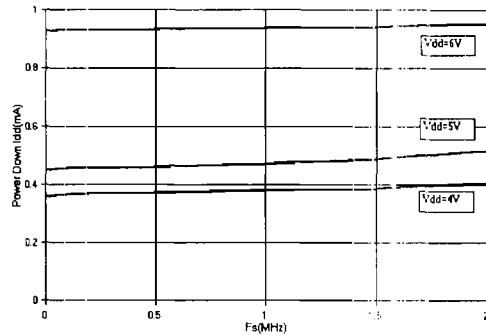
MP8799

PERFORMANCE CHARACTERISTICS
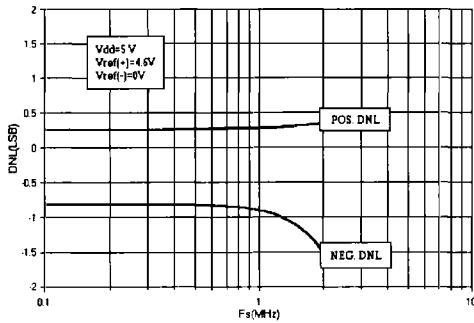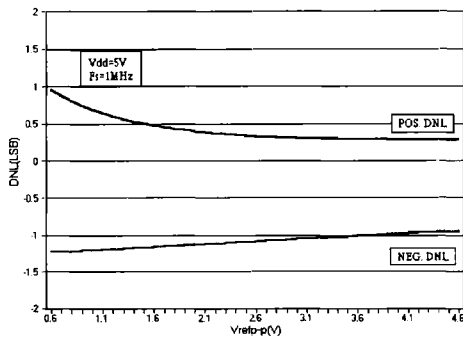
Graph 1. DNL vs. Sampling Frequency
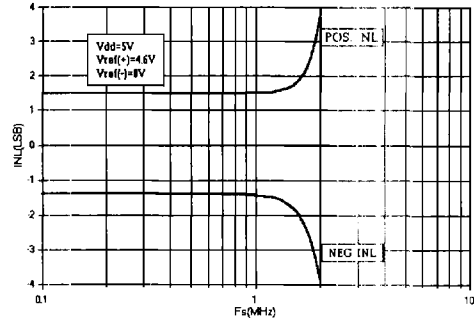
Graph 2. INL vs. Sampling Frequency
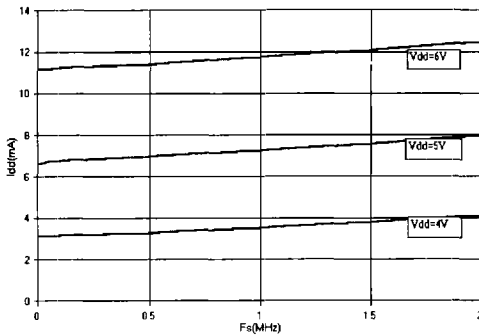
Graph 3. Supply Current vs. Sampling Frequency
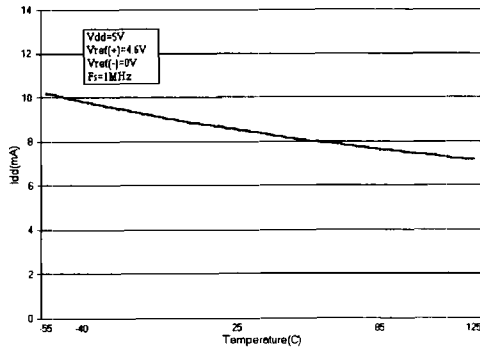
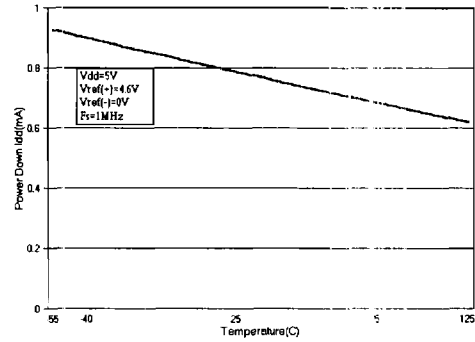**Graph 4. Power Down Current vs. Sampling Frequency**

Graph 5. DNL vs. Reference Voltage
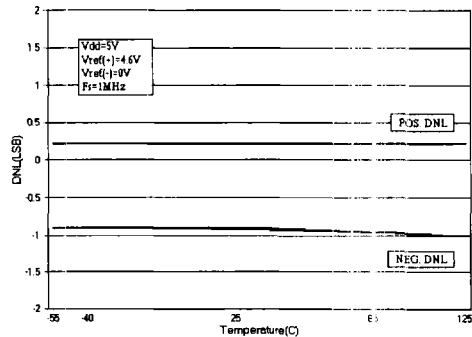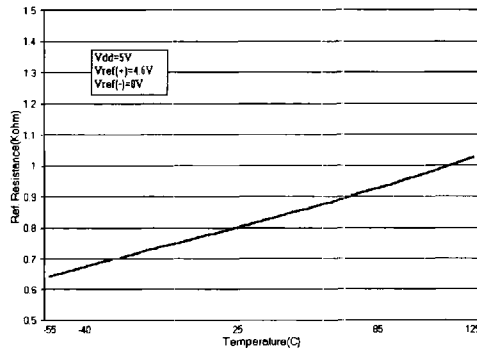
Graph 6. DNL vs. Temperature

Graph 7. Supply Current vs.
Temperature

Graph 8. Power Down Current vs.
Temperature

3

Graph 9. Reference Resistance vs.
Temperature