LH53V4P00

CMOS 4M (512K × 8/256K × 16) MROM

FEATURES

- 524,288 × 8 bit organization
  (Byte mode: $\overline{BYTE}$ = V_{IL})
  262,144 × 16 bit organization
  (Word mode: $\overline{BYTE}$ = V_{IH})
- Access time: 120 ns (MAX.)
- Supply current:
  - Operating: 35 mA (MAX.)
  - Standby: 30 µA (MAX.)
- Three-state output
- Power supply: 2.7 V to 3.6 V
- Static operation
- Package:
  40-pin, 525-mil SOP
- Others:
  - Non programmable
  - Not designed or rated as radiation hardened
  - CMOS process (P type silicon substrate)

DESCRIPTION

The LH53V4P00 is a 4M-bit CMOS mask ROM (mask-programmable-read-only memory) organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

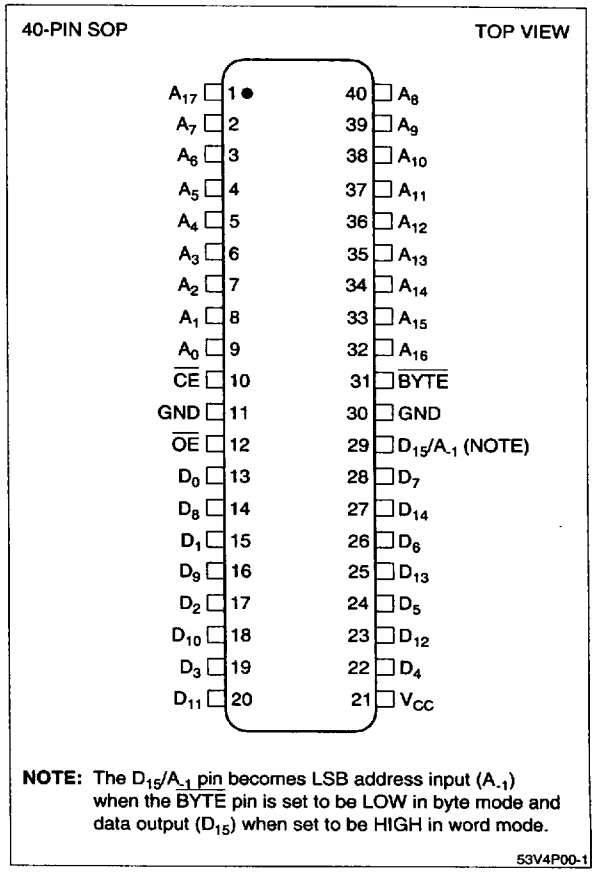


Figure 1. Pin Connections

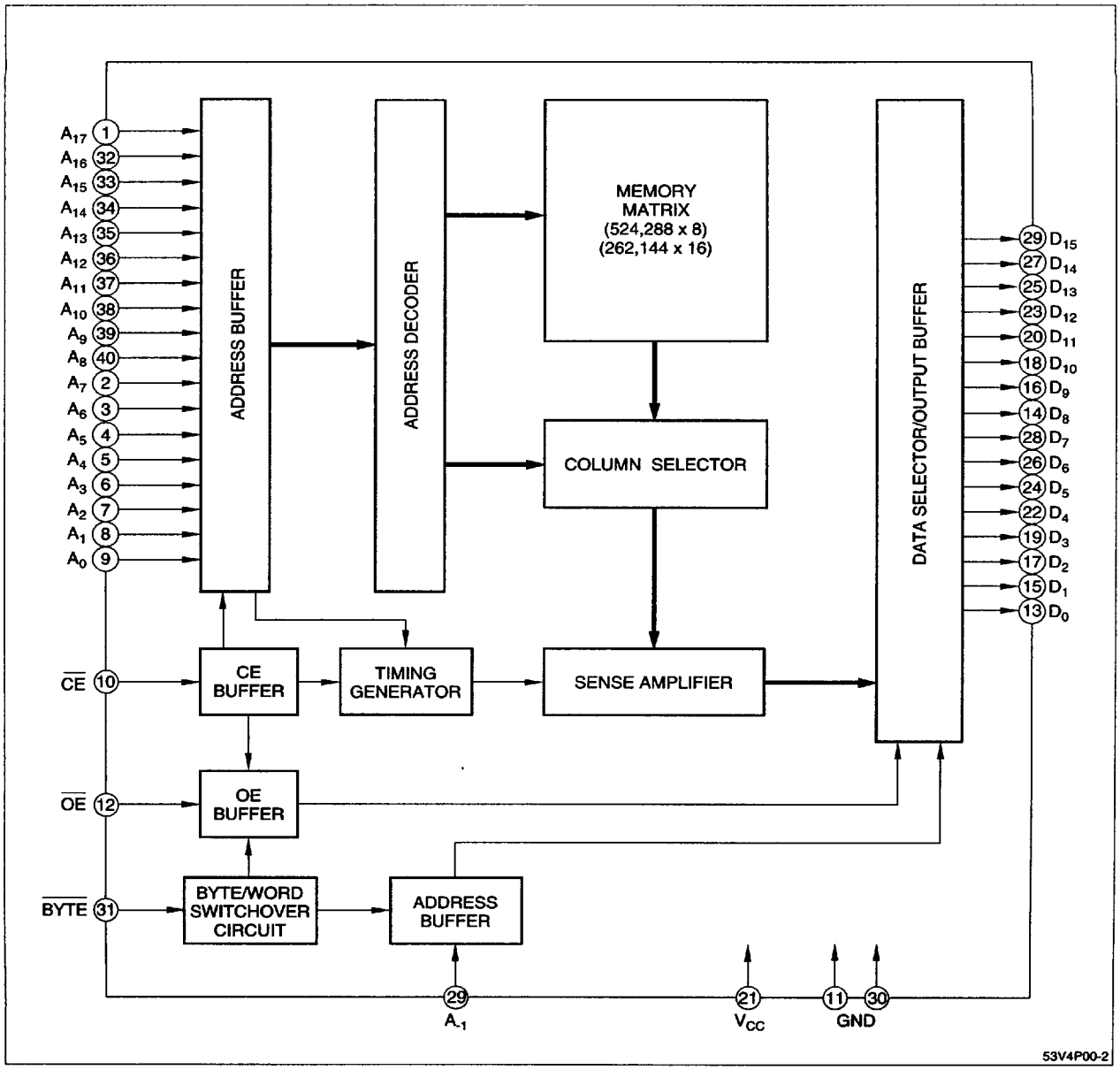


Figure 2. LH53V4P00 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{17}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	×8-bit/×16-bit (byte/word) mode select input

SIGNAL	PIN NAME
$\overline{CE}$	Chip enable input
$\overline{OE}$	Output enable input
V_{CC}	Power pin
GND	Ground

NOTE:

1. The D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the $\overline{BYTE}$ pin is set to be low in byte mode and data output (D_{15}) when set to be high in word mode.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	DATA OUTPUT		ADDRESS INPUT		SUPPLY CURRENT
			D_0 - D_7	D_8 - D_{15}	LSB	MSB	
H	X	X	High-Z	High-Z	—	—	Standby
L	H	X	High-Z	High-Z	—	—	Operating
L	L	H	D_0 - D_7	D_8 - D_{15}	A_0	A_{17}	Operating
L	L	L	D_0 - D_7	High-Z	A_{-1}	A_{17}	Operating

NOTE:
X = Don't care; High-Z = High-impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +4.6	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	T_{OPR}	-20 to +70	°C
Storage temperature	T_{STG}	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = -20 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	—	3.6	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V - 3.6 V, T_A = -20 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input 'High' voltage	V_{IH}	—	0.7 × V_{CC}	V_{CC} + 0.3	V	—
Input 'Low' voltage	V_{IL}	—	-0.3	0.2 × V_{CC}	V	—
Output 'High' voltage	V_{OH}	I_{OH} = -100 µA	V_{CC} - 0.4	—	V	—
Output 'Low' voltage	V_{OL}	I_{OL} = 400 µA	—	0.4	V	—
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}	—	5	µA	—
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}	—	5	µA	1
Operating current	I_{CC1}	t_{RC} = 120 ns	—	35	mA	2
	I_{CC2}	t_{RC} = 1 µs	—	25	mA	2
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}	—	1	mA	—
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V	—	30	µA	—
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C	—	10	pF	—
Output capacitance	C_{OUT}		—	10	pF	—

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH}, output is open
2. V_{IN} = V_{IH}, V_{IL}, $\overline{CE}$ = V_{IL}, output is open

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.7 V - 3.6 V, T_A = -20 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120	—	ns	—
Address access time	t_{AA}	—	120	ns	—
Chip enable access time	t_{ACE}	—	120	ns	—
Output enable delay time	t_{OE}	—	60	ns	—
Output hold time	t_{OH}	0	—	ns	—
Output floating time	t_{CHZ}	—	60	ns	1
	t_{OHZ}	—	60	ns	

NOTE:
1. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	$0.2 \times V_{CC}$ - $0.7 \times V_{CC}$
Input signal rise time	10 ns
Input signal fall time	10 ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load condition	1TTL + 100 pF

NOTE:
It is recommended that a decoupling capacitor be connected beween V_{CC} and GND pin.

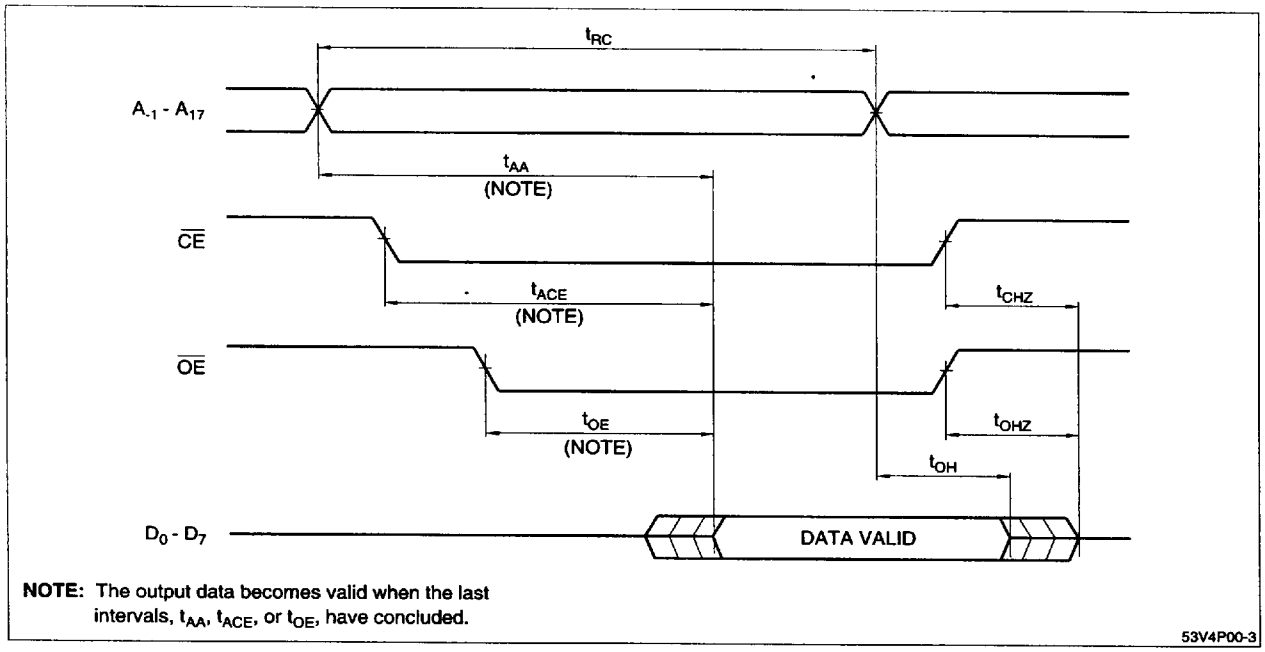


Figure 3. Byte Mode ($\overline{BYTE}$ = V_{IL})

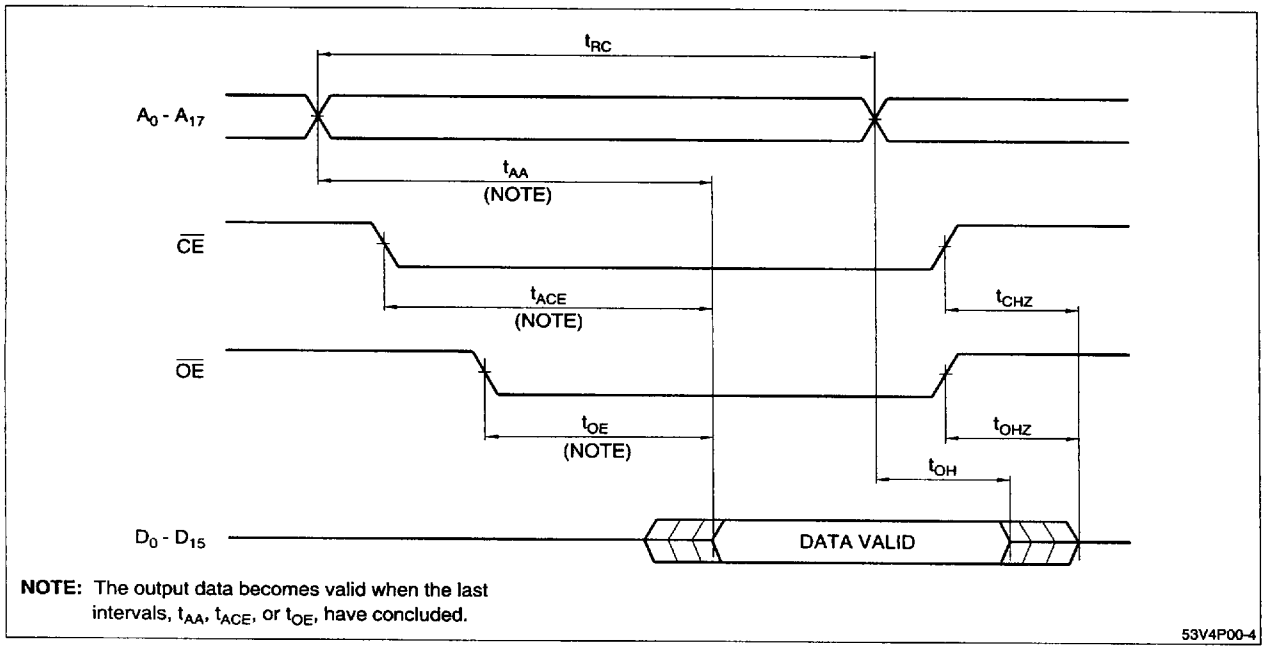
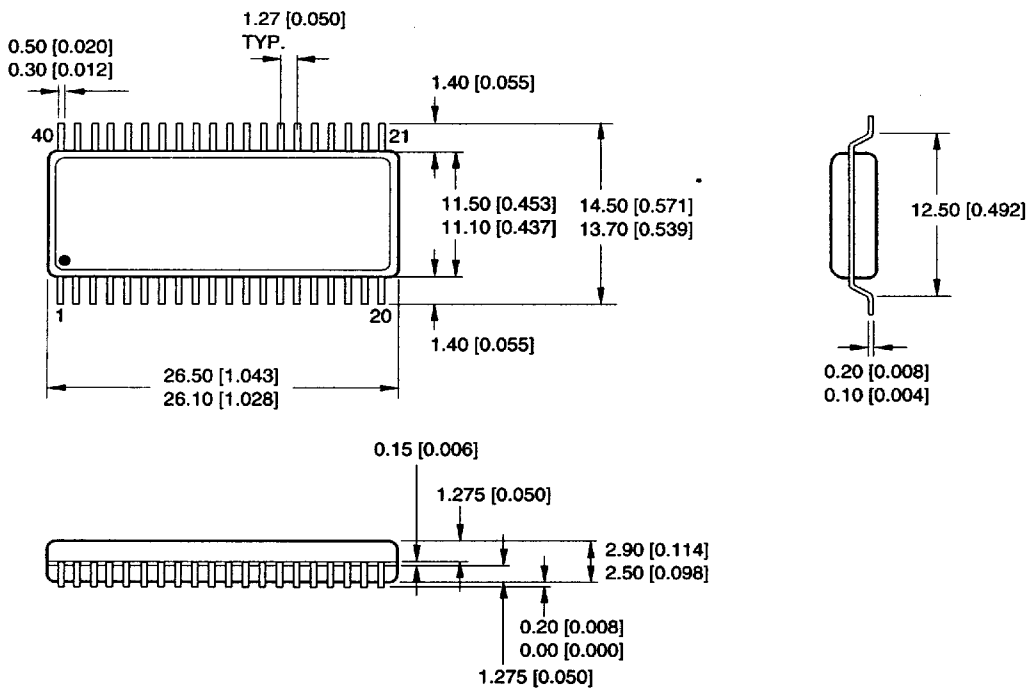


Figure 3. Word Mode ($\overline{BYTE}$ = V_{IH})

PACKAGE DIAGRAM

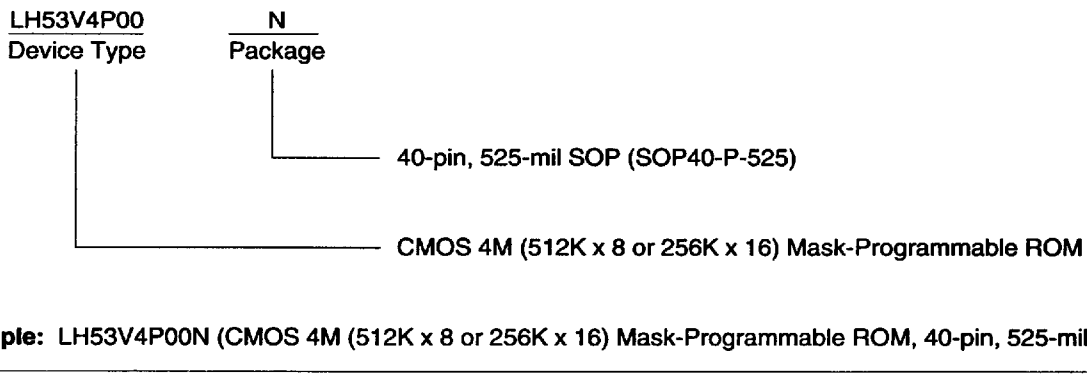
40SOP (SOP040-P-0525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40SOP

ORDERING INFORMATION



Example: LH53V4P00N (CMOS 4M (512K x 8 or 256K x 16) Mask-Programmable ROM, 40-pin, 525-mil SOP)

53V4P00-5