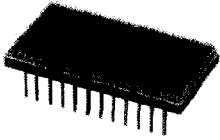


14-BIT DEGLITCHED DIGITAL-TO-ANALOG CONVERTER
20 MHZ UPDATE RATE, VOLTAGE OUTPUT



DESCRIPTION

Continuing DDC's series of leadership display DACs, the DA-02325 is a 14 bit, 20 MHz update rate, deglitched hybrid digital-to-analog (D/A) converter with a low impedance voltage output. Its input registers, precision dc voltage reference, and track and hold (T/H) deglitcher output provide the complete solution to low noise DAC requirements. Packaged in a small 24-pin DDIP, the DA-02325 operates over the full -55°C to +125°C temperature range and military processing is available (consult factory).

DA-02325 is available in linearity grades of 13 bits ($\pm 0.006\%$) and 12 bits ($\pm 0.012\%$). It is available with two

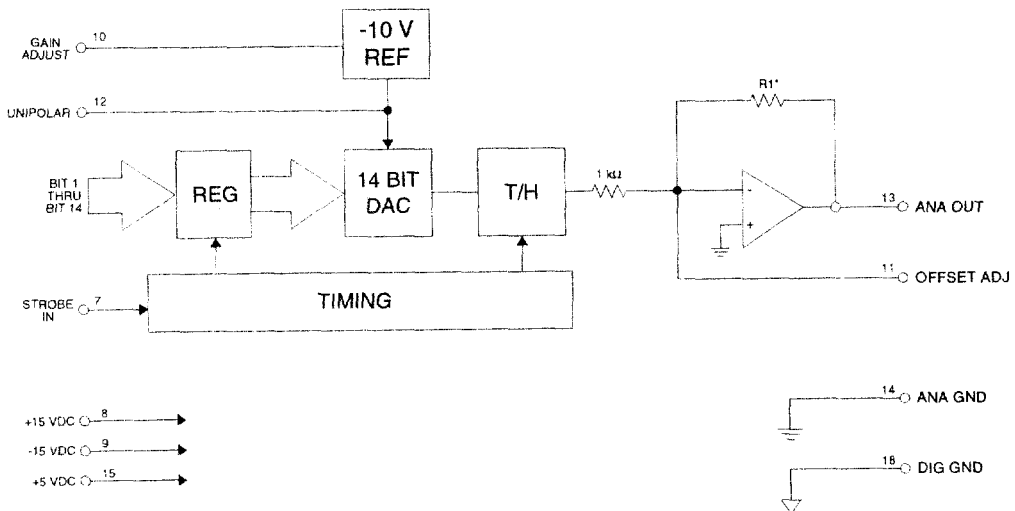
different output voltage ranges. Offset and gain errors can be trimmed to zero with external potentiometers.

APPLICATIONS

With its 14-bit resolution, low glitch voltage output, and small hermetic package, the DA-02325 is ideal for the most demanding low noise DAC requirements. It is particularly well-suited for applications such as vector-stroke CRT displays, waveform generators, and automatic test equipment.

FEATURES

- **Full Function:**
Includes Input Registers and Track/Hold Deglitcher Output
- **High Speed:**
*20 MHz Update Rate for Small Step Changes
 1 μ sec Setting for F.S.*
- **Small Size:**
24-Pin DDIP or Flat Pack Cofired Package Hybrid
- **Wide Operating Temperature:**
-55°C to +125°C



* NOTE: R1 = 2 kΩ FOR 10 V F.S.R. AND 4 kΩ FOR 20 V F.S.R.

FIGURE 1. DA-02325 BLOCK DIAGRAM

TABLE 1. DA-02325 SPECIFICATIONS

PARAMETER	UNITS	VALUE	
		13 BIT LIN	12 BIT LIN
RESOLUTION	BITS	14	14
ACCURACY			
Linearity Error	% FSR	±0.006 max	±0.012 max
Linearity Error Tempco	ppm FSR/°C	±1 max	±2 max
Gain Error (1)	% FSR	±0.2	±0.4
Gain Error Tempco	ppm FSR/°C	±25 max	±25 max
Offset Error (1)	mV	±0.1	±0.2
Offset Error Tempco	ppm FSR/°C	±20 max	±20 max
Monotonicity	Bits	13	12
DYNAMICS			
Settling Time to ±0.01% FSR			
±10 V FS Change	nsec	1 max	
±5 V FS Change	nsec	1 max	
1 LSB Change	nsec	50 max	
Slew Rate	V/μsec	30 typ, 15 min	
Glitch (2)			
Voltage	mVpp	10 typ, 30 max	
Energy	mV nsec	250 typ, 750 max	
DIGITAL INPUTS			
Logic Compatibility		TTL	
Data Inputs			
Logic "1" Level	V	+2.0 to +5	
Logic "0" Level	V	0 to +0.8	
Loading		1 standard LS TTL load	
Coding (negative output)		Offset Binary (Bipolar) Binary (Unipolar)	
Strobe Input (3)			
Logic "1" Level	V	+2.0 to 5	
Logic "0" Level	V	0 to +0.8	
Loading		2 standard S TTL loads	
Width	nsec	10 min	
ANALOG OUTPUT			
Voltage Ranges (4)	V	±10, ±5, 0 to +10	
Current Load	mA	±10 max	
Impedance	Ω	0.3 max	
POWER SUPPLIES		OUTPUT CONFIGURATION	
		+10 V or 0 to +10 V	+5 V
+15 V Supply			
Tolerance	V	+14.25 to +15.75	+11.5 to +15.75
Max Voltage	V	+18 max	+18 max
Current Drain	mA	50 typ, 80 max	50 typ, 80 max
-15 V Supply			
Tolerance	V	+14.25 to +15.75	+11.5 to +15.75
Max Voltage	V	-18 min	-18 min
Current Drain	mA	40 typ, 75 max	40 typ, 75 max
+5 V Supply			
Tolerance	V	+4.75 to +5.25	+4.75 to +5.25
Max Voltage	V	+7 min	+7 min
Current Drain	mA	45 typ, 75 max	45 typ, 75 max

TABLE 1. DA-02325 SPECIFICATIONS (CONTD)

PARAMETER	UNITS	VALUES
POWER DISSIPATION	W	1.6 typ, 2.7 max
TEMPERATURE RANGE		
Operating (Case)		
-1 Option	°C	-55 to +125
-3 Option	°C	0 to +70
Storage	°C	-65 to +150
θ _{J-C}	°C/W	10
θ _{J-C}	°C/W	42
PHYSICAL CHARACTERISTICS		
Package		24-pin DDIP hybrid
Size	in (mm)	1.300 x 0.790 x 0.210 (33.02 x 20.07 x 5.33)
Weight	oz (g)	0.4 (11.3)

NOTES:

- (1) Gain and offset errors are trimmable to zero.
- (2) Glitch is at 1 MHz update rate with a 5 MHz filter in 10 V range.
- (3) Strobe input is a positive pulse. Data transferred on rising edge.
- (4) Output voltage ranges are selectable by model number (see Ordering Information).

INTRODUCTION

The DA-02325 is a complete self-contained deglitched D/A converter. As shown in the block diagram (FIGURE 1), it contains a precision DAC, input registers, a precision dc reference, a track/hold deglitcher output, and timing circuits. Its layout and compatible components provide the complete solution to low noise DAC design problems.

TIMING

Upon Application of a STROBE IN signal, the input registers are updated and the DA-02325 output is held constant. As shown in FIGURE 2, the rising edge of the STROBE IN signal latches the input data. Internal timing circuits generate a pulse which is used to open the T/H. The output remains constant since the op amp feedback capacitor is charged. During the hold mode interval of approximately 20 nanoseconds, the DAC is changing value and its output glitch is settling to zero. At the end of the hold interval the T/H returns to its original track mode level. The DA-02325 then changes to its new output level. The track/hold has effectively "masked out" the DAC glitch.

EXTERNAL TRIMS

Factory adjustment of DA-02325 offset and gain errors result in performance that is adequate for most applications. For more critical applications, DA-02325 provides pins for external trimming offset and gain errors to zero. FIGURE 3 illustrates trim pot values and circuit connections for external trims.

OUTPUT VOLTAGE PROGRAMMING

The DA-02325 can be set for one of three different output voltage ranges. For the ±10 V full scale (FS) range ("1" version), no external connections are required; for ±5 V range ("5" version), no external connections are required; for 0 to +10 V range ("5" version), pin 11 must be jumpered to pin 12.

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SETTLING

The DA-02325 settling time of 1 μ sec max for a FS input and 50 nsec max for a 1 LSB change is based on one strobe to the D/A and waiting for settling to $\pm 0.001\%$ Full Scale Range (FSR). For FS settling of the analog output at an update rate of 15 MHz, the T/H duty cycle must be considered. Since the encode rate is 15 MHz, there are a total of 46.66 nsec between strobes. For 20 nsec of this period the T/H is in HOLD where, by definition, the slew rate is zero. The remaining TRACK time of 46.66 nsec slews at 15 V/ μ sec min. As a consequence, the settling time to 0.01% FSR for a full scale change at a 15 MHz update rate is 1.14 μ sec because seven periods of HOLD, each of 20 nsec duration, are added to the overall settling time. The T/H duty cycle must be considered for calculation of settling time at high update frequencies.

LAYOUT PRECAUTIONS

To achieve the minimum noise performance available from the DA-02325 deglitched D/A converter, high-frequency layout considerations must be kept in mind when designing its printed circuit board. All analog conductor lengths must be kept as short as possible to minimize ground impedances. Digital inputs and the analog output must be kept separated from each other to minimize crosstalk. Circuits connected to the analog output must be kept close to the D/A converter package as possible. Circuit connections to the external adjustment (offset and gain) pins must be kept separate from digital lines to minimize noise coupling.

POWER SUPPLY DECOUPLING

Decoupling capacitors are recommended on each supply to minimize noise. Each of the power supplies should have a 1 microfarad or larger tantalum capacitor in parallel with a 0.01 microfarad ceramic capacitor. All capacitors must be mounted as close as possible to the hybrid package.

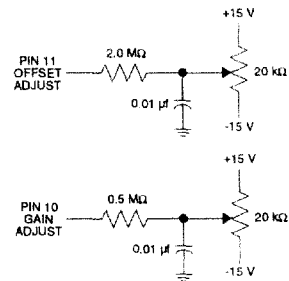


FIGURE 3. EXTERNAL TRIM CIRCUITS

TABLE 2. INPUT DATA CODING		
INPUT DATA	OUTPUT VOLTAGE(1)	
	BIPOLAR	UNIPOLAR(2)
11 1111 1111 1111	+4.9994 V	+9.9994 V
10 0000 0000 0000	0	+5.0000 V
01 1111 1111 1111	-0.0006 V	+4.9994 V
00 0000 0000 0000	-5.0000 V	0

NOTES:

- (1) For "5" version; bipolar voltages double for "1" version.
- (2) Unipolar not available for "1" version; +15 V supplies required for "5" version unipolar output.

TABLE 3. PIN FUNCTION TABLE			
PIN	FUNCTION	PIN	FUNCTION
1	Bit 6	24	Bit 7
2	Bit 5	23	Bit 8
3	Bit 4	22	Bit 9
4	Bit 3	21	Bit 10
5	Bit 2	20	Bit 11
6	Bit 1 (MSB)	19	Bit 12
7	Strobe In	18	Digital Ground
8	+15 V supply	17	Bit 13
9	-15 V supply	16	Bit 14 (LSB)
10	Gain Adjust	15	+5 V supply
11	Offset Adjust	14	Analog Ground
12	Unipolar	13	Vout

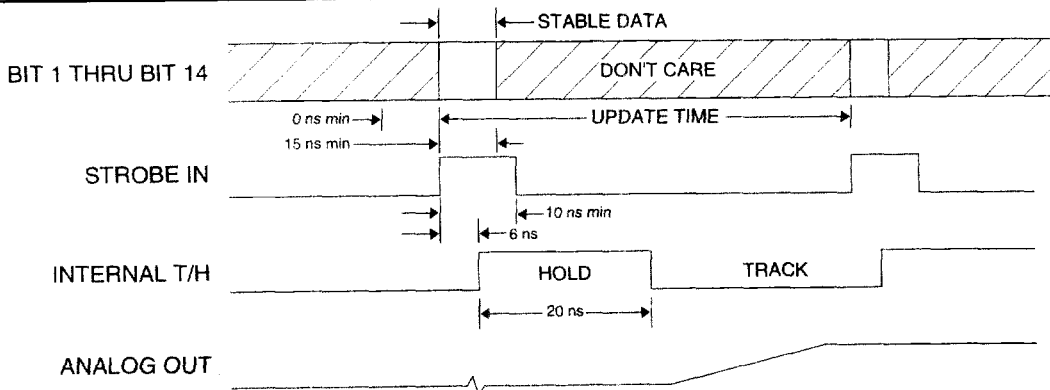
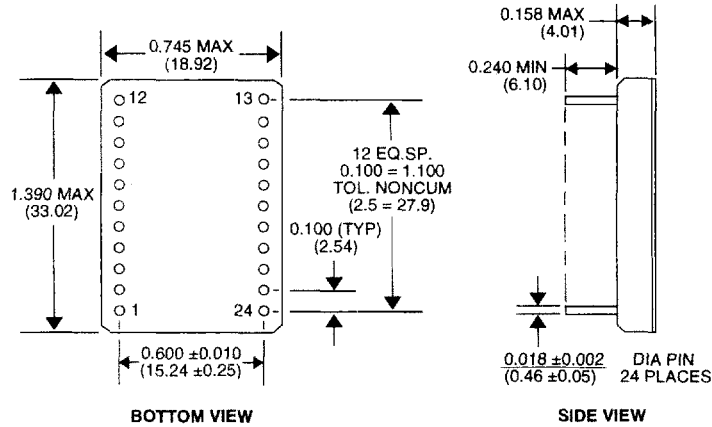


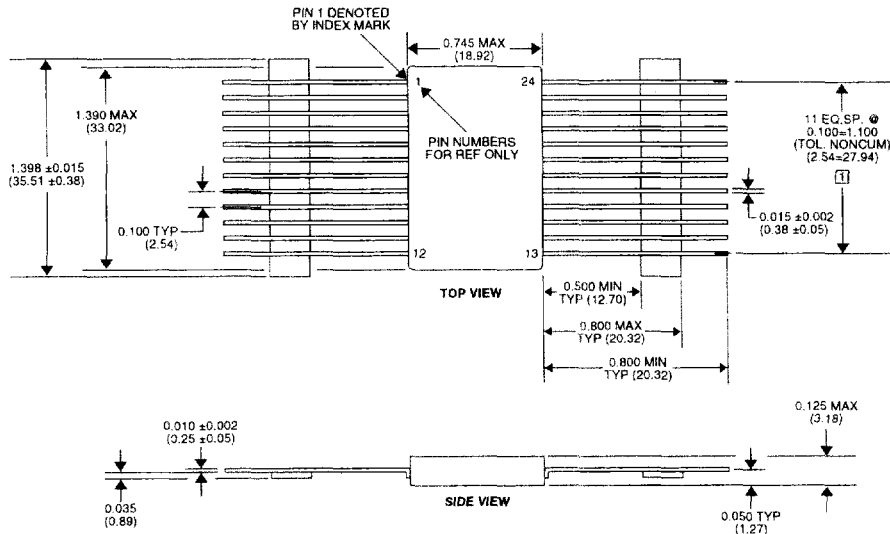
FIGURE 2. TIMING DIAGRAM

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- Notes:
1. Dimensions are in inches (mm).
 2. Lead identification numbers are for reference only.
 3. Lead spacing dimensions apply at seating plane.
 4. Pin material meets solderability requirements to MIL-STD-202E, Method 208C.

FIGURE 4. DA-02325-D MECHANICAL OUTLINE (24-PIN COFIED DDIP)



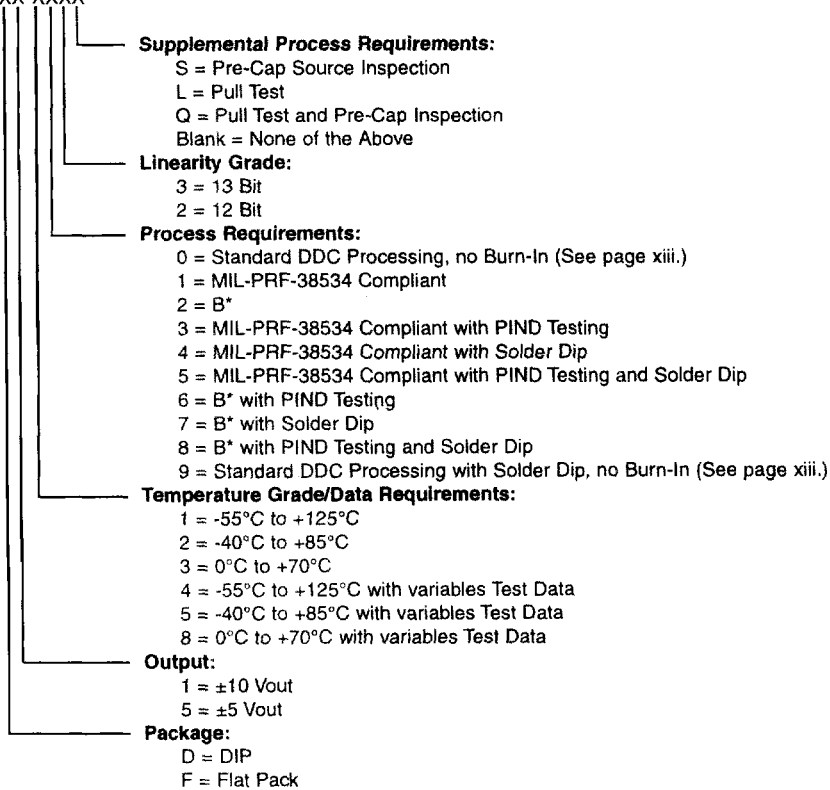
1 LEAD CLUSTER TO BE CENTRALIZED ABOUT CASE CENTERLINE WITHIN ±0.010 (0.25)

Note: Dimensions are in inches (mm).

FIGURE 5. DA-02325-F MECHANICAL OUTLINE (24-PIN COFIED FLAT PACK)

ORDERING INFORMATION

DA-02325XX-XXXX



*Standard DDC Processing with burn-in and full temperature test — see table on page xiii.