AMD

Am29LV001B/Am29LV010B

1 Megabit (128 K x 8-Bit)
CMOS 3.0 Volt-only Boot or Uniform Sector Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 µm process technology**
- **High performance**
  - — Full voltage range: access times as fast as 55 ns
  - — Regulated voltage range: access times as fast as 45 ns
- **Ultra low power consumption (typical values at 5 MHz)**
  - — 200 nA Automatic Sleep mode current
  - — 200 nA standby mode current
  - — 7 mA read current
  - — 15 mA program/erase current
- **Flexible sector architecture**
  - — Am29LV001: one 8 Kbyte, two 4 Kbyte, and seven 16 Kbyte

    Am29LV010: eight 16 Kbyte
  - — Supports full chip erase
  - — Sector Protection features:

    Hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked in-suystem or via programming equipment

    Temporary Sector Unprotect feature allows code changes in prviously plocked sectors
- **Unlock Bypass Mode Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Top or bottom boot block configurations available (Am29LV001 only)**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle guarantee per sector**
- **Package option**
  - — 32-pin TSOP
  - — 32-pin PLCC
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Erase Suspend/Erase Resume**
  - — Supports reading data from or programming data to a sector that is not being erased
- **Hardware reset pin (RESET#) (Am29LV001 only)**
  - — Hardware method for resetting the device to reading array data

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GENERAL DESCRIPTION

The Am29LV001B and Am29LV010B are 1 Mbit, 3.0 Volt-only Flash memory devices organized as 131,072 bytes. The Am29LV001B has a boot sector architecture, whereas the Am29LV010B has a uniform sector architecture, and lacks the RESET# output. These two devices are otherwise identical.

The device is offered in 32-pin PLCC and 32-pin TSOP packages. The byte-wide (x8) data appears on DQ7–DQ0. All read, erase, and program operations are accomplished using only a single power supply. The device can also be programmed in standard EPROM programmers.

The standard Am29LV001B and Am29LV010B offer access times of 45, 55, 70, and 120 ns (90 and 100 ns parts are also available), allowing high speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single power supply** (2.7 V–3.6V) for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV001B and Am29LV010B are entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** (Am29LV001 only) terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

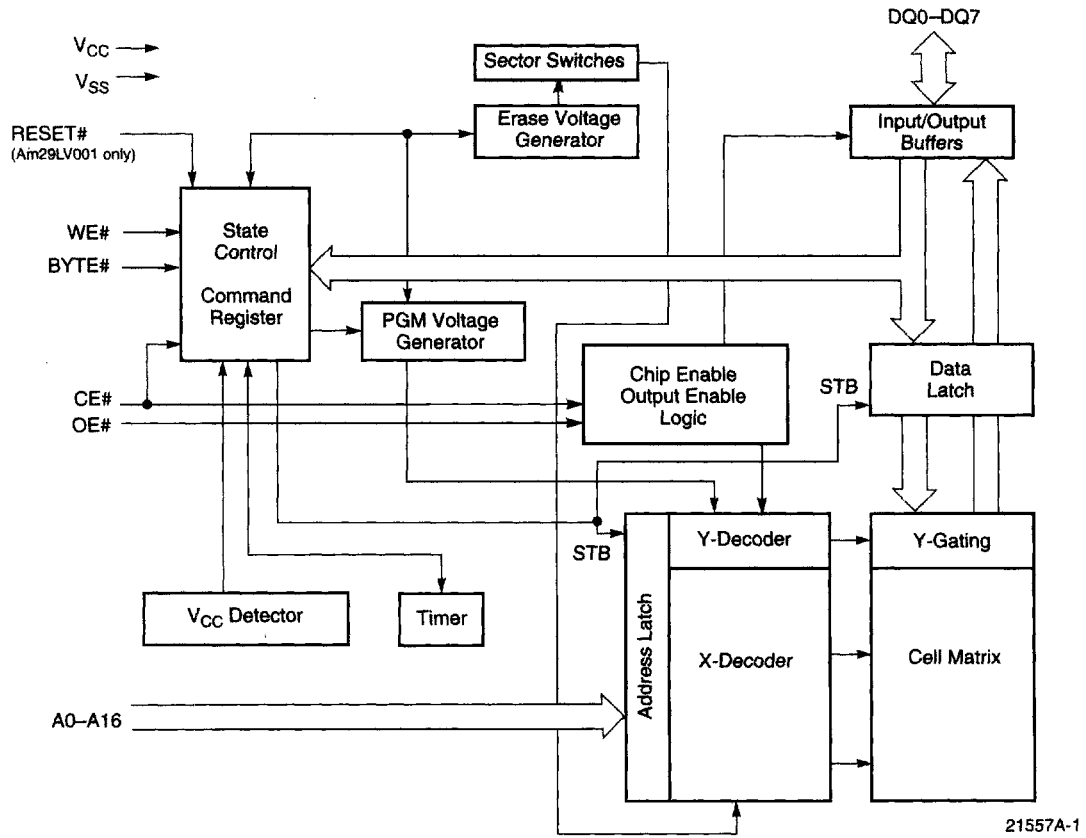
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

PRODUCT SELECTOR GUIDE

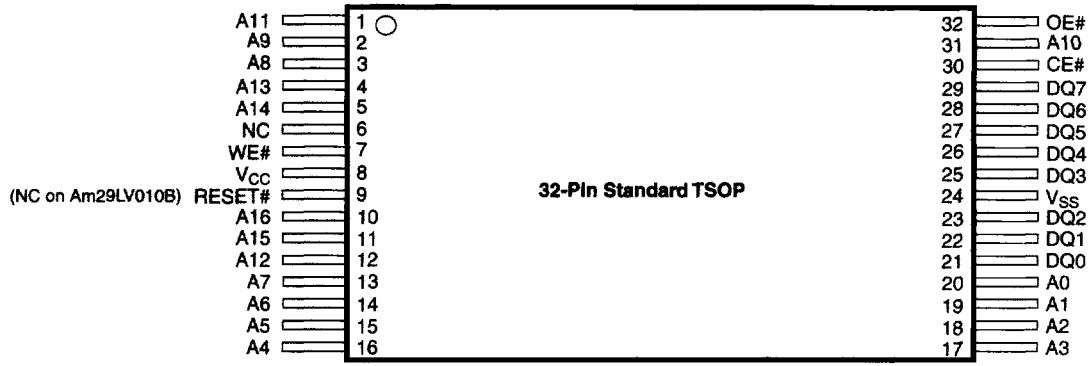
Family Part Number		Am29LV001B/Am29LV010B			
Speed Options	Regulated Voltage Range: V_{CC} =3.0–3.6 V	**-45R**			
	Full Voltage Range: V_{CC} = 2.7–3.6 V		**-55**	**-70**	**-120**
Max access time, ns (t_{ACC})		45	55	70	120
Max CE# access time, ns (t_{CE})		45	55	70	120
Max OE# access time, ns (t_{OE})		30	30	35	50

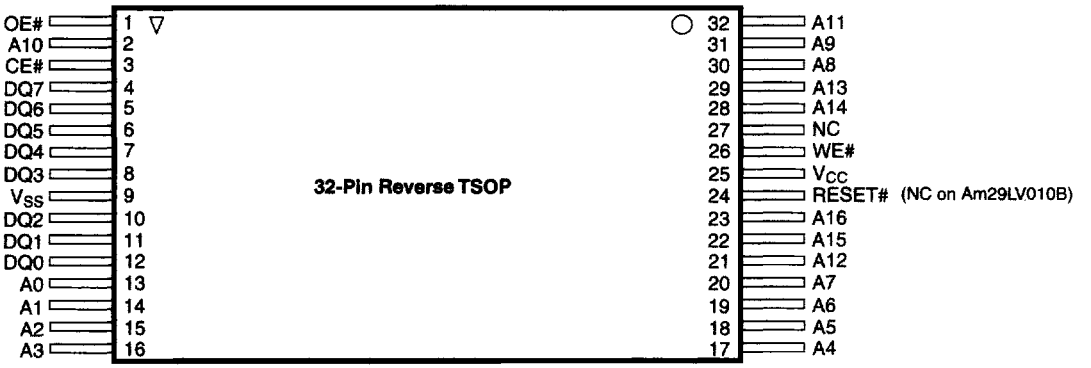
Note: *See "AC Characteristics" for full specifications.*

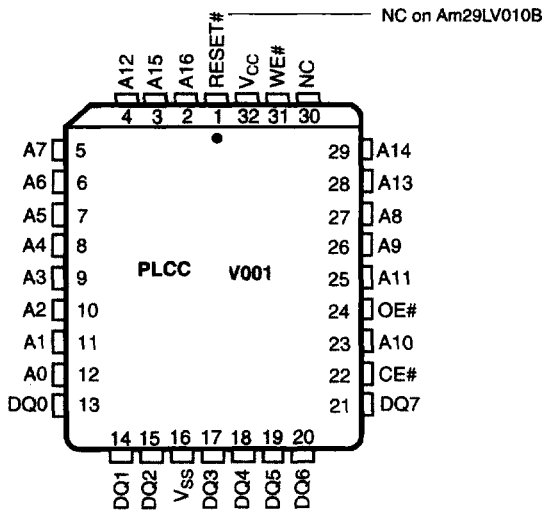
BLOCK DIAGRAM



CONNECTION DIAGRAMS







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PIN CONFIGURATION

A0–A16 = 17 addresses

DQ0–DQ7 = 8 data inputs/outputs

CE# = Chip enable

OE# = Output enable

WE# = Write enable

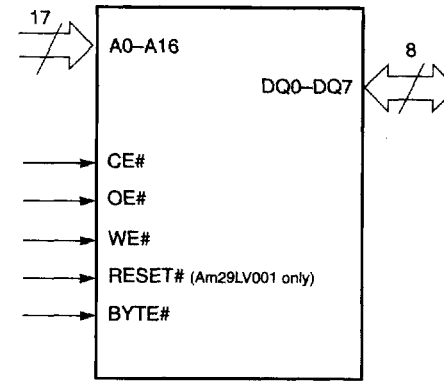
RESET# = Hardware reset pin, active low (Am29LV001 only)

V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)

V_{SS} = Device ground

NC = Pin not connected internally

LOGIC SYMBOL



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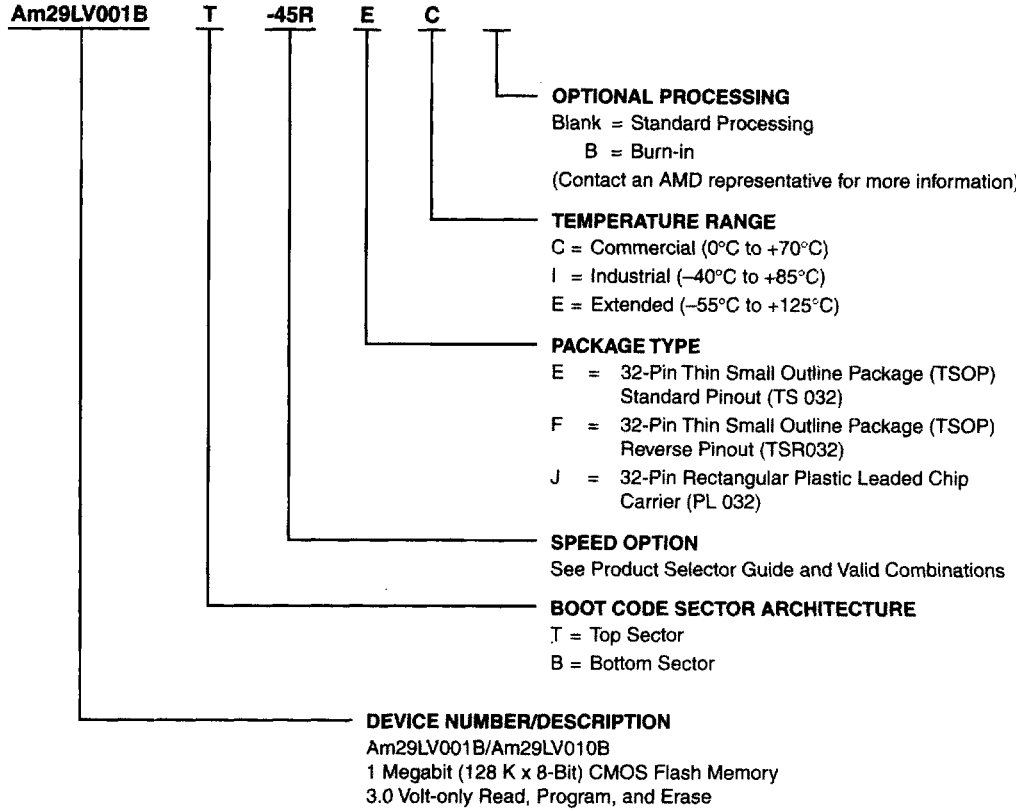
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am29LV001BT-45R, Am29LV001BB-45R, Am2LV010B-45R	EC, FC, JC
Am29LV001BT-55, Am29LV001BB-55, Am2LV010B-55R	EC, EI, EE, FC, FI, FE, JC, JI, JE
Am29LV001BT-70, Am29LV001BB-70, Am2LV010B-70	
Am29LV001BT-120, Am29LV001BB-120, Am2LV010B-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.