IGLOO™ Low-Power Flash FPGAs with Flash*Freeze™ Technology

FlashLock

Features and Benefits

Low Power

- 1.2 V or 1.5 V Core Voltage for Low Power
- Supports Single-Voltage System Operation
- 5 µW Power Consumption in Flash*Freeze Mode
- Low-Power Active FPGA Operation (from 25 µW)
- Flash*Freeze Technology Enables Ultra-Low Power Consumption while Maintaining FPGA Content
- Flash*Freeze Pin Allows Easy Entry To / Exit From Ultra-Low-Power Flash*Freeze Mode

High Capacity

- 30 k to 1 Million System Gates
- Up to 144 kbits of True Dual-Port SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design When Powered Off

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption (except AGL030 devices) via JTAG (IEEE 1532–compliant)
- FlashLock® to Secure FPGA Contents

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os (AGL250 and above)
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—Up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X (except AGL030), and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS (AGL250 and above)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold Sparing I/Os (AGL030 only)
- Programmable Output Slew Rate (except AGL030) and Drive Strength
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages Across the IGLOO Family

Clock Conditioning Circuit (CCC) and PLL (except AGL030)

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase-Shift, Multiply/Divide, Delay Capabilities and External Feedback, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 250 MHz)

Embedded Memory

- 1 kbit of FlashROM User-Nonvolatile Memory
- SRAMs and FIFOs with Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)

Table 1 • **IGLOO Product Family**

IGLOO Devices	AGL030	AGL060 [3]	AGL125	AGL250	AGL600	AGL1000
System Gates	30 k	60 k	125 k	250 k	600 k	1 M
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	13,824	24,576
Quiescent Current (typical) in Flash*Freeze Mode (µA)	4	8	14	28	60	102
RAM kbits (1,024 bits)	–	18	36	36	108	144
4,608-Bit Blocks	–	4	8	8	24	32
FlashROM Bits	1 k	1 k	1 k	1 k	1 k	1 k
Secure (AES) ISP	–	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	1	1	1	1	1
VersaNet Globals[1]	6	18	18	18	18	18
I/O Banks	2	2	2	4	4	4
Maximum User I/Os	81	96	133	143	235	300
Package Pins						
CS		CS196	CS196	CS196 [3]		
QFN	QN132	QN132	QN132	QN132		
VQFP	VQ100	VQ100	VQ100	VQ100		
FBGA		FG144	FG144	FG144	FG144, FG256, FG484	FG144, FG256, FG484

Notes:

1. *Six chip (main) and twelve quadrant global networks are available for AGL060 and above.*
2. *For higher densities and support of additional features, refer to the IGLOO™e Low-Power Flash FPGAs with Flash*Freeze Technology datasheet.*
3. *Device/package support TBD.*

I/Os Per Package[1]

IGLOO Devices	AGL030	AGL060 [6]	AGL125	AGL250 [2]		AGL600		AGL1000	
	I/O Type								
Package Dimensions (mm)	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs	Single-Ended I/O [2]	Differential I/O Pairs
VQ100 (14 × 14)	79	71	71	68	13		–	–	–
QN132 (8 × 8)	81	80	84	87	19		–	–	–
CS196 (8 × 8)	–	96	133	143 [6]	30 [6]		–	–	–
FG144 (13 × 13)	–	96	97	97	24	97	25	97	25
FG256 (17 × 17)	–	–	–	–	–	177	43	177	44
FG484 (23 × 23)	–	–	–	–	–	235	60	300	74

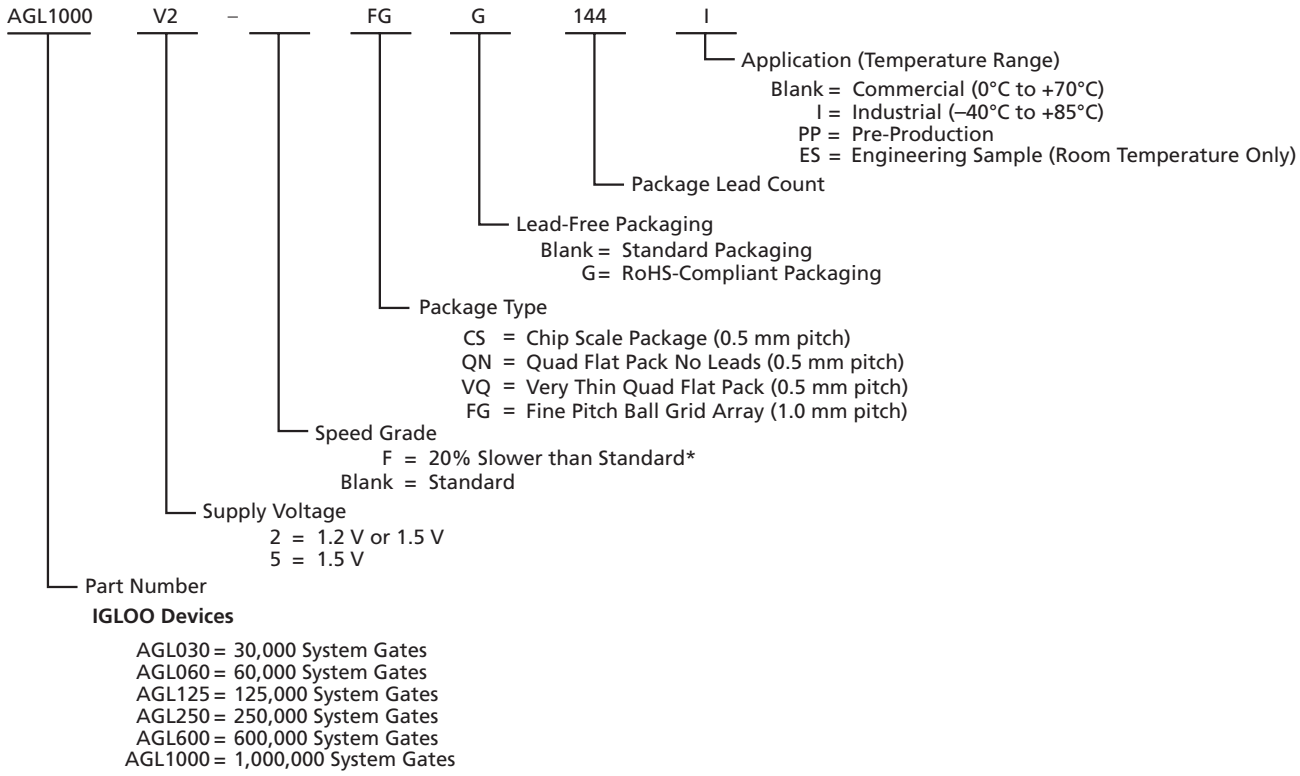
Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to "Package Pin Assignments" starting on page 4-1 to ensure compliance with design and board migration requirements.*
2. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
3. *FG256 and FG484 are footprint-compatible packages.*
4. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
5. *"G" indicates RoHS-compliant packages. Refer to "IGLOO Ordering Information" on page iii for the location of the "G" in the part number.*
6. *Device/package support TBD.*

Packaging Tables

Pinout tables not published in this document will be added in future revisions of the datasheet. For updates, contact your local Actel sales representative.

IGLOO Ordering Information



Note: **The DC and switching characteristics for the –F speed grade targets are based only on simulation. The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*

Temperature Grade Offerings

Package	AGL030	AGL060 [3]	AGL125	AGL250	AGL600	AGL1000
QN132	C, I	C, I	C, I	C, I	–	–
VQ100	C, I	C, I	C, I	C, I	–	–
CS196	–	C, I	C, I	C, I [3]	–	–
FG144	–	C, I	C, I	C, I	C, I	C, I
FG256	–	–	–	–	C, I	C, I
FG484	–	–	–	–	C, I	C, I

Notes:

1. *C = Commercial temperature range: 0°C to 70°C*
2. *I = Industrial temperature range: –40°C to 85°C*
3. *Device/package support TBD*

Speed Grade and Temperature Grade Matrix

Temperature Grade	–F [1]	Std.
C [2]	✓	✓
I [3]	–	✓

Notes:

1. *The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.*
2. *C = Commercial temperature range: 0°C to 70°C*
3. *I = Industrial temperature range: –40°C to 85°C*

Contact your local Actel representative for device availability (http://www.actel.com/contact/default.aspx).

Table of Contents

Introduction and Overview

General Description

The IGLOO family of flash FPGAs, based on a 130-nm flash process, offers the lowest power FPGA, a single-chip solution, small footprint packages, reprogrammability, and an abundance of advanced features.

The Flash*Freeze technology used in IGLOO devices enables entering and exiting an ultra-low-power mode that consumes as little as 5 µW while retaining SRAM and register data. Flash*Freeze technology simplifies power management through I/O and clock management with rapid recovery to operation mode.

The Low Power Active capability (static idle) allows for ultra-low-power consumption (from 25 µW) while the IGLOO device is completely functional in the system. This allows the IGLOO device to control system power management based on external inputs (e.g., scanning for keyboard stimulus) while consuming minimal power.

Nonvolatile flash technology gives IGLOO devices the advantage of being a secure, low power, single-chip solution that is live at power-up (LAPU). IGLOO is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost.

These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

IGLOO devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The AGL030 device has no PLL or RAM support. IGLOO devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 288 user I/Os.

Flash*Freeze Technology

The IGLOO device offers unique Flash*Freeze technology, allowing the device to enter and exit ultra-low-power Flash*Freeze mode. IGLOO devices do not need additional components to turn off I/Os or clocks while retaining the design information, SRAM content, and registers. Flash*Freeze technology is combined with in-system programmability, which enables users to quickly and easily upgrade and update their designs in the final stages of manufacturing or in the field. The ability of IGLOO V2 devices to support a 1.2 V core voltage allows further reduction in power consumption, thus achieving the lowest total system power.

When the IGLOO device enters Flash*Freeze mode, the device automatically shuts off the clocks and inputs to the FPGA core; when the device exits Flash*Freeze mode, all activity resumes and data is retained.

The availability of low-power modes, combined with reprogrammability, a single-chip and single-voltage solution, and availability of small-footprint, high pin-count packages, make IGLOO devices the best fit for portable electronics.

Flash Advantages

Low Power

Flash-based IGLOO devices exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. IGLOO devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

IGLOO devices also have low dynamic power consumption to further maximize power savings; power is even further reduced by the use of a 1.2 V core voltage.

Low dynamic power consumption, combined with low static power consumption and Flash*Freeze technology, gives the IGLOO device the lowest total system power offered by any FPGA.

Security

The nonvolatile, flash-based IGLOO devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. IGLOO devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

IGLOO devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in IGLOO devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. IGLOO devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. IGLOO devices with AES-based

security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed IGLOO device cannot be read back, although secure design verification is possible.

Security, built into the FPGA fabric, is an inherent component of the IGLOO family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The IGLOO family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure, making remote ISP possible. An IGLOO device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based IGLOO FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based IGLOO devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based IGLOO devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the IGLOO device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based IGLOO devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

IGLOO flash FPGAs allow the user to quickly enter and exit Flash*Freeze mode. This is done almost instantly (within 1 µs) and the device retains configuration and data in registers and RAM. Unlike SRAM-based FPGAs the device does not need to reload configuration and design state from external memory components; instead it retains all necessary information to resume operation immediately.

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, Flash-based IGLOO devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The IGLOO family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the IGLOO family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/communications, computing, and avionics markets.

Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-4 for more information.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of IGLOO flash-based FPGAs. Once it is programmed, the flash cell configuration element of IGLOO FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Advanced Flash Technology

The IGLOO family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising

device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

IGLOO family FPGAs utilize design and process techniques to minimize power consumption in all modes of operation.

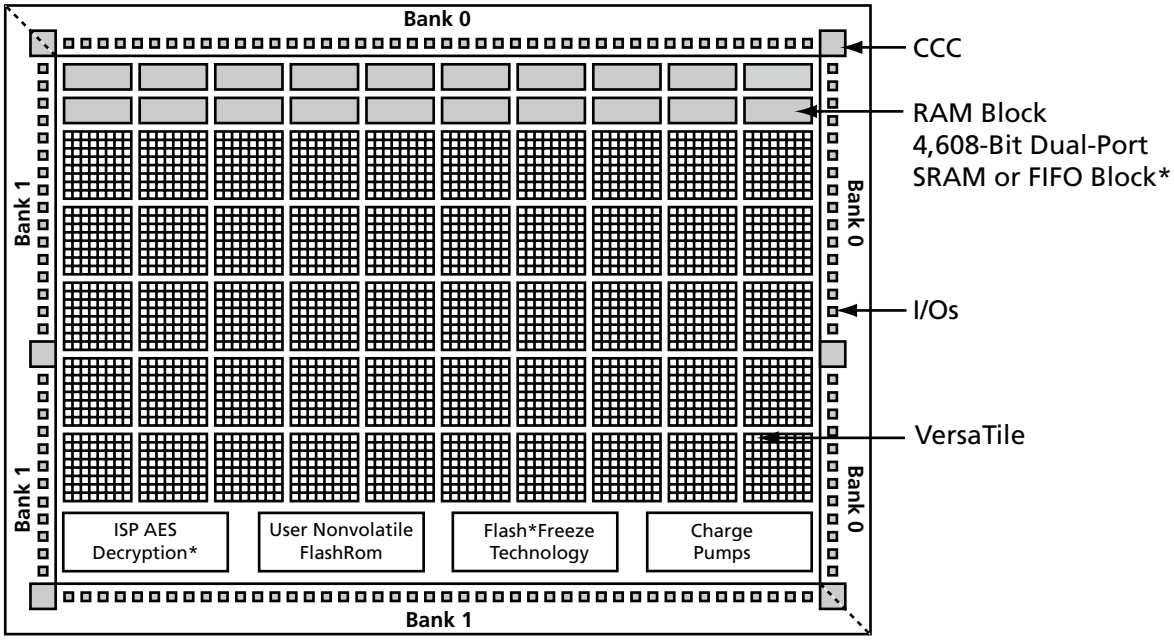
Advanced Architecture

The proprietary IGLOO architecture provides granularity comparable to standard-cell ASICs. The IGLOO device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- Flash*Freeze technology
- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[1]
- Extensive CCCs and PLLs[1]
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the IGLOO core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC® family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface.



Note: **Not supported by AGL030*

Figure 1-1 • **IGLOO Device Architecture Overview with Two I/O Banks (AGL030, AGL060, and AGL125)**

1. *The AGL030 does not support PLL or SRAM.*

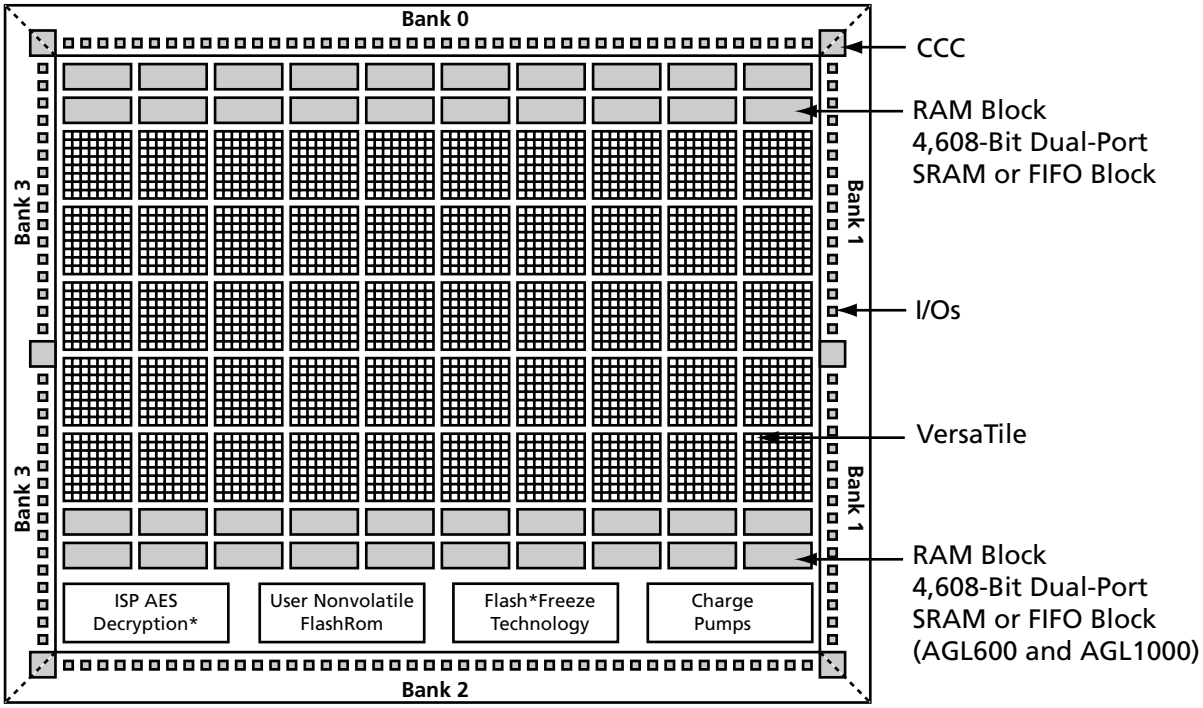


Figure 1-2 • **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, and AGL1000)**

Flash*Freeze Technology

The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 25 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode. For more information on how to use Flash*Freeze capability and other low power modes, refer to the "Flash*Freeze Technology and Low-Power Modes" section on page 2-50.

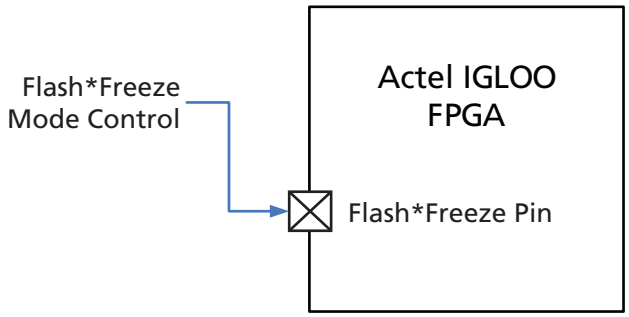


Figure 1-3 • **IGLOO Flash*Freeze Mode**

VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC[PLUS]® core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

For more information about VersaTiles, refer to the "VersaTile" section on page 2-2.

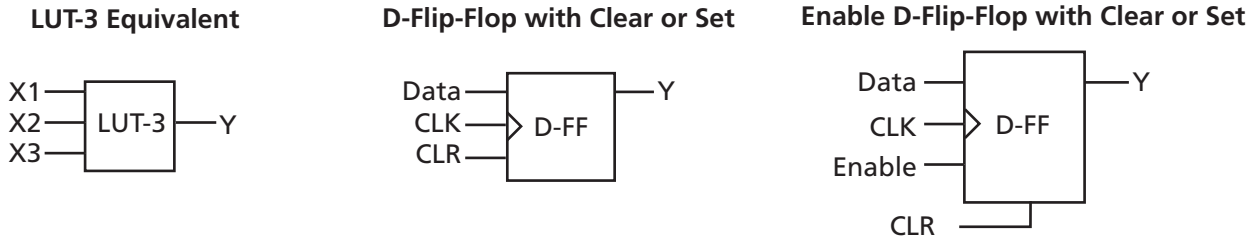


Figure 1-4 • **VersaTile Configurations**

User Nonvolatile FlashROM

Actel IGLOO devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard IGLOO IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the AGL030 device), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel IGLOO development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

IGLOO devices (except the AGL030 device) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in the AGL030 device).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

IGLOO devices provide designers with very flexible clock conditioning capabilities. Each member of the IGLOO family contains six CCCs. One CCC (center west side) has a PLL. The AGL030 does not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access (refer to the "Clock Conditioning Circuits" section on page 2-14 for more information).

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (250 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. Refer to Table 2-22 on page 2-47 for details on I/O bank configuration. The configuration of these banks determines the I/O standards supported (see Table 2-22 on page 2-47 for more information).

Each I/O module contains several input, output, and enable registers (Figure 2-24 on page 2-34). These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, BLVDS, and M-LVDS I/Os for point-to-point communications

See the "DDR Module Specifications" section on page 3-71 for more information.

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, BLVDS, and M-LVDS. BLVDS and M-LVDS can support up to 20 loads.

Related Documents

Application Notes

*Actel IGLOO™/e Flash*Freeze™ Technology and Low Power Modes*
http://www.actel.com/documents/IGLOO_e_LP_AN.pdf

User's Guides

SmartGen Cores Reference Guide
http://www.actel.com/documents/genguide_ug.pdf
Designer User's Guide
http://www.actel.com/documents/designer_ug.pdf
Fusion, IGLOO/e and ProASIC3/E Macro Library Guide
http://www.actel.com/documents/pa3_libguide_ug.pdf

Device Architecture

Introduction

Flash Technology

Advanced Flash Switch

Unlike SRAM FPGAs, the IGLOO family uses a live-at-power-up ISP flash switch as its programming element. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable programming to connect signal lines to the appropriate VersaTile inputs and outputs. In the flash switch, two transistors share the floating gate, which stores the programming information (Figure 2-1). One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. The latter is used to connect or separate routing nets, or to configure VersaTile logic. It is also used to erase the floating gate. Dedicated high-performance lines are connected as required using the flash switch for fast, low-skew, global signal distribution throughout the device core. Maximum core utilization is possible for virtually any design. The use of the flash switch technology also removes the possibility of firm errors, which are increasingly common in SRAM-based FPGAs.

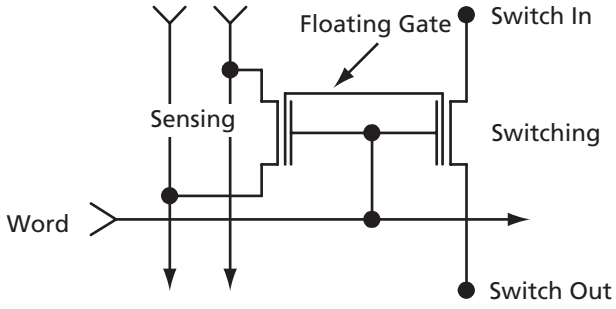


Figure 2-1 • **IGLOO Flash-Based Switch**

Device Overview

The IGLOO device family consists of six distinct programmable architectural features (Figure 2-2 and Figure 2-3 on page 2-3):

- FPGA fabric/core (VersaTiles)
- Routing and clock resources (VersaNets)
- FlashROM
- Dedicated SRAM/FIFO memory (except AGL030)
- Advanced I/O structure
- Flash*Freeze technology and low-power modes

Core Architecture

VersaTile

The proprietary IGLOO family architecture provides granularity comparable to gate arrays. The IGLOO device core consists of a sea-of-VersaTiles architecture.

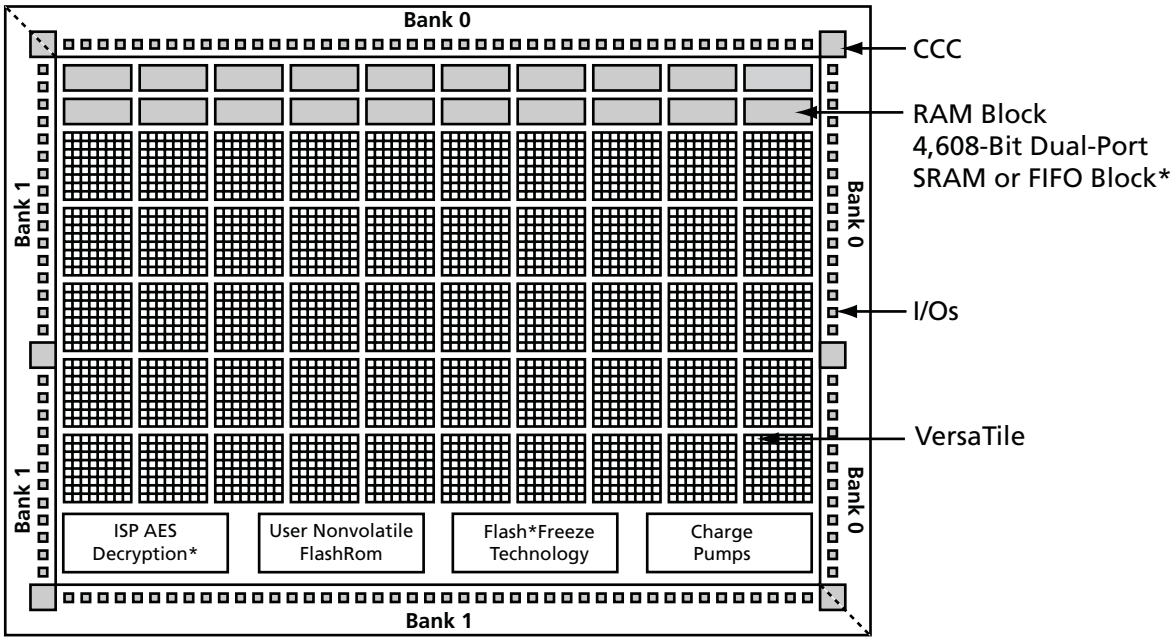
As illustrated in Figure 2-4 on page 2-4, there are four inputs in a logic VersaTile cell, and each VersaTile can be configured using the appropriate flash switch connections:

- Any 3-input logic function
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set (on a fourth input)

VersaTiles can flexibly map the logic and sequential gates of a design. The inputs of the VersaTile can be inverted (allowing bubble pushing), and the output of the tile can connect to high-speed, very-long-line routing resources. VersaTiles and larger functions can be connected with any of the four levels of routing hierarchy.

When the VersaTile is used as an enable D-flip-flop, SET/CLR is supported by a fourth input. The SET/CLR signal can only be routed to this fourth input over the VersaNet (global) network. However, if in the user's design the SET/CLR signal is not routed over the VersaNet network, a compile warning message will be given, and the intended logic function will be implemented by two VersaTiles instead of one.

The output of the VersaTile is F2 (Figure 2-4 on page 2-4) when the connection is to the ultra-fast local lines, or YL when the connection is to the efficient long-line or very-long-line resources.



Note: **Not supported by AGL030*

Figure 2-2 • **IGLOO Device Architecture Overview with Two I/O Banks (AGL030, AGL060, and AGL125)**

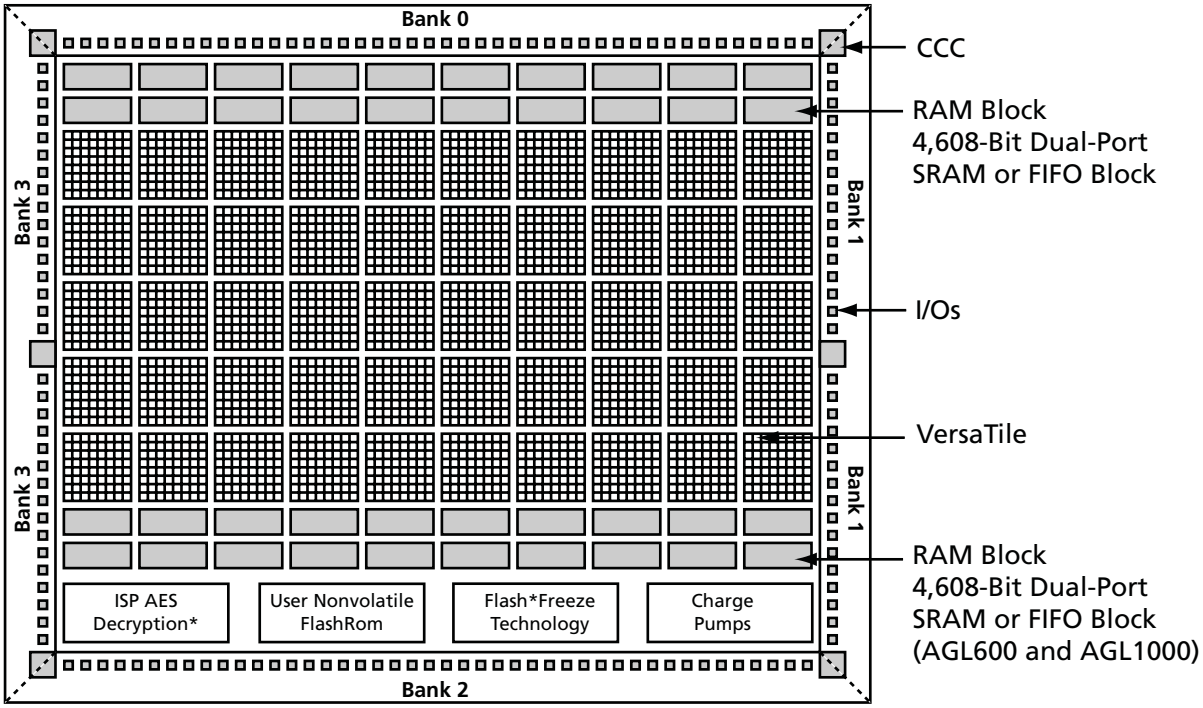
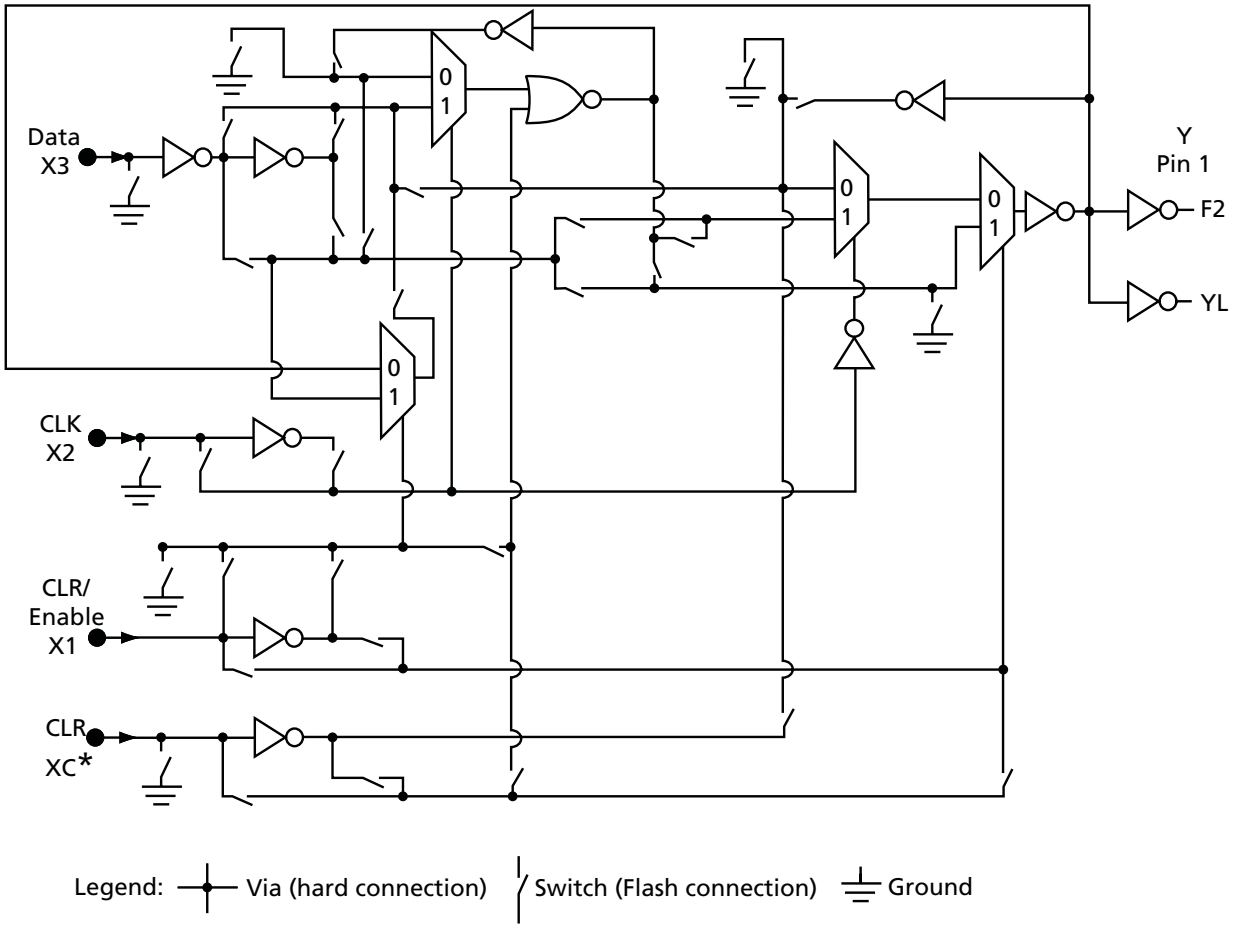


Figure 2-3 • **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, and AGL1000)**



Note: **This input can only be connected to the global clock distribution network.*

Figure 2-4 • **IGLOO Core VersaTile**

Array Coordinates

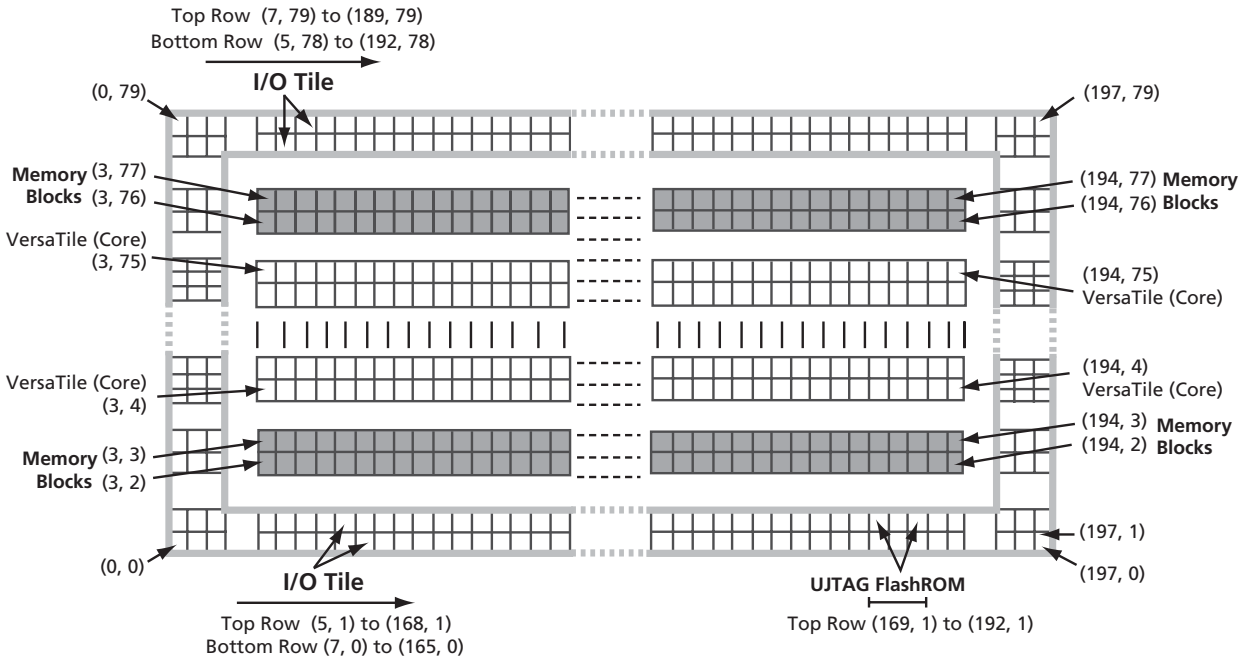
During many place-and-route operations in the Actel Designer software tool, it is possible to set constraints that require array coordinates. Table 2-1 provides array coordinates of core cells and memory blocks. The array coordinates are measured from the lower left (0, 0). They can be used in region constraints for specific logic groups/blocks, designated by a wildcard, and can contain core cells, memories, and I/Os.

I/O and cell coordinates are used for placement constraints. Two coordinate systems are needed because there is not a one-to-one correspondence between I/O cells and core cells. In addition, the I/O coordinate system changes depending on the die/package combination. It is not listed in Table 2-1. The Designer ChipPlanner tool provides the array coordinates of all I/O locations. I/O and cell coordinates are used for placement constraints. However, I/O placement is easier by package pin assignment.

Figure 2-5 illustrates the array coordinates of an device. For more information on how to use array coordinates for region/placement constraints, see the *Designer User's Guide* or online help (available in the software) for IGLOO software tools.

Table 2-1 • **IGLOO Array Coordinates**

	VersaTiles				Memory Rows		All	
	Min.		Max.		Bottom	Top	Min.	Max.
Device	x	y	x	y	(x, y)	(x, y)	(x, y)	(x, y)
AGL030	–	–	–	–	–	–	–	–
AGL060	3	2	66	25	None	(3, 26)	(0, 0)	(69, 29)
AGL125	3	2	130	25	None	(3, 26)	(0, 0)	(133, 29)
AGL250	3	2	130	49	None	(3, 50)	(0, 0)	(133, 53)
AGL600	3	4	194	75	(3, 2)	(3, 76)	(0, 0)	(197, 79)
AGL1000	3	4	258	99	(3, 2)	(3, 100)	(0, 0)	(261, 103)



Note: *The vertical I/O tile coordinates are not shown. West side coordinates are {(0, 2) to (2, 2)} to {(0, 77) to (2, 77)}; east side coordinates are {(195, 2) to (197, 2)} to {(195, 77) to (197, 77)}.*

Figure 2-5 • **Array Coordinates for AGL600**

Routing Architecture

Routing Resources

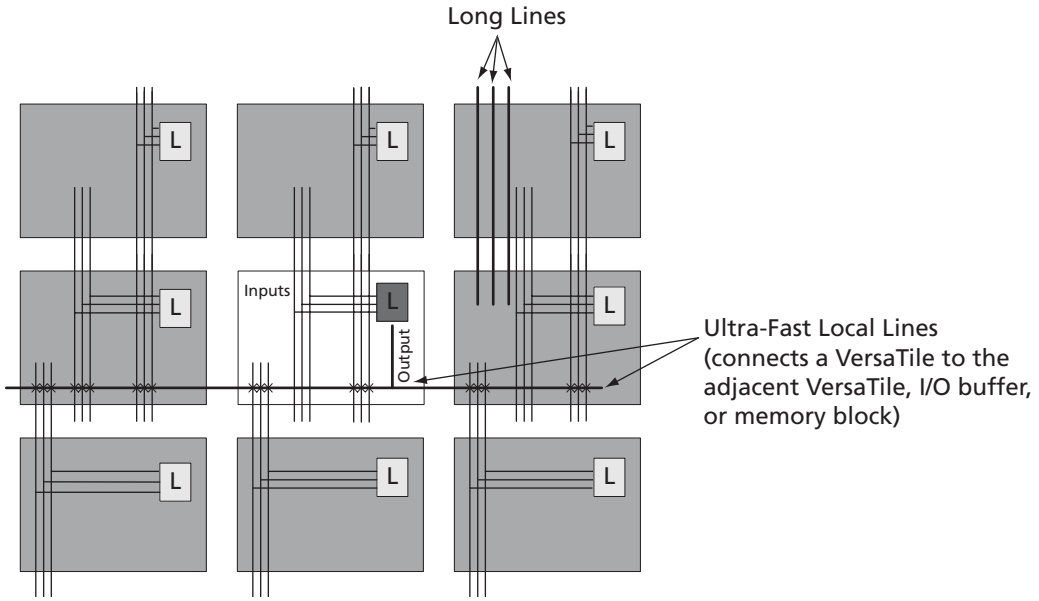
The routing structure of IGLOO devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra-fast local resources; efficient long-line resources; high-speed, very-long-line resources; and the high-performance VersaNet networks.

The ultra-fast local resources are dedicated lines that allow the output of each VersaTile to connect directly to every input of the eight surrounding VersaTiles (Figure 2-6). The exception to this is that the SET/CLR input of a VersaTile configured as a D-flip-flop is driven only by the VersaTile global network.

The efficient long-line resources provide routing for longer distances and higher-fanout connections. These resources vary in length (spanning one, two, or four VersaTiles), run both vertically and horizontally, and cover the entire IGLOO device (Figure 2-7 on page 2-7). Each VersaTile can drive signals onto the efficient long-line resources, which can access every input of every VersaTile. Routing software automatically inserts active buffers to limit loading effects.

The high-speed, very-long-line resources, which span the entire device with minimal delay, are used to route very long or high-fanout nets: length +/–12 VersaTiles in the vertical direction and length +/–16 in the horizontal direction from a given core VersaTile (Figure 2-8 on page 2-8). Very long lines in IGLOO devices have been enhanced over those in previous ProASIC families. This provides a significant performance boost for long-reach signals.

The high-performance VersaNet global networks are low-skew, high-fanout nets that are accessible from external pins or internal logic (Figure 2-9 on page 2-10). These nets are typically used to distribute clocks, resets, and other high-fanout nets requiring minimum skew. The VersaNet networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all VersaTiles.



Note: *Input to the core cell for the D-flip-flop set and reset is only available via the VersaNet global network connection.*

Figure 2-6 • **Ultra-Fast Local Lines Connected to the Eight Nearest Neighbors**

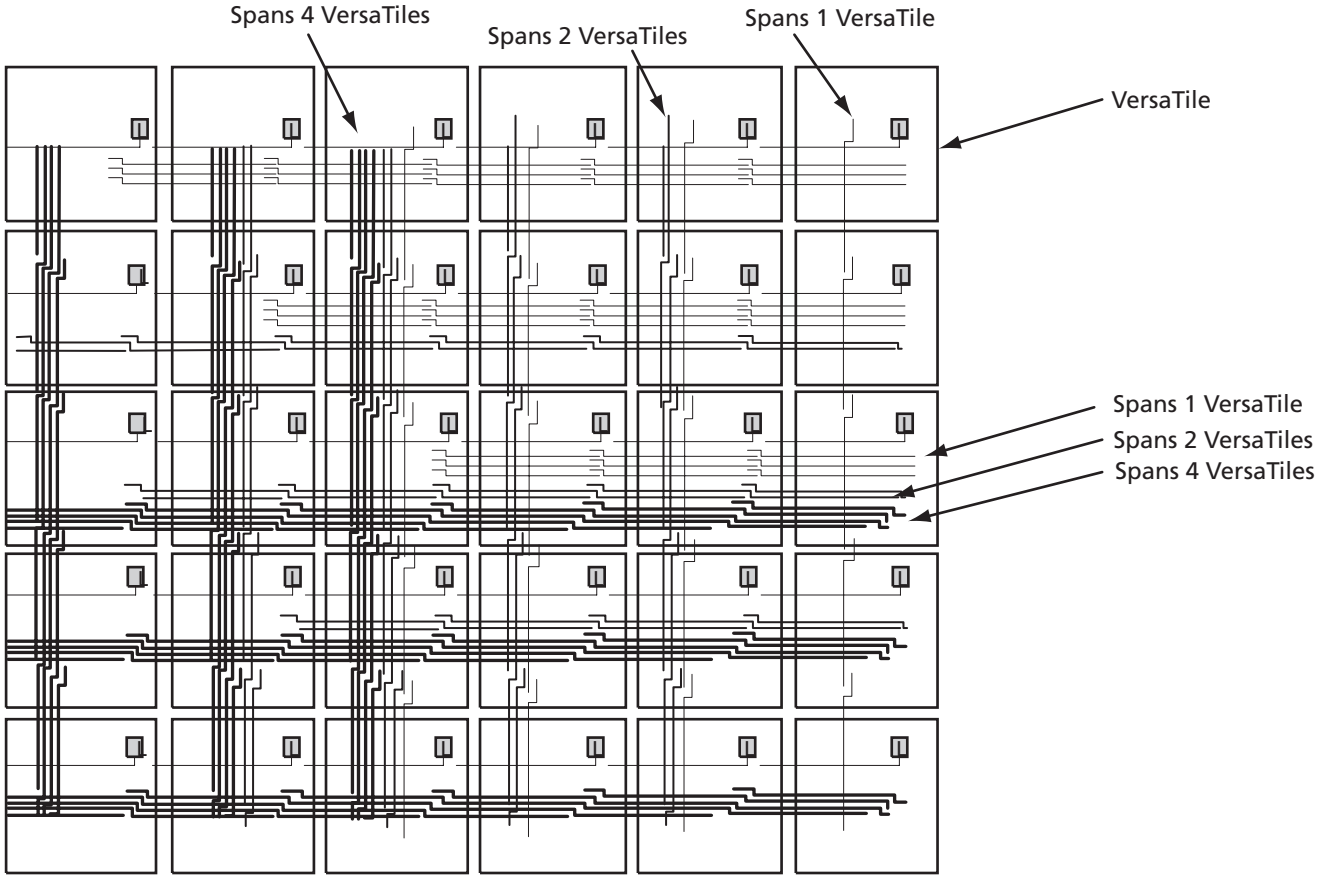


Figure 2-7 • **Efficient Long-Line Resources**

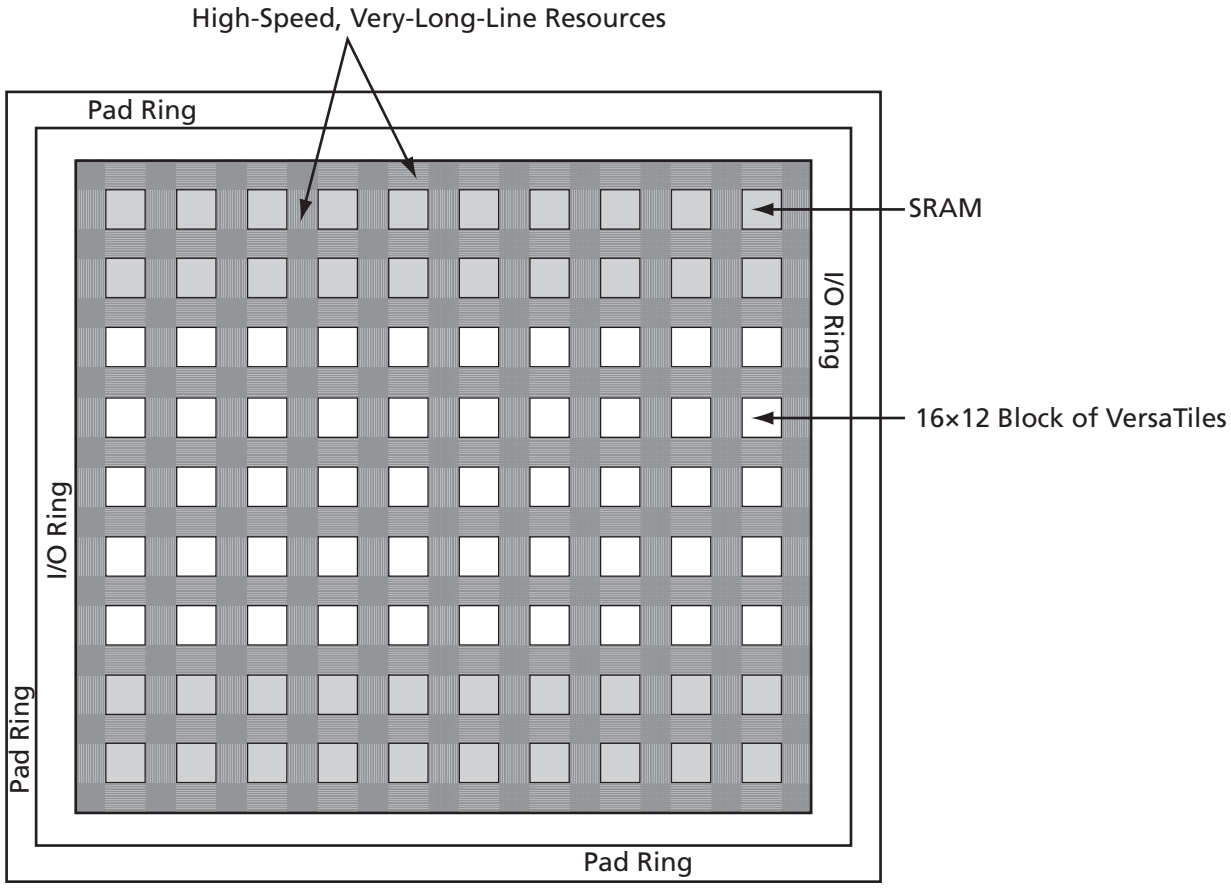


Figure 2-8 • **Very-Long-Line Resources**

Clock Resources (VersaNets)

IGLOO devices offer powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has up to six CCCs. The west CCC also contains a phase-locked loop (PLL) core, delay lines, a phase shifter (0°, 90°, 180°, 270°), and clock multipliers/dividers. Each CCC has all the circuitry needed for the selection and interconnection of inputs to the VersaNet global network. The east and west CCCs each have access to three VersaNet global lines on each side of the chip (six total lines). The CCCs at the four corners each have access to three quadrant global lines in each quadrant of the chip (except AGL030).

Advantages of the VersaNet Approach

One of the architectural benefits of IGLOO is the set of powerful and low-delay VersaNet global networks. IGLOO offers six chip (main) global networks that are distributed from the center of the FPGA array (Figure 2-9 on page 2-10). In addition, IGLOO devices have three regional globals in each of the four chip quadrants. Each core VersaTile has access to nine global network resources: three quadrant and six chip (main) global networks, and a total of 18 globals on the device. Each of these networks contains spines and ribs that reach all the VersaTiles in the quadrants (Figure 2-10 on page 2-11). This flexible VersaNet global network architecture allows users to map up to 144 different internal/external clocks in a IGLOO device. Details on the VersaNet networks are given in Table 2-2 on page 2-11. The flexible use of the IGLOO VersaNet global network allows the designer to address several design requirements. User applications that are clock-resource-intensive can easily route external or gated internal clocks using VersaNet global routing networks. Designers can also drastically reduce delay penalties and minimize resource usage by mapping critical, high-fanout nets to the VersaNet global network.

In AGL030 devices, all six VersaNets are driven from three southern I/Os, located toward the east and west sides. Each of these tiles can be configured to select a central I/O on its respective side or an internal routed signal as the input signal. The AGL030 does not support any clock conditioning circuitry, nor does it contain the VersaNet global network concept of top and bottom spines.

VersaNet Global Networks and Spine Access

The IGLOO architecture contains a total of 18 segmented global networks that can access the VersaTiles, SRAM, and I/O tiles of the IGLOO device. There are nine global network resources in each device quadrant: three quadrant globals and six chip (main) global networks. Each device has a total of 18 globals. These VersaNet global networks offer fast, low-skew routing resources for high-fanout nets, including clock signals. In addition, these highly segmented global networks offer users the flexibility to create low-skew local networks using spines for up to 144internal/external clocks (in an AGL1000 device) or other high-fanout nets in IGLOO devices. Optimal usage of these low-skew networks can result in significant improvement in design performance on IGLOO devices.

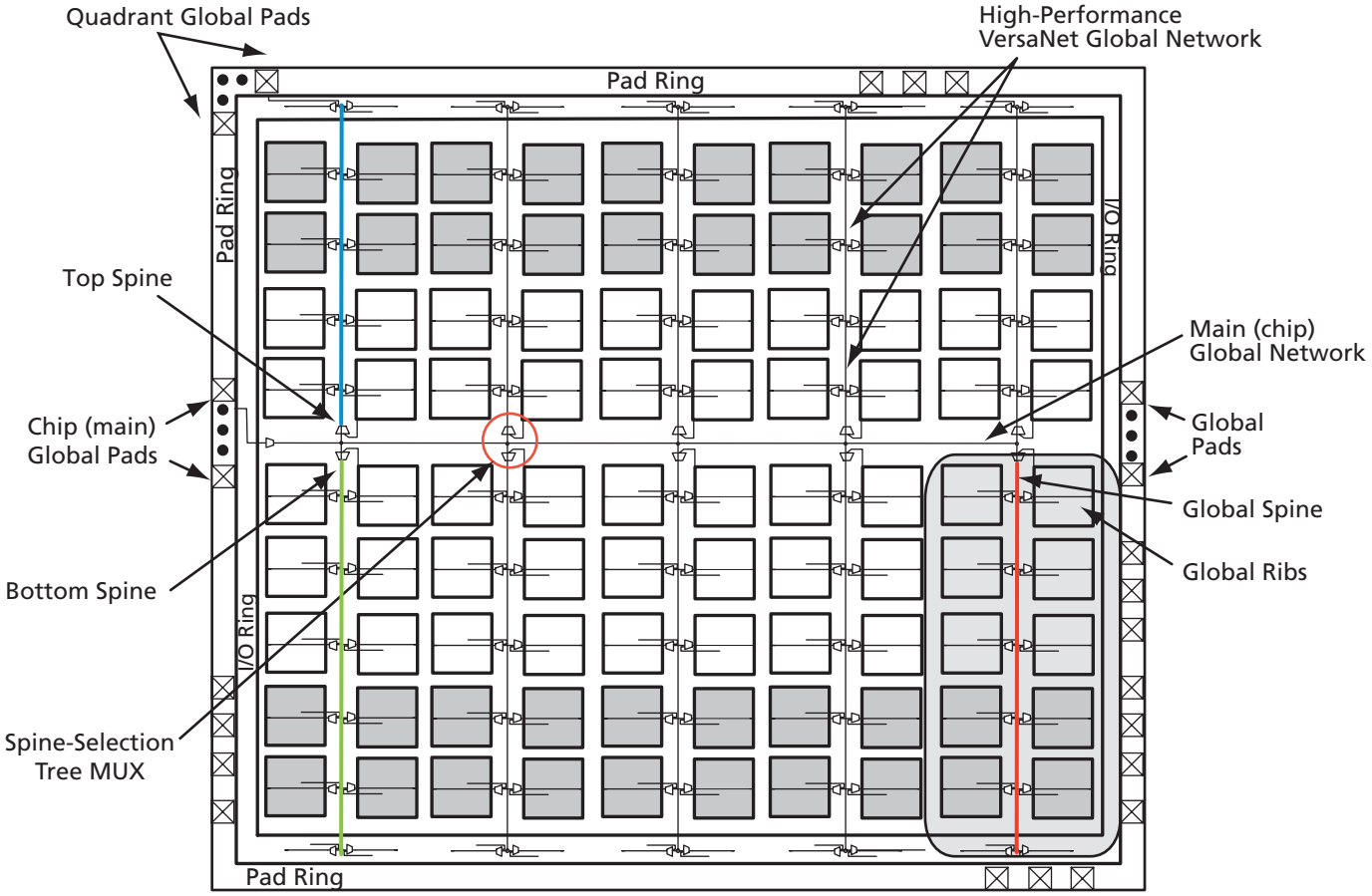
The nine spines available in a vertical column reside in global networks with two separate regions of scope: the quadrant global network, which has three spines, and the chip (main) global network, which has six spines. Note that there are three quadrant spines in each quadrant of the device (except for AGL030). There are four quadrant global network regions per device (Figure 2-10 on page 2-11).

The spines are the vertical branches of the global network tree, shown in Figure 2-11 on page 2-12. Each spine in a vertical column of a chip (main) global network is further divided into two equal-length spine segments: one in the top and one in the bottom half of the die.

Each spine and its associated ribs cover a certain area of the IGLOO device (the "scope" of the spine; see Figure 2-9 on page 2-10). Each spine is accessed by the dedicated global network MUX tree architecture, which defines how a particular spine is driven—either by the signal on the global network from a CCC, for example, or by another net defined by the user (Figure 2-12 on page 2-13). Quadrant spines can be driven from user I/Os on the north and south sides of the die. The ability to drive spines in the quadrant global networks can have a significant effect on system performance for high-fanout inputs to a design.

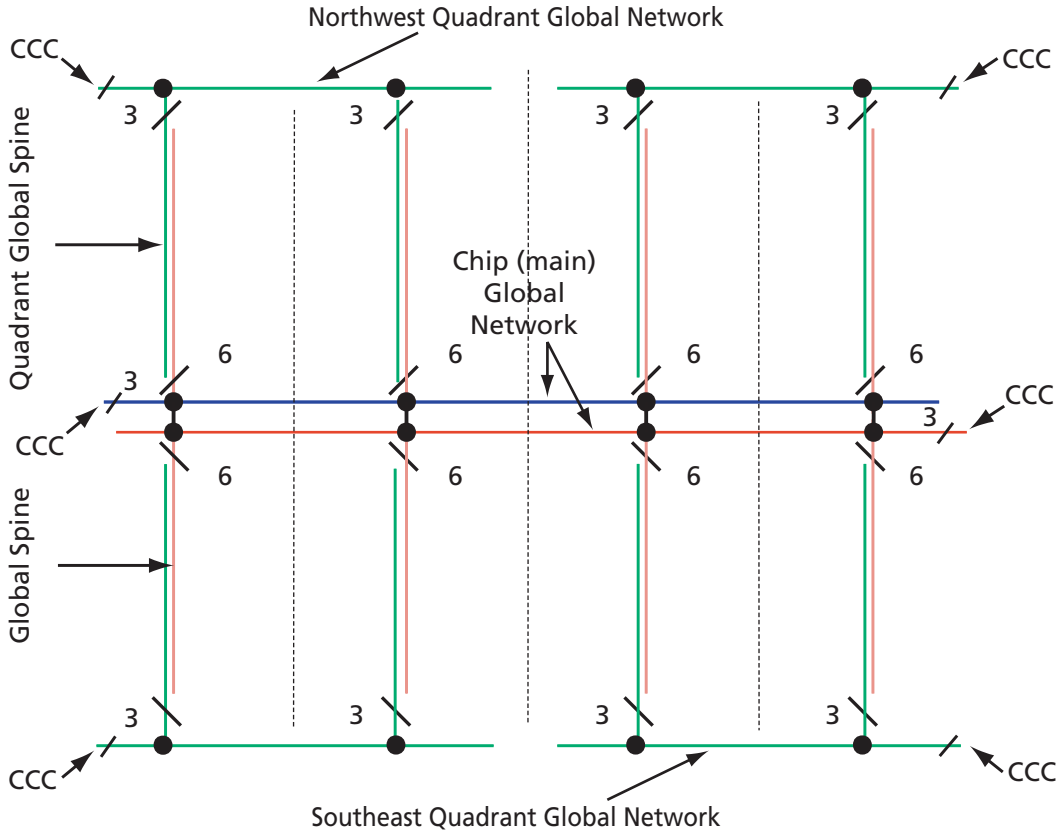
Details of the chip (main) global network spine-selection MUX are presented in Figure 2-12 on page 2-13. The spine drivers for each spine are located in the middle of the die.

Quadrant spines are driven from a north or south rib. Access to the top and bottom ribs is from the corner CCC or from the I/Os on the north and south sides of the device.



Note: *Not applicable to the AGL030 device.*

Figure 2-9 • **Overview of IGLOO VersaNet Global Network**



Note: *Not applicable to the AGL030 device.*

Figure 2-10 • **Global Network Architecture**

Table 2-2 • **IGLOO Globals/Spines/Rows by Device**

	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
Global VersaNets (trees)*	6	9	9	9	9	9
VersaNet Spines/Tree	4	4	4	8	12	16
Total Spines	24	36	36	72	108	144
VersaTiles in Each Top or Bottom Spine	384	384	384	768	1,152	1,536
Total VersaTiles	768	1,536	3,072	6,144	13,824	24,576
Rows in Each Top or Bottom Spine	–	12	12	24	36	48

Note: **There are six chip (main) globals and three globals per quadrant (except in the AGL030 device).*

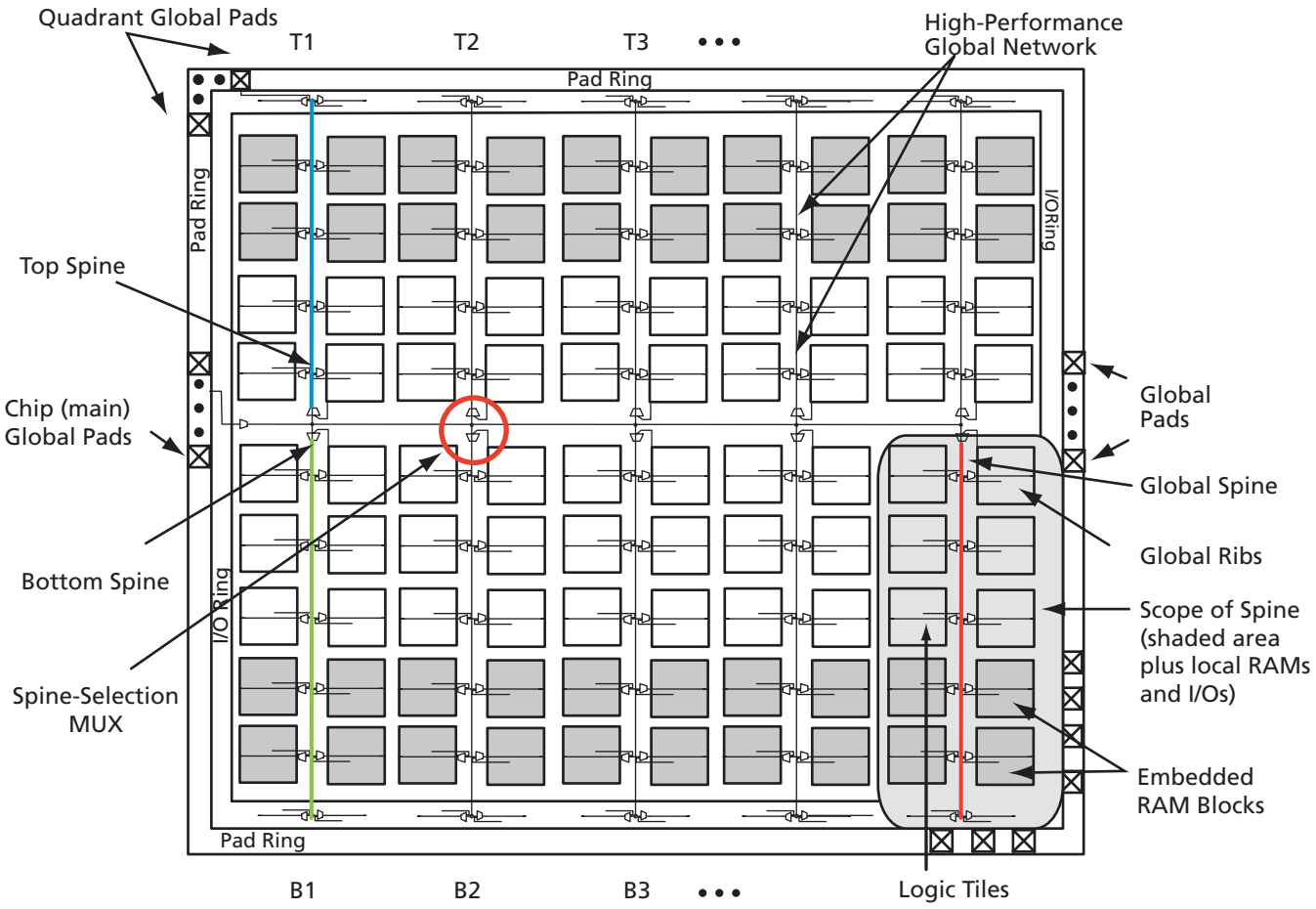


Figure 2-11 • **IGLOO Spines in a Global Clock Tree Network**

Clock Aggregation

Clock aggregation allows for multi-spine clock domains. A MUX tree provides the necessary flexibility to allow long lines or I/Os to access domains of one, two, or four global spines. Signal access to the clock aggregation system is achieved through long-line resources in the central rib, and also through local resources in the north and south ribs, allowing I/Os to feed directly into the clock system. As Figure 2-13 indicates, this access system is contiguous.

There is no break in the middle of the chip for the north and south I/O VersaNet access. This is different from the quadrant clocks located in these ribs, which only reach the middle of the rib.

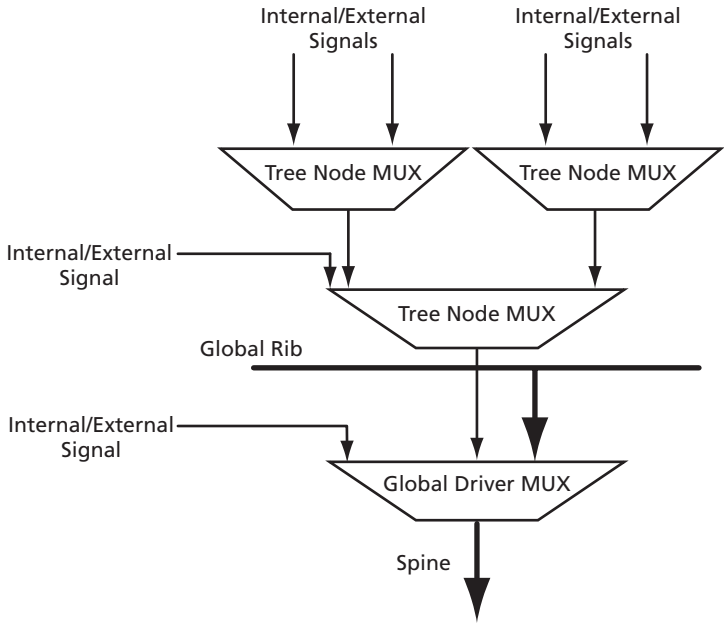


Figure 2-12 • **Spine Selection MUX of Global Tree**

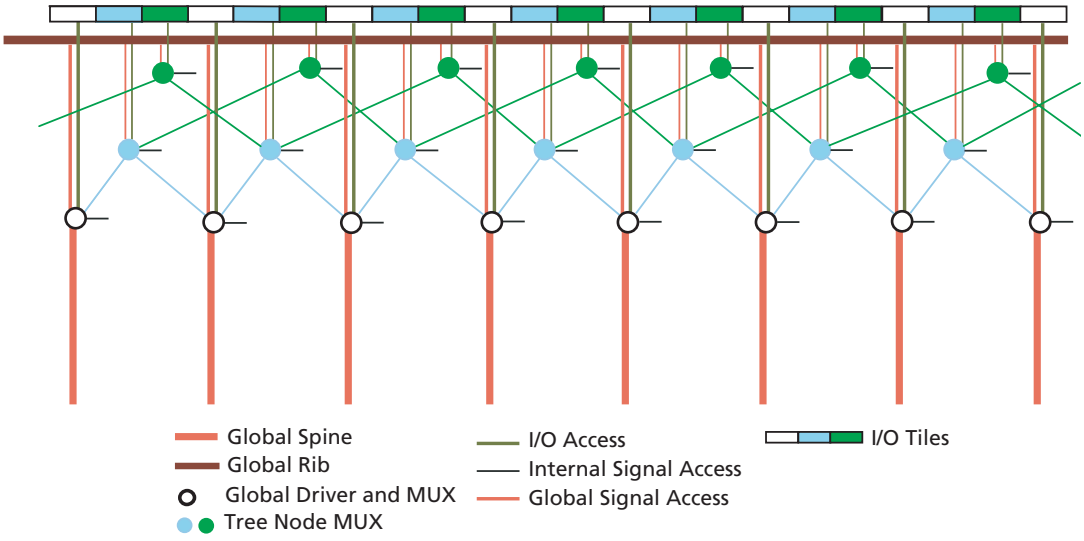


Figure 2-13 • **Clock Aggregation Tree Architecture**

Clock Conditioning Circuits

Overview of Clock Conditioning Circuitry

In IGLOO devices, the CCCs are used to implement frequency division, frequency multiplication, phase shifting, and delay operations.

The CCCs are available in six chip locations—each of the four chip corners and the middle of the east and west chip sides.

Each CCC can implement up to three independent global buffers (with or without programmable delay) or a PLL function (programmable frequency division/multiplication, phase shift, and delays) with up to three global outputs. Unused global outputs of a PLL can be used to implement independent global buffers, up to a maximum of three global outputs for a given CCC.

A global buffer can be placed in any of the three global locations (CLKA-GLA, CLKB-GLB, or CLKC-GLC) of a given CCC.

A PLL macro uses the CLKA CCC input to drive its reference clock. It uses the GLA and, optionally, the GLB and GLC global outputs to drive the global networks. A PLL macro can also drive the YB and YC regular core outputs. The GLB (or GLC) global output cannot be reused if the YB (or YC) output is used (Figure 2-14 on page 2-15). Refer to the "PLL Macro" section on page 2-16 for more information.

Each global buffer, as well as the PLL reference clock, can be driven from one of the following:

- 3 dedicated single-ended I/Os using a hardwired connection
- 2 dedicated differential I/Os using a hardwired connection
- The FPGA core

The CCC block is fully configurable, either via flash configuration bits set in the programming bitstream or through an asynchronous interface. This asynchronous interface is dynamically accessible from inside the IGLOO device to permit parameter changes (such as divide ratios) during device operation. To increase the versatility and flexibility of the clock conditioning system, the CCC configuration is determined either by the user during the design process, with configuration data being stored in flash memory as part of the device programming procedure, or by writing data into a dedicated shift register during normal device operation. This latter mode allows the user to dynamically reconfigure the CCC without the need for core programming. The shift register is accessed through a simple serial interface. Refer to the "CCC Electrical Specifications" section on page 2-19 for more information.

Global Buffers with No Programmable Delays

The CLKBUF and CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS macros are composite macros that include an I/O macro driving a global buffer, which uses a hardwired connection.

The CLKBUF, CLKBUF_LVPECL/LVDS/BLVDS/M-LVDS, and CLKINT macros are pass-through clock sources and do not use the PLL or provide any programmable delay functionality.

The CLKINT macro provides a global buffer function driven by the FPGA core.

Many specific CLKBUF macros support the wide variety of single-ended and differential I/O standards supported by IGLOO devices. The available CLKBUF macros are described in the *Fusion, IGLOO/e and ProASIC3/E Macro Library Guide*.

Global Buffer with Programmable Delay

The CLKDLY macro is a pass-through clock source that does not use the PLL, but provides the ability to delay the clock input using a programmable delay. The CLKDLY macro takes the selected clock input and adds a user-defined delay element. This macro generates an output clock phase shift from the input clock.

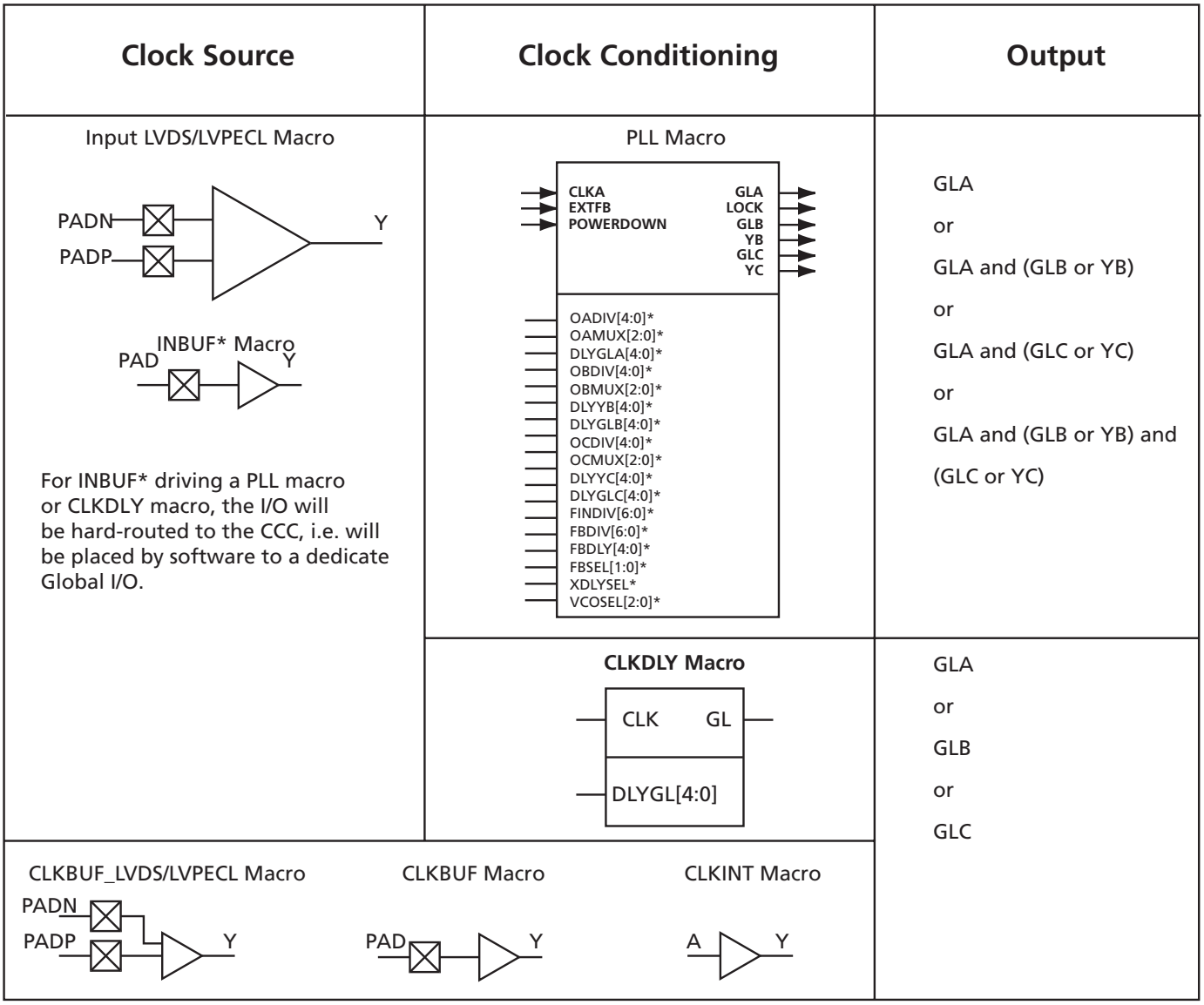
The CLKDLY macro can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

Many specific INBUF macros support the wide variety of single-ended and differential I/O standards supported by the IGLOO family. The available INBUF macros are described in the *Fusion, IGLOO/e and ProASIC3/E Macro Library Guide*.

The CLKDLY macro can be driven directly from the FPGA core.

The CLKDLY macro can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

The visual CLKDLY configuration in the SmartGen part of the Libero IDE and Designer tools allows the user to select the desired amount of delay and configures the delay elements appropriately. SmartGen also allows the user to select the input clock source. SmartGen will automatically instantiate the special macro, PLLINT, when needed.



Notes:

1. *Visit the Actel website for future application notes concerning dynamic PLL reconfiguration. The PLL is only supported on the west center CCC. The AGL030 has no PLL support. Refer to the "PLL Macro" section on page 2-16 for signal descriptions.*
2. *Refer to the Fusion, IGLOO/e and ProASIC3/E Macro Library Guide for more information.*
3. *Many standard-specific INBUF macros (for example, INBUF_LVDS) support the wide variety of single-ended and differential I/O standards supported by the IGLOO family. The available INBUF macros are described in the Fusion, IGLOO/e and ProASIC3/E Macro Library Guide.*

Figure 2-14 • **IGLOO CCC Options**

PLL Macro[1]

The PLL functionality of the clock conditioning block is supported by the PLL macro. Note that the PLL macro reference clock uses the CLKA input of the CCC block, which is only accessible from the global A[0:2] package pins. Refer to Figure 2-15 on page 2-17 for more information.

The PLL macro provides five derived clocks (three independent) from a single reference clock. The PLL macro also provides power-down input and lock output signals. See Figure 2-17 on page 2-18 for more information.

Inputs:

- CLKA: selected clock input
- POWERDOWN (active low): disables PLLs. The default state is Powerdown On (active low).
- EXTFB: allows an external signal to be compared to a reference clock in the PLL core's phase detector

Outputs:

- LOCK: indicates that PLL output has locked on the input reference signal
- GLA, GLB, GLC: outputs to respective global networks
- YB, YC: allows output from the CCC to be routed back to the FPGA core

As previously described, the PLL allows up to five flexible and independently configurable clock outputs. Figure 2-20 on page 2-21 illustrates the various clock output options and delay elements.

As illustrated, the PLL supports three distinct output frequencies from a given input clock. Two of these (GLB and GLC) can be routed to the B and C global network access, respectively, and/or routed to the device core (YB and YC).

There are five delay elements to support phase control on all five outputs (GLA, GLB, GLC, YB, and YC).

There is also a delay element in the feedback loop that can be used to advance the clock relative to the reference clock.

The PLL macro reference clock can be driven by an INBUF* macro to create a composite macro, where the I/O macro drives the global buffer (with programmable delay) using a hardwired connection. In this case, the I/O must be placed in one of the dedicated global I/O locations.

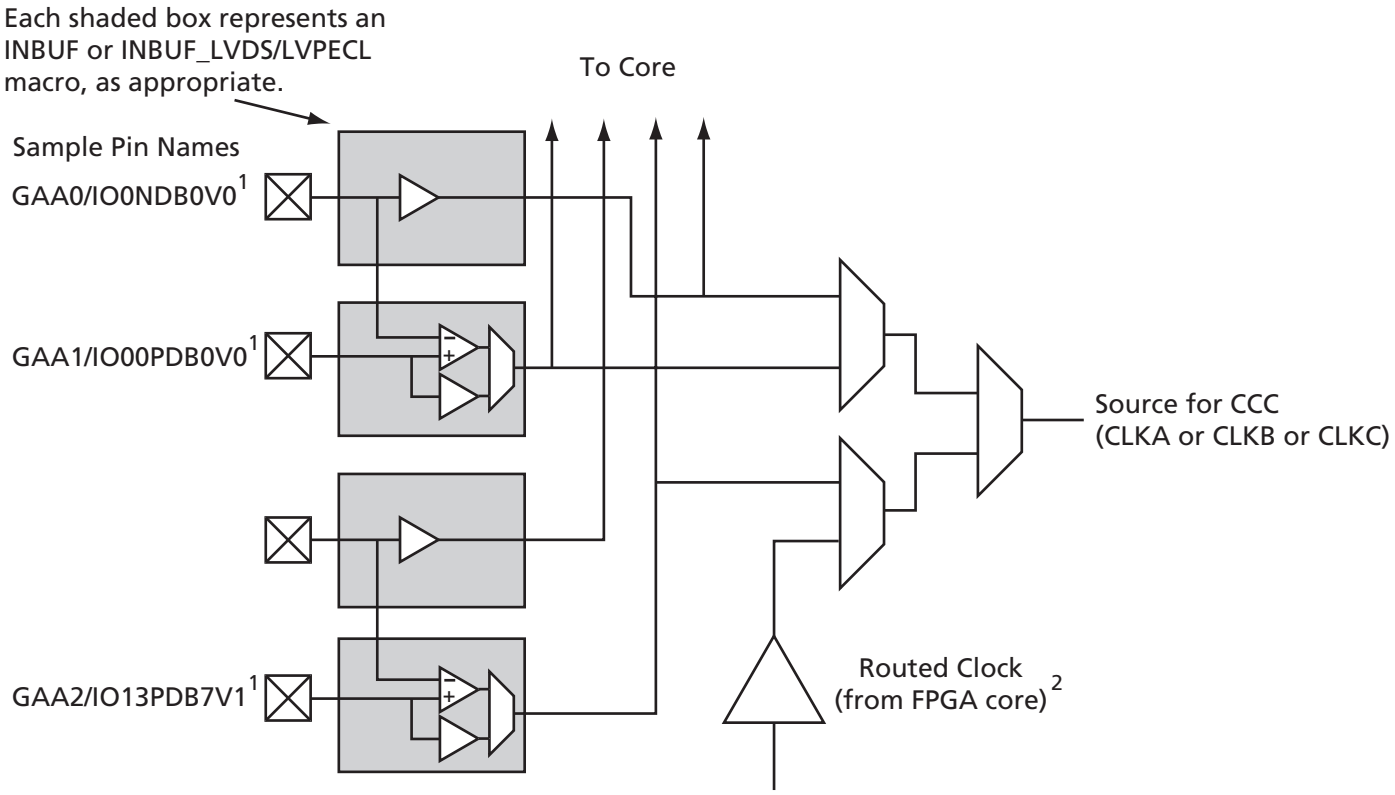
The PLL macro reference clock can be driven directly from the FPGA core.

The PLL macro reference clock can also be driven from an I/O that is routed through the FPGA regular routing fabric. In this case, users must instantiate a special macro, PLLINT, to differentiate from the hardwired I/O connection described earlier.

During power-up, the PLL outputs will toggle around the maximum frequency of the VCO gear selected. Toggle frequencies can range from 40 MHz to 250 MHz. This will continue as long as the clock input (CLKA) is constant (HIGH or LOW). This can be prevented by LOW assertion of the POWERDOWN signal.

The visual PLL configuration in SmartGen, part of the Libero IDE and Designer tools, will derive the necessary internal divider ratios based on the input frequency and desired output frequencies selected by the user. SmartGen also allows the user to select the various delays and phase shift values necessary to adjust the phases between the reference clock (CLKA) and the derived clocks (GLA, GLB, GLC, YB, and YC). SmartGen also allows the user to select the input clock source. SmartGen automatically instantiates the special macro, PLLINT, when needed.

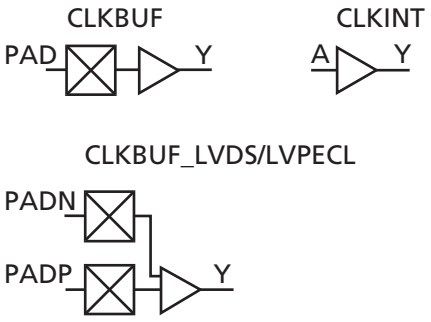
1. *The AGL030 device has no CCC, and thus does not include a PLL.*



Notes:

1. *Represents the global input pins. Globals have direct access to the clock conditioning block and are not routed via the FPGA fabric. Refer to the "User I/O Naming Convention" section on page 2-56 for more information.*
2. *Instantiate the routed clock source input as follows:*
   a) Connect the output of a logic element to the clock input of a PLL, CLKDLY, or CLKINT macro.
   b) Do not place a clock source I/O (INBUF or INBUF_LVPECL/LVDS/BLVDS/M-LVDS/DDR) in a relevant global pin location.
3. *LVDS-, BLVDS-, and M-LVDS–based clock sources are only available on AGL250 through AGL1000 devices. AGL030, AGL060, and AGL125 support single-ended clock sources only. The AGL030 device does not contain a PLL.*

Figure 2-15 • **Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT**



Note: *The AGL030 device does not support this feature.*

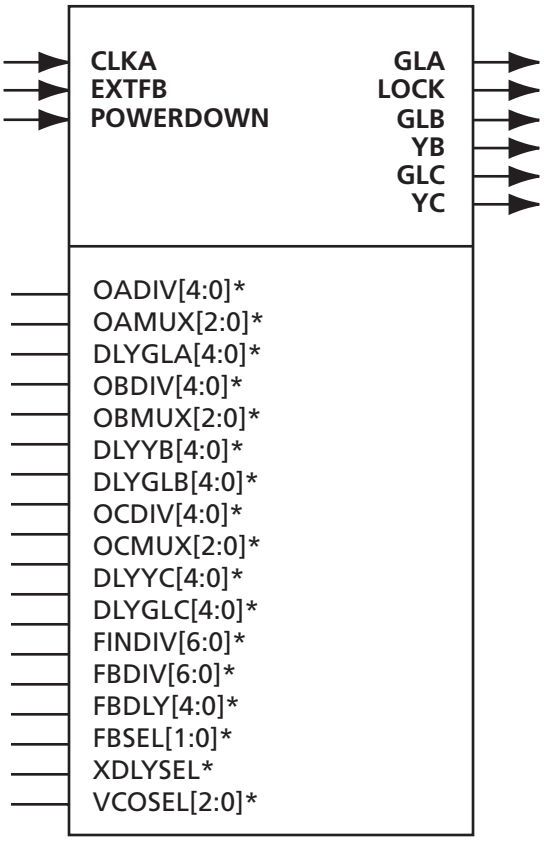
Figure 2-16 • **CLKBUF and CLKINT**

Table 2-3 • **Available IGLOO I/O Standards within CLKBUF and CLKBUF_LVDS/LVPECL Macros**

CLKBUF Macros
CLKBUF_LVCMOS5
CLKBUF_LVCMOS33[1]
CLKBUF_LVCMOS18
CLKBUF_LVCMOS15
CLKBUF_PCI
CLKBUF_LVDS[2]
CLKBUF_LVPECL

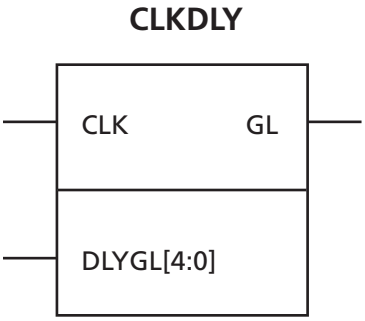
Notes:

1. *By default, the CLKBUF macro uses the 3.3 V LVTTL I/O technology. For more details, refer to the Fusion, IGLOO/e and ProASIC3/E Macro Library Guide.*
2. *BLVDS and M-LVDS standards are supported by CLKBUF_LVDS.*



Note: **Visit the Actel website for future application notes concerning the dynamic PLL.*
The AGL030 device does not contain a PLL.

Figure 2-17 • **CCC/PLL Macro**



Note: *The CLKDLY macro uses programmable delay element type 2.*

Figure 2-18 • **CLKDLY**

CCC Electrical Specifications

Timing Characteristics

Table 2-4 • **IGLOO CCC/PLL Specification**
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		250	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		250	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			330		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		1.00		1.20	%
24 MHz to 100 MHz		1.75		2.00	%
100 MHz to 250 MHz		2.50		5.60	%
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		0.97		11.3	ns
Delay Range in Block: Programmable Delay 2 [1, 2]		0.025		11.3	ns
Delay Range in Block: Fixed Delay [1, 2]			3		ns

Notes:

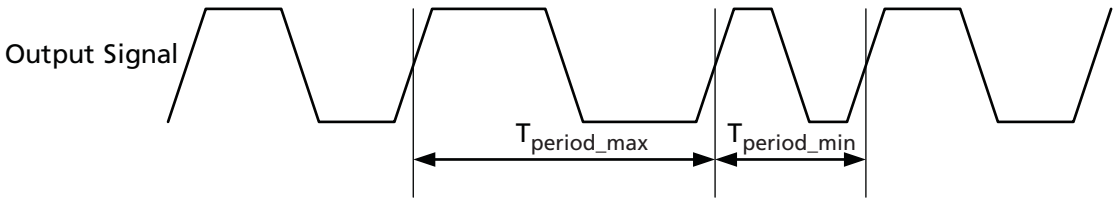
1. *This delay is a function of voltage and temperature. See Table 3-6 on page 3-6 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.5 V*
3. *The AGL030 device does not support PLL.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*

Table 2-5 • **IGLOO CCC/PLL Specification For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter		Min.	Typ.	Max.	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}		1.5		200	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}		0.75		200	MHz
Delay Increments in Programmable Delay Blocks [1, 2]			530		ps
Number of Programmable Values in Each Programmable Delay Block				32	
Input Period Jitter				1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}		Max Peak-to-Peak Period Jitter			
		1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz		1.00		1.20	%
24 MHz to 100 MHz		1.75		2.00	%
100 MHz to 250 MHz		2.50		5.60	%
Acquisition Time	LockControl = 0			300	µs
	LockControl = 1			6.0	ms
Tracking Jitter	LockControl = 0			1.6	ns
	LockControl = 1			0.8	ns
Output Duty Cycle		48.5		51.5	%
Delay Range in Block: Programmable Delay 1 [1, 2]		1.74		18.2	ns
Delay Range in Block: Programmable Delay 2 [1, 2]		0.025		18.2	ns
Delay Range in Block: Fixed Delay [1, 2]			4.5		ns

Notes:

1. *This delay is a function of voltage and temperature. See Table 3-7 on page 3-6 for deratings.*
2. *T_J = 25°C, V_{CC} = 1.2 V*
3. *The AGL030 device does not support PLL.*
4. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by period jitter parameter.*



Note: *Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.*

Figure 2-19 • **Peak-to-Peak Jitter Definition**

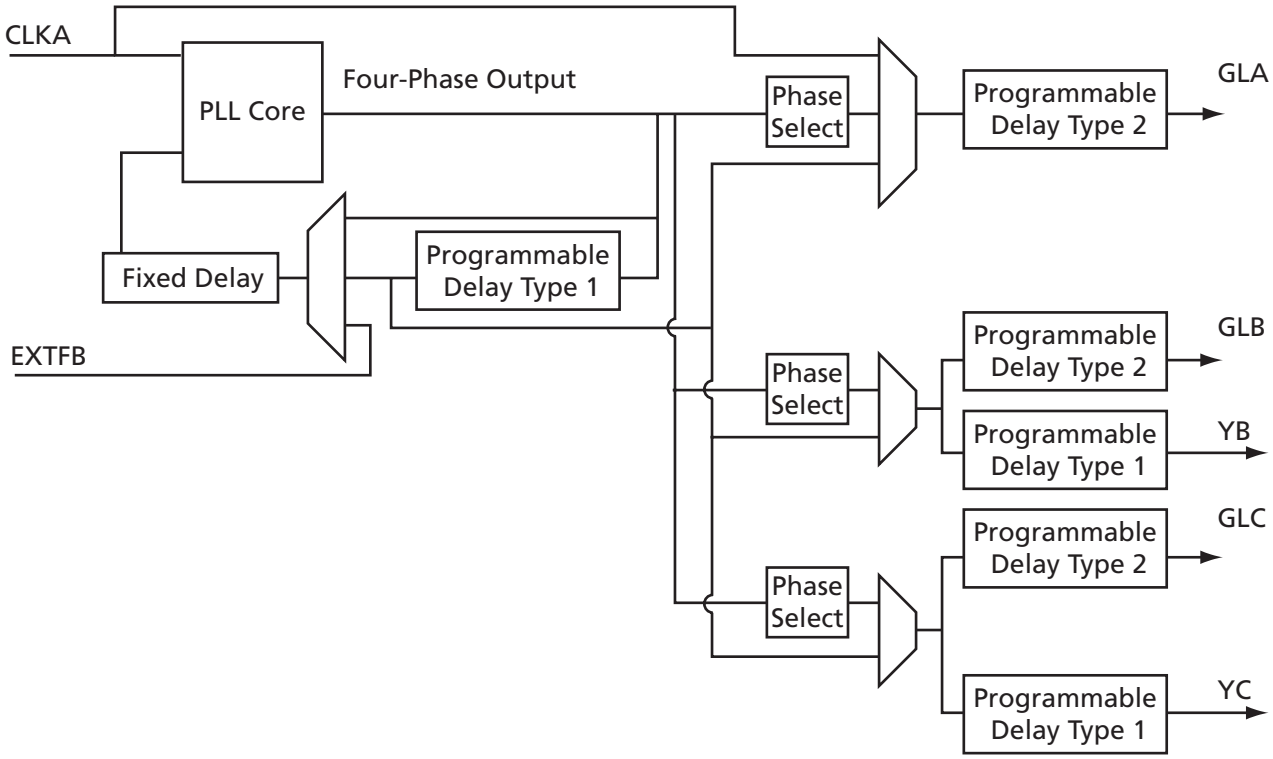
CCC Physical Implementation[2]

The CCC is composed of the following (Figure 2-20):

- PLL core
- 3 phase selectors
- 6 programmable delays and 1 fixed delay that advances/delays phase
- 5 programmable frequency dividers that provide frequency multiplication/division (not shown in Figure 2-20 because they are automatically configured based on the user's required frequencies)
- 1 dynamic shift register that provides CCC dynamic reconfiguration capability

CCC Programming

The CCC block is fully configurable, either via static flash configuration bits in the array, set by the user in the programming bitstream, or through an asynchronous dedicated shift register dynamically accessible from inside the IGLOO device. The dedicated shift register permits changes in parameters such as PLL divide ratios and delays during device operation. This latter mode allows the user to dynamically reconfigure the PLL without the need for core programming. The register file is accessed through a simple serial interface.



Notes:

1. *Refer to the "Clock Conditioning Circuits" section on page 2-14 and Table 2-4 on page 2-19 and Table 2-5 on page 2-20 for signal descriptions.*
2. *Clock divider and clock multiplier blocks are not shown in this figure or in SmartGen. They are automatically configured based on the user's required frequencies.*

Figure 2-20 • **IGLOO PLL Block**

2. *The AGL030 device does not contain a PLL.*

Nonvolatile Memory (NVM)

Overview of User Nonvolatile FlashROM

IGLOO devices have 1 kbit of on-chip nonvolatile flash memory that can be read from the FPGA core fabric. The FlashROM is arranged in 8 banks of 128 bits during programming. The 128 bits in each bank are addressable as 16 bytes during the read back of the FlashROM from the FPGA core (Figure 2-21).

The FlashROM can only be programmed via the IEEE 1532 JTAG port. It cannot be programmed directly from the FPGA core. When programming, each of the eight 128-bit banks can be selectively reprogrammed. The FlashROM can only be reprogrammed on a bank boundary. Programming involves an automatic, on-chip bank erase prior to reprogramming the bank. The FlashROM supports synchronous read. The address is latched on the rising edge of the clock, and the new output data is stable after the falling edge of the same clock cycle. Refer to Figure 3-43 on page 3-102 for the timing diagram. The FlashROM can be read on byte boundaries. The upper three bits of the FlashROM address from the FPGA core define the bank being accessed. The lower four bits of the FlashROM address from the FPGA core define which of the 16 bytes in the bank is being accessed.

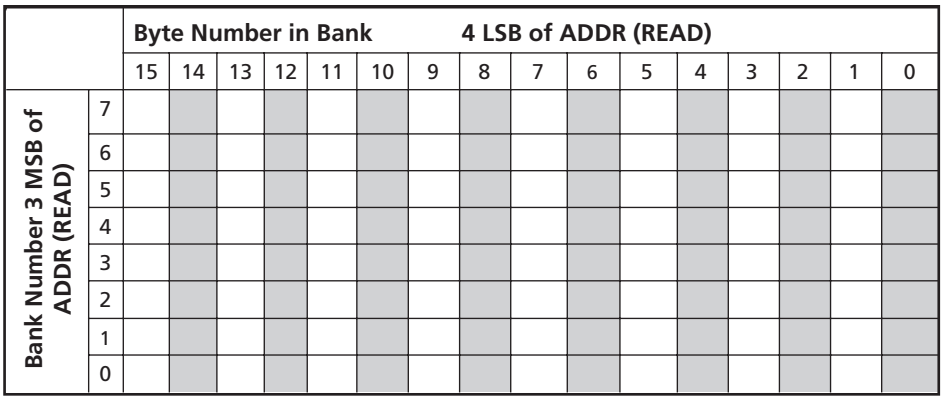


Figure 2-21 • **FlashROM Architecture**

SRAM and FIFO[3]

IGLOO devices (AGL250, AGL600, and AGL1000) have embedded SRAM blocks along their north and south sides; AGL060 and AGL125 devices have embedded SRAM blocks on the north side only. The AGL030 does not include SRAM or FIFO. To meet the needs of high-performance designs, the memory blocks operate strictly in synchronous mode for both read and write operations. The read and write clocks are completely independent, and each may operate at any desired frequency up to 250 MHz.

- 4k×1, 2k×2, 1k×4, 512×9 (dual-port RAM—2 read, 2 write or 1 read, 1 write)
- 512×9, 256×18 (2-port RAM—1 read and 1 write)
- Sync write, sync pipelined / nonpipelined read

The IGLOO memory block includes dedicated FIFO control logic to generate internal addresses and external flag logic (FULL, EMPTY, AFULL, AEMPTY). Block diagrams of the memory modules are illustrated in Figure 2-22 on page 2-24.

Simultaneous dual-port read/write and write/write operations at the same address are allowed when certain timing requirements are met.

During RAM operation, addresses are sourced by the user logic and the FIFO controller is ignored. In FIFO mode, the internal addresses are generated by the FIFO controller and routed to the RAM array by internal MUXes. Refer to Figure 2-23 on page 2-25 for more information about the implementation of the embedded FIFO controller.

The IGLOO architecture enables the read and write sizes of RAMs to be organized independently, allowing for bus conversion. For example, the write side size can be set to 256×18 and the read size to 512×9.

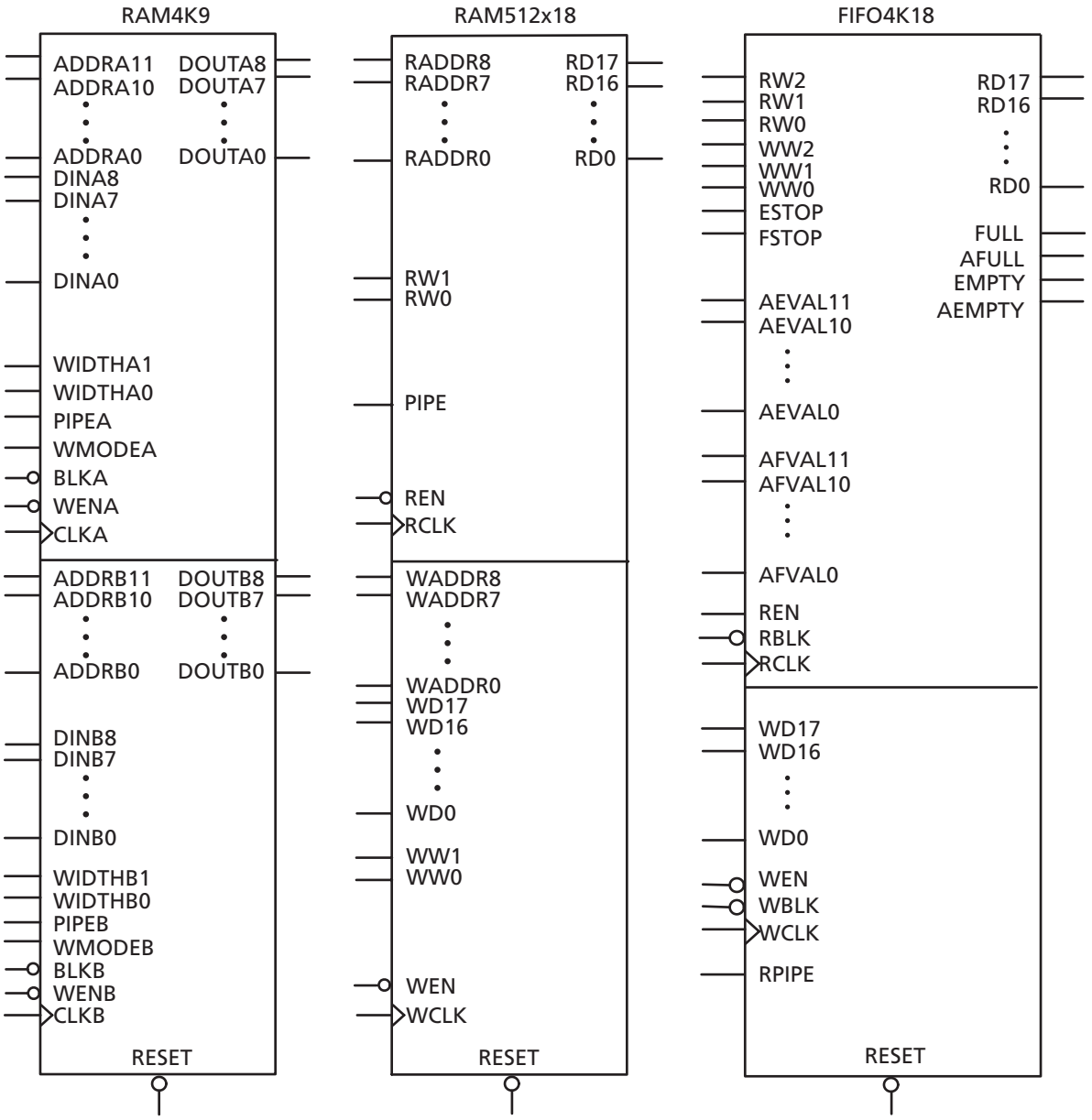
Both the write width and read width for the RAM blocks can be specified independently with the WW (write width) and RW (read width) pins. The different D×W configurations are: 256×18, 512×9, 1k×4, 2k×2, and 4k×1.

Refer to the allowable RW and WW values supported for each of the RAM macro types in Table 2-6 on page 2-26.

When widths of one, two, or four are selected, the ninth bit is unused. For example, when writing nine-bit values and reading four-bit values, only the first four bits and the second four bits of each nine-bit value are addressable for read operations. The ninth bit is not accessible.

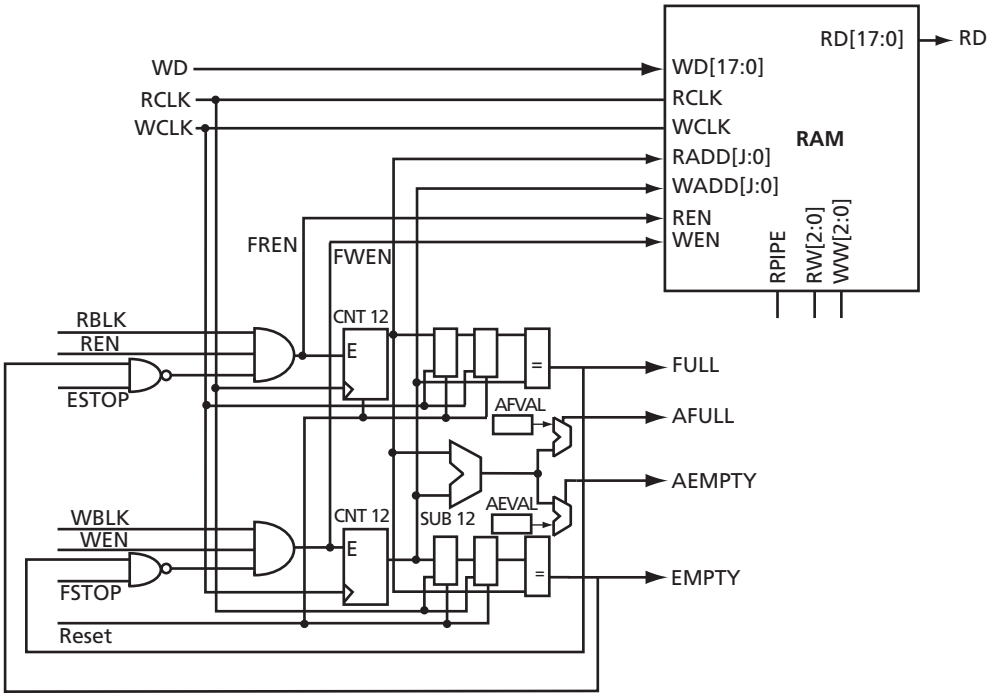
Conversely, when writing four-bit values and reading nine-bit values, the ninth bit of a read operation will be undefined. The RAM blocks employ little-endian byte order for read and write operations.

3. The AGL030 device does not support SRAM or FIFO.



Note: *The AGL030 device does not support SRAM or FIFO.*

Figure 2-22 • **Supported Basic RAM Macros**



Note: *The AGL030 device does not support SRAM or FIFO.*

Figure 2-23 • **IGLOO RAM Block with Embedded FIFO Controller**

Signal Descriptions for RAM4K9[4]

The following signals are used to configure the RAM4K9 memory element:

WIDTHA and WIDTHB

These signals enable the RAM to be configured in one of four allowable aspect ratios (Table 2-6).

Table 2-6 • **Allowable Aspect Ratio Settings for WIDTHA[1:0]**

WIDTHA[1:0]	WIDTHB[1:0]	D×W
00	00	4k×1
01	01	2k×2
10	10	1k×4
11	11	512×9

Note: *The aspect ratio settings are constant and cannot be changed on the fly.*

BLKA and BLKB

These signals are active low and will enable the respective ports when asserted. When a BLKx signal is deasserted, that port's outputs hold the previous value.

WENA and WENB

These signals switch the RAM between read and write modes for the respective ports. A LOW on these signals indicates a write operation, and a HIGH indicates a read.

CLKA and CLKB

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

PIPEA and PIPEB

These signals are used to specify pipelined read on the output. A LOW on PIPEA or PIPEB indicates a nonpipelined read, and the data appears on the corresponding output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the corresponding output in the next clock cycle.

WMODEA and WMODEB

These signals are used to configure the behavior of the output when the RAM is in write mode. A LOW on these signals makes the output retain data from the previous read. A HIGH indicates pass-through behavior, wherein the data being written will appear immediately on the output. This signal is overridden when the RAM is being read.

RESET

This active low signal resets the control logic, forces the output hold state registers to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-147 on page 3-93 for the specifications.

ADDRA and ADDRB

These are used as read or write addresses, and they are 12 bits wide. When a depth of less than 4 k is specified, the unused high-order bits must be grounded (Table 2-7).

Table 2-7 • **Address Pins Unused/Used for Various Supported Bus Widths**

	ADDRx	
D×W	Unused	Used
4k×1	None	[11:0]
2k×2	[11]	[10:0]
1k×4	[11:10]	[9:0]
512×9	[11:9]	[8:0]

Note: *The "x" in ADDRx implies A or B.*

DINA and DINB

These are the input data signals, and they are nine bits wide. Not all nine bits are valid in all configurations. When a data width less than nine is specified, unused high-order signals must be grounded (Table 2-8).

DOUTA and DOUTB

These are the nine-bit output data signals. Not all nine bits are valid in all configurations. As with DINA and DINB, high-order bits may not be used (Table 2-8). The output data on unused pins is undefined.

Table 2-8 • **Unused/Used Input and Output Data Pins for Various Supported Bus Widths**

	DINx/DOUTx	
D×W	Unused	Used
4k×1	[8:1]	[0]
2k×2	[8:2]	[1:0]
1k×4	[8:4]	[3:0]
512×9	None	[8:0]

Note: *The "x" in DINx or DOUTx implies A or B.*

4. The AGL030 device does not support SRAM or FIFO.

Signal Descriptions for RAM512X18[5]

RAM512X18 has slightly different behavior than RAM4K9, as it has dedicated read and write ports.

WW and RW

These signals enable the RAM to be configured in one of the two allowable aspect ratios (Table 2-9).

Table 2-9 • **Aspect Ratio Settings for WW[1:0]**

WW[1:0]	RW[1:0]	D×W
01	01	512×9
10	10	256×18
00, 11	00, 11	Reserved

WD and RD

These are the input and output data signals, and they are 18 bits wide. When a 512×9 aspect ratio is used for write, WD[17:9] are unused and must be grounded. If this aspect ratio is used for read, RD[17:9] are undefined.

WADDR and RADDR

These are read and write addresses, and they are nine bits wide. When the 256×18 aspect ratio is used for write or read, WADDR[8] or RADDR[8] are unused and must be grounded.

WCLK and RCLK

These signals are the write and read clocks, respectively. They can be clocked on the rising or falling edge of WCLK and RCLK.

WEN and REN

These signals are the write and read enables, respectively. They are both active low by default. These signals can be configured as active high.

RESET

This active low signal resets the control logic, forces the output hold state registers to zero, disables reads and writes from the SRAM block, and clears the data hold registers when asserted. It does not reset the contents of the memory array.

While the RESET signal is active, read and write operations are disabled. As with any asynchronous reset signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-148 on page 3-94 for the specifications.

PIPE

This signal is used to specify pipelined read on the output. A LOW on PIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

Clocking

The dual-port SRAM blocks are only clocked on the rising edge. SmartGen allows falling-edge-triggered clocks by adding inverters to the netlist, hence achieving dual-port SRAM blocks that are clocked on either edge (rising or falling). For dual-port SRAM, each port can be clocked on either edge and/or by separate clocks by port.

IGLOO devices support inversion (bubble pushing) throughout the FPGA architecture, including the clock input to the SRAM modules. Inversions added to the SRAM clock pin on the design schematic or in the HDL code will be automatically accounted for during design compile without incurring additional delay in the clock path.

The two-port SRAM can be clocked on the rising or falling edge of WCLK and RCLK.

If negative-edge RAM and FIFO clocking is selected for memory macros, clock edge inversion management (bubble pushing) is automatically used within the IGLOO development tools, without performance penalty.

Modes of Operation

There are two read modes and one write mode:

- Read Nonpipelined (synchronous—1 clock edge): In the standard read mode, new data is driven onto the RD bus in the same clock cycle following RA and REN valid. The read address is registered on the read port clock active edge, and data appears at RD after the RAM access time. Setting PIPE to OFF enables this mode.
- Read Pipelined (synchronous—2 clock edges): The pipelined mode incurs an additional clock delay from address to data but enables operation at a much higher frequency. The read address is registered on the read port active clock edge, and the read data is registered and appears at RD after the second read clock edge. Setting PIPE to ON enables this mode.
- Write (synchronous—1 clock edge): On the write clock active edge, the write data is written into the SRAM at the write address when WEN is HIGH. The setup times of the write address, write enables, and write data are minimal with respect to the write clock. Write and read transfers are described with timing requirements in the "DDR Module Specifications" section on page 3-71.

5. *The AGL030 device does not support SRAM or FIFO.*

RAM Initialization

Each SRAM block can be individually initialized on power-up by means of the JTAG port using the UJTAG mechanism (refer to the "JTAG 1532" section on page 2-63). The shift register for a target block can be selected and loaded with the proper bit configuration to enable serial loading. The 4,608 bits of data can be loaded in a single operation.

Signal Descriptions for FIFO4K18[6]

The following signals are used to configure the FIFO4K18 memory element:

WW and RW

These signals enable the FIFO to be configured in one of the five allowable aspect ratios (Table 2-10).

Table 2-10 • **Aspect Ratio Settings for WW[2:0]**

WW[2:0]	RW[2:0]	D×W
000	000	4k×1
001	001	2k×2
010	010	1k×4
011	011	512×9
100	100	256×18
101, 110, 111	101, 110, 111	Reserved

WBLK and RBLK

These signals are active low and will enable the respective ports when LOW. When the RBLK signal is HIGH, that port's outputs hold the previous value.

WEN and REN

Read and write enables. WEN is active low and REN is active high by default. These signals can be configured as active high or low.

WCLK and RCLK

These are the clock signals for the synchronous read and write operations. These can be driven independently or with the same driver.

RPIPE

This signal is used to specify pipelined read on the output. A LOW on RPIPE indicates a nonpipelined read, and the data appears on the output in the same clock cycle. A HIGH indicates a pipelined read, and data appears on the output in the next clock cycle.

RESET

This active low signal resets the control logic and forces the output hold state registers to zero when asserted. It does not reset the contents of the memory array (Table 2-11).

While the RESET signal is active, read and write operations are disabled. As with any asynchronous RESET signal, care must be taken not to assert it too close to the edges of active read and write clocks. Refer to the tables beginning with Table 3-151 on page 3-100 for the specifications.

WD

This is the input data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. When a data width less than 18 is specified, unused higher-order signals must be grounded (Table 2-11).

RD

This is the output data bus and is 18 bits wide. Not all 18 bits are valid in all configurations. Like the WD bus, high-order bits become unusable if the data width is less than 18. The output data on unused pins is undefined (Table 2-11).

Table 2-11 • **Input Data Signal Usage for Different Aspect Ratios**

D×W	WD/RD Unused
4k×1	WD[17:1], RD[17:1]
2k×2	WD[17:2], RD[17:2]
1k×4	WD[17:4], RD[17:4]
512×9	WD[17:9], RD[17:9]
256×18	–

ESTOP, FSTOP

ESTOP is used to stop the FIFO read counter from further counting once the FIFO is empty (i.e., the EMPTY flag goes HIGH). A HIGH on this signal inhibits the counting.

FSTOP is used to stop the FIFO write counter from further counting once the FIFO is full (i.e., the FULL flag goes HIGH). A HIGH on this signal inhibits the counting.

For more information on these signals, refer to the "ESTOP and FSTOP Usage" section on page 2-29.

FULL, EMPTY

When the FIFO is full and no more data can be written, the FULL flag asserts HIGH. The FULL flag is synchronous to WCLK to inhibit writing immediately upon detection of a full condition and to prevent overflows. Since the write address is compared to a resynchronized (and thus time-delayed) version of the read address, the FULL flag will remain asserted until two WCLK active edges after a read operation eliminates the full condition.

When the FIFO is empty and no more data can be read, the EMPTY flag asserts HIGH. The EMPTY flag is synchronous to RCLK to inhibit reading immediately upon detection of an empty condition and to prevent

6. *The AGL030 device does not support SRAM or FIFO.*

underflows. Since the read address is compared to a resynchronized (and thus time-delayed) version of the write address, the EMPTY flag will remain asserted until two RCLK active edges after a write operation removes the empty condition.

For more information on these signals, refer to the "FIFO Flag Usage Considerations" section.

AFULL, AEMPTY

These are programmable flags and will be asserted on the threshold specified by AFVAL and AEVAL, respectively.

When the number of words stored in the FIFO reaches the amount specified by AEVAL while reading, the AEMPTY output will go HIGH. Likewise, when the number of words stored in the FIFO reaches the amount specified by AFVAL while writing, the AFULL output will go HIGH.

AFVAL, AEVAL

The AEVAL and AFVAL pins are used to specify the almost-empty and almost-full threshold values. They are 12-bit signals. For more information on these signals, refer to the "FIFO Flag Usage Considerations" section.

ESTOP and FSTOP Usage

The ESTOP pin is used to stop the read counter from counting any further once the FIFO is empty (i.e., the EMPTY flag goes HIGH). Likewise, the FSTOP pin is used to stop the write counter from counting any further once the FIFO is full (i.e., the FULL flag goes HIGH).

The FIFO counters in the IGLOO device start the count at zero, reach the maximum depth for the configuration (e.g., 511 for a 512×9 configuration), and then restart at zero. An example application for ESTOP, where the read counter keeps counting, would be writing to the FIFO once and reading the same content over and over without doing another write.

FIFO Flag Usage Considerations

The AEVAL and AFVAL pins are used to specify the 12-bit AEMPTY and AFULL threshold values. The FIFO contains separate 12-bit write address (WADDR) and read address (RADDR) counters. WADDR is incremented every time a write operation is performed, and RADDR is incremented every time a read operation is performed. Whenever the difference between WADDR and RADDR is greater than or equal to AFVAL, the AFULL output is asserted. Likewise, whenever the difference between WADDR and RADDR is less than or equal to AEVAL, the AEMPTY output is asserted. To handle different read and write aspect ratios, AFVAL and AEVAL are expressed in terms of total data bits instead of total data words. When users specify AFVAL and AEVAL in terms of read or write words, the SmartGen tool translates them into bit addresses and configures these signals automatically. SmartGen configures the AFULL flag to assert when the write address exceeds the read address by at least a predefined value. In a 2k×8 FIFO, for example, a value of 1,500 for AFVAL means that the AFULL flag will be asserted after a write when the difference between the write address and the read address reaches 1,500 (there have been at least 1,500 more writes than reads). It will stay asserted until the difference between the write and read addresses drops below 1,500.

The AEMPTY flag is asserted when the difference between the write address and the read address is less than a predefined value. In the example above, a value of 200 for AEVAL means that the AEMPTY flag will be asserted when a read causes the difference between the write address and the read address to drop to 200. It will stay asserted until that difference rises above 200. Note that the FIFO can be configured with different read and write widths; in this case, the AFVAL setting is based on the number of write data entries, and the AEVAL setting is based on the number of read data entries. For aspect ratios of 512×9 and 256×18, only 4,096 bits can be addressed by the 12 bits of AFVAL and AEVAL. The number of words must be multiplied by 8 and 16 instead of 9 and 18. The SmartGen tool automatically uses the proper values. To avoid halfwords being written or read, which could happen if different read and write aspect ratios were specified, the FIFO will assert FULL or EMPTY as soon as at least one word cannot be written or read. For example, if a two-bit word is written and a four-bit word is being read, the FIFO will remain in the empty state when the first word is written. This occurs even if the FIFO is not completely empty, because in this case, a complete word cannot be read. The same is applicable in the full state. If a four-bit word is written and a two-bit word is read, the FIFO is full and one word is read. The FULL flag will remain asserted because a complete word cannot be written at this point.

Advanced I/Os

Introduction

IGLOO devices feature a flexible I/O structure, supporting a range of mixed voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V) through a bank-selectable voltage. Table 2-12, Table 2-13, and Table 2-22 on page 2-47 show the voltages and the compatible I/O standards. I/Os provide programmable slew rates (except AGL030), drive strengths, and weak pull-up and pull-down circuits. 3.3 V PCI and 3.3 V PCI-X are 5 V–tolerant. See the "5 V Input Tolerance" section on page 2-40 for possible implementations of 5 V tolerance.

All I/Os are in a known state during power-up, and any power-up sequence is allowed without current impact. Refer to the "I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)" section on page 3-4 for more information. During power-up, before reaching activation levels, the I/O input and output buffers are disabled while the weak pull-up is enabled. Activation levels are described in Table 3-2 on page 3-2.

I/O Tile

The IGLOO I/O tile provides a flexible, programmable structure for implementing a large number of I/O standards. In addition, the registers available in the I/O tile in selected I/O banks can be used to support high-performance register inputs and outputs, with register enable if desired (Figure 2-24 on page 2-34). The registers can also be used to support the JESD-79C Double Data Rate (DDR) standard within the I/O structure (see the "Double Data Rate (DDR) Support" section on page 2-35 for more information).

As depicted in Figure 2-24 on page 2-34, all I/O registers share one CLR port. The output register and output enable register share one CLK port. Refer to the "I/O Registers" section on page 2-34 for more information.

I/O Banks and I/O Standards Compatibility

I/Os are grouped into I/O voltage banks. There are four I/O banks on the AGL250 through AGL1000. The AGL030, AGL060, and AGL125 have two I/O banks. Each I/O voltage bank has dedicated I/O supply and ground voltages (VMV/GNDQ for input buffers and V_{CCI}/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. Table 2-13 shows the required voltage compatibility values for each of these voltages.

For more information about I/O and global assignments to I/O banks in a device, refer to the specific pin table for the device in the "Package Pin Assignments" section on page 4-1 and the "User I/O Naming Convention" section on page 2-56.

I/O standards are compatible if their V_{CCI} and VMV values are identical. VMV and GNDQ are "quiet" input power supply pins and are not used on AGL030.

In the AGL030 device, all inputs and disabled outputs are voltage tolerant up to 3.3 V.

Table 2-12 • **IGLOO Supported I/O Standards**

	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000
Single-Ended						
LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V / 1.8 V / 1.5 V, LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
3.3 V PCI/PCI-X	–	✓	✓	✓	✓	✓
Differential						
LVPECL, LVDS, BLVDS, M-LVDS	–	–	–	✓	✓	✓

Table 2-13 • **V_{CCI} Voltages and Compatible IGLOO Standards**

V_{CCI} and VMV (typical)	**Compatible Standards**
3.3 V	LVTTL/LVCMOS 3.3, PCI 3.3, PCI-X 3.3 LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, LVDS, BLVDS, M-LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5

I/O Banks

IGLOO I/Os are divided into multiple technology banks. The IGLOO family has two to four banks, and the number of banks is device-dependent.

AGL030, AGL060, and AGL125 support two I/O banks, whereas AGL600 and AGL1000 support four I/O banks. The bank types have different characteristics, such as drive strength, the I/O standards supported, and timing and power differences.

There are three types of banks in the IGLOO family: Advanced I/O banks, Standard+ I/O banks, and Standard I/O banks.

Advanced I/O banks offer single-ended and differential capabilities. These banks are available on the east and west sides of AGL250, AGL600, and AGL1000 devices.

Standard+ I/O banks offer LVTTL/LVCMOS and PCI single-ended I/O standards. These banks are available on the north and south sides of AGL250, AGL600, and AGL1000, and on all sides of AGL125 and AGL060.

Standard I/O banks offer LVTTL/LVCMOS single-ended I/O standards. These banks are available on all sides of AGL030 devices.

Table 2-14 shows the I/O bank types, devices and bank locations supported, drive strength, slew rate control, and supported standards.

Table 2-14 • **IGLOO Bank Types Definition and Differences**

I/O Bank Type	Device and Bank Location	Drive Strength	Slew Rate Control	I/O Standards Supported		
				LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, BLVDS, M-LVDS
Standard	AGL030 (all banks)	Refer to Table 2-24 on page 2-48.	Yes	✓	Not Supported	Not Supported
Standard+	AGL060 and AGL125 (all banks)	Refer to Table 2-25 on page 2-49.	Yes	✓	✓	Not Supported
	North and south banks of AGL250 to AGL1000 devices	Refer to Table 2-25 on page 2-49.	Yes	✓	✓	Not Supported
Advanced	East and west banks of AGL250 to AGL1000 devices	Refer to Table 2-26 on page 2-49.	Yes	✓	✓	✓

Features Supported on Every I/O

Table 2-15 lists all features supported by transmitter/receiver for single-ended and differential I/Os.

Table 2-15 • **IGLOO I/O Features**

Feature	Description
Single-Ended Transmitter Features	• Hot insertion: AGL030: Hot insertion in every mode All other IGLOO devices: No hot insertion • Weak pull-up and pull-down • 2 slew rates (except AGL030) • Skew between output buffer enable/disable time: 2 ns delay on rising edge and 0 ns delay on falling edge (see "Selectable Skew between Output Buffer Enable and Disable Times" on page 2-45 for more information) • 3 drive strengths • 5 V–tolerant receiver ("5 V Output Tolerance" section on page 2-44) • LVTTL/LVCMOS 3.3 V outputs compatible with 5 V TTL inputs ("5 V Output Tolerance" section on page 2-44) • High performance (Table 2-16)
Single-Ended Receiver Features	• Electrostatic discharge (ESD) protection • High performance (Table 2-16) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output-induced noise.
Differential Receiver Features (AGL250 through AGL1000)	• ESD protection • High performance (Table 2-16) • Separate ground plane for GNDQ pin and power plane for VMV pin are used for input buffer to reduce output-induced noise.
CMOS-Style LVDS, BLVDS, M-LVDS, or LVPECL Transmitter	• Two I/Os and external resistors are used to provide a CMOS-style LVDS, DDR LVDS, BLVDS, and M-LVDS/LVPECL transmitter solution. • Weak pull-up and pull-down • High slew rate

Table 2-16 • **Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO Devices (maximum drive strength and high slew selected)**

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	200 MHz
LVCMOS 2.5 V	250 MHz
LVCMOS 1.8 V	200 MHz
LVCMOS 1.5 V	130 MHz
PCI	200 MHz
PCI-X	200 MHz
LVDS	350 MHz
LVPECL	350 MHz

Table 2-17 • **IGLOO Maximum I/O Frequency for Single-Ended and Differential I/Os in All Bank Types (maximum drive strength and high slew selected)—for IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	180 MHz
LVCMOS 2.5 V	230 MHz
LVCMOS 1.8 V	180 MHz
LVCMOS 1.5 V	120 MHz
PCI	180 MHz
PCI-X	180 MHz
LVDS	300 MHz
LVPECL	300 MHz

Table 2-18 • **IGLOO Maximum I/O Frequency for Single-Ended and Differential I/Os in All Bank Types (maximum drive strength and high slew selected)—for IGLOO V2, 1.2 V DC Core Supply Voltage**

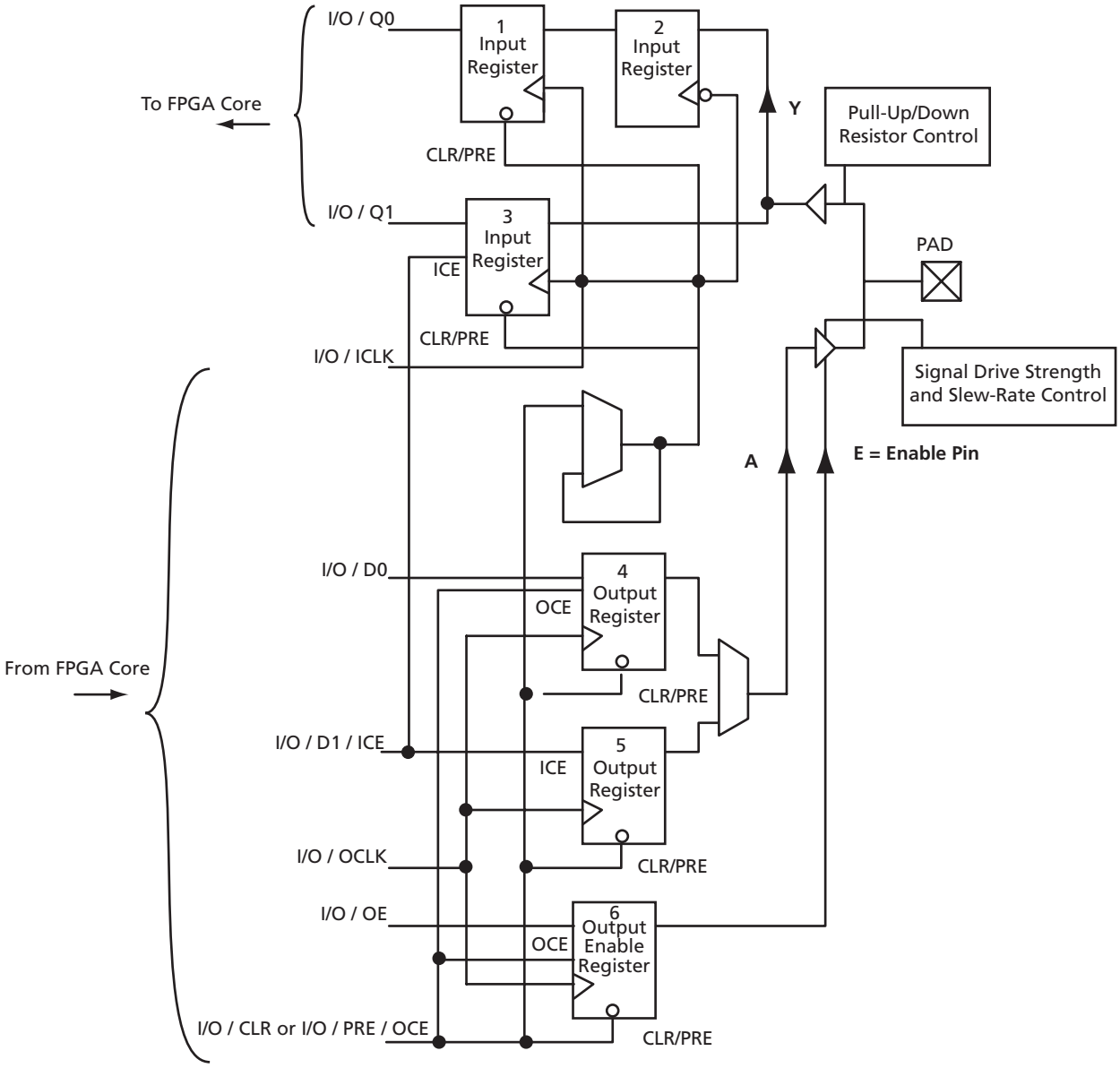
Specification	Performance Up To
LVTTL/LVCMOS 3.3 V	TBD
LVCMOS 2.5 V	TBD
LVCMOS 1.8 V	TBD
LVCMOS 1.5 V	TBD
PCI	TBD
PCI-X	TBD
LVDS	TBD
LVPECL	TBD

I/O Registers

Each I/O module contains several input, output, and enable registers. Refer to Figure 2-24 for a simplified representation of the I/O block.

The number of input registers is selected by a set of switches (not shown in Figure 2-24) between registers to implement single-ended or differential data transmission to and from the FPGA core. The Designer software sets these switches for the user.

A common CLR/PRE signal is employed by all I/O registers when I/O register combining is used. Input Register 2 does not have a CLR/PRE pin, as this register is used for DDR implementation.



Note: *IGLOO I/Os have registers to support DDR functionality (see the "Double Data Rate (DDR) Support" section on page 2-35 for more information).*

Figure 2-24 • **I/O Block Logical Representation**

Double Data Rate (DDR) Support

IGLOO devices support 350 MHz DDR inputs and outputs. In DDR mode, new data is present on every transition of the clock signal. Clock and data lines have identical bandwidths and signal integrity requirements, making them very efficient for implementing very high-speed systems.

High-speed DDR interfaces can be implemented using LVDS. The DDR feature is primarily implemented in the FPGA core periphery and is not limited to any I/O standard.

Input Support for DDR

The basic structure to support a DDR input is shown in Figure 2-25. Three input registers are used to capture incoming data, which is presented to the core on each rising edge of the I/O register clock.

Each I/O tile on IGLOO devices supports DDR inputs.

Output Support for DDR

The basic DDR output structure is shown in Figure 2-26 on page 2-36. New data is presented to the output every half clock cycle. Note: DDR macros and I/O registers do not require additional routing. The combiner automatically recognizes the DDR macro and pushes its registers to the I/O register area at the edge of the chip. The routing delay from the I/O registers to the I/O buffers is already taken into account in the DDR macro.

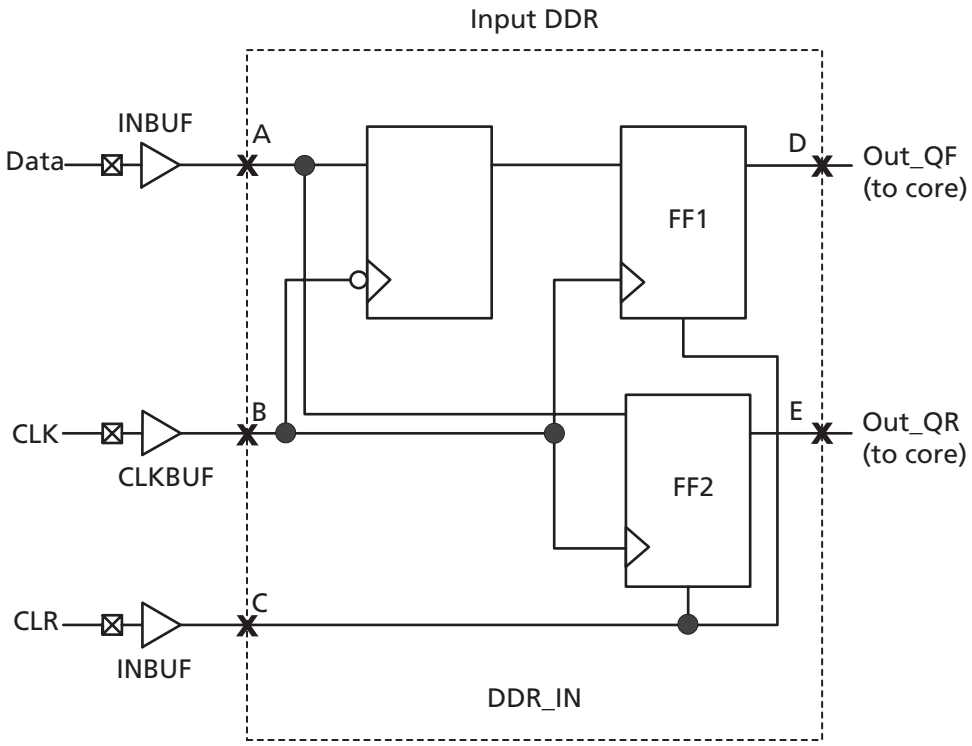


Figure 2-25 • **DDR Input Register Support in IGLOO Devices**

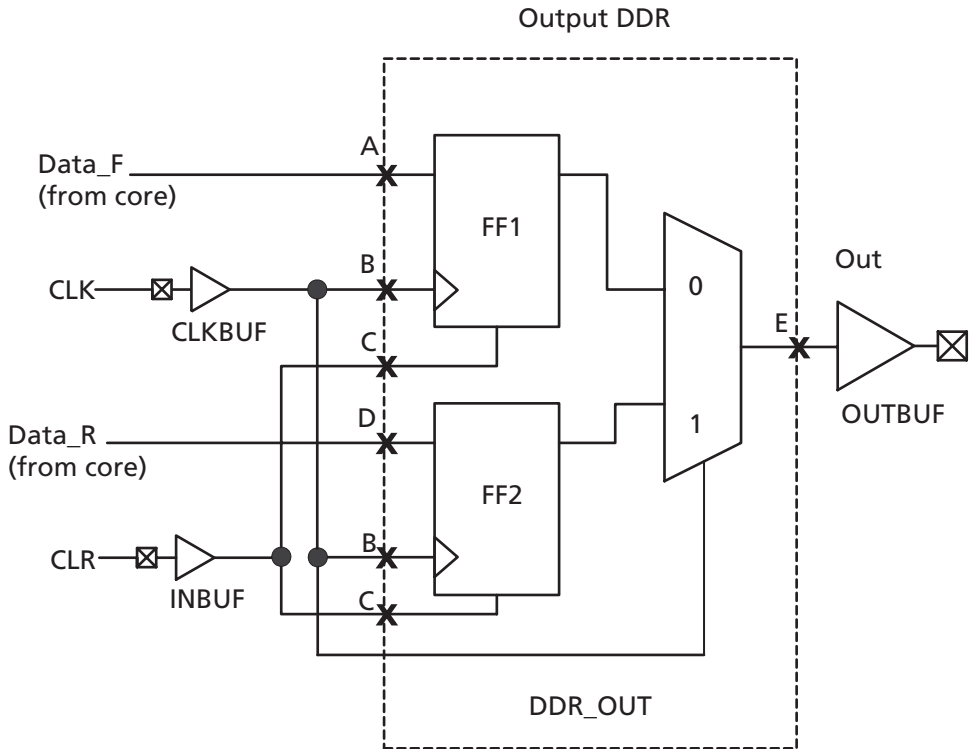


Figure 2-26 • **DDR Output Support in IGLOO Devices**

Hot-Swap Support

Hot-swapping (also called hot plugging) is the operation of hot insertion or hot removal of a card in a powered-up system. The levels of hot-swap support and examples of related applications are described in Table 2-19 on page 2-37. The I/Os also need to be configured in hot insertion mode if hot plugging compliance is required. The AGL030 device has an I/O structure that allows the support of Level 3 and Level 4 hot-swap with only two levels of staging.

Table 2-19 • **Levels of Hot-Swap Support**

Hot-Swapping Level	Description	Power Applied to Device	Bus State	Card Ground Connection	Device Circuitry Connected to Bus Pins	Example of Application with Cards Containing IGLOO Devices	Compliance of IGLOO Devices
1	Cold-swap	No	–	–	–	System and card with Actel FPGA chip are powered down and the card is plugged into the system. Then the power supplies are turned on for the system but not for the FPGA on the card.	AGL030: Compliant Other IGLOO devices: Compliant if the bus switch is used to isolate FPGA I/Os from the rest of the system.
2	Hot-swap while reset	Yes	Held in reset state	Must be made and maintained for 1 ms before, during, and after insertion/ removal	–	In the PCI hot-plug specification, reset control circuitry isolates the card busses until the card supplies are at their nominal operating levels and stable.	AGL030: Compliant I/Os can but do not have to be set to hot insertion mode. Other IGLOO devices: Compliant
3	Hot-swap while bus idle	Yes	Held idle (no ongoing I/O processes during insertion/ removal)	Same as Level 2	Must remain glitch-free during power-up or power-down	Board bus shared with card bus is "frozen," and there is no toggling activity on the bus. It is critical that the logic states set on the bus signal are not disturbed during card insertion/removal.	AGL030: Compliant with 2 levels of staging (first: GND, second: all other pins) Other IGLOO devices: Compliant: Option 1 – 2 levels of staging (first: GND, second: all other pins) together with bus switch on the I/Os Option 2 – 3 levels of staging (first: GND, second: supplies, third: all other pins)
4	Hot-swap on an active bus	Yes	Bus may have active I/O processes ongoing, but device being inserted or removed must be idle.	Same as Level 2	Same as Level 3	There is activity on the system bus, and it is critical that the logic states set on the bus signal are not disturbed during card insertion/removal.	AGL030: Compliant with 2 levels of staging (first: GND, second: all other pins) Other IGLOO devices: Compliant: Option 1 – 2 levels of staging (first: GND, second: all other pins) together with bus switch on the I/Os Option 2 – 3 levels of staging (first: GND, second: supplies, third: all other pins)

For boards and cards with three levels of staging, card power supplies must have time to reach their final values before the I/Os are connected. Pay attention to the sizing of power supply decoupling capacitors on the card to ensure that the power supplies are not overloaded with capacitance.

Cards with three levels of staging should have the following sequence:

- Grounds
- Powers
- I/Os and other pins

For Level 3 and Level 4 compliance with the AGL030 device, cards with two levels of staging should have the following sequence:

- Grounds
- Powers, I/Os, and other pins

Cold-Sparing Support

Cold-sparing means that a subsystem with no power applied (usually a circuit board) is electrically connected to the system that is in operation. This means that all input buffers of the subsystem must present very high input impedance with no power applied so as not to disturb the operating portion of the system.

The AGL030 device fully supports cold-sparing, since the I/O clamp diode is always off (see Table 2-14 on page 2-31). For other IGLOO devices, since the I/O clamp diode is always active, cold-sparing can be accomplished either by employing a bus switch to isolate the device I/Os from the rest of the system or by driving each IGLOO I/O pin to 0 V.

If the AGL030 is used in applications requiring cold-sparing, a discharge path from the power supply to ground should be provided. This can be done with a discharge resistor or a switched resistor. This is necessary because the AGL030 does not have built-in I/O clamp diodes.

If the resistor is chosen, the resistor value must be calculated based on decoupling capacitance on a given power supply on the board (this decoupling capacitance is in parallel with the resistor). The RC time constant should ensure full discharge of supplies before cold-sparing functionality is required. The resistor is necessary to ensure that the power pins are discharged to ground every time there is an interruption of power to the device.

I/O cold-sparing may add additional current if a pin is configured with either a pull-up or pull-down resistor and driven in the opposite direction. A small static current is induced on each I/O pin when the pin is driven to a voltage opposite to the weak pull resistor. The current is equal to the voltage drop across the input pin divided by the pull resistor. Refer to Table 3-38 on page 3-27 for the specific pull resistor value for the corresponding I/O standard.

For example, assuming an LVTTL 3.3 V input pin is configured with a weak pull-up resistor, a current will flow through the pull-up resistor if the input pin is driven LOW. For LVTTL 3.3 V, the pull-up resistor is ~45 kΩ, and the resulting current is equal to 3.3 V / 45 kΩ = 73 µA for the I/O pin. This is true also when a weak pull-down is chosen and the input pin is driven HIGH. This current can be avoided by driving the input LOW when a weak pull-down resistor is used and driving it HIGH when a weak pull-up resistor is used.

This current draw can occur in the following cases:

- In Active and Static modes:
  - Input buffers with pull-up, driven LOW
  - Input buffers with pull-down, driven HIGH
  - Bidirectional buffers with pull-up, driven LOW
  - Bidirectional buffers with pull-down, driven HIGH
  - Output buffers with pull-up, driven LOW
  - Output buffers with pull-down, driven HIGH
  - Tristate buffers with pull-up, driven LOW
  - Tristate buffers with pull-down, driven HIGH
- In Flash*Freeze mode:
  - Input buffers with pull-up, driven LOW
  - Input buffers with pull-down, driven HIGH
  - Bidirectional buffers with pull-up, driven LOW
  - Bidirectional buffers with pull-down, driven HIGH

Electrostatic Discharge (ESD) Protection

IGLOO devices are tested per JEDEC Standard JESD22-A114-B.

IGLOO devices contain clamp diodes at every I/O, global, and power pad. Clamp diodes protect all device pads against damage from ESD as well as from excessive voltage transients.

Each I/O has two clamp diodes. One diode has its positive (P) side connected to the pad and its negative (N) side connected to V_{CCI}. The second diode has its P side connected to GND and its N side connected to the pad. During operation, these diodes are normally biased in the off state, except when transient voltage is significantly above V_{CCI} or below GND levels.

In AGL030, the first diode is always off. In other IGLOO devices, the clamp diode is always on and cannot be switched off.

By selecting the appropriate I/O configuration, the diode is turned on or off. Refer to Table 2-20 on page 2-39 for more information about the I/O standards and the clamp diode.

The second diode is always connected to the pad, regardless of the I/O configuration selected.

Table 2-20 • **I/O Hot-Swap and 5 V Input Tolerance Capabilities in IGLOO Devices**

I/O Assignment	Clamp Diode[1]		Hot Insertion		5 V Input Tolerance[2]		Input Buffer	Output Buffer
	AGL030	Other IGLOO Devices	AGL030	Other IGLOO Devices[3]	AGL030	Other IGLOO Devices		
3.3 V LVTTL/LVCMOS	No	Yes	Yes	Yes	Yes[2]	Yes[2]	Enabled/Disabled	
3.3 V PCI, 3.3 V PCI-X	N/A	Yes	N/A	Yes	N/A	Yes[2]	Enabled/Disabled	
LVCMOS 2.5 V [5]	No	Yes	Yes	Yes	Yes[2]	Yes[4]	Enabled/Disabled	
LVCMOS 2.5 V / 5.0 V [6]	N/A	Yes	N/A	Yes	N/A	Yes[4]	Enabled/Disabled	
LVCMOS 1.8 V	No	Yes	Yes	Yes	No	No	Enabled/Disabled	
LVCMOS 1.5 V	No	Yes	Yes	Yes	No	No	Enabled/Disabled	
Differential, LVDS/ BLVDS/M-LVDS/ LVPECL	N/A	Yes	N/A	Yes	N/A	No	Enabled/Disabled	

Notes:

1. *The clamp diode is always off for the AGL030 device and always active for other IGLOO devices.*
2. *Can be implemented with an external IDT bus switch, resistor divider, or Zener with resistor.*
3. *Refer to Table 2-19 on page 2-37 for device-compliant information.*
4. *Can be implemented with an external resistor and an internal clamp diode.*
5. *The LVCMOS 2.5 V I/O standard is supported by the AGL030 device only. In the SmartGen Core Reference Guide, select the LVCMOS25 macro for LVCMOS 2.5 V I/O standard support for the AGL030 device.*
6. *The LVCMOS 2.5 V / 5.0 V I/O standard is supported by all IGLOO devices except AGL030. In the SmartGen Core Reference Guide, select the LVCMOS5 macro for LVCMOS 2.5 V / 5.0 V I/O standard support for all IGLOO devices except AGL030.*

5 V Input Tolerance

I/Os can support 5 V input tolerance when LVTTL 3.3 V, LVCMOS 3.3 V, LVCMOS 2.5 V, and LVCMOS 2.5 V / 5.0 V configurations are used (see Table 2-20 on page 2-39 for more details). There are four recommended solutions for achieving 5 V receiver tolerance (see Figure 2-27 to Figure 2-30 on page 2-43 for details of board and macro setups). All the solutions meet a common requirement of limiting the voltage at the input to 3.6 V or less. In fact, the I/O absolute maximum voltage rating is 3.6 V, and any voltage above 3.6 V may cause long-term gate oxide failures.

Solution 1

The board-level design must ensure that the reflected waveform at the pad does not exceed the limits provided in Table 3-2 on page 3-2. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the two external resistors as explained below. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

Here are some examples of possible resistor values (based on a simplified simulation model with no line effects and 10 Ω transmitter output resistance, where Rtx_out_high = (V_{CCI} – V_{OH}) / I_{OH}, Rtx_out_low = V_{OL} / I_{OL}).

Example 1 (high speed, high current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 36 Ω (±5%), P(r1)min = 0.069 Ω

R2 = 82 Ω (±5%), P(r2)min = 0.158 Ω

Imax_tx = 5.5 V / (82 × 0.95 + 36 × 0.95 + 10) = 45.04 mA

t_{RISE} = t_{FALL} = 0.85 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Example 2 (low–medium speed, medium current):

Rtx_out_high = Rtx_out_low = 10 Ω

R1 = 220 Ω (±5%), P(r1)min = 0.018 Ω

R2 = 390 Ω (±5%), P(r2)min = 0.032 Ω

Imax_tx = 5.5 V / (220 × 0.95 + 390 × 0.95 + 10) = 9.17 mA

t_{RISE} = t_{FALL} = 4 ns at C_pad_load = 10 pF (includes up to 25% safety margin)

t_{RISE} = t_{FALL} = 20 ns at C_pad_load = 50 pF (includes up to 25% safety margin)

Other values of resistors are also allowed as long as the resistors are sized appropriately to limit the voltage at the receiving end to 2.5 V < Vin (rx) < 3.6 V when the transmitter sends a logic 1. This range of Vin_dc (rx) must be assured for any combination of transmitter supply (5 V ± 0.5 V), transmitter output resistance, and board resistor tolerances.

Temporary overshoots are allowed according to Table 3-4 on page 3-3.

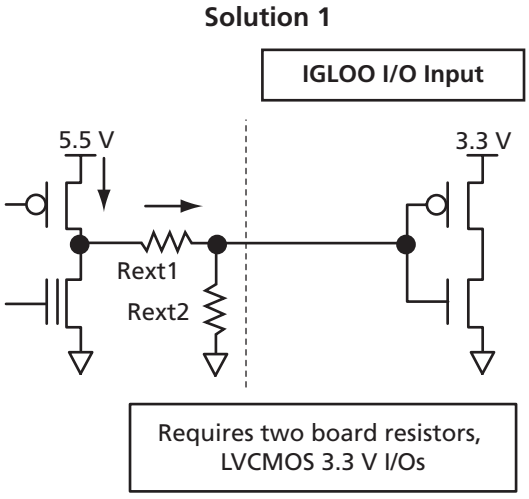


Figure 2-27 • **IGLOO Solution 1**

Solution 2

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-3. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the external resistors and Zener, as shown in Figure 2-28. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

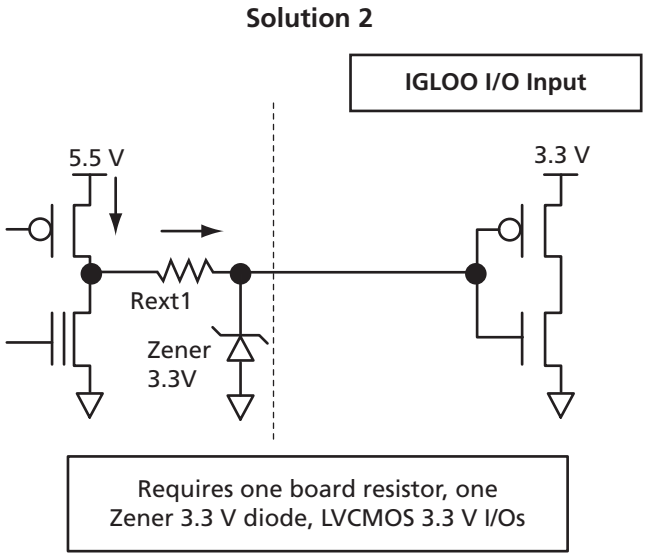


Figure 2-28 • **IGLOO Solution 2**

Solution 3

The board-level design must ensure that the reflected waveform at the pad does not exceed limits provided in Table 3-4 on page 3-3. This is a requirement to ensure long-term reliability.

This scheme will also work for a 3.3 V PCI/PCI-X configuration, but the internal diode should not be used for clamping, and the voltage must be limited by the bus switch, as shown in Figure 2-29. Relying on the diode clamping would create an excessive pad DC voltage of 3.3 V + 0.7 V = 4 V.

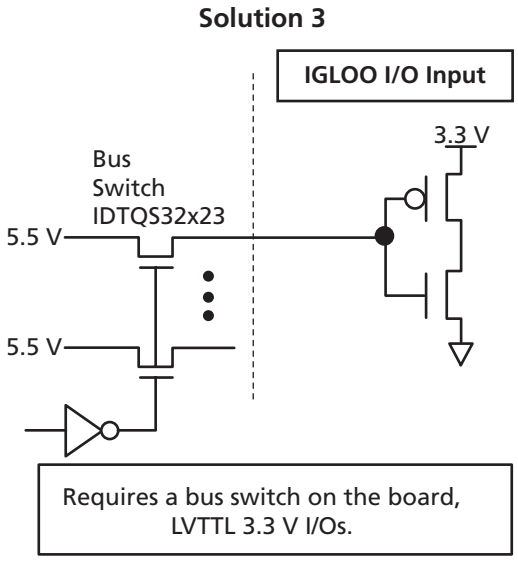


Figure 2-29 • **IGLOO Solution 3**

Solution 4

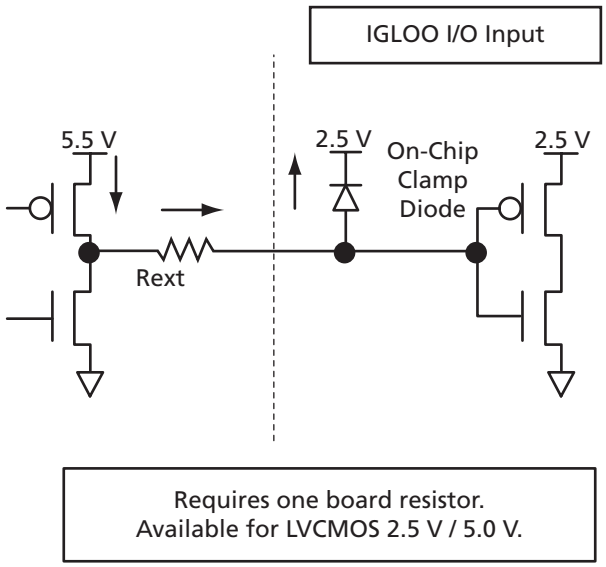


Figure 2-30 • **IGLOO Solution 4**

Table 2-21 • **Comparison Table for 5 V–Compliant Receiver Scheme**

Scheme	Board Components	Speed	Current Limitations
1	Two resistors	Low to High[1]	Limited by transmitter's drive strength
2	Resistor and Zener 3.3 V	Medium	Limited by transmitter's drive strength
3	Bus switch	High	N/A
4	Minimum resistor value[2, 3, 4, 5] • R = 47 Ω at T_J = 70°C • R = 150 Ω at T_J = 85°C • R = 420 Ω at T_J = 100°C	Medium	Maximum diode current at 100% duty cycle, signal constantly at '1' • 52.7 mA at T_J = 70°C / 10-year lifetime • 16.5 mA at T_J = 85°C / 10-year lifetime • 5.9 mA at T_J = 100°C / 10-year lifetime For duty cycles other than 100%, the currents can be increased by a factor of 1 / (duty cycle). Example: 20% duty cycle at 70°C Maximum current = (1 / 0.2) × 52.7 mA = 5 × 52.7 mA = 263.5 mA

Notes:

1. *Speed and current consumption increase as the board resistance values decrease.*
2. *Resistor values ensure I/O diode long-term reliability.*
3. *At 70°C, customers could still use 420 Ω on every I/O.*
4. *At 85°C, a 5 V solution on every other I/O is permitted, since the resistance is lower (150 Ω) and the current is higher. Also, the designer can still use 420 Ω and use the solution on every I/O.*
5. *At 100°C, the 5 V solution on every I/O is permitted, since 420 Ω are used to limit the current to 5.9 mA.*

5 V Output Tolerance

IGLOO I/Os must be set to 3.3 V LVTTL or 3.3 V LVCMOS mode to reliably drive 5 V TTL receivers. It is also critical that there be NO external I/O pull-up resistor to 5 V, since this resistor would pull the I/O pad voltage beyond the 3.6 V absolute maximum value and consequently cause damage to the I/O.

When set to 3.3 V LVTTL or 3.3 V LVCMOS mode, IGLOO I/Os can directly drive signals into 5 V TTL receivers. In fact, V_{OL} = 0.4 V and V_{OH} = 2.4 V in both 3.3 V LVTTL and 3.3 V LVCMOS modes exceeds the V_{IL} = 0.8 V and V_{IH} = 2 V level requirements of 5 V TTL receivers. Therefore, level 1 and level 0 will be recognized correctly by 5 V TTL receivers.

Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout

SSOs can cause signal integrity problems on adjacent signals that are not part of the SSO bus. Both inductive and capacitive coupling parasitics of bond wires inside packages and of traces on PCBs will transfer noise from SSO busses onto signals adjacent to those busses. Additionally, SSOs can produce ground bounce noise and V_{CCI} dip noise. These two noise types are caused by rapidly changing currents through GND and V_{CCI} package pin inductances during switching activities (EQ 2-1 and EQ 2-2).

$$\text{Ground bounce noise voltage} = L(GND) \times di/dt \quad \textit{EQ 2-1}$$

$$V_{CCI} \text{ dip noise voltage} = L(V_{CCI}) \times di/dt \quad \textit{EQ 2-2}$$

Any group of four or more input pins switching on the same clock edge is considered an SSO bus. The shielding should be done both on the board and inside the package unless otherwise described.

In-package shielding can be achieved in several ways; the required shielding will vary depending on whether pins next to the SSO bus are LVTTL/LVCMOS inputs, LVTTL/LVCMOS outputs, or GTL/SSTL/HSTL/LVDS/LVPECL inputs and outputs. Board traces in the vicinity of the SSO bus have to be adequately shielded from mutual coupling and inductive noise that can be generated by the SSO bus. Also, noise generated by the SSO bus needs to be reduced inside the package.

PCBs perform an important function in feeding stable supply voltages to the IC and, at the same time, maintaining signal integrity between devices.

Key issues that need to considered are as follows:

- Power and ground plane design and decoupling network design
- Transmission line reflections and terminations

Selectable Skew between Output Buffer Enable and Disable Times

The configurable skew block is used to delay the output buffer assertion (enable) without affecting deassertion (disable) time.

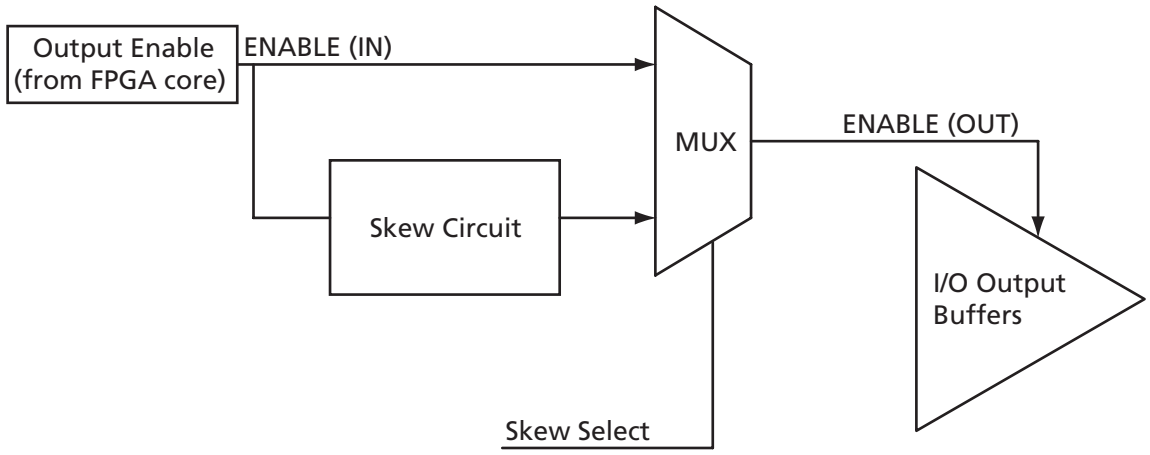


Figure 2-31 • **Block Diagram of Output Enable Path**

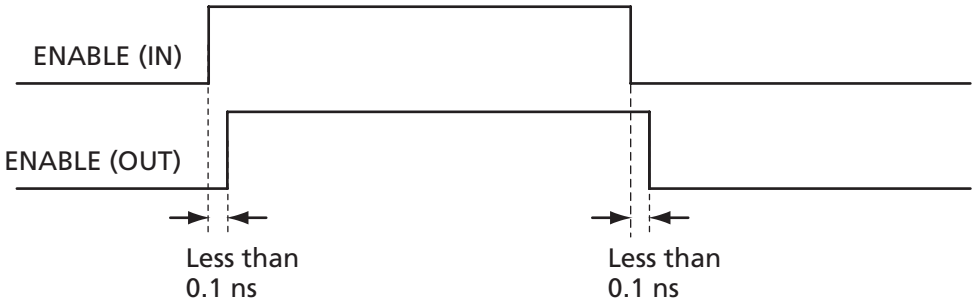


Figure 2-32 • **Timing Diagram (option 1: bypasses skew circuit)**

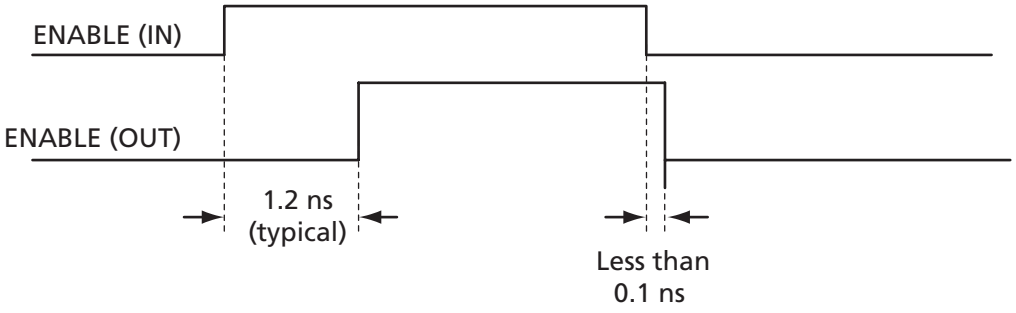


Figure 2-33 • **Timing Diagram (option 2: enables skew circuit)**

At the system level, the skew circuit can be used in applications where transmission activities on bidirectional data lines need to be coordinated. This circuit, when selected, provides a timing margin that can prevent bus contention and subsequent data loss and/or transmitter over-stress due to transmitter-to-transmitter current shorts. Figure 2-34 presents an example of the skew circuit implementation in a bidirectional communication system. Figure 2-35 shows how bus contention is created, and Figure 2-36 on page 2-47 shows how it can be avoided with the skew circuit.

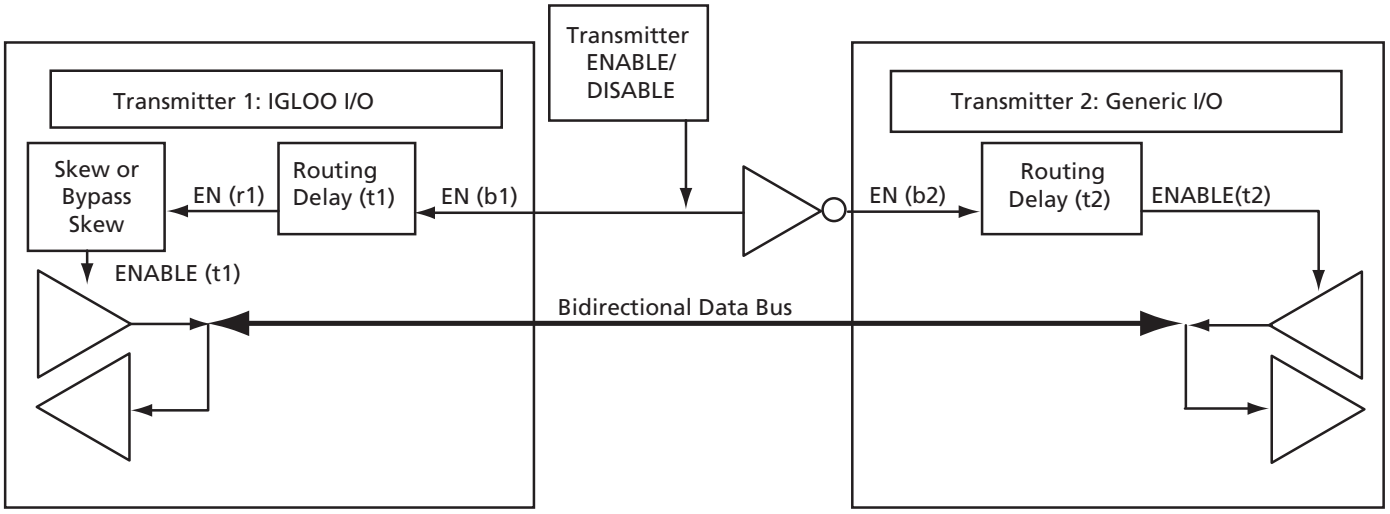


Figure 2-34 • **Example of Implementation of Skew Circuits in Bidirectional Transmission Systems Using IGLOO Devices**

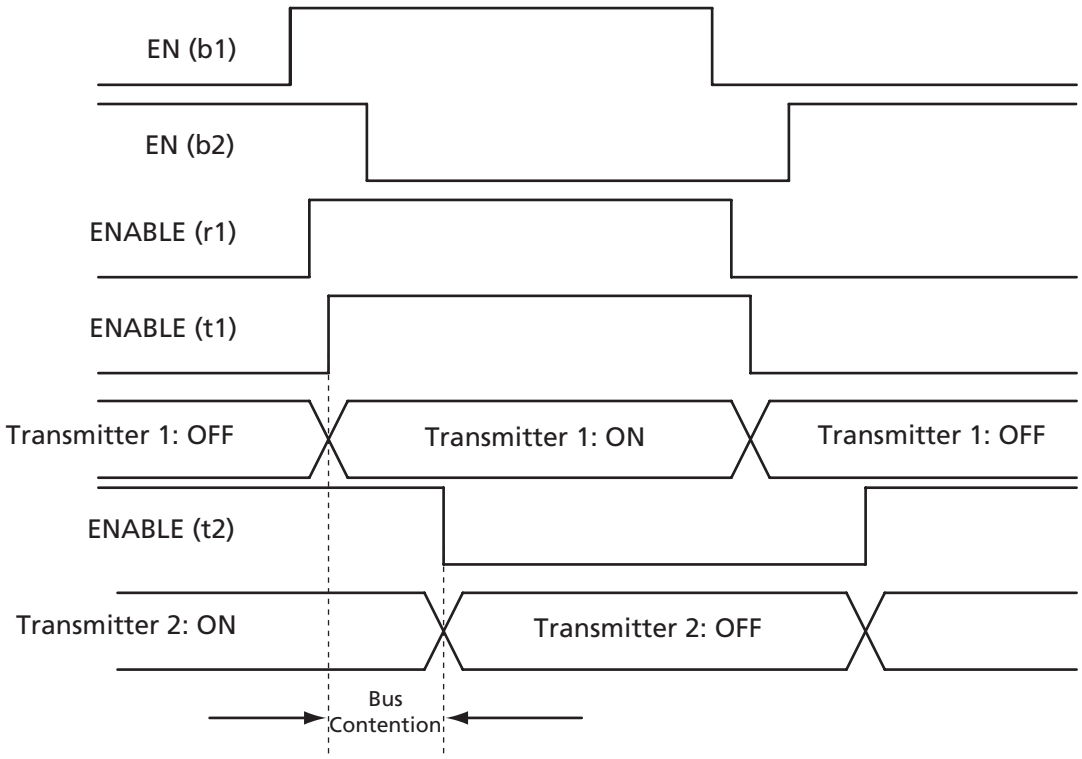


Figure 2-35 • **Timing Diagram (bypasses skew circuit)**

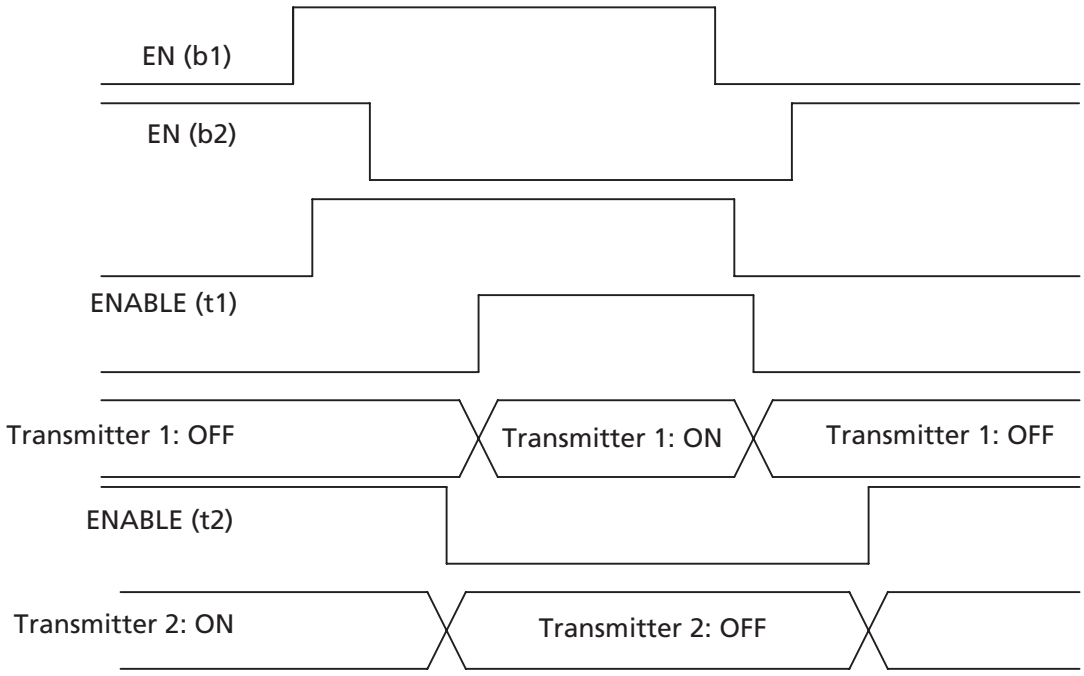


Figure 2-36 • **Timing Diagram (with skew circuit selected)**

I/O Software Support

In the IGLOO development software, default settings have been defined for the various I/O standards supported. Changes can be made to the default settings via the use of attributes; however, not all I/O attributes are applicable for all I/O standards. Table 2-22 lists the valid I/O attributes that can be manipulated by the user for each I/O standard.

Single-ended I/O standards in IGLOO devices support up to five different drive strengths.

Table 2-22 • **IGLOO I/O Attributes vs. I/O Standard Applications**

I/O Standard	SLEW (output only)	OUT_DRIVE (output only)	SKEW (all macros with OE)*	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓
LVCMOS 1.5 V	✓	✓	✓	✓	✓	✓
PCI (3.3 V)			✓		✓	✓
PCI-X (3.3 V)	✓		✓		✓	✓
LVDS, BLVDS, M-LVDS			✓			✓
LVPECL						✓

Note: **Applies to all IGLOO devices except AGL030.*

Table 2-23 lists the default values for the above selectable I/O attributes as well as those that are preset for that I/O standard. See Table 2-24 for SLEW and OUT_DRIVE settings.

Table 2-23 • **IGLOO I/O Default Attributes**

I/O Standards	SLEW (output only)	OUT_DRIVE (output only)	SKEW (tribuf and bibuf only)	RES_PULL	OUT_LOAD (output only)	COMBINE_REGISTER
LVTTL/LVCMOS 3.3 V	See Table 2-24.	See Table 2-24.	Off	None	35 pF	–
LVCMOS 2.5 V			Off	None	35 pF	–
LVCMOS 2.5/5.0 V			Off	None	35 pF	–
LVCMOS 1.8 V			Off	None	35 pF	–
LVCMOS 1.5 V			Off	None	35 pF	–
PCI (3.3 V)			Off	None	10 pF	–
PCI-X (3.3 V)			Off	None	10 pF	–
LVDS, BLVDS, M-LVDS			Off	None	0 pF	–
LVPECL			Off	None	0 pF	–

Weak Pull-Up and Weak Pull-Down Resistors

IGLOO devices support optional weak pull-up and pull-down resistors on each I/O pin. When the I/O is pulled up, it is connected to the V_{CCI} of its corresponding I/O bank. When it is pulled down, it is connected to GND. Refer to Table 3-38 on page 3-27 for more information.

Configuration of the pull-up or pull-down of the I/O can be used to set the I/O to a certain state while the device is in Flash*Freeze mode. Refer to the "Flash*Freeze Technology and Low-Power Modes" section on page 2-50 for more information.

The Flash*Freeze (FF) pin cannot be configured with a weak pull-down or pull-up I/O attribute as the signal needs to be driven at all times.

Slew Rate Control and Drive Strength

IGLOO devices support output slew rate control: high and low. Actel recommends the high slew rate option to minimize the propagation delay. This high-speed option may introduce noise into the system if appropriate signal integrity measures are not adopted. Selecting a low slew rate reduces this kind of noise but adds some delays in the system. Low slew rate is recommended when bus transients are expected. Drive strength should also be selected according to the design requirements and noise immunity of the system.

The output slew rate and multiple drive strength controls are available in LVTTL/LVCMOS 3.3 V, LVCMOS 2.5 V, LVCMOS 2.5 V / 5.0 V input, LVCMOS 1.8 V, and LVCMOS 1.5 V. All other I/O standards have a high output slew rate by default.

For AGL030, refer to Table 2-24; for other IGLOO devices, refer to Table 2-25 and Table 2-26 for more information about the slew rate and drive strength specification.

Table 2-24 • **IGLOO Output Drive (OUT_DRIVE) for Standard I/O Bank Type (AGL030 device)**

I/O Standards	OUT_DRIVE (mA)				Slew	
	2	4	6	8		
LVTTL/LVCMOS 3.3 V	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	–	–	–	High	Low

Note: *Refer to Table 2-14 on page 2-31 for I/O bank type definition.*

Table 2-25 • **IGLOO Output Drive for Standard+ I/O Bank Type**

I/O Standards	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	Slew	
LVTTL	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	–	–	High	Low
LVCMOS 1.5 V	✓	✓	–	–	–	–	High	Low

Notes:

1. *There will be a difference in timing between the Standard+ I/O banks and the Advanced I/O banks (Table 2-26). Refer to the I/O timing tables beginning on page 3-31 and Table 2-12 on page 2-30 for the standards supported by each device.*
2. *Refer to Table 2-14 on page 2-31 for I/O bank type definition.*

Table 2-26 • **IGLOO Output Drive for Advanced I/O Bank Type**

I/O Standards	2 mA	4 mA	6 mA	8 mA	12 mA	16 mA	24 mA	Slew	
LVTTL	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 3.3 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 2.5/5.0 V	✓	✓	✓	✓	✓	✓	✓	High	Low
LVCMOS 1.8 V	✓	✓	✓	✓	✓	✓	–	High	Low
LVCMOS 1.5 V	✓	✓	✓	✓	✓	–	–	High	Low

Notes:

1. *There will be a difference in timing between the Advanced I/O banks and the Standard+ I/O banks (Table 2-25). Refer to the I/O timing tables beginning on page 3-31 and Table 2-12 on page 2-30 for the standards supported by each device.*
2. *Refer to Table 2-14 on page 2-31 for I/O bank type definition.*

Flash*Freeze Technology and Low-Power Modes

The Actel IGLOO family offers ultra-low power consumption in Active and Static modes by utilizing the unique Flash*Freeze technology.

IGLOO devices offer various power-saving modes that enable every system to utilize modes that achieve the lowest total system power.

Low-Power Active capability (static idle) allows for ultra-low power consumption (from 25 µW) while the IGLOO device is operational in the system by maintaining SRAM, registers, I/Os, and logic functions.

Flash*Freeze technology provides an ultra-low-power static mode (Flash*Freeze mode) that retains all SRAM and register information with rapid recovery to Active (operating) mode. The mechanism enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze (FF) pin while all power supplies are kept in their original states. In addition, I/Os and clocks connected to the FPGA can still be driven or toggling without impact on device power consumption. While in Flash*Freeze mode, the device retains all core register states and SRAM information. No power is consumed by the I/O banks, clocks, JTAG pins, or PLLs, and the IGLOO device consumes as little as 5 µW in this mode.

Power Conservation Techniques

IGLOO FPGAs provide many ways to conserve power; however, there are also many design techniques that can be used to reduce power on the board. Actel recommends that the user tie any unused power supplies (such as V_{CCPLL}, V_{CCI}, VMV, and V_{PUMP}) and unused I/O signals to the ground plane.

Using low-voltage CMOS I/O standard signals and the lowest drive strength will reduce switching and result with lower power consumption in Active mode.

Low-Power Modes Overview

Table 2-27 summarizes the IGLOO low-power modes that achieve power consumption reduction when the FPGA or system is idle.

Table 2-27 • **IGLOO Power Modes Summary**

Mode		V_{CCI}	V_{CC}	Core	Clocks	ULSICC Macro	To Enter Mode	To Resume Operation	Trigger
Active		On	On	On	On	N/A	Initiate clock	None	–
Static	Idle	On	On	On	Off	N/A	Stop clock	Initiate clock	External
	Flash*Freeze type 1	On	On	On	On†	N/A	Assert FF pin	Deassert FF pin	External
	Flash*Freeze type 2	On	On	On	On†	Used to enter Flash*Freeze mode	Assert FF pin and assert LSICC	Deassert FF pin	External
Sleep		On	Off	Off	Off	N/A	Shut down V_{CC}	Turn on V_{CC} supply	External
Shutdown		Off	Off	Off	Off	N/A	Shut down V_{CC} and V_{CCI} supplies	Turn on V_{CC} and V_{CCI} supplies	External

Note: *†External clocks can be left toggling when while the device is in Flash*Freeze mode. Clocks generated by the embedded PLL will be turned off automatically.*

Static (idle) Mode

In Static (idle) mode, none of the clock inputs is switching, and static power is the only power consumed by the device. This mode can be achieved by switching off the incoming clocks to the FPGA benefitting from reduced power consumption. In addition, I/Os draw only minimal leakage current. In this mode, embedded SRAM, I/Os, and registers retain their values so the device can enter and exit this mode just by switching the clocks on or off.

If the device embedded PLL is used as the clock source, Static (idle) mode can easily be entered by pulling LOW the PLL POWERDOWN pin (active low), which will turn off the PLL.

Flash*Freeze Mode

IGLOO FPGAs offer an ultra-low static power mode to reduce power consumption while preserving the state of the registers and SRAM contents, without switching off any power supplies, inputs, or input clocks.

Flash*Freeze technology enables the user to switch to Flash*Freeze mode within 1 µs, thus simplifying low-power design implementation. The Flash*Freeze (FF) pin (active low) is a dedicated pin used to enter or exit Flash*Freeze mode directly, or the pin can be routed internally to the FPGA core to allow the user's logic to decide if and when it is safe to transition to this mode. If the FF pin is not used, it can be used as a regular I/O, benefitting from the inherent low power consumption of the IGLOO devices.

The FF pin has a built-in glitch filter that ensures spurious glitches are filtered out to prevent entering or exiting Flash*Freeze mode accidentally.

There are two ways to use Flash*Freeze mode. In Flash*Freeze type 1, entering and exiting the mode is exclusively controlled by the assertion and deassertion of the FF pin. In Flash*Freeze mode type 2, entering and exiting the mode is controlled by both the FF pin AND the user-defined LSICC signal available in the ULSICC macro.

Refer to Table 2-28 for Flash*Freeze (FF) pin and LSICC signal assertion and deassertion values.

Table 2-28 • **Flash*Freeze Mode Type 1 and Type 2 – Signal Assertion and Deassertion Values**

Signal	Assertion Value	Deassertion Value
Flash*Freeze (FF) pin	Logic '0'	Logic '1'
LSICC signal	Logic '1'	Logic '0'

Notes:

1. *The Flash*Freeze (FF) pin is an active low signal and LSICC is an active high signal.*
2. *LSICC signal is used only in Flash*Freeze mode type 2.*

Flash*Freeze Type 1: Control by Dedicated Flash*Freeze Pin

The device will enter Flash*Freeze mode 1 µs after the dedicated FF pin is asserted, and returns to normal operation when the FF pin is deasserted (Figure 2-37). In this mode, FF pin assertion or deassertion is the only condition that determines entering or exiting Flash*Freeze mode after 1 µs. This mode is implemented by enabling Flash*Freeze mode (default setting) in the Compile option of the Actel Designer software.

The FF pin threshold voltages are defined by V_{CCI} and the supported single-ended I/O standard in the corresponding I/O bank. Figure 2-37 shows the concept of FF pin control in Flash*Freeze mode type 1.

Figure 2-38 on page 2-52 shows the timing diagram for entering and exiting Flash*Freeze mode type 1.

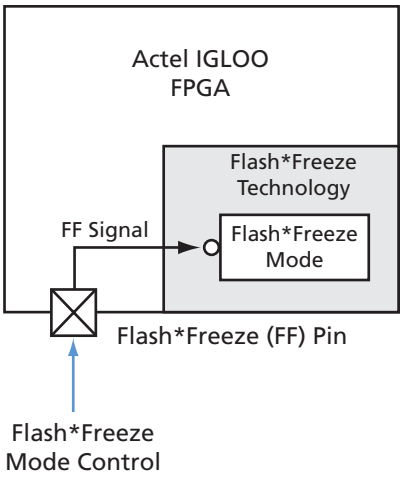


Figure 2-37 • **IGLOO Flash*Freeze Mode Type 1 – Controlled by the Flash*Freeze Pin**

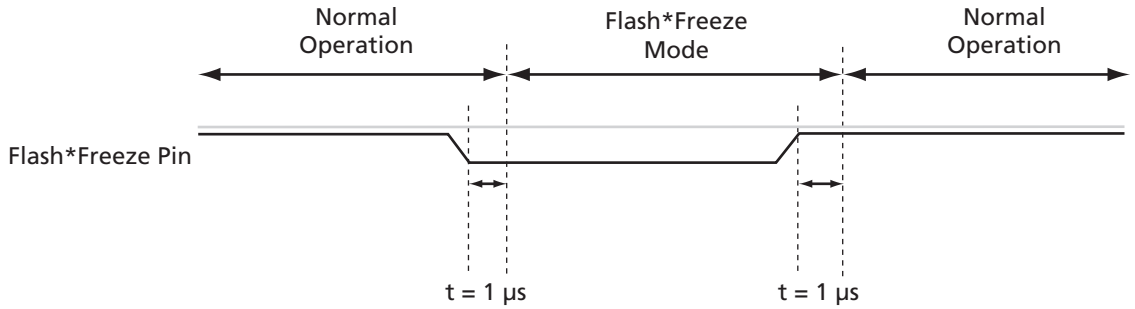


Figure 2-38 • **Flash*Freeze Mode Type 1 – Timing Diagram**

Flash*Freeze Type 2: Control by Dedicated Flash*Freeze Pin and Internal Logic

The device can enter Flash*Freeze mode by activating the FF pin together with other user-defined control logic or delay circuitry within the FPGA core (Figure 2-39). This method enables the design to perform important activities before allowing the device to enter Flash*Freeze mode, such as transitioning into a safe state or completing the processing of a critical event. The device will only enter Flash*Freeze mode when the Flash*Freeze pin is asserted and the ULSICC macro input signal, called the LSICC signal, is asserted. One condition is not sufficient to enter Flash*Freeze mode type 2; both the FF pin and LSICC signal must be asserted.

When Flash*Freeze type 2 is implemented in the design, the ULSICC macro needs to be instantiated by the user. There are no functional differences with the device when ULSICC macro is instantiated or not, and LSICC signal is asserted or deasserted. The LSICC signal is used only to control entering Flash*Freeze mode. Figure 2-40 on page 2-53 shows the timing diagram for entering and exiting Flash*Freeze mode type 2.

After exiting Flash*Freeze mode type 2 by deasserting the Flash*Freeze pin, the LSICC signal needs to be deasserted by the user design. This will prevent entering Flash*Freeze mode by asserting the Flash*Freeze pin only.

Refer to the *Actel IGLOOe Flash*Freeze Technology and Low Power Modes* application note for more information about the software implementation of this mode.

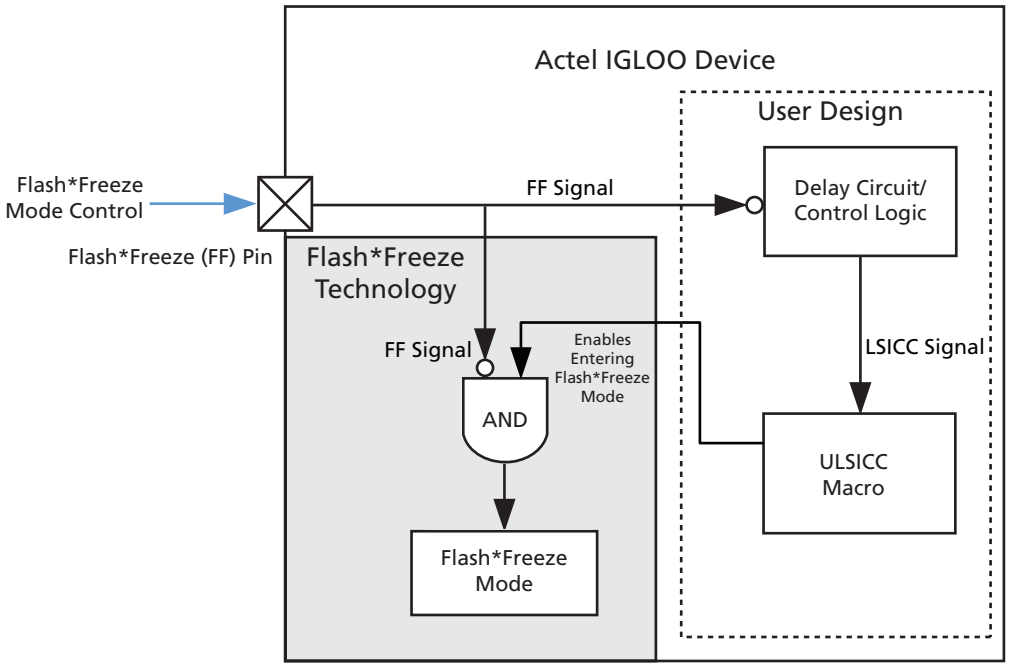


Figure 2-39 • **IGLOO Flash*Freeze Mode Type 2 – Controlled by Flash*Freeze Pin and Internal Logic (LSICC signal)**

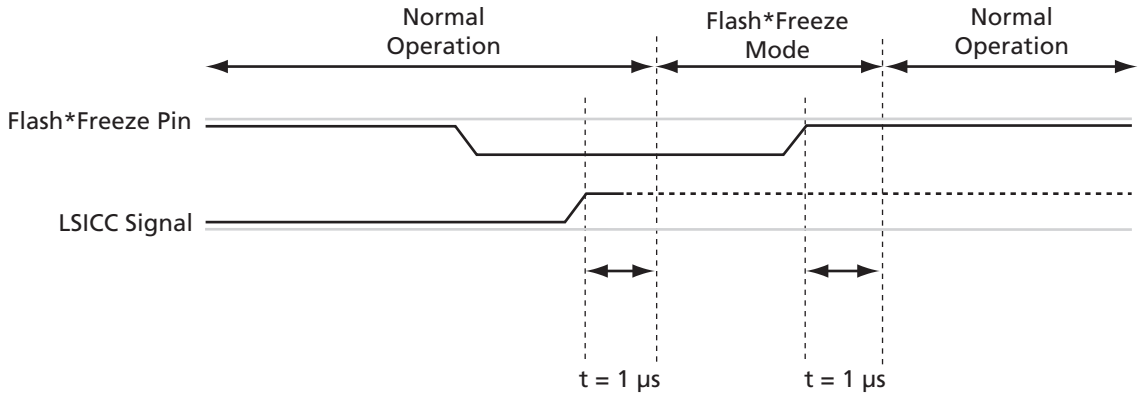


Figure 2-40 • **Flash*Freeze Mode Type 2 – Timing Diagram**

Users can also assert the input of the LSICC signal internally during normal operation. In this case, there is no difference between Flash*Freeze mode type 1 and type 2, and the FF pin exclusively controls entering and exiting Flash*Freeze mode.

In Flash*Freeze mode Type 2 operation, entering Flash*Freeze mode is done within 1 µs after asserting the last signal that triggers Flash*Freeze mode (FF pin or LSICC signal), assuming one of the signals is already asserted. In Flash*Freeze mode type 1 operation, entering Flash*Freeze mode is done within 1 µs after asserting the FF pin only.

In Flash*Freeze mode type 1 and type 2, exiting Flash*Freeze mode is done within 1 µs after deasserting the FF pin only.

Table 2-29 summarizes the Flash*Freeze mode implementations.

Table 2-29 • **Flash*Freeze Mode Usage**

Flash*Freeze Mode Type	Description	Flash*Freeze Pin State	Instantiate ULSICC Macro	LSICC Signal	Operating Mode
1	Flash*Freeze mode is controlled only by the FF pin.	Deasserted	No	N/A	Normal operation
		Asserted	No	N/A	Flash*Freeze mode
2	Flash*Freeze mode is controlled by the FF pin and LSICC signal.	"Don't care"	Yes	Deasserted	Normal operation
		Deasserted	Yes	"Don't care"	Normal operation
		Asserted	Yes	Asserted	Flash*Freeze mode

Note: *Refer to Table 2-28 on page 2-51 for Flash*Freeze pin and LSICC signal assertion and deassertion values.*

I/O State in Flash*Freeze Mode

When the device enters Flash*Freeze mode, I/Os will become tristated. If the weak pull-up or pull-down feature is used, the I/Os will maintain the configured weak pull-up or pull-down status. This feature enables the design to set the I/O state to a certain level that is determined by the pull-up/-down configuration. For example, use the output buffer and enable weak pull-down to drive a signal LOW to an external component while the IGLOO device is in Flash*Freeze mode.

Table 2-30 shows the I/O pad state based on the configuration and buffer type.

Note that configuring weak pull-up or pull-down for the FF pin is not allowed.

Table 2-30 • **Flash*Freeze Mode (type 1 and type 2)—I/O Pad State**

Buffer Type		Internal Weak Pull-Up/-Down	I/O Pad State in Flash*Freeze Mode
Input		Enabled	Weak pull-up/pull-down*
		Disabled	Tristate*
Output		Enabled	Weak pull-up/pull-down
		Disabled	Tristate
Tristate output buffer	E = 0 (tristate)	N/A	Tristate
	E = 1 (output)	N/A	Tristate
Bidirectional	E = 0 (input)	Enabled	Weak pull-up/pull-down*
		Disabled	Tristate*
	E = 1 (output)	Enabled	Weak pull-up/pull-down
		Disabled	Tristate

Note: **Internal core logic driven by this input buffer will be tied to logic 1 as long as the device is in Flash*Freeze mode.*

Flash*Freeze Mode Design Considerations

Entering Flash*Freeze Mode

- The device was designed and optimized to enter Flash*Freeze mode only when power supplies are stable. If the device is being powered up while the FF pin is asserted (Flash*Freeze mode type 1) or both FF pin and LSICC signal are asserted (Flash*Freeze mode type 2), the device is expected to enter Flash*Freeze mode within 5 µs after the I/Os and FPGA core have reached their activation levels.
- If the device is already powered up and then the FF pin is asserted, the device will enter Flash*Freeze mode within 1 µs (type 1). In Flash*Freeze mode type 2 operation, entering Flash*Freeze mode is done within 1 µs after both FF pin and LSICC signal are asserted. Exiting Flash*Freeze mode is done within 1 µs after deasserting the FF pin only.
- If an embedded PLL is used, entering Flash*Freeze mode will automatically power down the PLL.
- The PLL output clocks will stop toggling within 1 µs after the assertion of the FF pin in type 1, or after both FF pin and LSICC signal are asserted in type 2. At the same time, I/Os will transition into the state specified in Table 2-30. The user design must ensure it is safe to enter Flash*Freeze mode.

During Flash*Freeze Mode

- Inputs and input clocks to the FPGA can toggle without any impact on static power consumption, assuming weak pull-up or pull-down is not selected.
- If weak pull-up or pull-down is selected and the input is driven to the opposite direction, power dissipation will occur.
- Any toggling signals will be charging and discharging the package pin capacitance.
- Outputs will be tristated, and the output of the input or bidirectional buffer tied to the internal logic will be set to logic 1. Refer to Table 2-30 for more information.
- JTAG operations such as JTAG commands, JTAG bypass, programming and authentication cannot be executed. The device must exit Flash*Freeze mode before JTAG commands can be sent.
- The FF pin must be externally driven (deasserted) for the device to stay in Flash*Freeze mode.
- The FF pin is still active; i.e., the pin is used to exit Flash*Freeze mode when deasserted.

Exiting Flash*Freeze Mode

- If the embedded PLL is used, the user design must allow maximum acquisition time for the PLL to acquire the lock signal.
- Within 0.5 µs of deasserting the FF pin, the input buffer can capture new input values. Within the next 0.5 µs, the output buffers are able to drive the new output values from the core.

Sleep Mode

Actel IGLOO FPGAs support Sleep mode when device functionality is not required. In Sleep mode, the FPGA core voltage supply (V_{CC}) is turned off (either grounded or floated) while other power supplies are left on, resulting in the FPGA core being turned off to reduce power consumption. While the IGLOO device is in Sleep mode, the rest of the system can still be operating and driving the input buffers of the IGLOO device. The driven inputs do not pull up the internal power planes, and the current draw is limited to minimal leakage current.

Table 2-31 shows the power supply status in Sleep mode. When the V_{CC} power supply is powered off, the corresponding power pin can be left floating or grounded.

Table 2-31 • **Sleep Mode—Power Supply Requirement for IGLOO Devices**

Power Supplies	IGLOO/e Devices
V_{CC}	Powered off
V_{CCI} = VMV	Powered on
V_{JTAG}	Powered on
V_{PUMP}	Powered on

Shutdown Mode

For AGL030 devices, Shutdown mode can be used by turning off all power supplies when the device function is not needed. Cold-sparing and hot-insertion features enable these devices to be powered down without turning off the entire system. When power returns, the live-at-power-up feature enables operation of the device after reaching the voltage activation point.

Refer to the *Actel IGLOO/e Flash*Freeze Technology and Low Power Modes* application note for more information on how to use tools and system implementation of the various power modes supported by IGLOO devices.

User I/O Naming Convention

Due to the comprehensive and flexible nature of IGLOO device user I/Os, a naming scheme is used to show the details of each I/O (Figure 2-41 and Figure 2-42 on page 2-57). The name identifies to which I/O bank it belongs, as well as pairing and pin polarity for differential I/Os.

I/O Nomenclature = FF/Gmn/IOuxwBy

Gmn is only used for I/Os that also have CCC access—i.e., global pins.

FF = Indicates the I/O dedicated for the Flash*Freeze mode activation pin

G = Global

m = Global pin location associated with each CCC on the device: A (northwest corner), B (northeast corner), C (east middle), D (southeast corner), E (southwest corner), and F (west middle)

n = Global input MUX and pin number of the associated Global location m, either A0, A1, A2, B0, B1, B2, C0, C1, or C2. Figure 2-15 on page 2-17 shows the three input pins per clock source MUX at CCC location m.

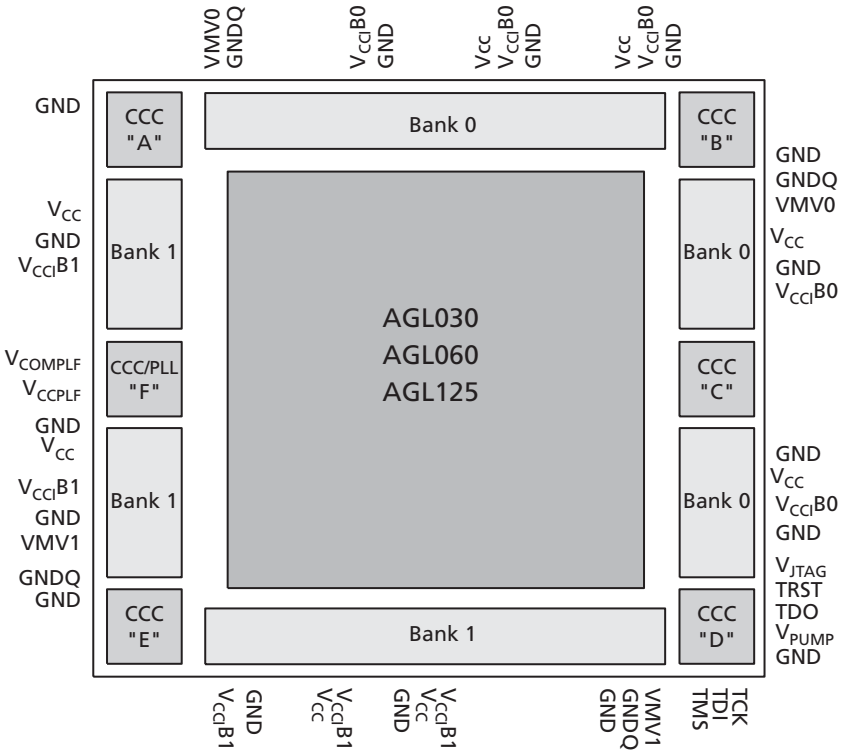
u = I/O pair number in the bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction

x = P or U (Positive), N or V (Negative) for differential pairs, or R (Regular—single-ended) for the I/Os that support single-ended and voltage-referenced I/O standards only.

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential (D) pairs, adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number (0–3). The Bank number starts at 0 from the northwest I/O bank and proceeds in a clockwise direction.



Note: *The AGL030 device does not support a PLL (V_{COMPLF} and V_{CCPLF} pins).*

Figure 2-41 • **Naming Conventions of IGLOO Devices with Two I/O Banks – Top View**

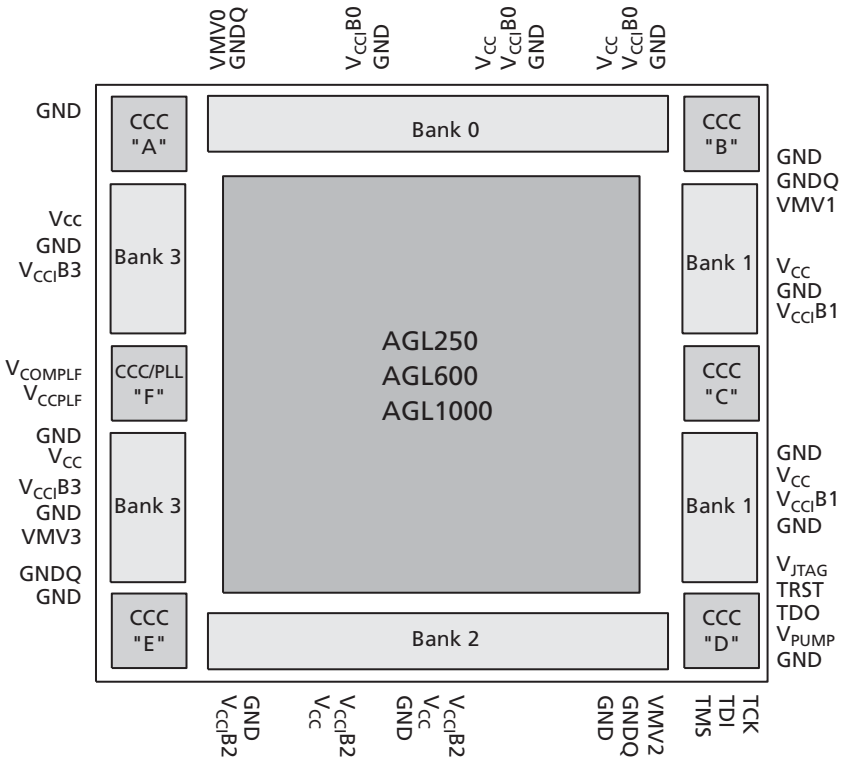


Figure 2-42 • **Naming Conventions of IGLOO Devices with Four I/O Banks – Top View**

Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

V_{CC} **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices and 1.2 V or 1.5 V for IGLOO V2 devices. V_{CC} is required for powering the JTAG state machine in addition to V_{JTAG}. Even when an IGLOO device is in bypass mode in a JTAG chain of interconnected devices, both V_{CC} and V_{JTAG} must remain powered to allow JTAG signals to pass through the IGLOO device.

For IGLOO V2 devices, V_{CC} can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in system programming when V_{CC} is at 1.5 V and the benefit of low-power operation when V_{CC} is at 1.2 V.

V_{CCI}Bx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are eight I/O banks on IGLOO devices plus a dedicated V_{JTAG} bank. Each bank can have a separate V_{CCI} connection. All I/Os in a bank will run off the same V_{CCI}Bx supply. V_{CCI} can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding V_{CCI} pins tied to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane is decoupled from the simultaneous switching noise originated from the output buffer V_{CCI} domain. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and V_{CCI} should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding V_{CCI} pins of the same bank (i.e., VMV0 to V_{CCI}B0, VMV1 to V_{CCI}B1, etc.).

V_{CCPLF} **PLL Supply Voltage[7]**

Supply voltage to analog PLL, nominally 1.5 V for IGLOO V5 devices and 1.2 V or 1.5 V for IGLOO V2 devices. If unused, V_{CCPLF} should be tied to either the power supply or GND.

V_{COMPLF} **PLL Ground[7]**

Ground to analog PLL power supplies. Unused V_{COMPLF} pins should be connected to GND.

V_{JTAG} **JTAG Supply Voltage**

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND. It should be noted that V_{CC} is required to be powered for JTAG operation; V_{JTAG} alone is insufficient. If an IGLOO device is in a JTAG chain of interconnected boards, the board containing the IGLOO device can be powered down, provided both V_{JTAG} and V_{CC} to the IGLOO part remain powered; otherwise, JTAG signals will not be able to transition the IGLOO device, even in bypass mode.

Actel recommends that V_{PUMP} and V_{JTAG} power supplies are kept separate with independent filtering capacitors rather than supplying them from a common rail.

V_{PUMP} **Programming Supply Voltage**

IGLOO devices support single-voltage ISP programming of the configuration flash and FlashROM. For programming, V_{PUMP} should be 3.3 V nominal. During normal device operation, V_{PUMP} can be left floating or can be tied (pulled up) to any voltage between 0 V and 3.45 V. Programming power supply voltage (V_{PUMP}) range is 3.15 V to 3.45 V.

When the V_{PUMP} pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across V_{PUMP} and GND, and positioned as close to the FPGA pins as possible.

7. The AGL030 device does not support this feature.

Actel recommends that V_{PUMP} and V_{JTAG} power supplies are kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI}. With V_{CCI}, VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance).
- Input buffer is disabled (with tristate value of high impedance).
- Weak pull-up is programmed.

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits" section on page 2-14. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct input into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the "User I/O Naming Convention" section on page 2-56 for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

The FF pin is a dedicated input pin that is used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall time. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

Table 2-32 shows the Flash*Freeze pin location on the available packages for IGLOO devices. The Flash*Freeze pin location is independent of device, allowing migration to larger or smaller IGLOO devices while maintaining the same pin location on the board.

Table 2-32 • **Flash*Freeze Pin Location in IGLOO Family Packages (device-independent)**

Package	Flash*Freeze Pin
CS196	TBD
QN132	B12
VQ100	27
FG144	L3
FG256	T3
FG484	W6

JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). V_{CC} must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; V_{JTAG} alone is insufficient. Both V_{JTAG} and V_{CC} to the IGLOO part must be supplied to allow JTAG signals to transition the IGLOO device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the V_{JTAG} pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Actel recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 2-33 for more information.

Table 2-33 • **Recommended Tie-Off Values for the TCK and TRST Pins**

V_{JTAG}	Tie-Off Resistance
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain.*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 2-33 and must satisfy the parallel resistance value requirement. The values in Table 2-33 correspond to the resistor recommended when a single device is used and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Actel recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC No Connect

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC Do Not Connect

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Software Tools

Overview of Tools Flow

The IGLOO family of FPGAs is fully supported by both Actel Libero IDE and Designer FPGA development software. Actel Libero IDE is an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (see the *Libero IDE flow diagram* located on the Actel website). Libero IDE includes Synplify® AE from Synplicity,® ViewDraw® AE from Mentor Graphics,® Model*Sim*® HDL Simulator from Mentor Graphics, WaveFormer Lite™ AE from SynaptiCAD,® PALACE™ AE Physical Synthesis from Magma Design Automation,™ and Designer software from Actel.

Actel Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes the following:

- SmartTime—a world-class integrated static timing analyzer and constraints editor that supports timing-driven place-and-route
- NetlistViewer—a design netlist schematic viewer
- ChipPlanner—a graphical floorplanner viewer and editor
- SmartPower—a tool that enables the designer to quickly estimate the power consumption of a design
- PinEditor—a graphical application for editing pin assignments and I/O attributes
- I/O Attribute Editor—a tool that displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format

With the Designer software, a user can lock the design pins before layout while minimally impacting the results of place-and-route. Additionally, Actel back-annotation flow is compatible with all the major simulators. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel Designer software is compatible with the most popular FPGA design entry and verification tools from EDA vendors such as Mentor Graphics, Synplicity, Synopsys, and Cadence.® The Designer software is available for both the Windows® and UNIX operating systems.

Programming

Programming can be performed using tools such as Silicon Sculptor II (BP Micro Systems) or FlashPro3 (Actel).

The user can generate STP programming files from the Designer software and use these files to program a device.

The IGLOO device can be serialized with a unique identifier stored in the FlashROM of each device. Serialization is an automatic assignment of serial numbers that are stored within the STAPL file used for programming. The area of the FlashROM used for holding such identifiers is defined using SmartGen, and the range of serial numbers to be used is defined at the time of STAPL file generation with FlashPoint. Serial number values for STAPL file generation can even be read from a file of predefined values. Serialized programming using a serialized STAPL file can be done through Actel In-House Programming (IHP), an external vendor using Silicon Sculptor software, or the ISP capabilities of the FlashPro software.

Refer to the "ISP" section on page 2-62 for programming conditions.

Security

IGLOO devices have a built-in 128-bit AES decryption core (except the AGL030 device). The decryption core facilitates secure in-system programming of the FPGA core array fabric and the FlashROM. The FlashROM and the FPGA core fabric can be programmed independently of each other, allowing the FlashROM to be updated without the need for change to the FPGA core fabric. The AES master key is stored in on-chip nonvolatile memory (flash). The AES master key can be preloaded into parts in a secure programming environment (such as the Actel In-House Programming center), and then "blank" parts can be shipped to an untrusted programming or manufacturing center for final personalization with an AES-encrypted bitstream. Late-stage product changes or personalization can be implemented easily and securely by simply sending a STAPL file with AES encrypted data. Secure remote field updates over public networks (such as the Internet) are possible by sending and programming a STAPL file with AES-encrypted data.

128-Bit AES Decryption[8]

The 128-bit AES standard (FIPS-192) block cipher is the NIST (National Institute of Standards and Technology) replacement for DES (Data Encryption Standard FIPS46-2). AES has been designed to protect sensitive government information well into the 21st century. It replaces the aging DES, which NIST adopted in 1977 as a Federal Information Processing Standard used by federal agencies to protect sensitive, unclassified information. The 128-bit AES standard has 3.4×10^{38} possible 128-bit key variants, and it has been estimated that it would take 1,000 trillion years to crack 128-bit AES cipher text using exhaustive techniques. Keys are stored (securely) in IGLOO devices in nonvolatile flash memory. All programming files sent to the device can be authenticated by the part prior to programming to ensure that bad programming data is not loaded into the part that may possibly damage it. All programming verification is performed on-chip, ensuring that the contents of IGLOO devices remain secure.

AES decryption can also be used on the 1,024-bit FlashROM to allow for secure remote updates of the FlashROM contents. This allows for easy, secure support for subscription model products.

ISP

IGLOO devices support IEEE 1532 ISP via JTAG and require a single V_{PUMP} voltage of 3.3 V during programming. In addition, programming via a microcontroller in a target system can be achieved.

IGLOO devices can be programmed in system when the device is using 1.5 V supply voltage to the FPGA core. IGLOO V2 devices can operate using either 1.2 V core voltage or 1.5 V core voltage hence when 1.2 V is used the device cannot be reprogrammed in the system although it has lower Active power than with 1.5 V core voltage.

IGLOO device can not be programmed in-system when the device is in Flash*Freeze mode. The IGLOO device should exit Flash*Freeze mode and be in normal operation for programming to start.

Programming operations could be achieved when the device is in normal operating mode and 1.5 V core voltage is used.

8. The AGL030 device does not support AES decryption.

JTAG 1532

IGLOO devices support the JTAG-based IEEE 1532 standard for ISP. In order to start JTAG operations the IGLOO device should exit Flash*Freeze mode and be in normal operation for before starting to send JTAG commands to the device. As part of this support, when a IGLOO device is in an unprogrammed state, all user I/O pins are disabled. This is achieved by keeping the global IO_EN signal deactivated, which also has the effect of disabling the input buffers. The SAMPLE/PRELOAD instruction captures the status of pads in parallel and shifts them out as new data is shifted in for loading into the Boundary Scan Register. When the IGLOO device is in an unprogrammed state, the SAMPLE/PRELOAD instruction has no effect on I/O status; however, it will continue to shift in new data to be loaded into the BSR. Therefore, when SAMPLE/PRELOAD is used on an unprogrammed device, the BSR will be loaded with undefined data.

For JTAG timing information on setup, hold, and fall times, refer to the *FlashPro User's Guide*.

Boundary Scan

IGLOO devices are compatible with IEEE Standard 1149.1, which defines a hardware architecture and the set of mechanisms for boundary scan testing. JTAG operations are used during boundary scan testing; therefore, the Flash*Freeze pin must be deasserted for successful boundary scan operations. The basic IGLOO boundary scan logic circuit is composed of the TAP controller, test data registers, and instruction register (Figure 2-45 on page 2-65). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD, and BYPASS) and the optional IDCODE instruction (Table 2-34).

Table 2-34 • **Boundary Scan Opcodes**

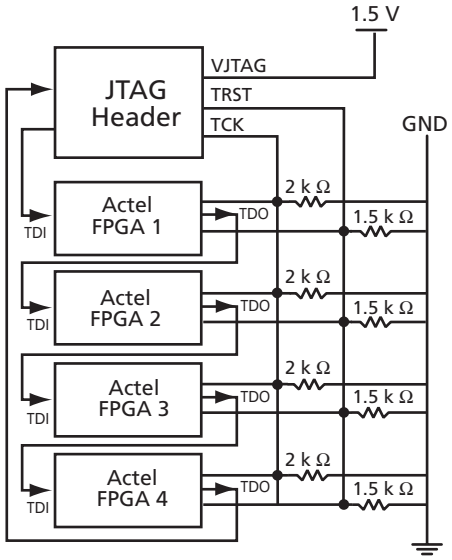
	Hex Opcode
EXTEST	00
HIGHZ	07
USERCODE	0E
SAMPLE/PRELOAD	01
IDCODE	0F
CLAMP	05
BYPASS	FF

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI, TDO (test data input and output), TMS (test mode selector), and TRST (test reset input). TMS, TDI, and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary scan test usage. Refer to the "JTAG Pins" section on page 2-60 for pull-up/down recommendations for TDO and TCK pins. Table 2-35 gives pull-down recommendations for the TRST and TCK pins.

Table 2-35 • **TRST and TCK Pull-Down Recommendations**

V_{JTAG}	Tie-Off Resistance*
V_{JTAG} at 3.3 V	200 Ω to 1 kΩ
V_{JTAG} at 2.5 V	200 Ω to 1 kΩ
V_{JTAG} at 1.8 V	500 Ω to 1 kΩ
V_{JTAG} at 1.5 V	500 Ω to 1 kΩ

Note: **Equivalent parallel resistance if more than one device is on JTAG chain (Figure 2-43)*



Note: *TCK is correctly wired with an equivalent tie-off resistance of 500 Ω, which satisfies the table for V_{JTAG} of 1.5 V. The resistor values for TRST are not appropriate in this case, as the tie-off resistance of 375 Ω is below the recommended minimum for V_{JTAG} = 1.5 V, but would be appropriate for a V_{JTAG} setting of 2.5 V or 3.3 V.*

Figure 2-43 • **Parallel Resistance on JTAG Chain of Devices**

The TAP controller is a 4-bit state machine (16 states) that operates as shown in Figure 2-44. The 1s and 0s represent the values that must be present on TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain HIGH for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

IGLOO devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number, and version). The boundary scan register observes and controls the state of each I/O pin. Each I/O cell has three boundary scan register cells, each with serial-in, serial-out, parallel-in, and parallel-out pins.

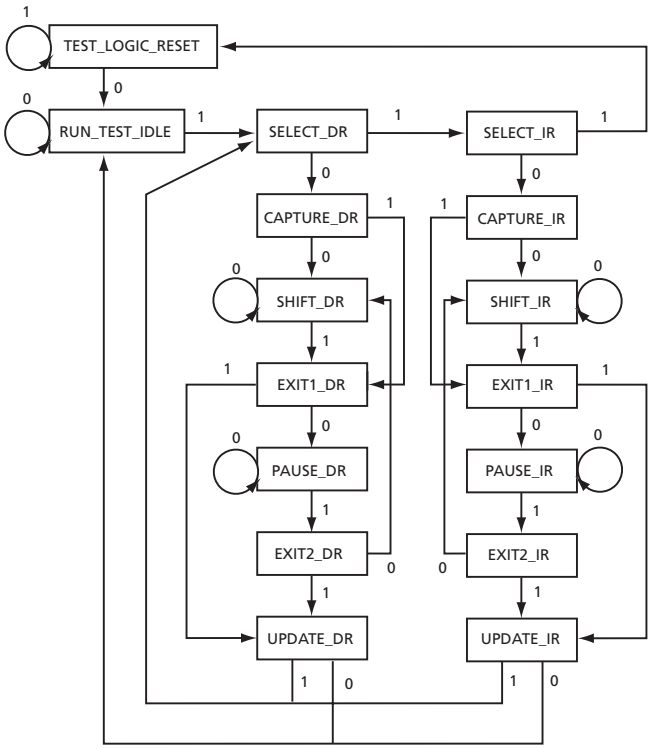


Figure 2-44 • **TAP State Machine**

The serial pins are used to serially connect all the boundary scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic I/O tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

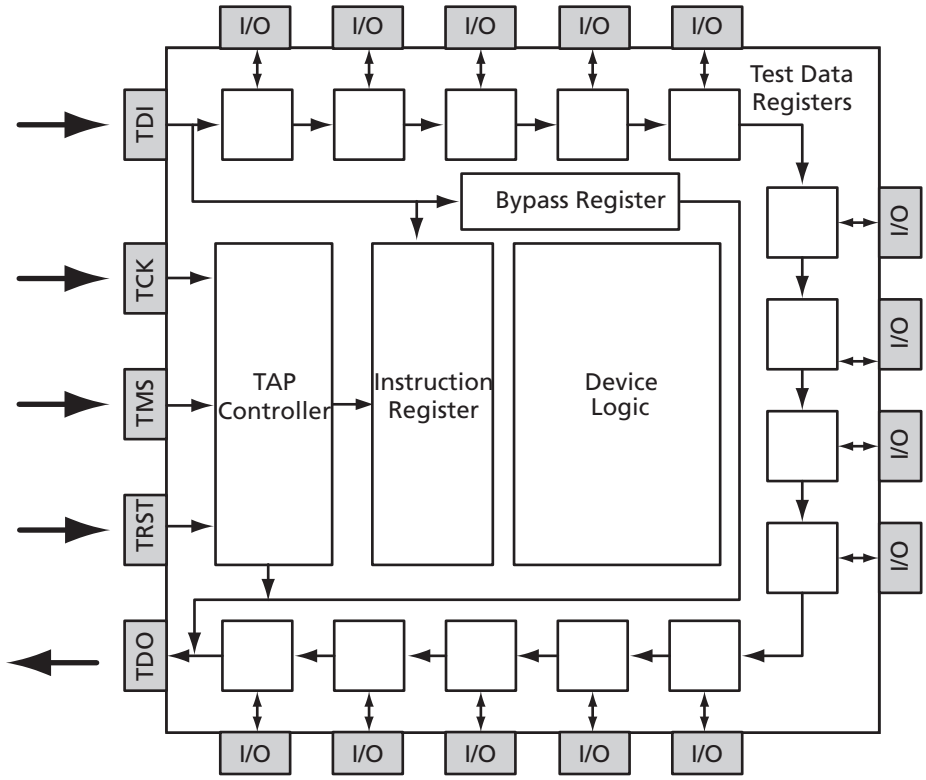


Figure 2-45 • **Boundary Scan Chain in IGLOO**

DC and Switching Characteristics

General Specifications

DC and switching characteristics for –F speed grade targets are based only on simulation.

The characteristics provided for the –F speed grade are subject to change after establishing FPGA specifications. Some restrictions might be added and will be reflected in future revisions of this document. The –F speed grade is only supported in the commercial temperature range.

Operating Conditions

Stresses beyond those listed in Table 3-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 3-2 on page 3-2 is not implied.

Table 3-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
V_{CC}	DC core supply voltage	–0.3 to 1.65	V
V_{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V_{PUMP}	Programming voltage	–0.3 to 3.75	V
V_{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V_{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V_{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage Temperature	–65 to +150	°C
T_J [2]	Junction Temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 3-4 on page 3-3.*
2. *For Flash programming and retention maximum limits refer to Table 3-3 on page 3-3 and for recommended operating limits refer to Table 3-2 on page 3-2.*

Table 3-2 • **Recommended Operating Conditions**

Symbol	Parameter		Commercial	Industrial	Units
T_J	Junction Temperature		0 to 70	–40 to +85	°C
V_{CC}	1.5 V DC core supply voltage[1]		1.425 to 1.575	1.425 to 1.575	V
	1.2 V DC core supply voltage[2]		1.14 to 1.26	1.14 to 1.26	V
V_{JTAG}	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation[5]	0 to 3.45V	0 to 3.45V	V
V_{CCPLL}	Analog power supply (PLL)	1.5 V DC core supply voltage[1]	1.4 to 1.6	1.4 to 1.6	V
		1.2 V DC core supply voltage[2]	1.14 to 1.26	1.14 to 1.26	V
V_{CCI} and VMV	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *For IGLOO V2 or V5 devices*
2. *For IGLOO V2 devices only*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 3-22 on page 3-19. VMV and V_{CCI} should be at the same voltage within a given I/O bank.*
4. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
5. *V_{PUMP} can be left floating during operation (not programming mode).*

Table 3-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C) [2]	Maximum Operating Junction Temperature T_J (°C) [2]
Commercial	500	20 years	110	110
Industrial	500	20 years	110	110

Notes:

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 3-1 on page 3-1 and Table 3-2 for device operating conditions and absolute limits.*

Table 3-4 • **Overshoot and Undershoot Limits (as measured on quiet I/Os)[1]**

V_{CCI} and VMV	Average V_{CCI}–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table refers only to overshoot/undershoot limits for simultaneous switching I/Os and does not provide PCI overshoot/undershoot limits.*

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every IGLOO device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 3-1.

There are five regions to consider during power-up.

IGLOO I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points (Figure 3-1).
2. $V_{CCI} > V_{CC} – 0.75$ V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

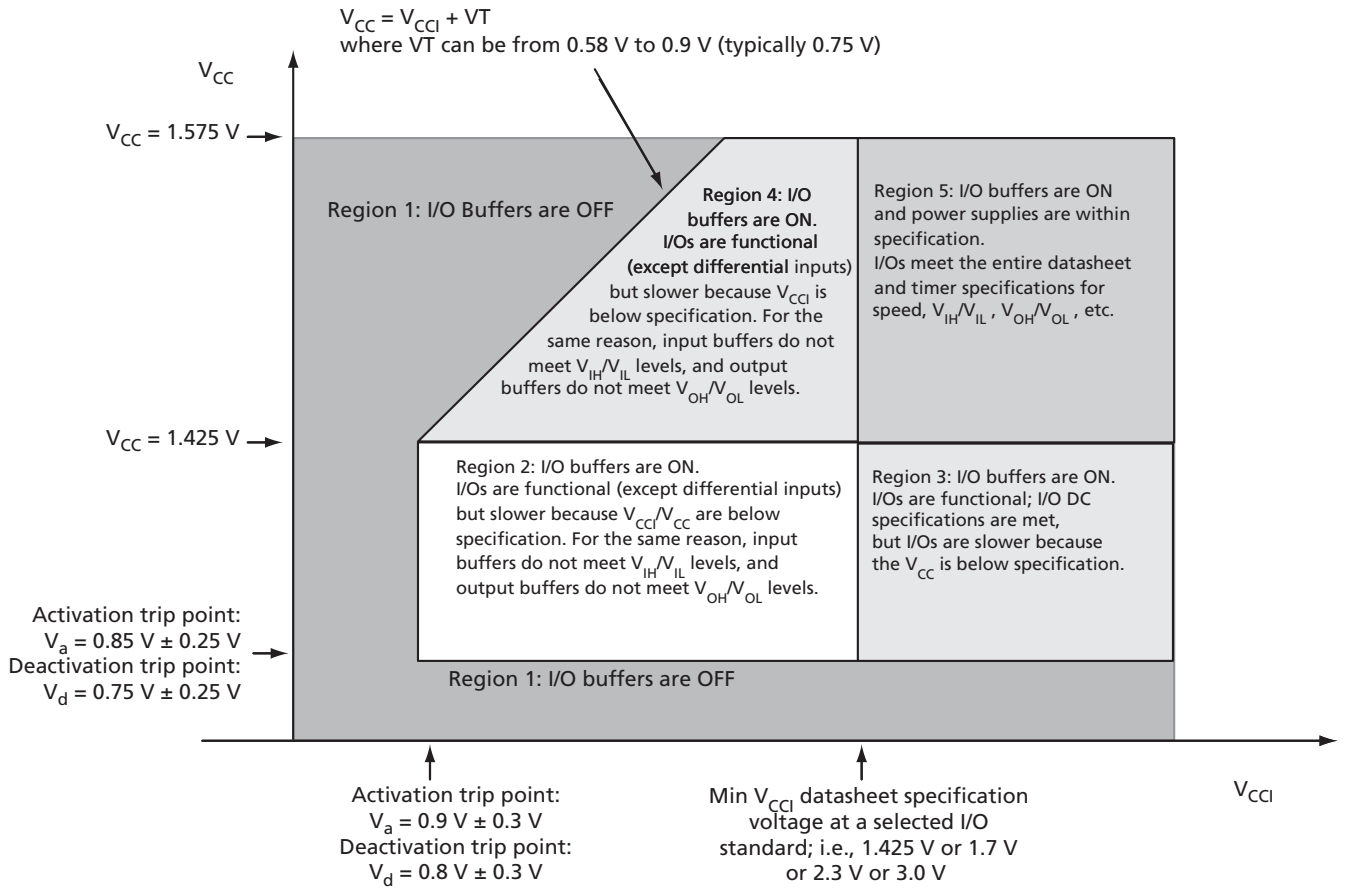


Figure 3-1 • **I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 3-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A \qquad \text{EQ 3-1}$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 3-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 3-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110\text{°C} - 70\text{°C}}{20.5\text{°C/W}} = 1.951\ \text{W} \qquad \text{EQ 3-2}$$

Table 3-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft./min.	θ_{ja} 500 ft./min.	Units
Quad Flat No Lead	AGL030	132	0.4	21.4	16.8	15.3	C/W
	AGL060	132	0.3	21.2	16.6	15.0	C/W
	AGL125	132	0.2	21.1	16.5	14.9	C/W
	AGL250	132	0.1	21.0	16.4	14.8	C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CSP)	All devices	196		57.8	47.6	43.3	C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	C/W
	See note*	256	3.8	26.6	22.8	21.5	C/W
	See note*	484	3.2	20.5	17.0	15.9	C/W
	See note*	896	2.4	13.6	10.4	9.4	C/W
	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

Note: **This information applies to all IGLOO devices except those listed below. Detailed device/package thermal information for all IGLOO devices will be available in future revisions of the datasheet.*

Temperature and Voltage Derating Factors

Table 3-6 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 70°C, V_{CC} = 1.425 V) For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.425	0.89	0.94	0.96	1.00	1.01	1.03
1.5	0.82	0.87	0.89	0.93	0.94	0.96
1.575	0.77	0.81	0.83	0.87	0.88	0.90

Table 3-7 • **Temperature and Voltage Derating Factors for Timing Delays (Normalized to T_J = 70°C, V_{CC} = 1.14 V) For IGLOO V2, 1.2 V DC Core Supply Voltage**

Array Voltage V_{CC} (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	110°C
1.14	0.91	0.94	0.97	1.00	1.01	1.02
1.2	0.79	0.82	0.84	0.87	0.88	0.89
1.26	0.71	0.74	0.76	0.78	0.79	0.80

Calculating Power Dissipation

Quiescent Supply Current

Table 3-8 • **Quiescent Supply Current (I_{DD}), IGLOO Flash*Freeze Mode†**

	Core Voltage	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	8	14	28	60	102	µA
	1.5 V	6	10	18	34	72	127	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, VMV, and I/O static currents in worst-case conditions.*

Table 3-9 • **Quiescent Supply Current (I_{DD}), IGLOO Sleep Mode (V_{CC} = 0 V)†**

	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
V_{CCI} = 1.5 V (all banks) Typical (25°C)	5	5	5	9	9	9	µA
V_{CCI} = 1.8 V (all banks) Typical (25°C)	5	5	5	11	11	11	µA
V_{CCI} = 2.5 V (all banks) Typical (25°C)	8	8	8	15	15	15	µA
V_{CCI} = 3.3 V (all banks) Typical (25°C)	10	10	10	20	20	20	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution.*

Table 3-10 • **Quiescent Supply Current (I_{DD}), IGLOO Shutdown Mode (V_{CC}, V_{CCI} = 0 V)†**

	Core Voltage	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	µA

Note: *†I_{DD} includes V_{CC}, V_{PUMP}, V_{CCI}, and VMV currents. Values do not include I/O static contribution.*

Table 3-11 • **Quiescent Supply Current, No IGLOO Flash*Freeze Mode[1]**

	Core Voltage	AGL030	AGL060	AGL125	AGL250	AGL600	AGL1000	Units
I_{CCA} Current[2]								
Typical (25°C)	1.2V	14	18	24	38	70	112	µA
	1.5V	16	20	28	44	82	137	µA
I_{CCI} or I_{JTAG} Current[3, 4]								
3.3 V Typical (25°C)	1.2 V / 1.5 V	5	5	5	5	5	5	µA
2.5 V Typical (25°C)	1.2 V / 1.5 V	4	4	4	4	4	4	µA
1.8 V Typical (25°C)	1.2 V / 1.5 V	3	3	3	3	3	3	µA
1.5 V Typical (25°C)	1.2 V / 1.5 V	2	2	2	2	2	2	µA

Notes:

1. *To calculate total device I_{DD}, multiply the number of banks used by I_{CCI} and add I_{CCA} contribution.*
2. *Includes V_{CC} and V_{PUMP} currents*
3. *Per V_{CCI} or V_{JTAG} bank*
4. *Values do not include I/O static contribution.*

Power Per I/O Pin

Table 3-12 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Advanced I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-13 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.72
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-14 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW)[1]	Dynamic Power P_{AC9} (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.79
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. *P_{DC2} is the static power (where applicable) measured on VMV.*
2. *P_{AC9} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-15 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-16 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings[1] Applicable to Standard Plus I/O Banks**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and VMV.*

Table 3-17 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings[1] Applicable to Standard I/O Banks**

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW)[2]	Dynamic Power P_{AC10} (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	431.08
2.5 V LVCMOS	35	2.5	–	247.36
1.8 V LVCMOS	35	1.8	–	128.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	89.46

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on V_{CC} and VMV.*

Power Consumption of Various Internal Resources

Table 3-18 • **Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030
P_{AC1}	Clock contribution of a Global Rib	14.48	12.77	11.03	11.03	9.3	9.3
P_{AC2}	Clock contribution of a Global Spine	2.48	1.85	1.58	0.81	0.81	0.41
P_{AC3}	Clock contribution of a VersaTile row	0.81					
P_{AC4}	Clock contribution of a VersaTile used as a sequential module	0.11					
P_{AC5}	First contribution of a VersaTile used as a sequential module	0.057					
P_{AC6}	Second contribution of a VersaTile used as a sequential module	0.207					
P_{AC7}	Contribution of a VersaTile used as a combinatorial Module	0.17					
P_{AC8}	Average contribution of a routing net	0.7					
P_{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 3-12 on page 3-7 through Table 3-14 on page 3-8.					
P_{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 3-15 on page 3-9 through Table 3-17 on page 3-9.					
P_{AC11}	Average contribution of a RAM block during a read operation	25.00					
P_{AC12}	Average contribution of a RAM block during a write operation	30.00					
P_{AC13}	Static PLL contribution	2.55 mW					
P_{AC14}	Dynamic contribution for PLL	2.60					

Note: **For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Table 3-19 • **Different Components Contributing to Dynamic Power Consumption in IGLOO Devices For IGLOO V2, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Dynamic Power (µW/MHz)					
		AGL1000	AGL600	AGL250	AGL125	AGL060	AGL030
PAC1	Clock contribution of a Global Rib	9.28	8.19	7.07	7.07	5.96	5.96
PAC2	Clock contribution of a Global Spine	1.59	1.19	1.01	0.52	0.52	0.26
PAC3	Clock contribution of a VersaTile row	0.52	0.52	0.52	0.519	0.519	0.519
PAC4	Clock contribution of a VersaTile used as a sequential module	0.07	0.07	0.07	0.071	0.071	0.071
PAC5	First contribution of a VersaTile used as a sequential module	0.05	0.05	0.05	0.045	0.045	0.045
PAC6	Second contribution of a VersaTile used as a sequential module	0.19	0.19	0.19	0.186	0.186	0.186
PAC7	Contribution of a VersaTile used as a combinatorial Module	0.11	0.11	0.11	0.109	0.109	0.109
PAC8	Average contribution of a routing net	0.45	0.45	0.45	0.449	0.449	0.449
PAC9	Contribution of an I/O input pin (standard dependent)	See Table 3-12 on page 3-7 through Table 3-14 on page 3-8.					
PAC10	Contribution of an I/O output pin (standard dependent)	See Table 3-15 on page 3-9 through Table 3-17 on page 3-9.					
PAC11	Average contribution of a RAM block during a read operation	25.00					
PAC12	Average contribution of a RAM block during a write operation	30.00					
PAC13	Static PLL contribution	2.55mW					
PAC14	Dynamic contribution for PLL	2.60					

Note: **For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Libero IDE.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 3-20 on page 3-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 3-21 on page 3-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 3-21 on page 3-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guideline are provided in Table 3-20 on page 3-14.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in Table 3-20 on page 3-14.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-20 on page 3-14.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-20 on page 3-14.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution—P_{NET}

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 3-20 on page 3-14.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—P_{INPUTS}

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-20 on page 3-14.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 3-20 on page 3-14.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 3-21 on page 3-14.

F_{CLK} is the global clock signal frequency.

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 3-21 on page 3-14.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{AC13} + P_{AC14} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 3-20 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 3-21 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

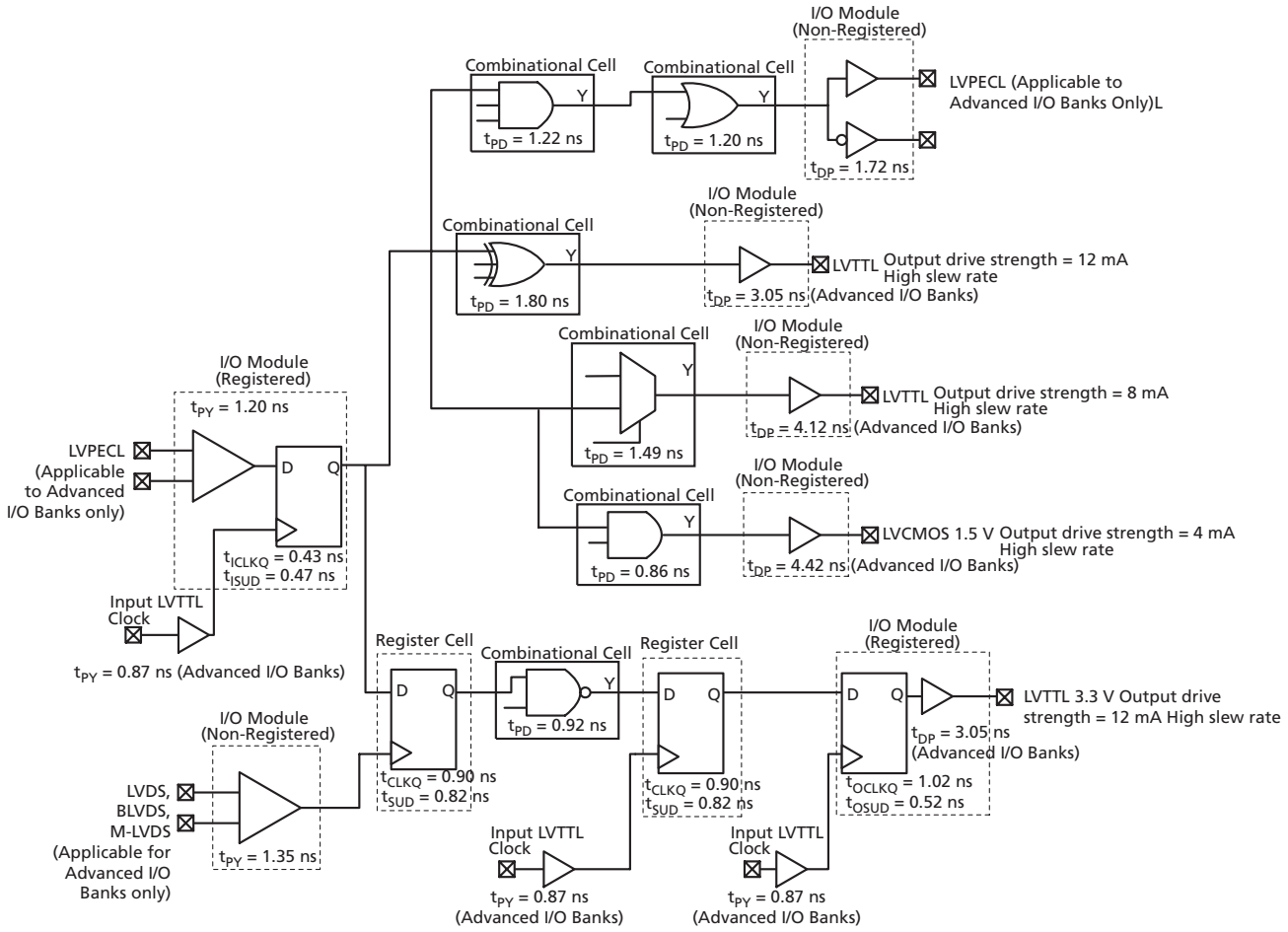


Figure 3-2 • **Timing Model**
Operating Conditions: Std. Speed, Commercial Temperature Range (T_J = 70°C), Worst Case V_{CC} = 1.425 V, for DC 1.5V Core Voltage, Applicable to V2 and V5 Devices

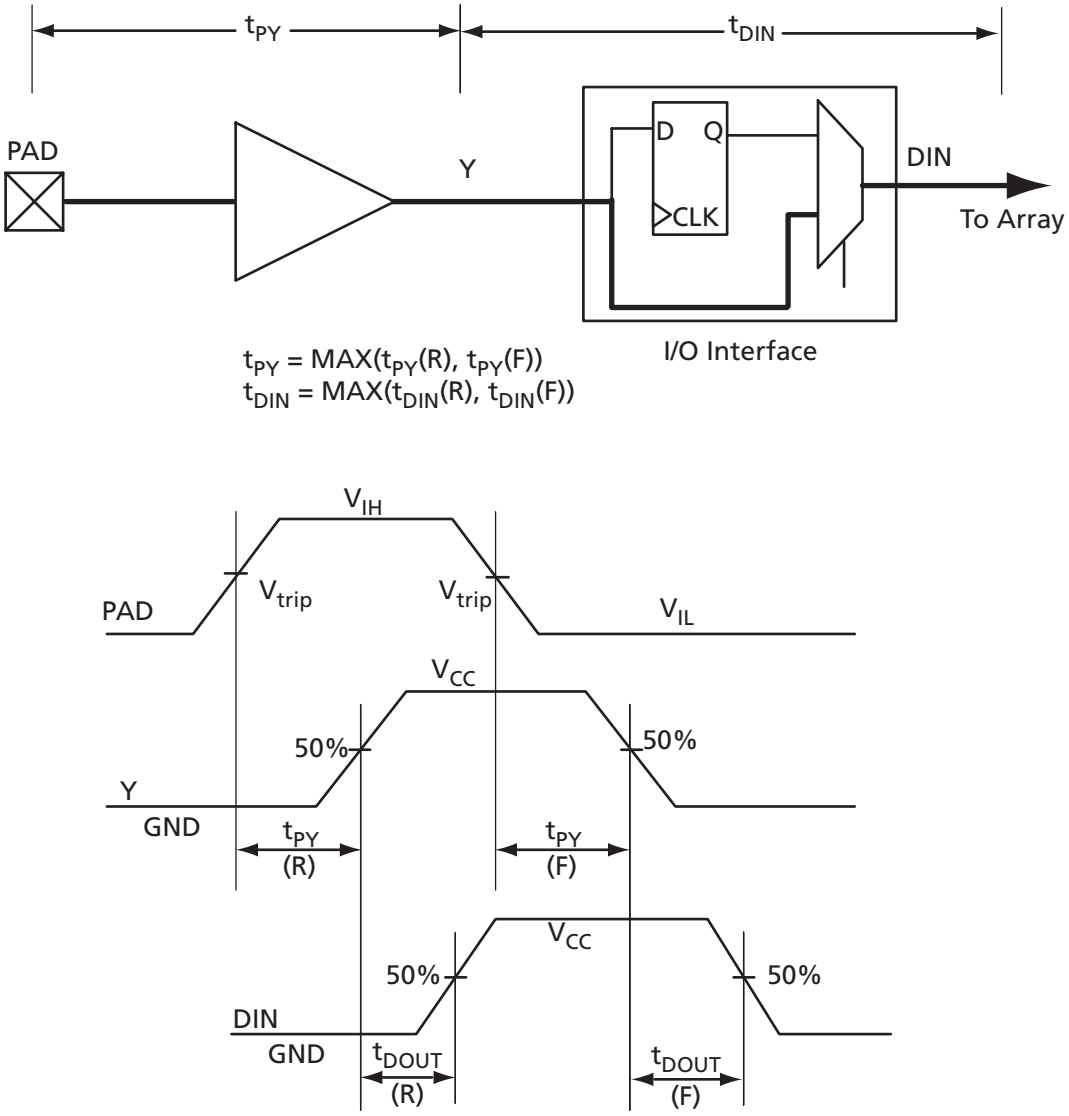


Figure 3-3 • **Input Buffer Timing Model and Delays (example)**

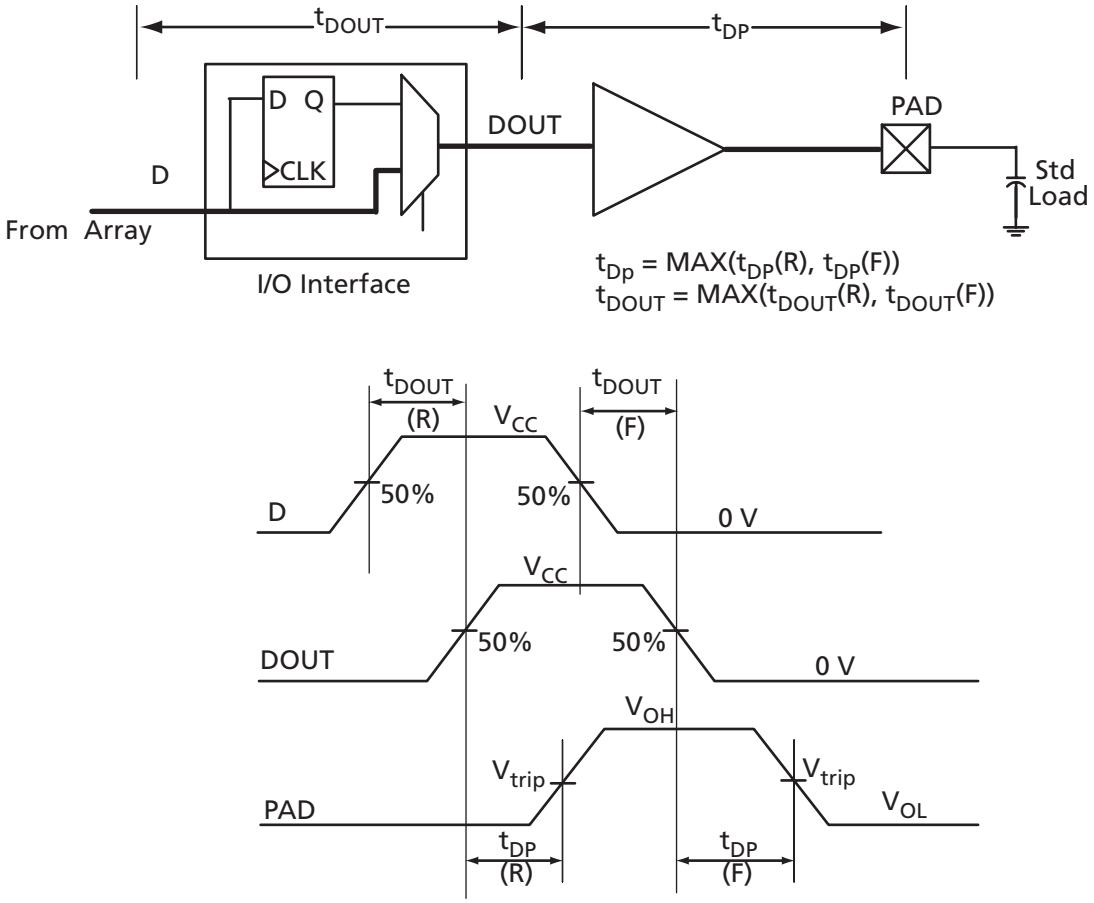


Figure 3-4 • **Output Buffer Model and Delays (example)**

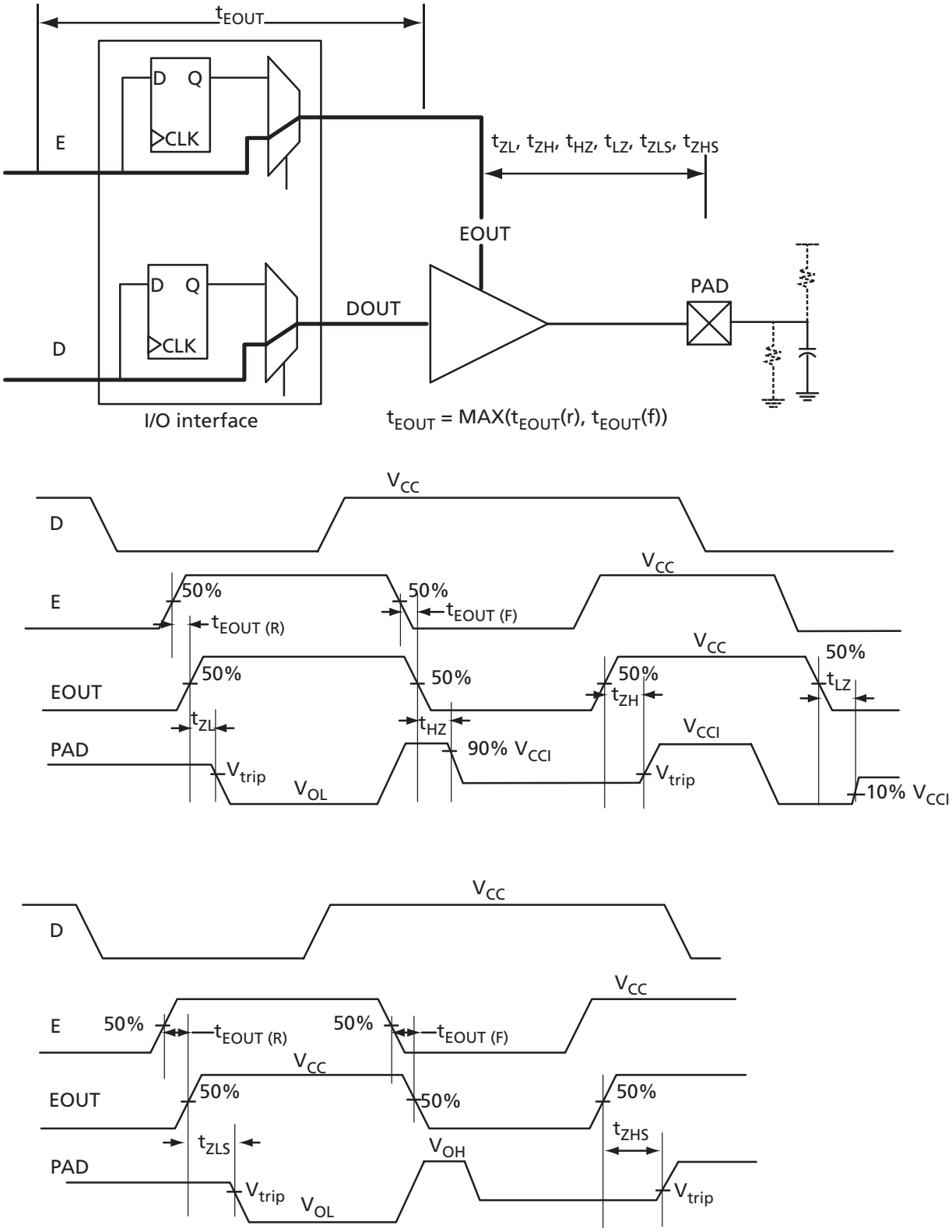


Figure 3-5 • **Tristate Output Buffer Timing Model and Delays (example)**

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 3-22 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: *Currents are measured at 85°C junction temperature.*

Table 3-23 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: *Currents are measured at 85°C junction temperature.*

Table 3-24 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard I/O Banks**

I/O Standard	Drive Strength	Slew Rate	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2

Note: *Currents are measured at 85°C junction temperature.*

Table 3-25 • **Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions**

	Commercial[1]		Industrial[2]	
	I_{IL}	I_{IH}	I_{IL}	I_{IH}
DC I/O Standards	**µA**	**µA**	**µA**	**µA**
3.3 V LVTTL /3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. *Commercial range (0°C < T_J < 70°C)*
2. *Industrial range (–40°C < T_J < 85°C)*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 3-26 • **Summary of AC Measuring Points**

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)
3.3 V PCI-X	0.285 * V_{CCI} (RR)
	0.615 * V_{CCI} (FF)

Table 3-27 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—HIGH to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to HIGH
t_{LZ}	Enable to Pad delay through the Output Buffer—LOW to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to LOW
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to HIGH
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 3-28 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V Applicable Advanced I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.98	3.05	0.19	0.87	0.67	3.11	2.49	2.74	3.13	6.74	6.12	ns
2.5 V LVCMOS	12 mA	High	35pF	–	0.98	3.08	0.19	1.10	0.67	3.14	2.96	2.81	3.01	6.77	6.59	ns
1.8 V LVCMOS	12 mA	High	35pF	–	0.98	3.05	0.19	1.03	0.67	3.11	2.65	3.11	3.49	6.74	6.28	ns
1.5 V LVCMOS	12 mA	High	35pF	–	0.98	3.47	0.19	1.20	0.67	3.54	3.07	3.29	3.58	7.17	6.70	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	0.98	2.38	0.19	0.75	0.67	2.43	1.82	2.74	3.13	6.06	5.45	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	0.98	2.38	0.19	0.72	0.67	2.43	1.82	2.74	3.13	6.06	5.45	ns
LVDS	24 mA	High	–	–	0.98	1.72	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.98	1.72	0.19	1.20	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Table 3-29 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V Applicable Standard Plus I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.98	2.69	0.19	0.87	0.67	2.74	2.22	2.43	2.87	6.37	5.85	ns
2.5 V LVCMOS	12 mA	High	35pF	–	0.98	2.72	0.19	1.11	0.67	2.77	2.65	2.45	2.77	6.40	6.28	ns
1.8 V LVCMOS	8 mA	High	35pF	–	0.98	3.35	0.19	1.04	0.67	3.20	3.35	2.53	2.74	6.83	6.98	ns
1.5 V LVCMOS	4 mA	High	35pF	–	0.98	3.96	0.19	1.21	0.67	3.69	3.96	2.60	2.75	7.32	7.59	ns
3.3 V PCI	Per PCI spec	High	10pF	25 2	0.98	2.02	0.19	0.75	0.67	2.06	1.54	2.43	2.87	5.69	5.17	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 2	0.98	2.02	0.19	0.72	0.67	2.06	1.54	2.43	2.87	5.69	5.17	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Table 3-30 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.425 V, Worst Case V_{CCI} = 3.0 V Applicable Standard I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	35 pF	–	0.98	2.18	0.19	0.85	0.67	2.22	1.76	2.01	2.32	ns
2.5 V LVCMOS	8 mA	High	35pF	–	0.98	2.22	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
1.8 V LVCMOS	4 mA	High	35pF	–	0.98	5.07	0.19	1.00	0.67	4.36	5.07	2.02	2.12	ns
1.5 V LVCMOS	2 mA	High	35pF	–	0.98	6.08	0.19	1.17	0.67	5.08	6.08	2.05	2.08	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Table 3-31 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI} = 3.0 V Applicable Advanced I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	1.57	3.57	0.26	0.98	1.11	3.64	2.97	3.23	3.92	9.45	8.78	ns
2.5 V LVCMOS	12 mA	High	35pF	–	1.57	3.56	0.26	1.20	1.11	3.63	3.39	3.28	3.77	9.44	9.20	ns
1.8 V LVCMOS	12 mA	High	35pF	–	1.57	3.47	0.26	1.11	1.11	3.53	3.05	3.56	4.17	9.34	8.85	ns
1.5 V LVCMOS	12 mA	High	35pF	–	1.57	3.85	0.26	1.27	1.11	3.92	3.45	3.74	4.21	9.73	9.26	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	1.57	2.90	0.26	0.86	1.11	2.95	2.29	3.23	3.92	8.76	8.10	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	1.57	2.90	0.26	0.86	1.11	2.95	2.29	3.23	3.92	8.76	8.10	ns
LVDS	24 mA	High	–	–	1.57	2.19	0.26	1.52	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	1.57	2.24	0.26	1.37	–	–	–	–	–	–	–	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Table 3-32 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI} = 3.0 V Applicable Standard Plus I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	1.57	3.19	0.26	0.97	1.11	3.25	2.66	2.91	3.62	9.06	8.46	ns
2.5 V LVCMOS	12 mA	High	35pF	–	1.57	3.20	0.26	1.20	1.11	3.25	3.04	2.92	3.50	9.06	8.85	ns
1.8 V LVCMOS	8 mA	High	35pF	–	1.57	3.71	0.26	1.11	1.11	3.60	3.71	2.98	3.38	9.41	9.52	ns
1.5 V LVCMOS	4 mA	High	35pF	–	1.57	4.30	0.26	1.27	1.11	4.06	4.30	3.05	3.36	9.87	10.11	ns
3.3 V PCI	Per PCI spec	High	10pF	25 [2]	1.57	2.52	0.26	0.85	1.11	2.57	1.98	2.91	3.62	8.37	7.78	ns
3.3 V PCI-X	Per PCI-X spec	High	10pF	25 [2]	1.57	2.52	0.26	0.85	1.11	2.57	1.98	2.91	3.62	8.37	7.78	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Table 3-33 • **Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case V_{CC} = 1.14 V, Worst Case V_{CCI} = 3.0 V Applicable Standard I/O banks**

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	35 pF	–	1.57	2.66	0.26	0.94	1.11	2.71	2.18	2.39	2.94	ns
2.5 V LVCMOS	8 mA	High	35pF	–	1.57	2.66	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
1.8 V LVCMOS	4 mA	High	35pF	–	1.57	5.42	0.26	1.08	1.11	4.72	5.42	2.37	2.61	ns
1.5 V LVCMOS	2 mA	High	35pF	–	1.57	6.41	0.26	1.22	1.11	5.41	6.41	2.39	2.54	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*
2. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 3-10 on page 3-55 for connectivity. This resistor is not required during normal operation.*

Detailed I/O DC Characteristics

Table 3-34 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 3-35 • **I/O Output Buffer Maximum Resistances[1] Applicable to Advanced I/O Banks**

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL/ 3.3V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 3-36 • **I/O Output Buffer Maximum Resistances[1] Applicable to Standard Plus I/O Banks**

Standard	Drive Strength	RPULL-DOWN (Ω)[2]	RPULL-UP (Ω)[3]
3.3 V LVTTL/ 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	0	0

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 3-37 • **I/O Output Buffer Maximum Resistances[1] Applicable to Standard I/O Banks**

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
2.5V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI}, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at http://www.actel.com/download/ibis/default.aspx.*
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} – V_{OHspec}) / I_{OHspec}$

Table 3-38 • **I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

V_{CCI}	$R_{(WEAK\ PULL-UP)}$[1] (Ω)		$R_{(WEAK\ PULL-DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL-UP-MAX)} = (V_{OLspec}) / I_{(WEAK\ PULL-UP-MIN)}$
2. $R_{(WEAK\ PULL-UP-MAX)} = (V_{CCImax} – V_{OHspec}) / I_{(WEAK\ PULL-UP-MIN)}$

Table 3-39 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Advanced I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: **T_J = 100°C*

Table 3-40 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Standard Plus I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Note: **T_J = 100°C*

Table 3-41 • **I/O Short Currents I_{OSH}/I_{OSL} Applicable to Standard I/O Banks**

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Note: **T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C, the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 3-42 • **Short Current Event Duration before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months

Table 3-43 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/BLVDS.M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: **The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 3-44 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	–0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-45 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	–0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	–0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-46 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

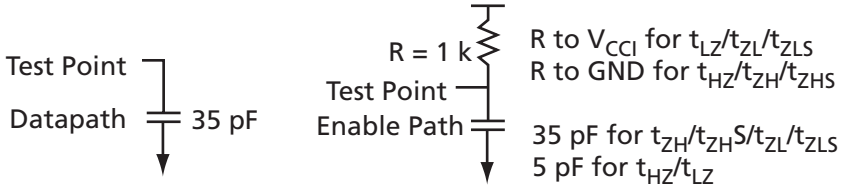


Figure 3-6 • **AC Loading**

Table 3-47 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 3-48 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	8.32	0.19	0.87	0.67	8.48	7.20	2.30	2.25	12.11	10.83	ns
6 mA	Std.	0.98	6.01	0.19	0.87	0.67	6.12	5.19	2.56	2.70	9.75	8.82	ns
8 mA	Std.	0.98	6.01	0.19	0.87	0.67	6.12	5.19	2.56	2.70	9.75	8.82	ns
12 mA	Std.	0.98	4.69	0.19	0.87	0.67	4.77	4.11	2.74	2.99	8.40	7.74	ns
16 mA	Std.	0.98	4.40	0.19	0.87	0.67	4.48	3.87	2.77	3.07	8.11	7.50	ns
24 mA	Std.	0.98	4.11	0.19	0.87	0.67	4.19	3.86	2.82	3.36	7.82	7.49	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-49 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	6.25	0.19	0.87	0.67	6.36	5.41	2.31	2.38	9.99	9.04	ns
6 mA	Std.	0.98	4.12	0.19	0.87	0.67	4.19	3.46	2.57	2.84	7.82	7.09	ns
8 mA	Std.	0.98	4.12	0.19	0.87	0.67	4.19	3.46	2.57	2.84	7.82	7.09	ns
12 mA	Std.	0.98	3.05	0.19	0.87	0.67	3.11	2.49	2.74	3.13	6.74	6.12	ns
16 mA	Std.	0.98	2.90	0.19	0.87	0.67	2.95	2.29	2.78	3.20	6.58	5.92	ns
24 mA	Std.	0.98	2.70	0.19	0.87	0.67	2.75	1.95	2.83	3.50	6.38	5.58	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-50 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	7.78	0.19	0.87	0.67	7.92	6.75	2.03	2.08	11.55	10.38	ns
6 mA	Std.	0.98	5.47	0.19	0.87	0.67	5.58	4.80	2.27	2.49	9.21	8.43	ns
8 mA	Std.	0.98	5.47	0.19	0.87	0.67	5.58	4.80	2.27	2.49	9.21	8.43	ns
12 mA	Std.	0.98	4.19	0.19	0.87	0.67	4.27	3.74	2.43	2.75	7.90	7.37	ns
16 mA	Std.	0.98	4.19	0.19	0.87	0.67	4.27	3.74	2.43	2.75	7.90	7.37	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-51 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	5.82	0.19	0.87	0.67	5.92	5.08	2.03	2.19	9.55	8.71	ns
6 mA	Std.	0.98	3.72	0.19	0.87	0.67	3.79	3.17	2.26	2.60	7.42	6.80	ns
8 mA	Std.	0.98	3.72	0.19	0.87	0.67	3.79	3.17	2.26	2.60	7.42	6.80	ns
12 mA	Std.	0.98	2.69	0.19	0.87	0.67	2.74	2.22	2.43	2.87	6.37	5.85	ns
16 mA	Std.	0.98	2.69	0.19	0.87	0.67	2.74	2.22	2.43	2.87	6.37	5.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-52 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	4.52	0.19	0.85	0.67	4.60	4.03	1.79	1.83	ns
4 mA	Std.	0.98	4.52	0.19	0.85	0.67	4.60	4.03	1.79	1.83	ns
6 mA	Std.	0.98	3.59	0.19	0.85	0.67	3.66	3.30	2.01	2.23	ns
8 mA	Std.	0.98	3.59	0.19	0.85	0.67	3.66	3.30	2.01	2.23	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-53 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	2.82	0.19	0.85	0.67	2.87	2.36	1.78	1.92	ns
4 mA	Std.	0.98	2.82	0.19	0.85	0.67	2.87	2.36	1.78	1.92	ns
6 mA	Std.	0.98	2.18	0.19	0.85	0.67	2.22	1.76	2.01	2.32	ns
8 mA	Std.	0.98	2.18	0.19	0.85	0.67	2.22	1.76	2.01	2.32	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Applies to 1.2 V DC Core Voltage

Table 3-54 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	8.84	0.26	0.98	1.11	9.01	7.68	2.80	3.01	14.82	13.49	ns
6 mA	Std.	1.57	6.53	0.26	0.98	1.11	6.65	5.67	3.05	3.46	12.46	11.48	ns
8 mA	Std.	1.57	6.53	0.26	0.98	1.11	6.65	5.67	3.05	3.46	12.46	11.48	ns
12 mA	Std.	1.57	5.21	0.26	0.98	1.11	5.31	4.59	3.23	3.75	11.12	10.40	ns
16 mA	Std.	1.57	4.92	0.26	0.98	1.11	5.01	4.36	3.27	3.83	10.82	10.16	ns
24 mA	Std.	1.57	4.64	0.26	0.98	1.11	4.72	4.34	3.31	4.12	10.53	10.15	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-55 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	6.76	0.26	0.98	1.11	6.89	5.89	2.80	3.16	12.70	11.70	ns
6 mA	Std.	1.57	4.63	0.26	0.98	1.11	4.72	3.94	3.06	3.62	10.53	9.75	ns
8 mA	Std.	1.57	4.63	0.26	0.98	1.11	4.72	3.94	3.06	3.62	10.53	9.75	ns
12 mA	Std.	1.57	3.57	0.26	0.98	1.11	3.64	2.97	3.23	3.92	9.45	8.78	ns
16 mA	Std.	1.57	3.41	0.26	0.98	1.11	3.48	2.77	3.27	3.99	9.29	8.57	ns
24 mA	Std.	1.57	3.22	0.26	0.98	1.11	3.28	2.43	3.32	4.29	9.09	8.23	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-56 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	8.28	0.26	0.97	1.11	8.43	7.18	2.52	2.81	14.24	12.99	ns
6 mA	Std.	1.57	5.98	0.26	0.97	1.11	6.09	5.23	2.75	3.22	11.89	11.04	ns
8 mA	Std.	1.57	5.98	0.26	0.97	1.11	6.09	5.23	2.75	3.22	11.89	11.04	ns
12 mA	Std.	1.57	4.69	0.26	0.97	1.11	4.78	4.18	2.92	3.49	10.59	9.98	ns
16 mA	Std.	1.57	4.69	0.26	0.97	1.11	4.78	4.18	2.92	3.49	10.59	9.98	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-57 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	6.32	0.26	0.97	1.11	6.43	5.52	2.52	2.94	12.24	11.33	ns
6 mA	Std.	1.57	4.22	0.26	0.97	1.11	4.30	3.61	2.75	3.36	10.11	9.42	ns
8 mA	Std.	1.57	4.22	0.26	0.97	1.11	4.30	3.61	2.75	3.36	10.11	9.42	ns
12 mA	Std.	1.57	3.19	0.26	0.97	1.11	3.25	2.66	2.91	3.62	9.06	8.46	ns
16 mA	Std.	1.57	3.19	0.26	0.97	1.11	3.25	2.66	2.91	3.62	9.06	8.46	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-58 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	5.00	0.26	0.94	1.11	5.09	4.45	2.16	2.43	ns
4 mA	Std.	1.57	5.00	0.26	0.94	1.11	5.09	4.45	2.16	2.43	ns
6 mA	Std.	1.57	4.07	0.26	0.94	1.11	4.14	3.72	2.39	2.83	ns
8 mA	Std.	1.57	4.07	0.26	0.94	1.11	4.14	3.72	2.39	2.83	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-59 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	3.29	0.26	0.94	1.11	3.35	2.78	2.16	2.54	ns
4 mA	Std.	1.57	3.29	0.26	0.94	1.11	3.35	2.78	2.16	2.54	ns
6 mA	Std.	1.57	2.66	0.26	0.94	1.11	2.71	2.18	2.39	2.94	ns
8 mA	Std.	1.57	2.66	0.26	0.94	1.11	2.71	2.18	2.39	2.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general purpose 2.5 V applications. It uses a 5 V–tolerant input buffer and push-pull output buffer.

Table 3-60 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-61 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min., V**	**Max., V**	**Min., V**	**Max., V**	**Max., V**	**Min., V**	**mA**	**mA**	**Max., mA[1]**	**Max., mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-62 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

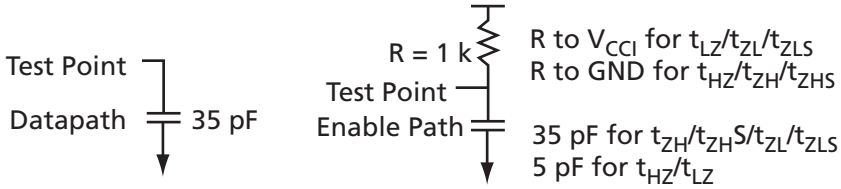


Figure 3-7 • **AC Loading**

Table 3-63 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 3-64 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	9.12	0.19	1.10	0.67	9.10	9.12	2.33	2.05	12.73	12.75	ns
6 mA	Std.	0.98	6.56	0.19	1.10	0.67	6.68	6.37	2.61	2.58	10.31	10.00	ns
8 mA	Std.	0.98	6.56	0.19	1.10	0.67	6.68	6.37	2.61	2.58	10.31	10.00	ns
12 mA	Std.	0.98	5.16	0.19	1.10	0.67	5.26	4.91	2.81	2.91	8.89	8.54	ns
16 mA	Std.	0.98	4.83	0.19	1.10	0.67	4.92	4.61	2.85	3.00	8.55	8.24	ns
24 mA	Std.	0.98	4.60	0.19	1.10	0.67	4.64	4.60	2.91	3.34	8.27	8.23	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-65 • **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	7.02	0.19	1.10	0.67	6.40	7.02	2.33	2.13	10.03	10.65	ns
6 mA	Std.	0.98	4.31	0.19	1.10	0.67	4.23	4.31	2.61	2.67	7.86	7.94	ns
8 mA	Std.	0.98	4.31	0.19	1.10	0.67	4.23	4.31	2.61	2.67	7.86	7.94	ns
12 mA	Std.	0.98	3.08	0.19	1.10	0.67	3.14	2.96	2.81	3.01	6.77	6.59	ns
16 mA	Std.	0.98	2.92	0.19	1.10	0.67	2.97	2.68	2.85	3.10	6.60	6.31	ns
24 mA	Std.	0.98	2.72	0.19	1.10	0.67	2.77	2.19	2.91	3.45	6.40	5.82	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-66 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	8.62	0.19	1.11	0.67	8.53	8.62	2.01	1.90	12.16	12.25	ns
6 mA	Std.	0.98	5.99	0.19	1.11	0.67	6.10	5.93	2.27	2.38	9.73	9.56	ns
8 mA	Std.	0.98	5.99	0.19	1.11	0.67	6.10	5.93	2.27	2.38	9.73	9.56	ns
12 mA	Std.	0.98	4.64	0.19	1.11	0.67	4.72	4.51	2.45	2.68	8.35	8.14	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-67 • **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.98	6.63	0.19	1.11	0.67	5.97	6.63	2.01	1.97	9.60	10.26	ns
6 mA	Std.	0.98	3.97	0.19	1.11	0.67	3.83	3.97	2.27	2.46	7.46	7.60	ns
8 mA	Std.	0.98	3.97	0.19	1.11	0.67	3.83	3.97	2.27	2.46	7.46	7.60	ns
12 mA	Std.	0.98	2.72	0.19	1.11	0.67	2.77	2.65	2.45	2.77	6.40	6.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-68 • **2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	5.03	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
4 mA	Std.	0.98	5.03	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
6 mA	Std.	0.98	4.01	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
8 mA	Std.	0.98	4.01	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-69 • **2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	2.87	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
4 mA	Std.	0.98	2.87	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
6 mA	Std.	0.98	2.22	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns
8 mA	Std.	0.98	2.22	0.19	1.07	0.67	2.26	2.03	2.00	2.20	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Applies to 1.2 V Core Voltage

Table 3-70 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	9.56	0.26	1.20	1.11	9.60	9.56	2.80	2.78	15.40	15.37	ns
6 mA	Std.	1.57	7.04	0.26	1.20	1.11	7.17	6.80	3.09	3.31	12.98	12.61	ns
8 mA	Std.	1.57	7.04	0.26	1.20	1.11	7.17	6.80	3.09	3.31	12.98	12.61	ns
12 mA	Std.	1.57	5.65	0.26	1.20	1.11	5.75	5.35	3.28	3.65	11.56	11.15	ns
16 mA	Std.	1.57	5.32	0.26	1.20	1.11	5.42	5.04	3.33	3.74	11.22	10.85	ns
24 mA	Std.	1.57	5.04	0.26	1.20	1.11	5.13	5.03	3.38	4.07	10.94	10.84	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-71 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	7.45	0.26	1.20	1.11	6.89	7.45	2.80	2.89	12.69	13.26	ns
6 mA	Std.	1.57	4.74	0.26	1.20	1.11	4.72	4.74	3.09	3.43	10.52	10.55	ns
8 mA	Std.	1.57	4.74	0.26	1.20	1.11	4.72	4.74	3.09	3.43	10.52	10.55	ns
12 mA	Std.	1.57	3.56	0.26	1.20	1.11	3.63	3.39	3.28	3.77	9.44	9.20	ns
16 mA	Std.	1.57	3.40	0.26	1.20	1.11	3.46	3.10	3.33	3.86	9.27	8.91	ns
24 mA	Std.	1.57	3.20	0.26	1.20	1.11	3.26	2.62	3.39	4.21	9.07	8.43	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-72 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	9.01	0.26	1.20	1.11	9.01	9.01	2.49	2.60	14.82	14.82	ns
6 mA	Std.	1.57	6.47	0.26	1.20	1.11	6.59	6.32	2.74	3.08	12.39	12.13	ns
8 mA	Std.	1.57	6.47	0.26	1.20	1.11	6.59	6.32	2.74	3.08	12.39	12.13	ns
12 mA	Std.	1.57	5.11	0.26	1.20	1.11	5.21	4.90	2.92	3.39	11.01	10.71	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-73 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	1.57	7.02	0.26	1.20	1.11	6.45	7.02	2.48	2.70	12.26	12.83	ns
6 mA	Std.	1.57	4.36	0.26	1.20	1.11	4.32	4.36	2.74	3.19	10.12	10.17	ns
8 mA	Std.	1.57	4.36	0.26	1.20	1.11	4.32	4.36	2.74	3.19	10.12	10.17	ns
12 mA	Std.	1.57	3.20	0.26	1.20	1.11	3.25	3.04	2.92	3.50	9.06	8.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-74 • **2.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	5.47	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
4 mA	Std.	1.57	5.47	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
6 mA	Std.	1.57	4.46	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
8 mA	Std.	1.57	4.46	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-75 • **2.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	3.31	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
4 mA	Std.	1.57	3.31	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
6 mA	Std.	1.57	2.66	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns
8 mA	Std.	1.57	2.66	0.26	1.15	1.11	2.71	2.42	2.37	2.79	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 3-76 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	16	16	74	91	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-77 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI}–0.45	8	8	44	35	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-78 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * V_{CCI}	0.65 * V_{CCI}	3.6	0.45	V_{CCI} – 0.45	4	4	17	22	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

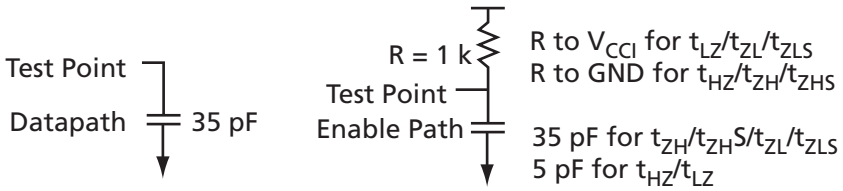


Figure 3-8 • **AC Loading**

Table 3-79 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	35

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 3-80 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	12.31	0.19	1.10	0.67	11.39	12.31	2.40	1.61	15.02	15.94	ns
4 mA	Std.	0.98	8.42	0.19	1.10	0.67	8.47	8.42	2.74	2.45	12.10	12.05	ns
6 mA	Std.	0.98	6.61	0.19	1.10	0.67	6.73	6.39	2.98	2.86	10.36	10.02	ns
8 mA	Std.	0.98	6.18	0.19	1.10	0.67	6.29	5.98	3.03	2.97	9.92	9.61	ns
12 mA	Std.	0.98	5.98	0.19	1.10	0.67	5.98	5.98	3.11	3.39	9.61	9.61	ns
16 mA	Std.	0.98	5.98	0.19	1.10	0.67	5.98	5.98	3.11	3.39	9.61	9.61	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-81 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	9.50	0.19	1.03	0.67	7.42	9.50	2.39	1.65	11.05	13.13	ns
4 mA	Std.	0.98	5.66	0.19	1.03	0.67	4.85	5.66	2.74	2.53	8.48	9.29	ns
6 mA	Std.	0.98	3.75	0.19	1.03	0.67	3.56	3.75	2.98	2.95	7.19	7.38	ns
8 mA	Std.	0.98	3.34	0.19	1.03	0.67	3.36	3.34	3.03	3.06	6.99	6.97	ns
12 mA	Std.	0.98	3.05	0.19	1.03	0.67	3.11	2.65	3.11	3.49	6.74	6.28	ns
16 mA	Std.	0.98	3.05	0.19	1.03	0.67	3.11	2.65	3.11	3.49	6.74	6.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-82 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	11.68	0.19	1.11	0.67	10.76	11.68	2.00	1.51	14.39	15.31	ns
4 mA	Std.	0.98	7.89	0.19	1.11	0.67	7.81	7.89	2.31	2.27	11.44	11.52	ns
6 mA	Std.	0.98	6.02	0.19	1.11	0.67	6.13	5.91	2.53	2.65	9.76	9.54	ns
8 mA	Std.	0.98	6.02	0.19	1.11	0.67	6.13	5.91	2.53	2.65	9.76	9.54	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-83 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	9.00	0.19	1.04	0.67	6.99	9.00	2.00	1.55	10.62	12.63	ns
4 mA	Std.	0.98	5.23	0.19	1.04	0.67	4.46	5.23	2.31	2.35	8.09	8.86	ns
6 mA	Std.	0.98	3.35	0.19	1.04	0.67	3.20	3.35	2.53	2.74	6.83	6.98	ns
8 mA	Std.	0.98	3.35	0.19	1.04	0.67	3.20	3.35	2.53	2.74	6.83	6.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-84 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	11.67	0.19	1.00	0.67	10.55	11.67	1.72	1.28	ns
4 mA	Std.	0.98	7.89	0.19	1.00	0.67	7.74	7.89	2.02	2.04	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-85 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	8.83	0.19	1.00	0.67	6.81	8.83	1.72	1.33	ns
4 mA	Std.	0.98	5.07	0.19	1.00	0.67	4.36	5.07	2.02	2.12	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-86 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	12.71	0.26	1.20	1.11	11.80	12.71	2.85	2.27	17.60	18.52	ns
4 mA	Std.	1.57	8.81	0.26	1.20	1.11	8.88	8.81	3.20	3.12	14.68	14.62	ns
6 mA	Std.	1.57	7.01	0.26	1.20	1.11	7.14	6.79	3.44	3.54	12.95	12.60	ns
8 mA	Std.	1.57	6.58	0.26	1.20	1.11	6.70	6.37	3.49	3.65	12.51	12.18	ns
12 mA	Std.	1.57	6.37	0.26	1.20	1.11	6.39	6.37	3.57	4.06	12.20	12.18	ns
16 mA	Std.	1.57	6.37	0.26	1.20	1.11	6.39	6.37	3.57	4.06	12.20	12.18	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-87 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	9.90	0.26	1.11	1.11	7.84	9.90	2.85	2.32	13.65	15.71	ns
4 mA	Std.	1.57	6.06	0.26	1.11	1.11	5.28	6.06	3.19	3.21	11.08	11.86	ns
6 mA	Std.	1.57	4.14	0.26	1.11	1.11	3.98	4.14	3.43	3.63	9.79	9.95	ns
8 mA	Std.	1.57	3.73	0.26	1.11	1.11	3.79	3.73	3.49	3.74	9.59	9.54	ns
12 mA	Std.	1.57	3.47	0.26	1.11	1.11	3.53	3.05	3.56	4.17	9.34	8.85	ns
16 mA	Std.	1.57	3.47	0.26	1.11	1.11	3.53	3.05	3.56	4.17	9.34	8.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-88 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	12.03	0.26	1.20	1.11	11.14	12.03	2.46	2.14	16.94	17.84	ns
4 mA	Std.	1.57	8.24	0.26	1.20	1.11	8.19	8.24	2.77	2.91	14.00	14.05	ns
6 mA	Std.	1.57	6.39	0.26	1.20	1.11	6.51	6.26	2.98	3.29	12.32	12.07	ns
8 mA	Std.	1.57	6.39	0.26	1.20	1.11	6.51	6.26	2.98	3.29	12.32	12.07	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-89 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	9.35	0.26	1.11	1.11	7.39	9.35	2.45	2.18	13.20	15.16	ns
4 mA	Std.	1.57	5.59	0.26	1.11	1.11	4.86	5.59	2.76	2.99	10.67	11.40	ns
6 mA	Std.	1.57	3.71	0.26	1.11	1.11	3.60	3.71	2.98	3.38	9.41	9.52	ns
8 mA	Std.	1.57	3.71	0.26	1.11	1.11	3.60	3.71	2.98	3.38	9.41	9.52	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-90 • **1.8 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	12.02	0.26	1.08	1.11	10.90	12.02	2.07	1.77	ns
4 mA	Std.	1.57	8.24	0.26	1.08	1.11	8.09	8.24	2.37	2.53	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-91 • **1.8 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	9.18	0.26	1.08	1.11	7.17	9.18	2.07	1.81	ns
4 mA	Std.	1.57	5.42	0.26	1.08	1.11	4.72	5.42	2.37	2.61	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 3-92 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	16	13	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	33	25	10	10
6 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	6	6	39	32	10	10
8 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	8	8	55	66	10	10
12 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	12	12	55	66	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-93 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	0	0	10	10
4 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	4	4	0	0	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 3-94 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA[1]	Max., mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*
3. *Software default selection highlighted in gray.*

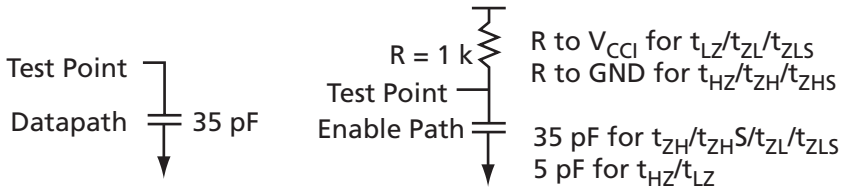


Figure 3-9 • **AC Loading**

Table 3-95 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 3-96 • **1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	10.20	0.19	1.10	0.67	10.34	10.20	2.87	2.37	13.97	13.83	ns
4 mA	Std.	0.98	8.14	0.19	1.10	0.67	8.29	7.71	3.14	2.85	11.92	11.34	ns
6 mA	Std.	0.98	7.61	0.19	1.10	0.67	7.75	7.21	3.20	2.98	11.38	10.84	ns
8 mA	Std.	0.98	7.27	0.19	1.10	0.67	7.40	7.21	3.30	3.46	11.03	10.84	ns
12 mA	Std.	0.98	7.27	0.19	1.10	0.67	7.40	7.21	3.30	3.46	11.03	10.84	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-97 • **1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	6.79	0.19	1.20	0.67	5.60	6.79	2.86	2.47	9.23	10.42	ns
4 mA	Std.	0.98	4.42	0.19	1.20	0.67	4.07	4.42	3.14	2.96	7.70	8.05	ns
6 mA	Std.	0.98	3.72	0.19	1.20	0.67	3.68	3.72	3.14	3.08	7.31	7.35	ns
8 mA	Std.	0.98	3.47	0.19	1.20	0.67	3.54	3.07	3.29	3.58	7.17	6.70	ns
12 mA	Std.	0.98	3.47	0.19	1.20	0.67	3.54	3.07	3.29	3.58	7.17	6.70	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-98 • **1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	9.58	0.19	1.11	0.67	9.58	9.58	2.36	2.21	13.21	13.21	ns
4 mA	Std.	0.98	7.44	0.19	1.11	0.67	7.58	7.15	2.61	2.65	11.21	10.78	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-99 • **1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.98	6.28	0.19	1.21	0.67	5.18	6.28	2.35	2.30	8.81	9.91	ns
4 mA	Std.	0.98	3.96	0.19	1.21	0.67	3.69	3.96	2.60	2.75	7.32	7.59	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-100 • **1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	9.60	0.19	1.17	0.67	9.53	9.60	2.05	1.99	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-101 • **1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.98	6.08	0.19	1.17	0.67	5.08	6.08	2.05	2.08	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-102 • **1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	10.59	0.26	1.20	1.11	10.70	10.59	3.32	3.01	16.51	16.39	ns
4 mA	Std.	1.57	8.49	0.26	1.20	1.11	8.64	8.09	3.59	3.49	14.45	13.90	ns
6 mA	Std.	1.57	7.96	0.26	1.20	1.11	8.10	7.59	3.65	3.62	13.91	13.39	ns
8 mA	Std.	1.57	7.62	0.26	1.20	1.11	7.76	7.59	3.75	4.10	13.57	13.40	ns
12 mA	Std.	1.57	7.62	0.26	1.20	1.11	7.76	7.59	3.75	4.10	13.57	13.40	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-103 • **1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	7.17	0.26	1.27	1.11	5.98	7.17	3.31	3.10	11.79	12.97	ns
4 mA	Std.	1.57	4.80	0.26	1.27	1.11	4.46	4.80	3.58	3.59	10.27	10.61	ns
6 mA	Std.	1.57	4.10	0.26	1.27	1.11	4.06	4.10	3.59	3.72	9.87	9.91	ns
8 mA	Std.	1.57	3.85	0.26	1.27	1.11	3.92	3.45	3.74	4.21	9.73	9.26	ns
12 mA	Std.	1.57	3.85	0.26	1.27	1.11	3.92	3.45	3.74	4.21	9.73	9.26	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-104 • **1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	9.92	0.26	1.20	1.11	9.91	9.92	2.81	2.81	15.72	15.73	ns
4 mA	Std.	1.57	7.77	0.26	1.20	1.11	7.92	7.49	3.06	3.25	13.73	13.30	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-105 • **1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.57	6.62	0.26	1.27	1.11	5.55	6.62	2.80	2.90	11.36	12.43	ns
4 mA	Std.	1.57	4.30	0.26	1.27	1.11	4.06	4.30	3.05	3.36	9.87	10.11	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-106 • **1.5 V LCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	9.93	0.26	1.22	1.11	9.83	9.93	2.39	2.45	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-107 • **1.5 V LCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 1.4 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.57	6.41	0.26	1.22	1.11	5.41	6.41	2.39	2.54	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 3-108 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced and Standard Plus I/Os**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

Table 3-109 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/Os**

3.3 V PCI/PCI-X	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	**Min, V**	**Max, V**	**Min, V**	**Max, V**	**Max, V**	**Min, V**	**mA**	**mA**	**Max, mA[1]**	**Max, mA[1]**	**µA[2]**	**µA[2]**
2 mA	–0.3	0.30 * V_{CCI}	0.7 * V_{CCI}	3.6	0.25 * V_{CCI}	0.75 * V_{CCI}	2	2	13	16	10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 3-10.

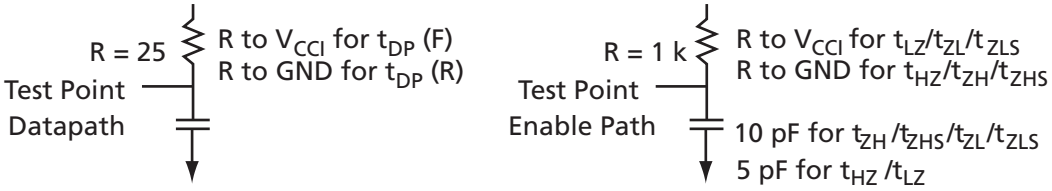


Figure 3-10 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 3-110.

Table 3-110 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * V_{CCI} for $t_{DP(R)}$ 0.615 * V_{CCI} for $t_{DP(F)}$	10

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 3-111 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.38	0.19	0.72	0.67	2.43	1.82	2.74	3.13	6.06	5.45	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-112 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.98	2.02	0.19	0.72	0.67	2.06	1.54	2.43	2.87	5.69	5.17	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-113 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.57	2.90	0.26	0.86	1.11	2.95	2.29	3.23	3.92	8.76	8.10	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-114 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	1.57	2.52	0.26	0.85	1.11	2.57	1.98	2.91	3.62	8.37	7.78	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-11. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, IGLOO also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

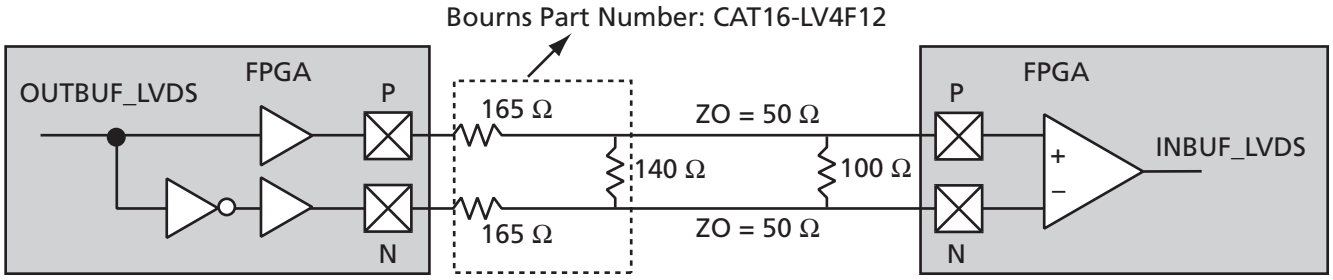


Figure 3-11 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 3-115 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output LOW Voltage	0.9	1.075	1.25	V
V_{OH}	Output HIGH Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0	–	2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common-Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350	–	mV

Notes:

1. *± 5%*
2. *Differential input voltage = ±350 mV*

Table 3-116 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 3-117 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.98	1.72	0.19	1.35	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 and Table 3-7 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-118 • **LVDS – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 2.3 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.57	2.19	0.26	1.52	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 and Table 3-7 on page 3-6 for derating values.*

BLVDS/M-LVDS

Bus LVDS (BLVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by BLVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 3-12. The input and output buffer delays are available in the LVDS section in Table 3-117 and Table 3-118.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

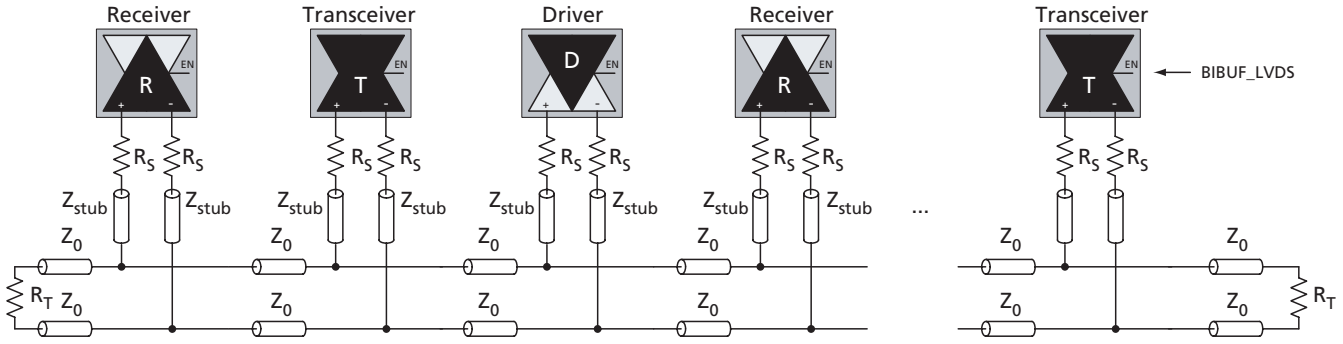


Figure 3-12 • **BLVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 3-13. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

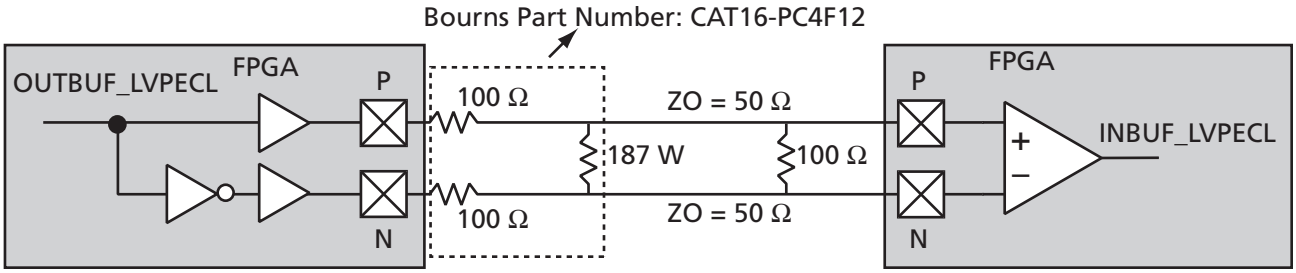


Figure 3-13 • **LVPECL Circuit Diagram and Board-Level Implementation**

Table 3-119 • **Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 3-120 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: **Measuring point = V_{trip}. See Table 3-26 on page 3-20 for a complete table of trip points.*

Timing Characteristics

1.5 V DC Core Voltage

Table 3-121 • **LVPECL – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.98	1.72	0.19	1.35	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-122 • **LVPECL – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V, Worst-Case V_{CCI} = 3.0 V
Applicable to Standard Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	1.57	2.24	0.26	1.37	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

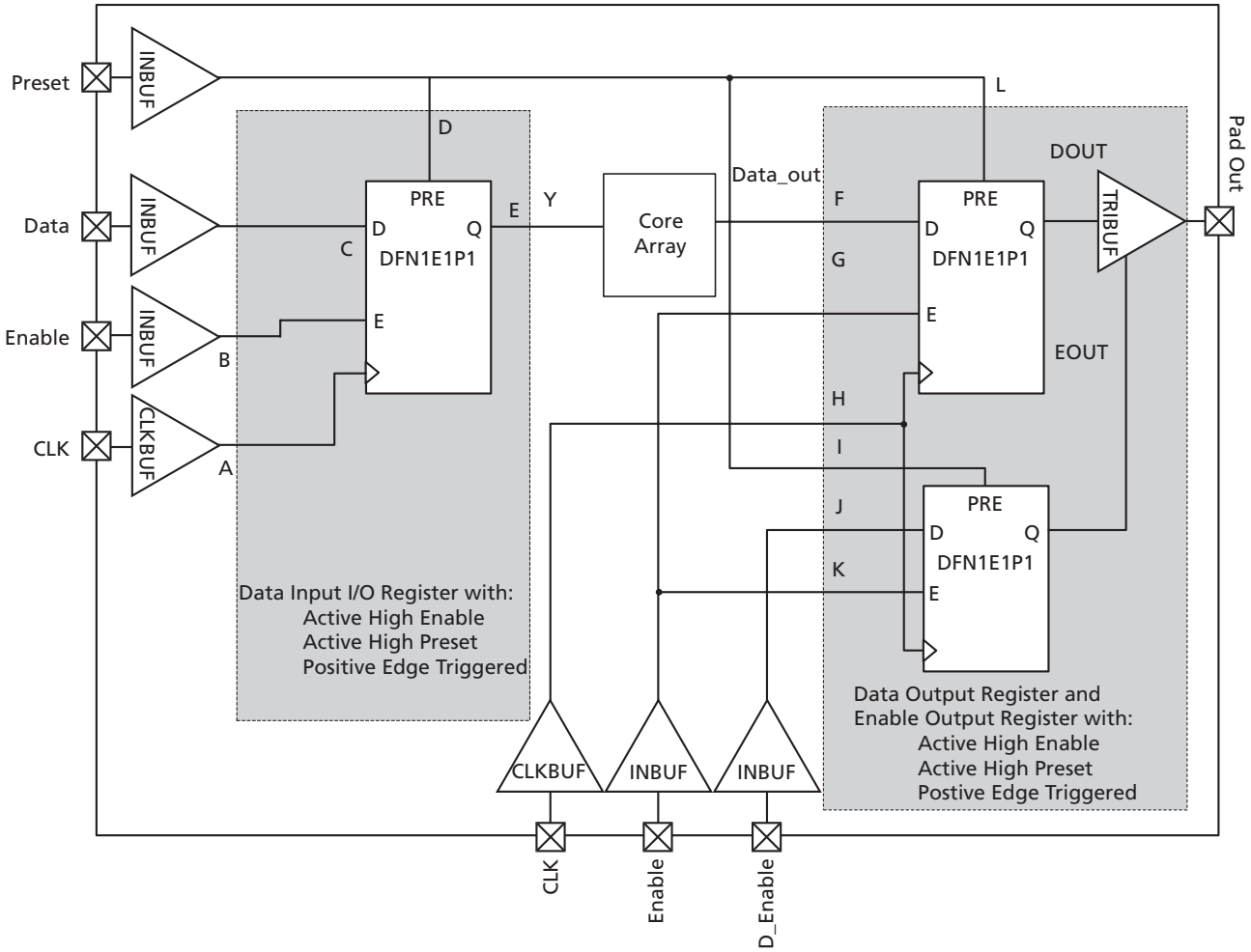


Figure 3-14 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 3-123 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: **See Figure 3-14 on page 3-61 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

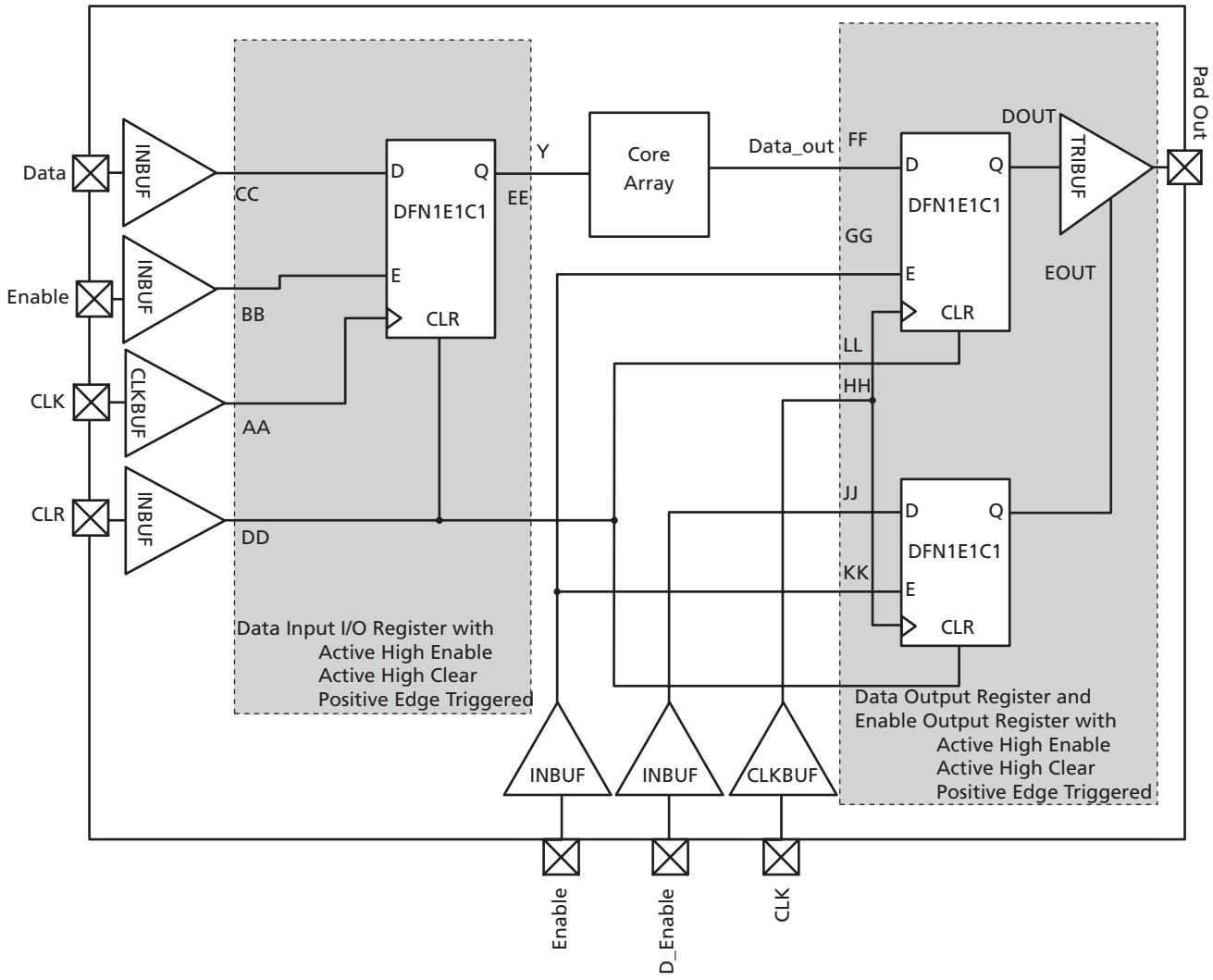


Figure 3-15 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 3-124 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: **See Figure 3-15 on page 3-63 for more information.*

Input Register

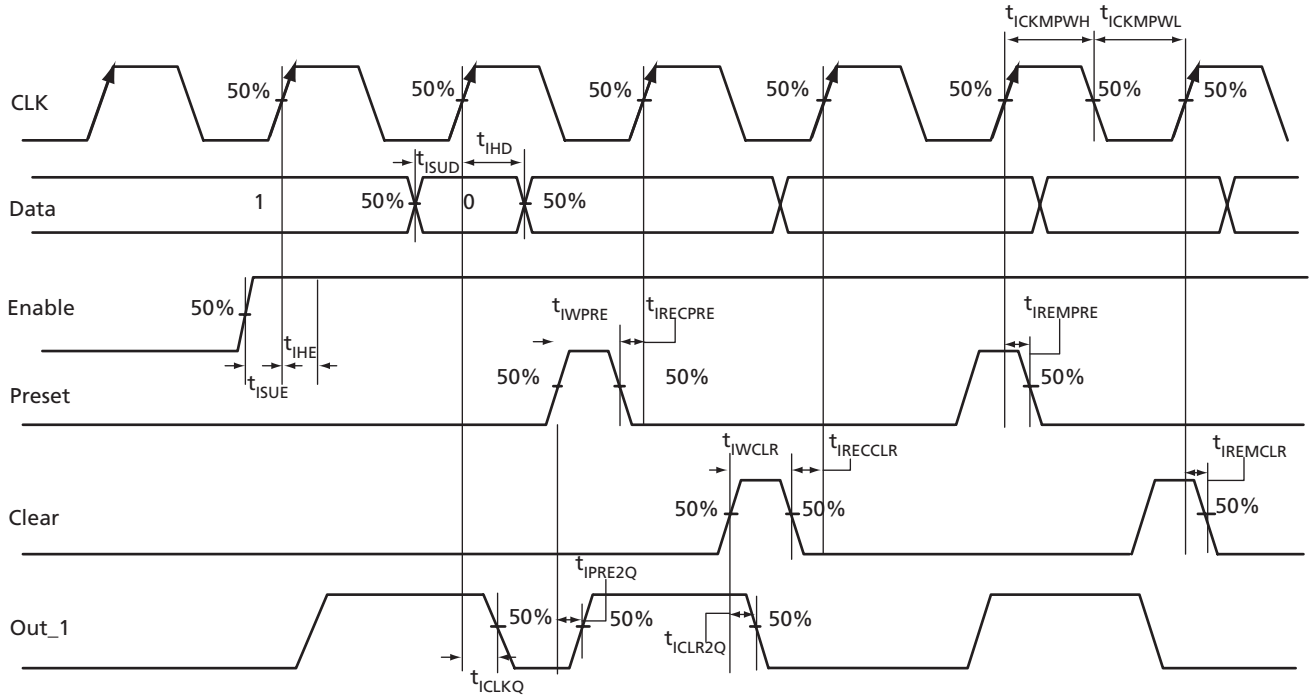


Figure 3-16 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-125 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.43	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.81	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.81	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-126 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.70	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.98	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	1.04	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.22	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.22	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width HIGH for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width LOW for the Input Data Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Output Register

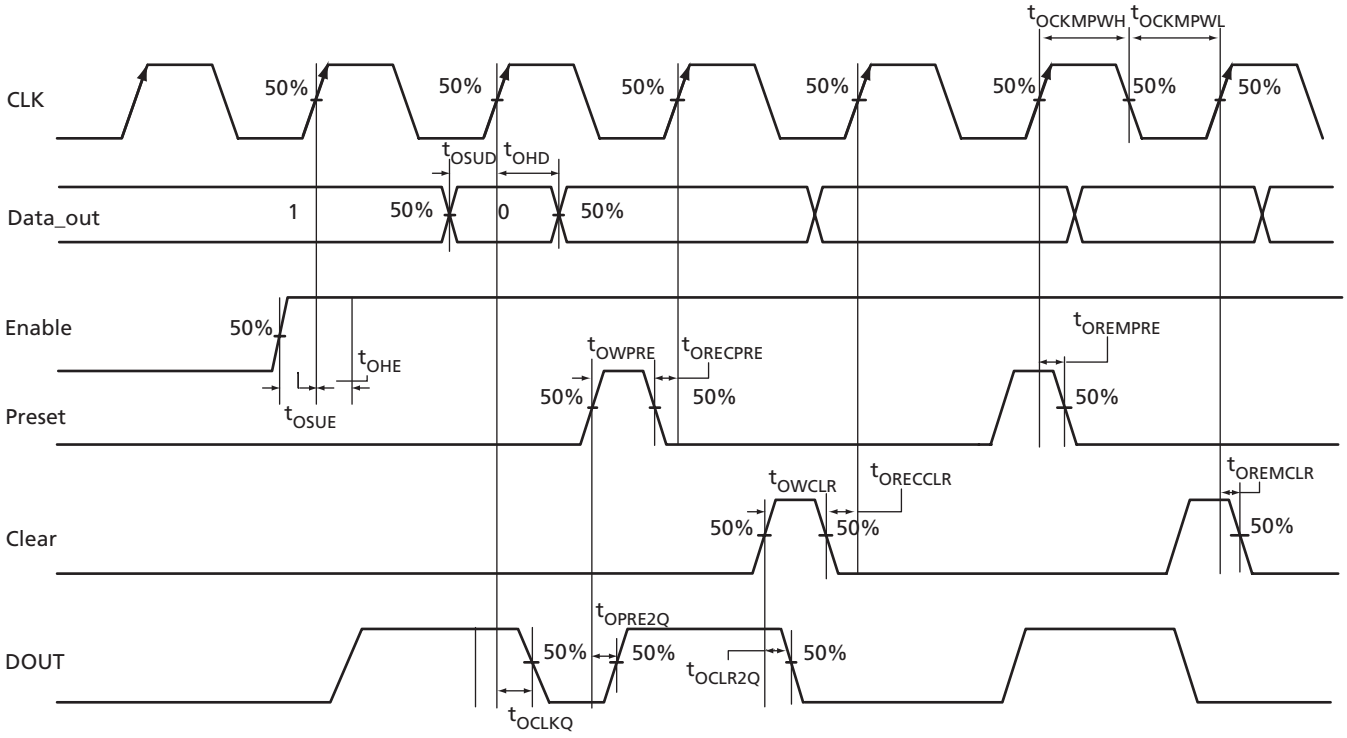


Figure 3-17 • **Output Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-127 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.02	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.52	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.70	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	1.37	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	1.37	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-128 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	1.56	ns
t_{OSUD}	Data Setup Time for the Output Data Register	1.17	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	1.13	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	2.01	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	2.01	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.19	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.19	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Data Register	0.31	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width LOW for the Output Data Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Output Enable Register

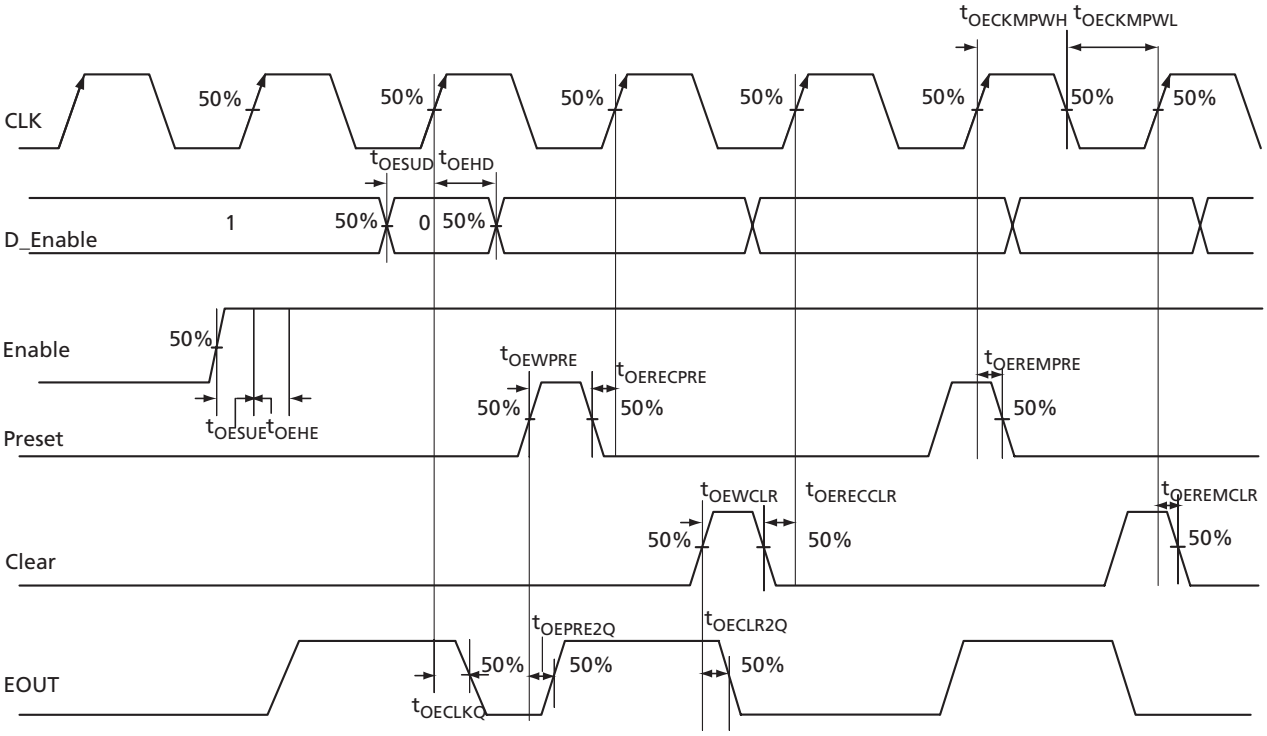


Figure 3-18 • **Output Enable Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-129 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.77	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.52	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.74	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.15	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.15	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-130 • **Output Enable Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.13	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.17	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.24	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.69	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.69	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.28	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

DDR Module Specifications

Input DDR Module

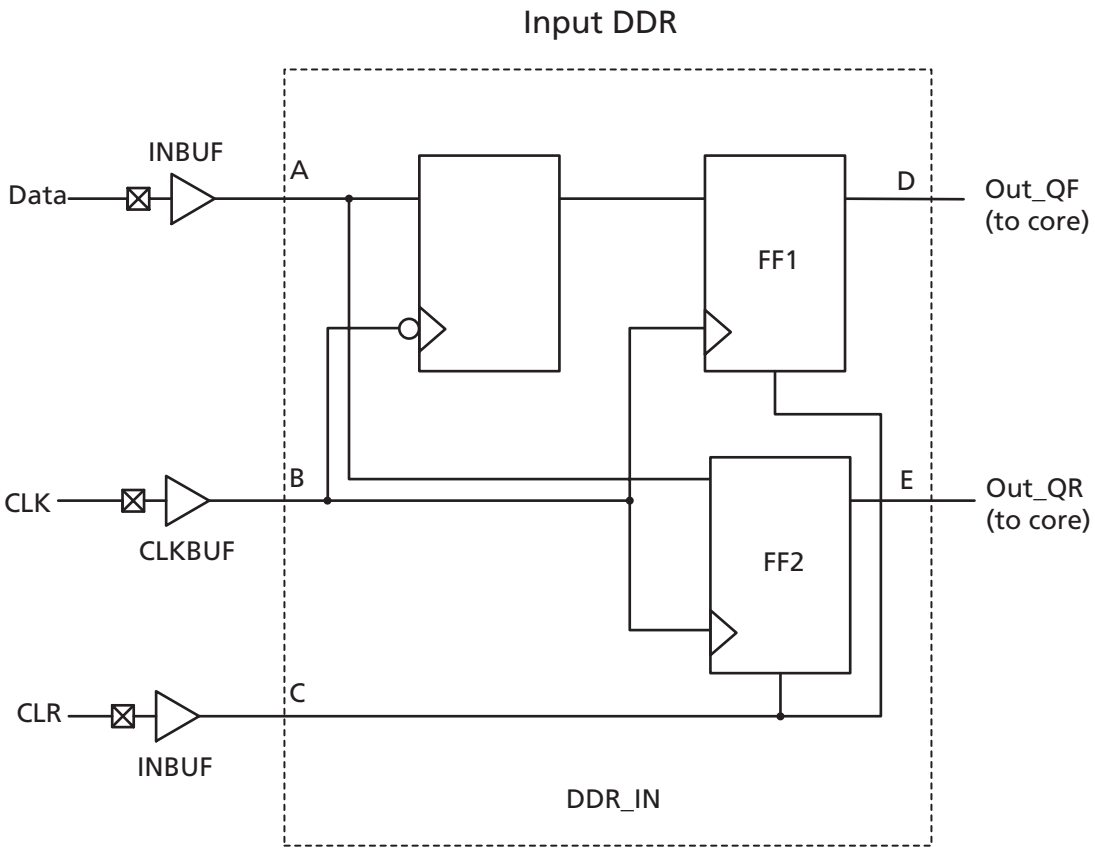


Figure 3-19 • **Input DDR Timing Model**

Table 3-131 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

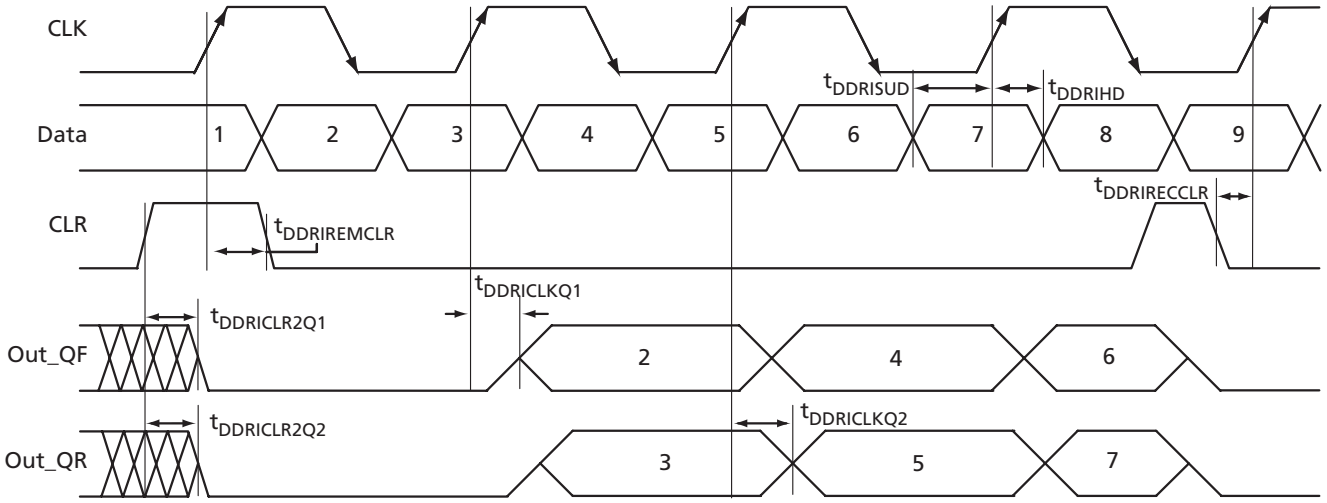


Figure 3-20 • **Input DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-132 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.49	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.66	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.51	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.83	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.99	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-133 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.78	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.96	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.94	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.25	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.44	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width HIGH for Input DDR	0.31	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width LOW for Input DDR	0.28	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	TBD	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Output DDR Module

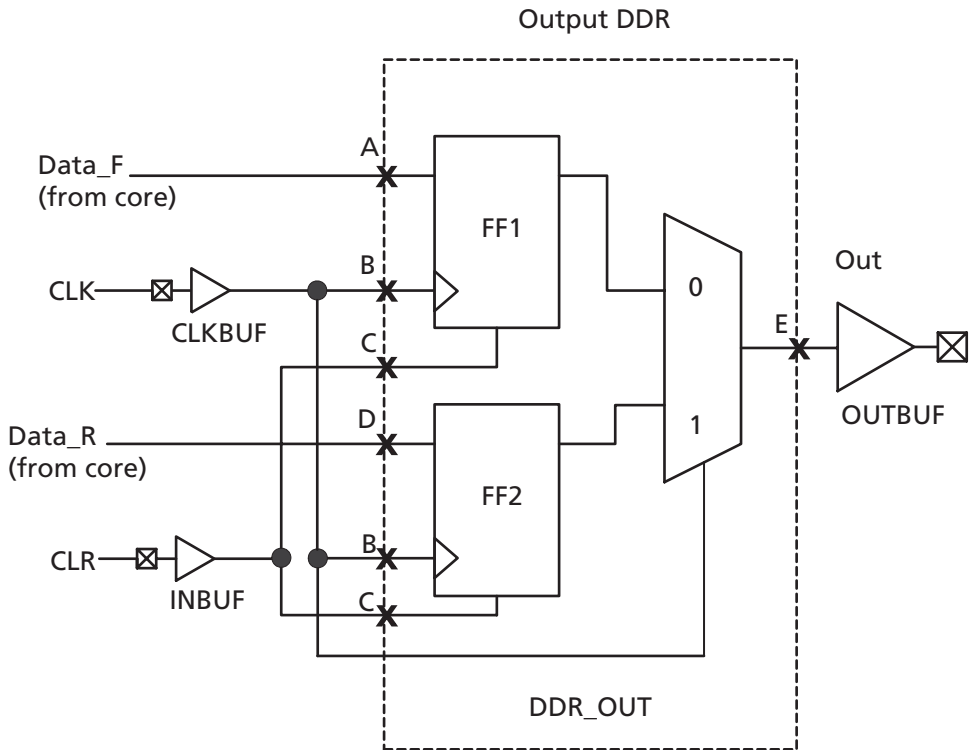


Figure 3-21 • **Output DDR Timing Model**

Table 3-134 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

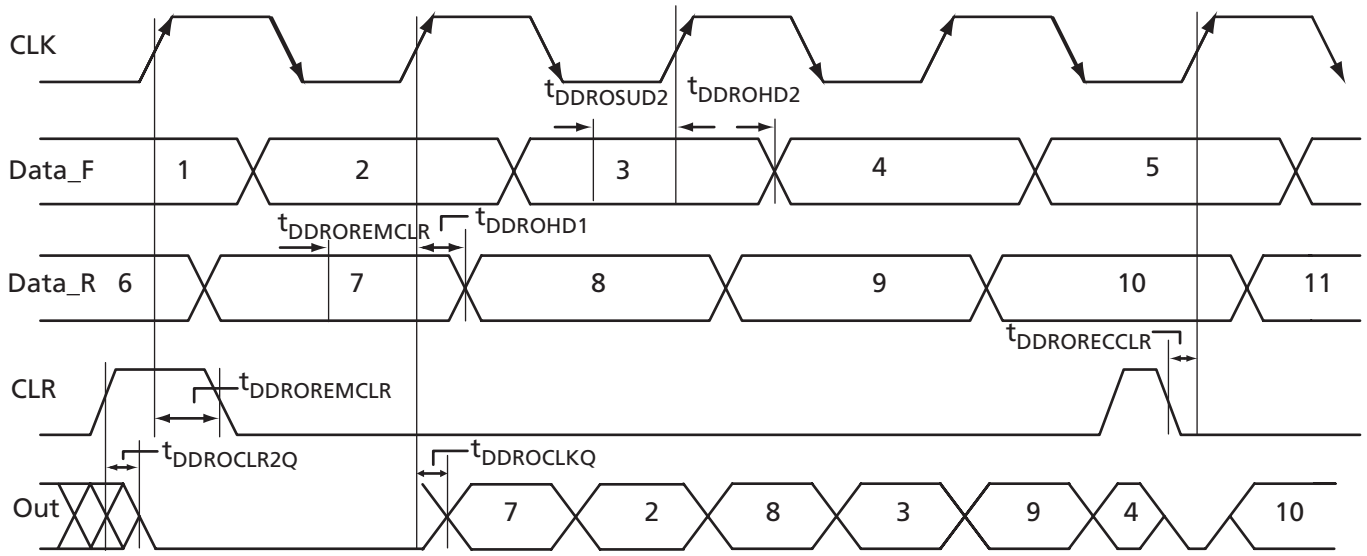


Figure 3-22 • **Output DDR Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-135 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.09	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.68	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.68	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	1.39	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-136 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	1.63	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	1.11	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	1.18	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	2.01	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.31	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width LOW for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOOe and ProASIC3E Macro Library Guide*.

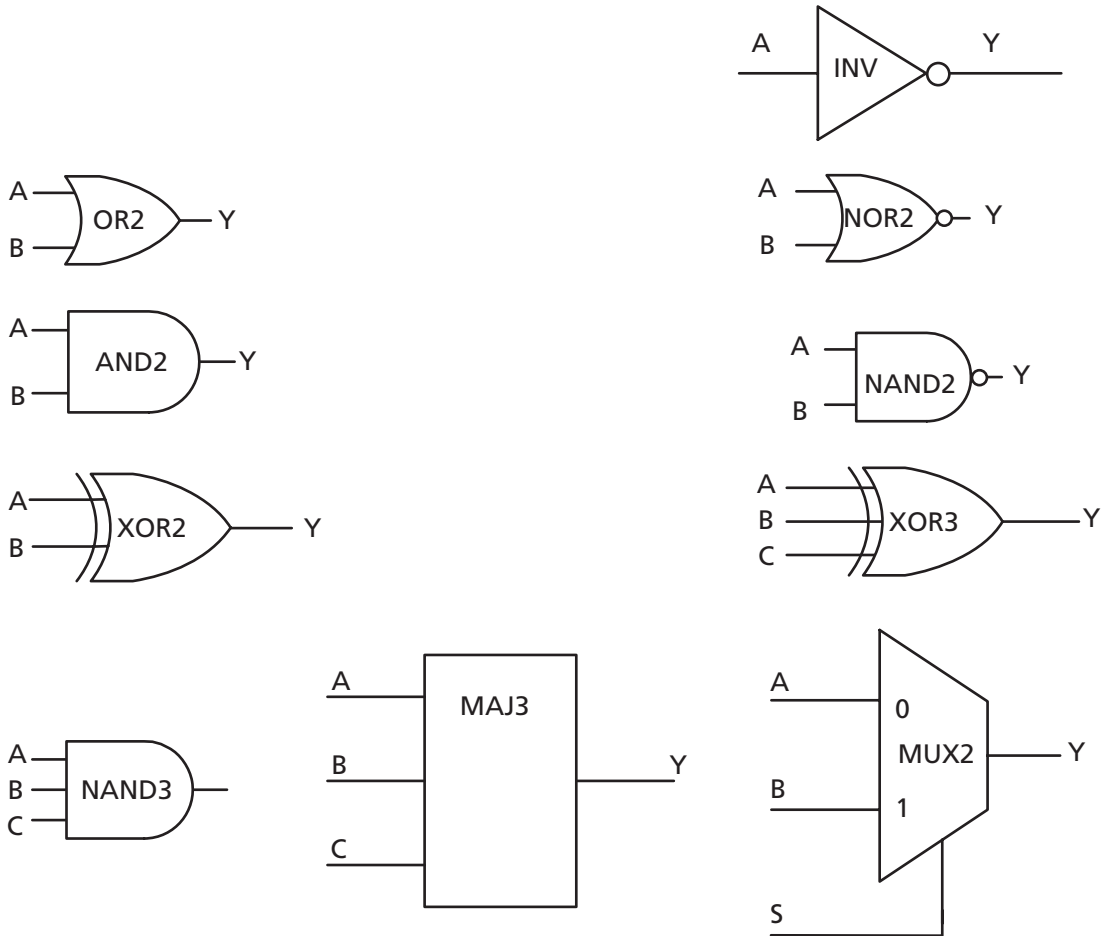


Figure 3-23 • **Sample of Combinatorial Cells**

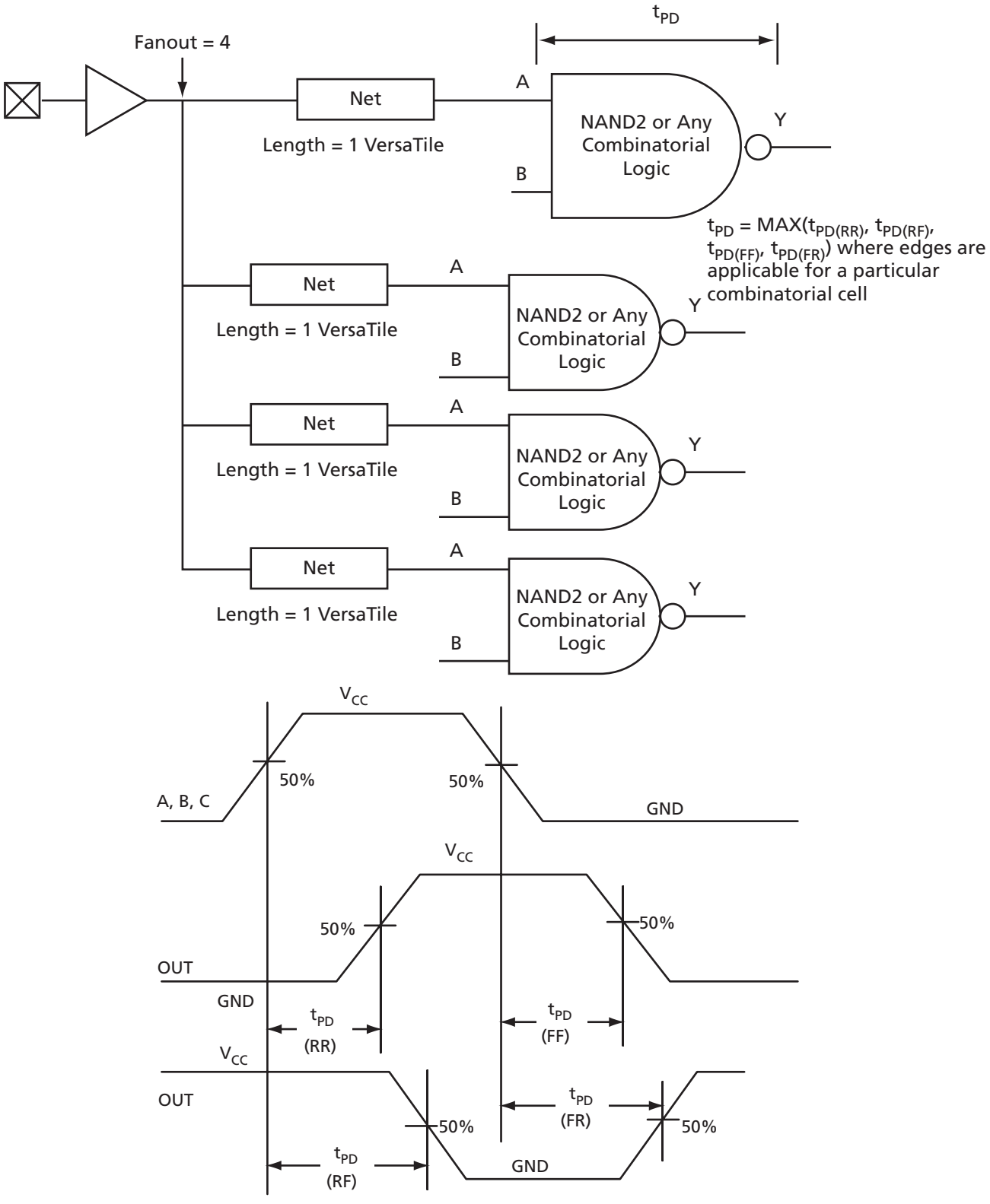


Figure 3-24 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-137 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	1.12	ns
AND2	Y = A · B	t_{PD}	0.86	ns
NAND2	Y = !(A · B)	t_{PD}	0.92	ns
OR2	Y = A + B	t_{PD}	1.20	ns
NOR2	Y = !(A + B)	t_{PD}	1.12	ns
XOR2	Y = A ⊕ B	t_{PD}	1.40	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	1.34	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	1.80	ns
MUX2	Y = A !S + B S	t_{PD}	1.49	ns
AND3	Y = A · B · C	t_{PD}	1.22	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-138 • **Combinatorial Cell Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	Y = !A	t_{PD}	2.12	ns
AND2	Y = A · B	t_{PD}	1.46	ns
NAND2	Y = !(A · B)	t_{PD}	1.63	ns
OR2	Y = A + B	t_{PD}	2.34	ns
NOR2	Y = !(A + B)	t_{PD}	2.12	ns
XOR2	Y = A ⊕ B	t_{PD}	2.50	ns
MAJ3	Y = MAJ(A , B, C)	t_{PD}	2.50	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	3.17	ns
MUX2	Y = A !S + B S	t_{PD}	2.87	ns
AND3	Y = A · B · C	t_{PD}	2.31	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

VersaTile Specifications as a Sequential Module

The IGLOO library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e and ProASIC3/E Macro Library Guide*.

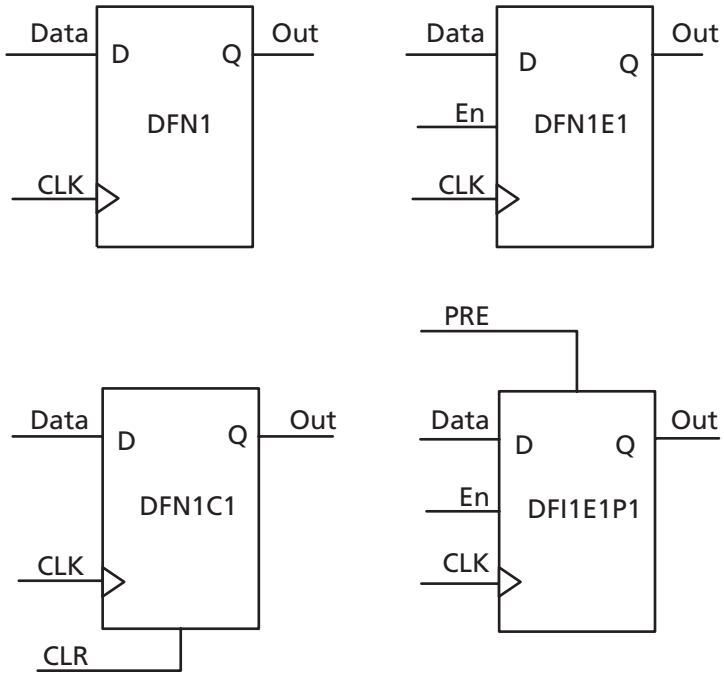


Figure 3-25 • **Sample of Sequential Cells**

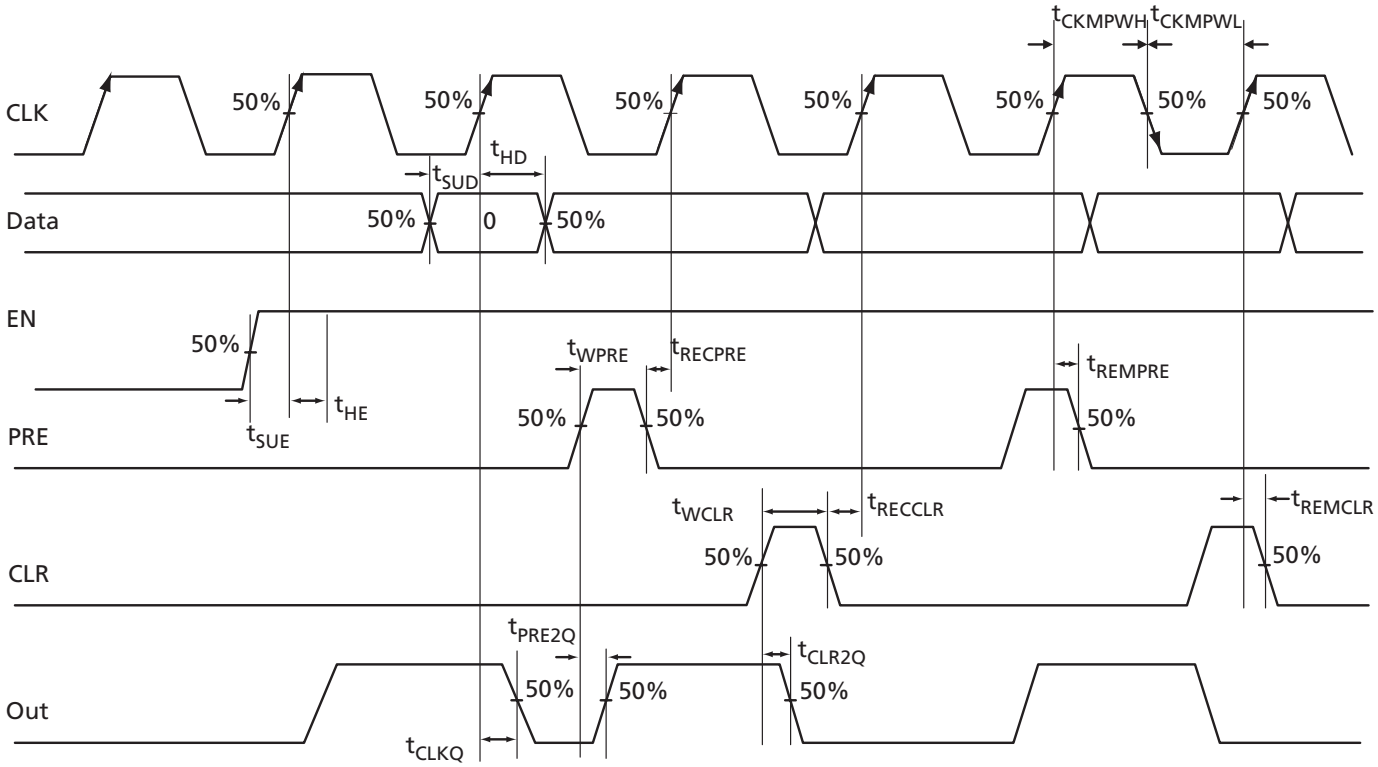


Figure 3-26 • **Timing Model and Waveforms**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-139 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.90	ns
t_{SUD}	Data Setup Time for the Core Register	0.82	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.73	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.61	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.62	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.56	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.56	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-140 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	1.65	ns
t_{SUD}	Data Setup Time for the Core Register	1.19	ns
t_{HD}	Data Hold Time for the Core Register	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	1.31	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.89	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.90	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.46	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.46	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.95	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.95	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Global Resource Characteristics

AGL250 Clock Tree Topology

Clock delays are device-specific. Figure 3-27 is an example of a global tree used for clock routing. The global tree presented in Figure 3-27 is driven by a CCC located on the west side of the AGL250 device. It is used to drive all D-flip-flops in the device.

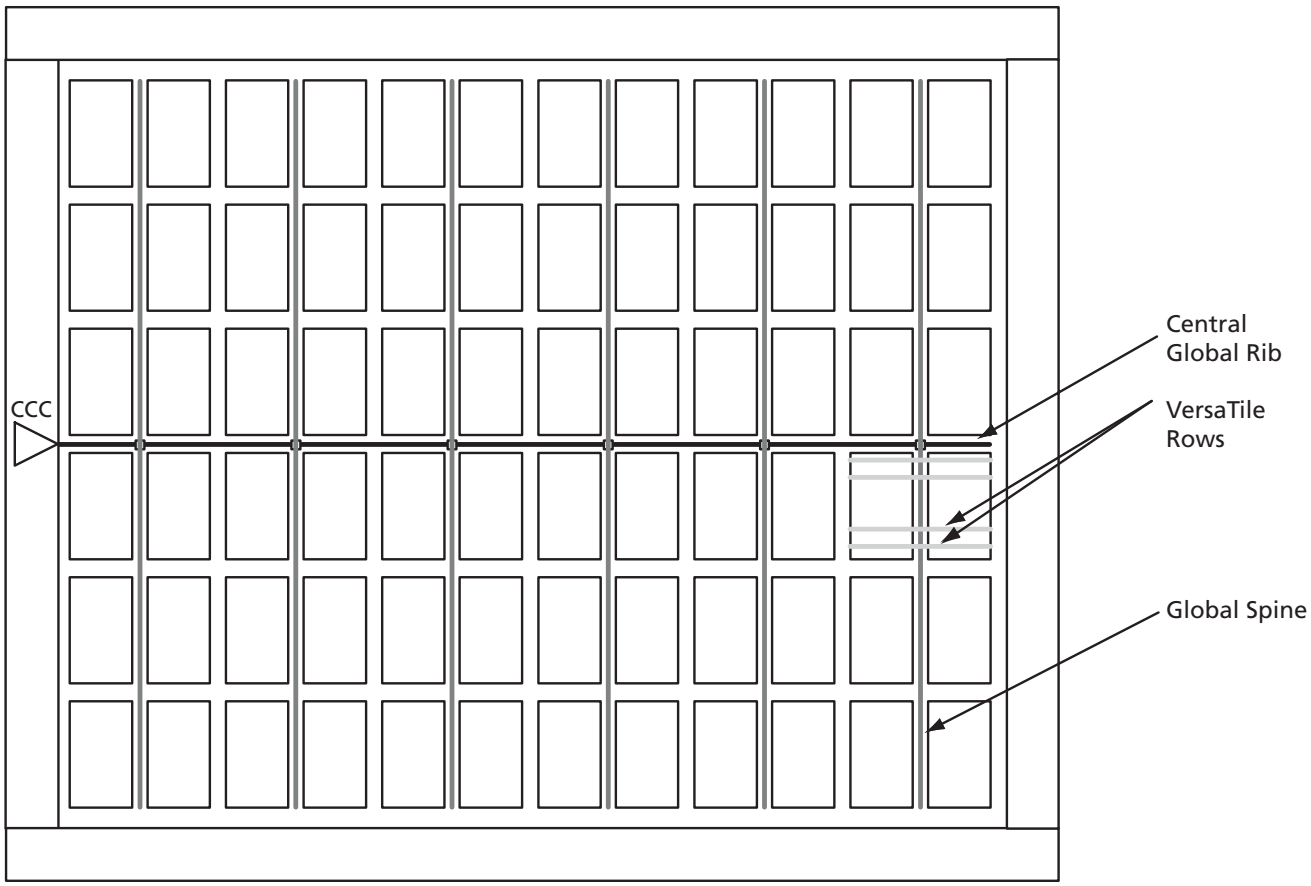


Figure 3-27 • **Example of Global Tree Use in an AGL250 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-14. Table 3-141 to Table 3-146 on page 3-86 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 3-141 • **AGL030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.23	1.44	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.25	1.52	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.30	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-142 • **AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.38	1.74	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.41	1.85	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.47	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-143 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.50	1.85	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.55	1.98	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.48	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-144 • **AGL030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	1.84	2.13	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.93	2.33	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.49	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-145 • **AGL125 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.12	2.60	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.21	2.85	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.73	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-146 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input LOW Delay for Global Clock	2.27	2.74	ns
t_{RCKH}	Input HIGH Delay for Global Clock	2.39	3.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width HIGH for Global Clock			ns
$t_{RCKMPWL}$	Minimum Pulse Width LOW for Global Clock			ns
t_{RCKSW}	Maximum Skew for Global Clock		0.74	ns
F_{RMAX}	Maximum Frequency for Global Clock			MHz

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Embedded SRAM and FIFO Characteristics

SRAM

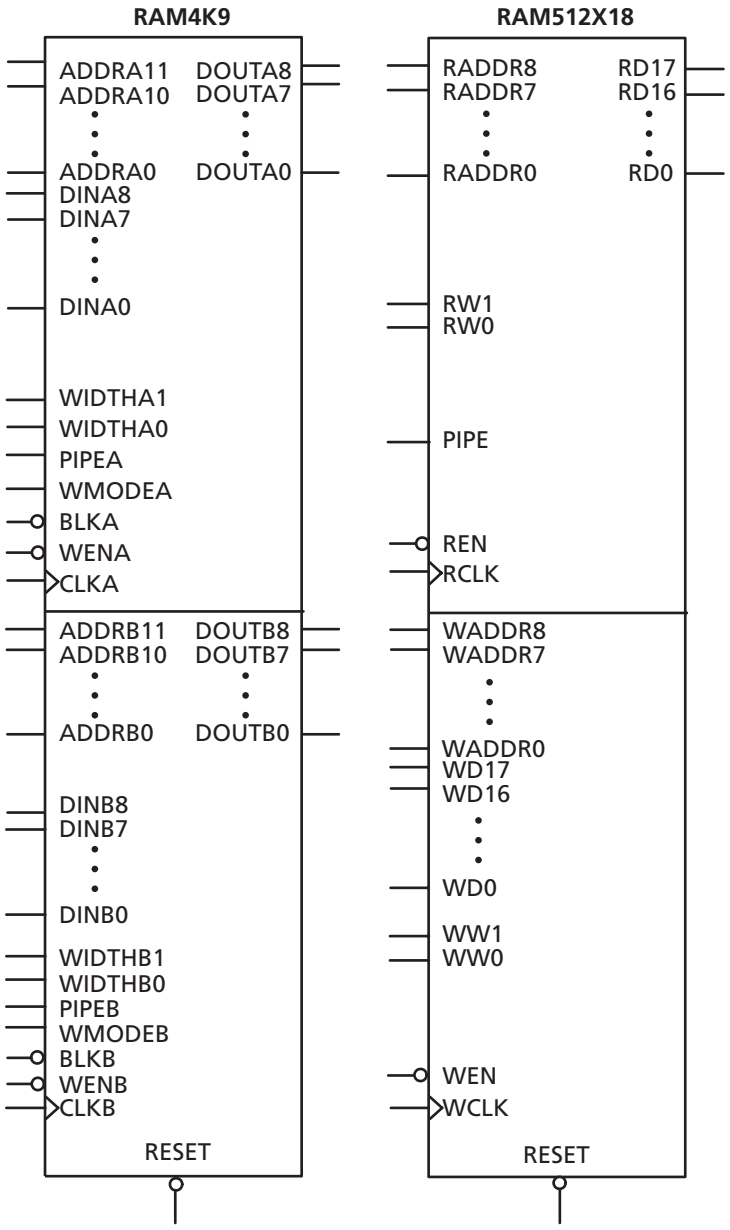


Figure 3-28 • **RAM Models**

Timing Waveforms

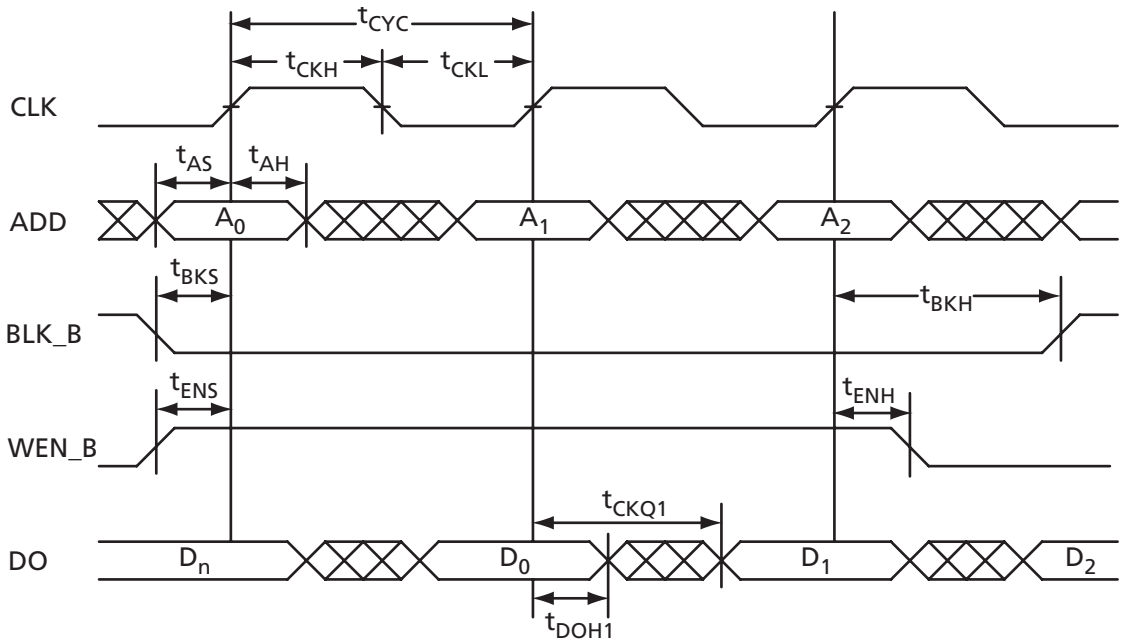


Figure 3-29 • **RAM Read for Pass-Through Output**

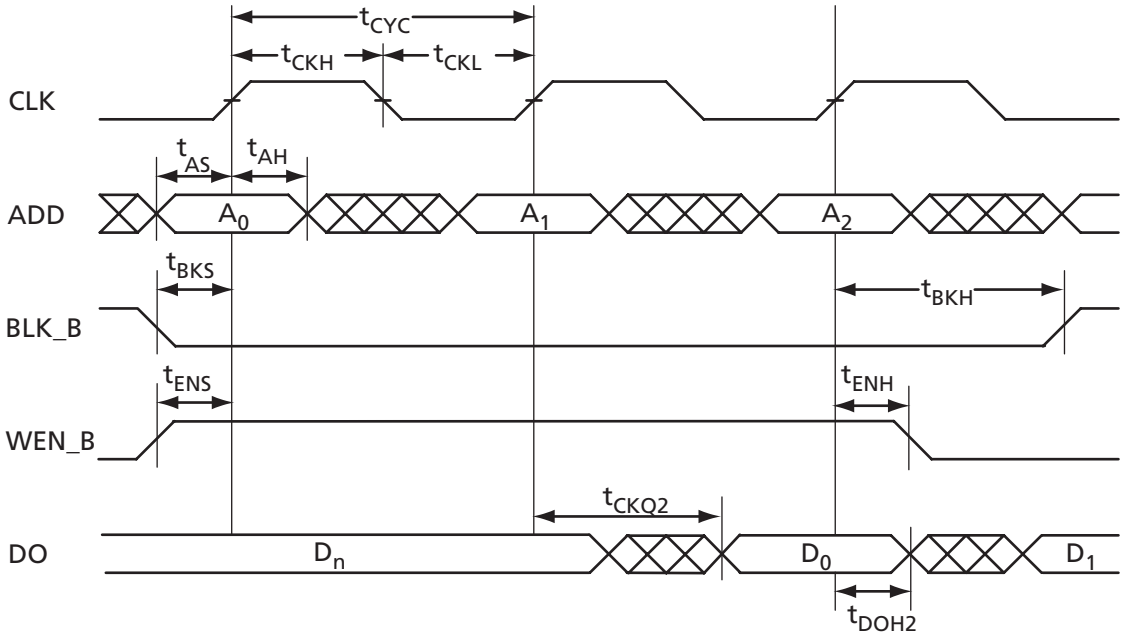


Figure 3-30 • **RAM Read for Pipelined Output**

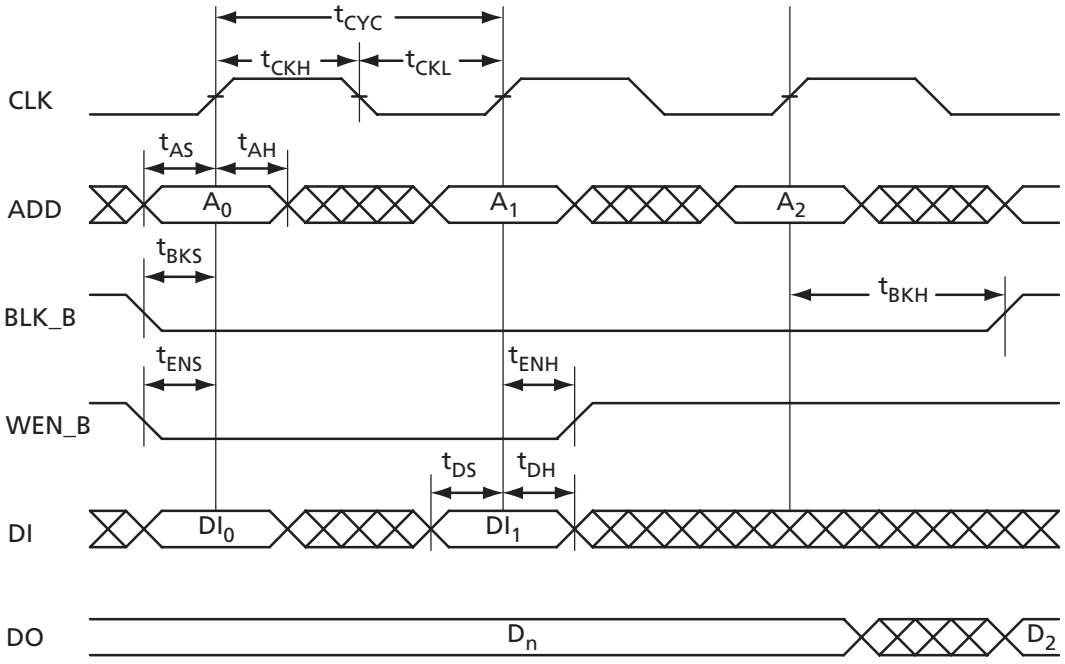


Figure 3-31 • **RAM Write, Output Retained (WMODE = 0)**

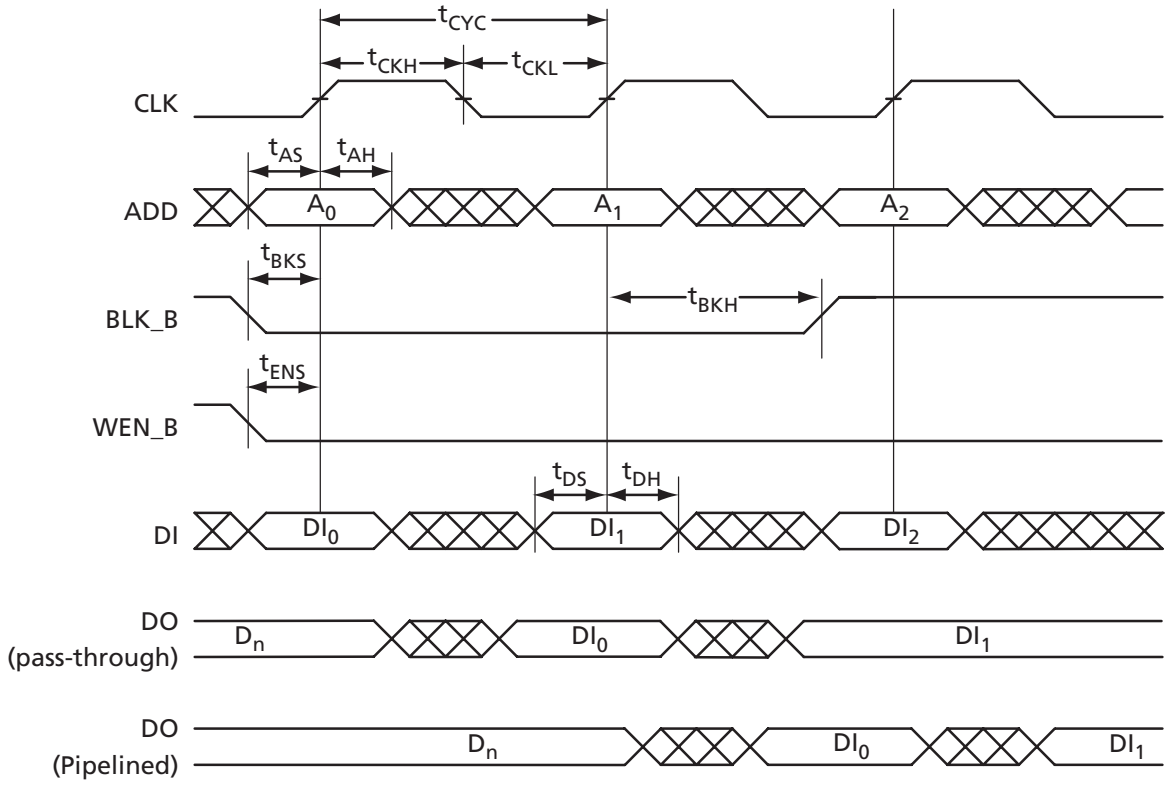


Figure 3-32 • **RAM Write, Output as Write Data (WMODE = 1)**

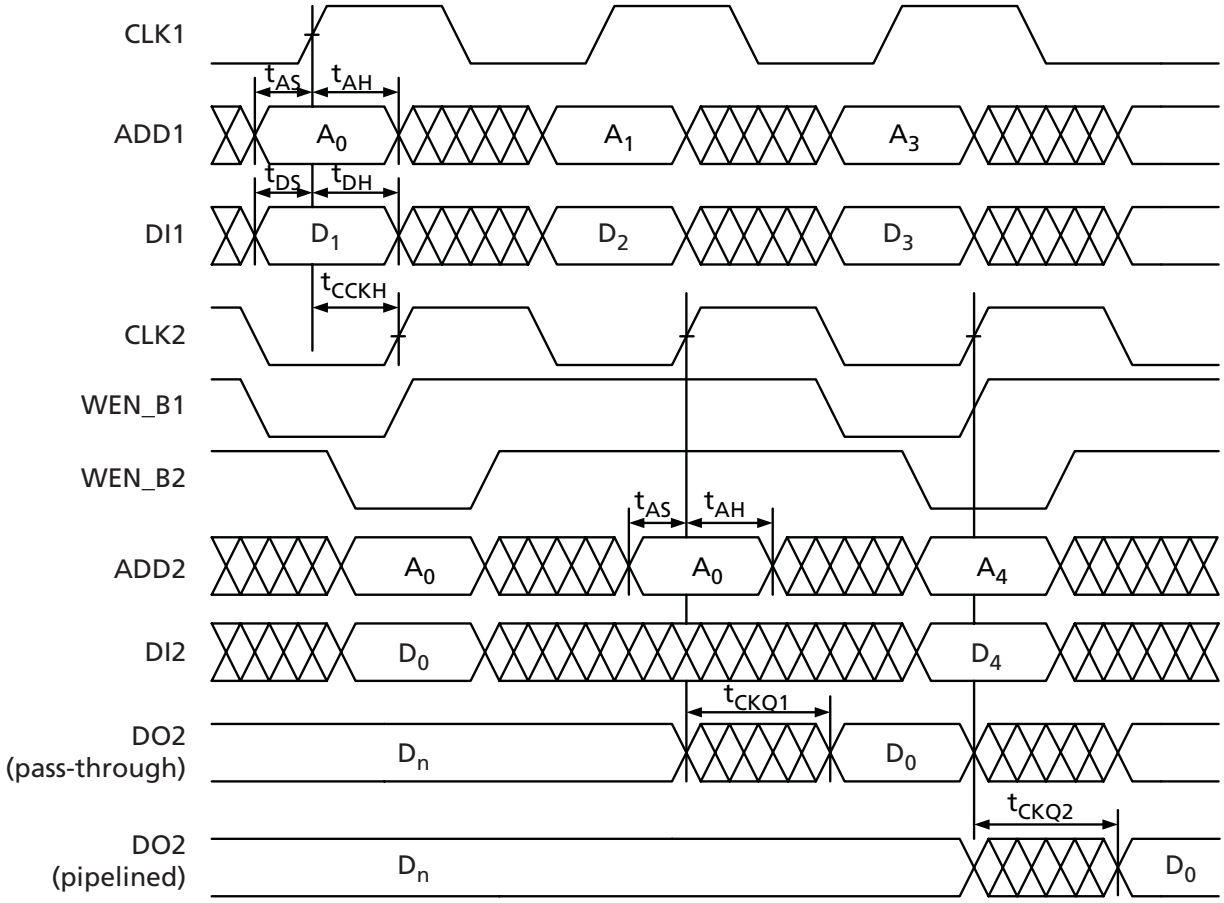


Figure 3-33 • **Write Access After Write onto Same Address**

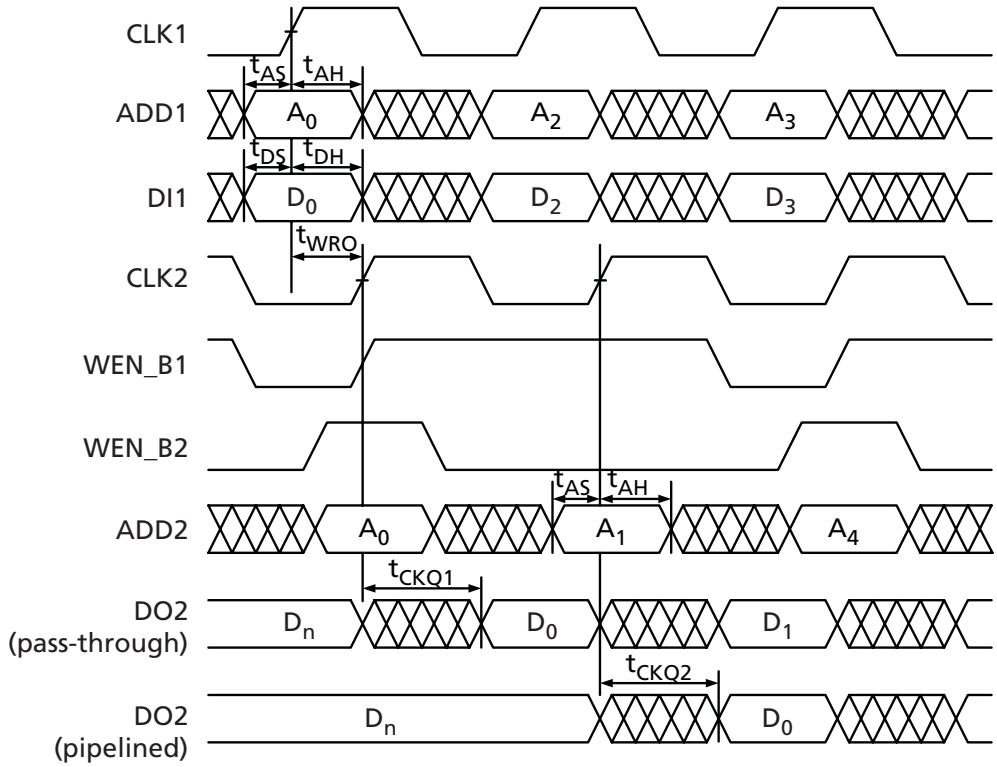


Figure 3-34 • **Read Access After Write onto Same Address**

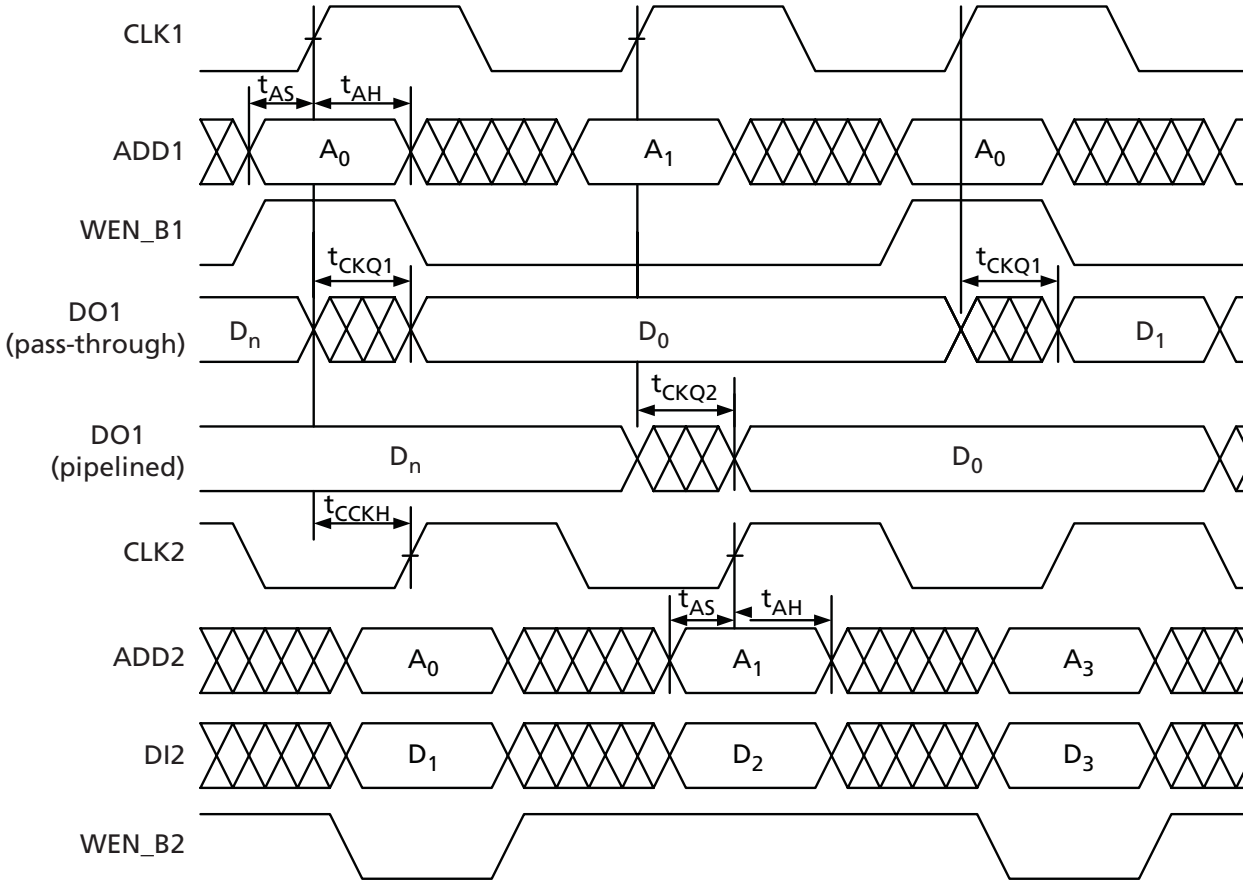


Figure 3-35 • **Write Access After Read onto Same Address**

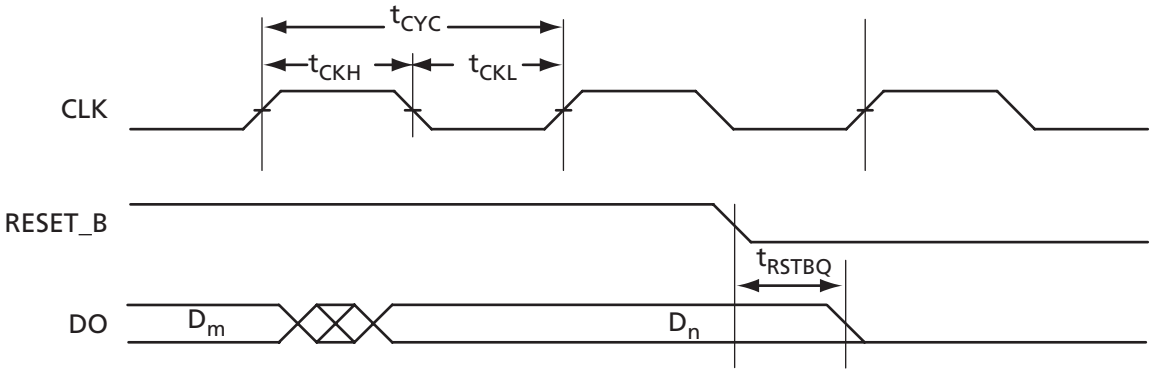


Figure 3-36 • **RAM Reset**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-147 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup time	0.84	ns
t_{AH}	Address Hold time	0.16	ns
t_{ENS}	REN_B, WEN_B Setup time	0.82	ns
t_{ENH}	REN_B, WEN_B Hold time	0.16	ns
t_{BKS}	BLK_B Setup time	1.67	ns
t_{BKH}	BLK_B Hold time	0.16	ns
t_{DS}	Input data (DI) Setup time	0.72	ns
t_{DH}	Input data (DI) Hold time	0.36	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	3.60	ns
	Clock High to New Data Valid on DO (flow-through, WMODE = 1)	3.12	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	1.84	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	1.23	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	2.58	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	2.10	ns
	RESET_B Low to Data Out Low on DO (pipelined)	2.10	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.24	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.56	ns
t_{CYC}	Clock Cycle time	5.17	ns
F_{MAX}	Maximum Frequency	193	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Table 3-148 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup time	0.84	ns
t_{AH}	Address Hold time	0.16	ns
t_{ENS}	REN_B, WEN_B Setup time	0.74	ns
t_{ENH}	REN_B, WEN_B Hold time	0.08	ns
t_{DS}	Input data (DI) Setup time	0.72	ns
t_{DH}	Input data (DI) Hold time	0.36	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	4.29	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	1.75	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	2.10	ns
	RESET_B Low to Data Out Low on DO (pipelined)	2.10	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.24	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.56	ns
t_{CYC}	Clock Cycle time	5.17	ns
F_{MAX}	Maximum Frequency	193	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-149 • **RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup time	1.53	ns
t_{AH}	Address Hold time	0.29	ns
t_{ENS}	REN_B, WEN_B Setup time	1.50	ns
t_{ENH}	REN_B, WEN_B Hold time	0.29	ns
t_{BKS}	BLK_B Setup time	3.05	ns
t_{BKH}	BLK_B Hold time	0.29	ns
t_{DS}	Input data (DI) Setup time	1.33	ns
t_{DH}	Input data (DI) Hold time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	6.61	ns
	Clock High to New Data Valid on DO (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	3.38	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	1.23	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	4.65	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	3.86	ns
	RESET_B Low to Data Out Low on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B Removal	1.12	ns
$t_{RECRSTB}$	RESET_B Recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.01	ns
t_{CYC}	Clock Cycle time	9.30	ns
F_{MAX}	Maximum Frequency	108	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Table 3-150 • **RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address Setup time	1.53	ns
t_{AH}	Address Hold time	0.29	ns
t_{ENS}	REN_B, WEN_B Setup time	1.36	ns
t_{ENH}	REN_B, WEN_B Hold time	0.15	ns
t_{DS}	Input data (DI) Setup time	1.33	ns
t_{DH}	Input data (DI) Hold time	0.66	ns
t_{CKQ1}	Clock High to New Data Valid on DO (output retained, WMODE = 0)	7.88	ns
t_{CKQ2}	Clock High to New Data Valid on DO (pipelined)	3.20	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	ns
t_{RSTBQ}	RESET_B Low to Data Out Low on DO (flow through)	3.86	ns
	RESET_B Low to Data Out Low on DO (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET_B Removal	1.12	ns
$t_{RECRSTB}$	RESET_B Recovery	5.93	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.01	ns
t_{CYC}	Clock Cycle time	9.30	ns
F_{MAX}	Maximum Frequency	108	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

FIFO

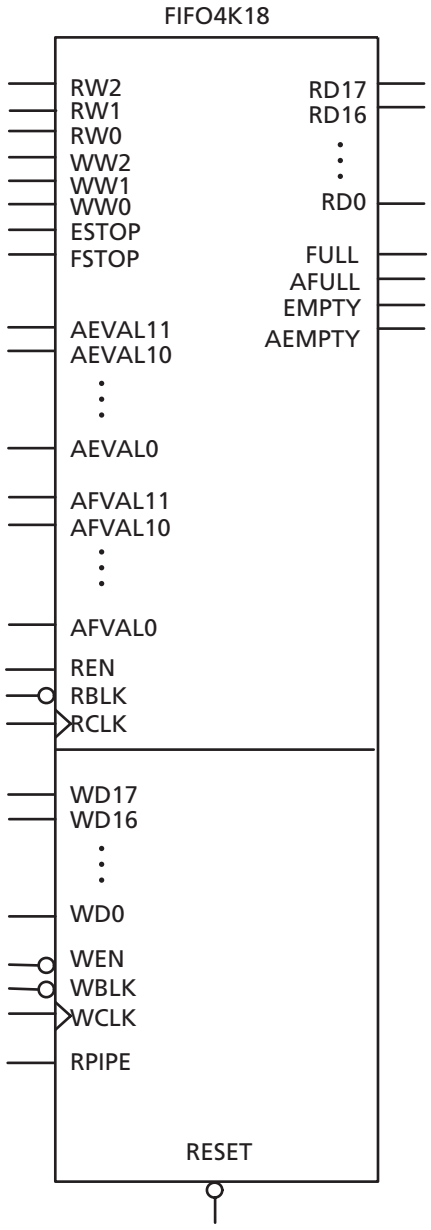


Figure 3-37 • **FIFO Model**

Timing Waveforms

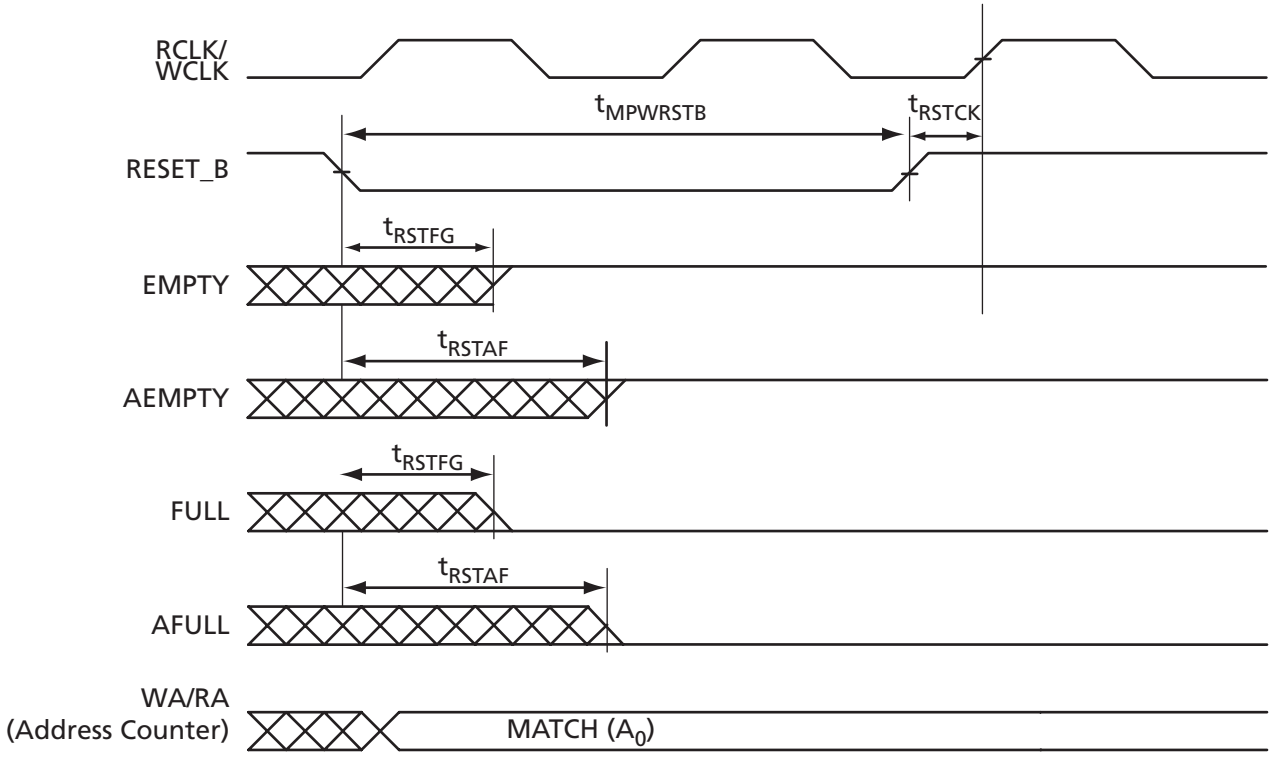


Figure 3-38 • **FIFO Reset**

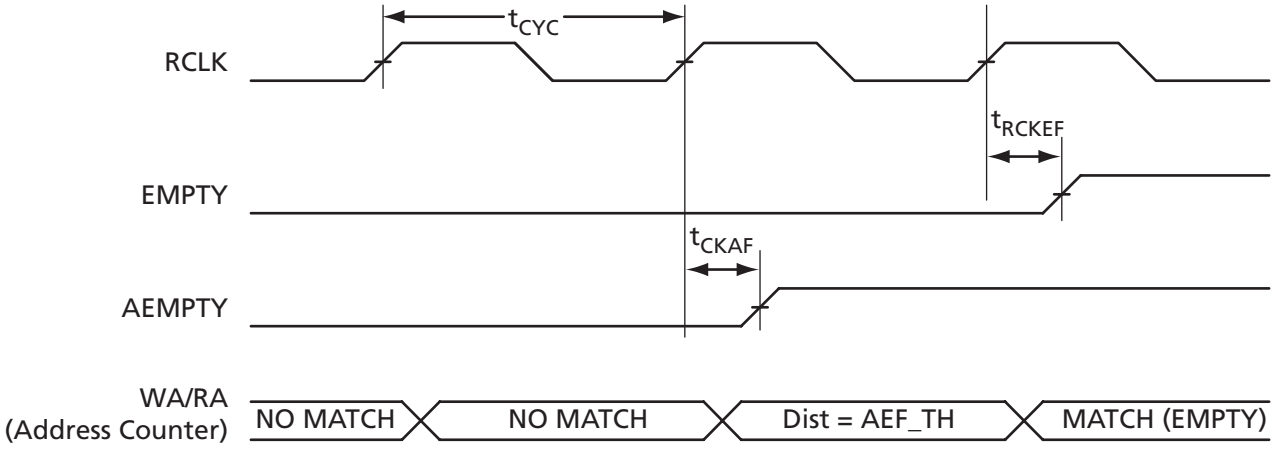


Figure 3-39 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

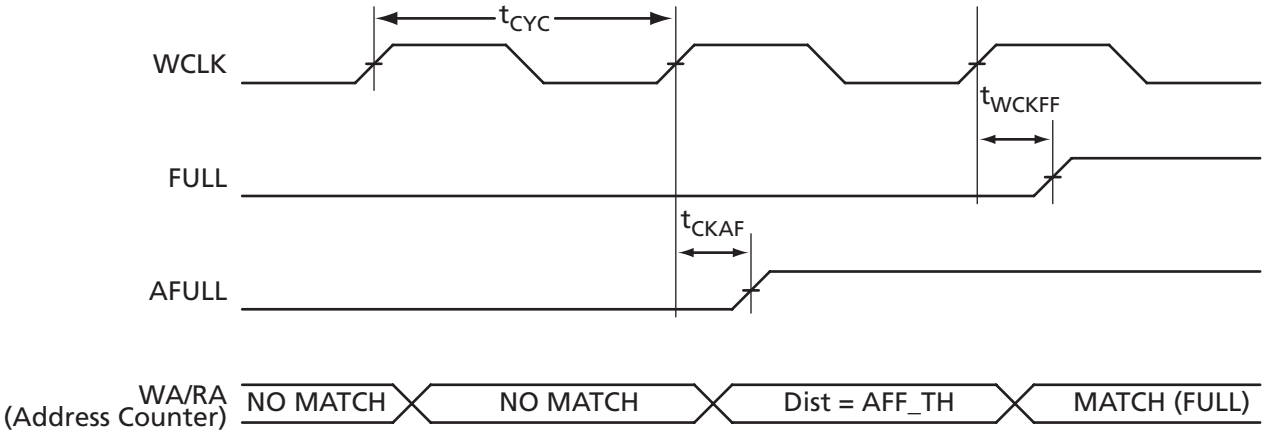


Figure 3-40 • **FIFO FULL Flag and AFULL Flag Assertion**

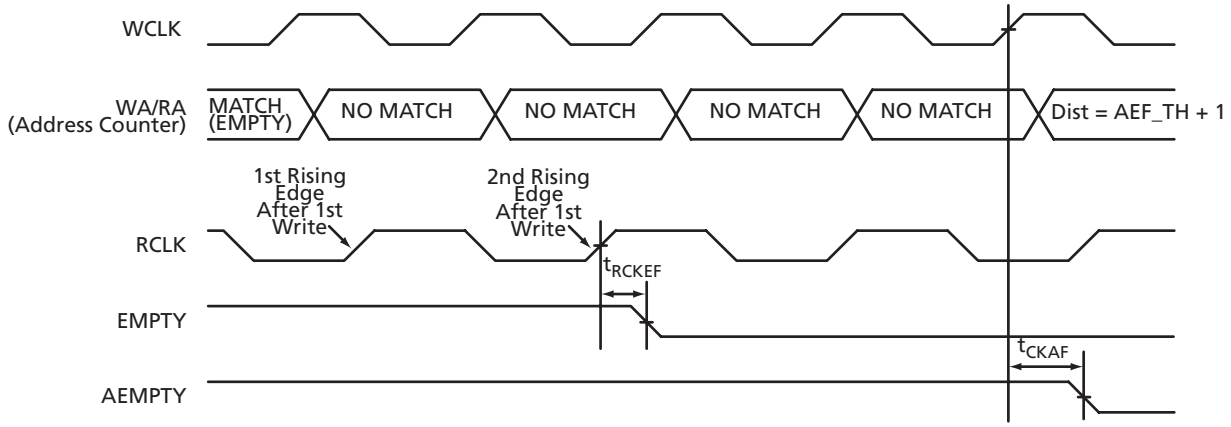


Figure 3-41 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

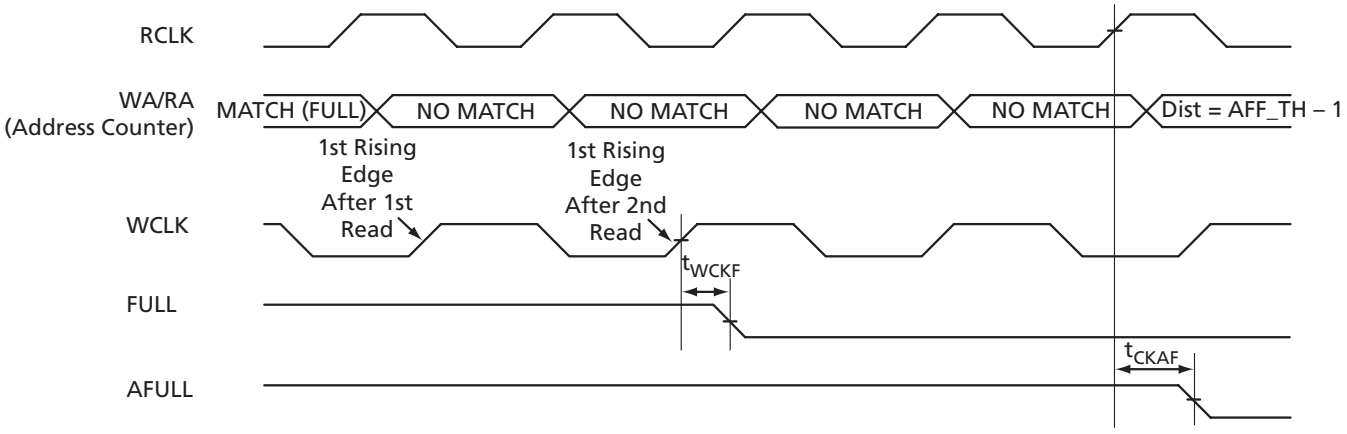


Figure 3-42 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-151 • **FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	2.03	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.16	ns
t_{BKS}	BLK_B Setup Time	0.30	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.77	ns
t_{DH}	Input Data (DI) Hold Time	0.25	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	3.39	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.83	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	3.60	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	3.42	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	13.10	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	3.55	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	12.97	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	2.06	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	2.06	ns
$t_{REMRSTB}$	RESET_B Removal	0.61	ns
$t_{RECRSTB}$	RESET_B Recovery	3.24	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.56	ns
t_{CYC}	Clock Cycle Time	5.17	ns
F_{MAX}	Maximum Frequency for FIFO	193	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

1.2 V DC Core Voltage

Table 3-152 • **FIFO**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	4.13	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.31	ns
t_{BKS}	BLK_B Setup Time	0.47	ns
t_{BKH}	BLK_B Hold Time	0.00	ns
t_{DS}	Input Data (DI) Setup Time	1.56	ns
t_{DH}	Input Data (DI) Hold Time	0.49	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	6.80	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	3.62	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	7.23	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	6.85	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	26.61	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	7.12	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	26.33	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	4.09	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	4.09	ns
$t_{REMRSTB}$	RESET_B Removal	1.23	ns
$t_{RECRSTB}$	RESET_B Recovery	6.58	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	1.01	ns
t_{CYC}	Clock Cycle Time	9.30	ns
F_{MAX}	Maximum Frequency for FIFO	108	MHz

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-7 on page 3-6 for derating values.*

Embedded FlashROM Characteristics

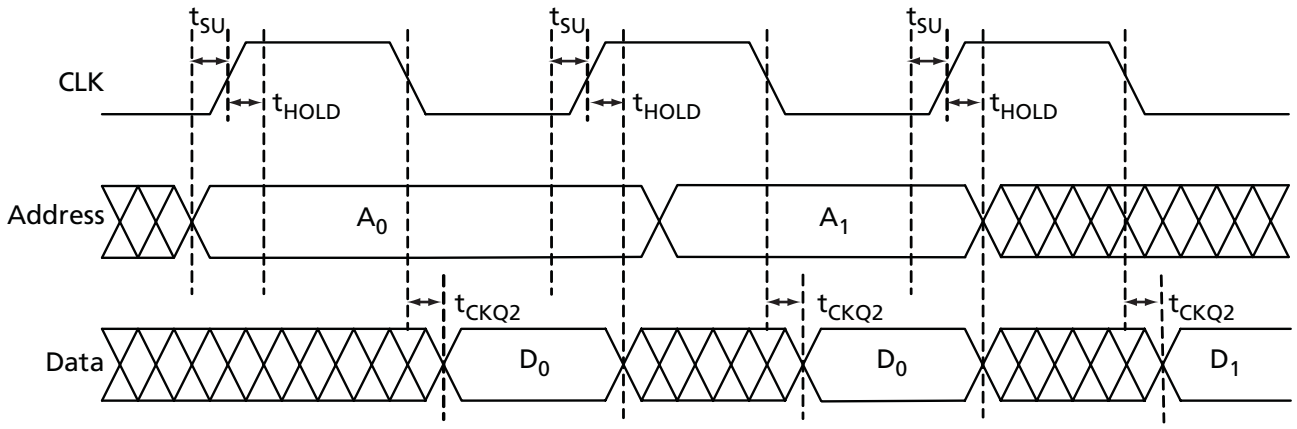


Figure 3-43 • **Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 3-153 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.425 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.58	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	34.47	ns
F_{MAX}	Maximum Clock Frequency	15	MHz

1.2 V DC Core Voltage

Table 3-154 • **Embedded FlashROM Access Time**
Worst Commercial-Case Conditions: T_J = 70°C, V_{CC} = 1.14 V

Parameter	Description	Std.	Units
t_{SU}	Address Setup Time	0.59	ns
t_{HOLD}	Address Hold Time	0.00	ns
t_{CK2Q}	Clock to Out	52.90	ns
F_{MAX}	Maximum Clock Frequency	10	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 3-15 for more details.

Timing Characteristics

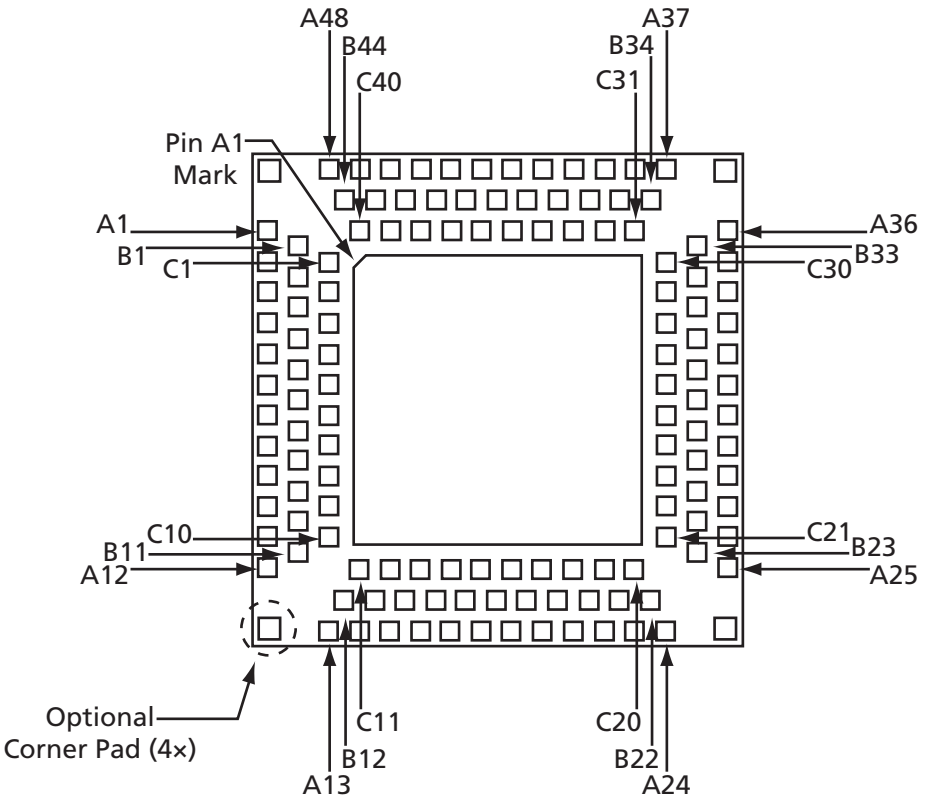
Table 3-155 • **JTAG 1532**
Commercial-Case Conditions: T_J = 70°C, Worst-Case V_{CC} = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (data out)				ns
t_{RSTB2Q}	Reset to Q (data out)				ns
F_{TCKMAX}	TCK Maximum Frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal Time				ns
$t_{TRSTREC}$	ResetB Recovery Time				ns
$t_{TRSTMPW}$	ResetB Minimum Pulse				ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 3-6 on page 3-6 for derating values.*

Package Pin Assignments

132-Pin QFN



Note: *This is the top view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

132-Pin QFN	
Pin Number	**AGL030 Function**
A1	IO80RSB1
A2	IO77RSB1
A3	NC
A4	IO76RSB1
A5	GEC0/IO73RSB1
A6	NC
A7	GEB0/IO71RSB1
A8	IO69RSB1
A9	NC
A10	V_{CC}
A11	IO67RSB1
A12	IO64RSB1
A13	IO59RSB1
A14	IO56RSB1
A15	NC
A16	IO55RSB1
A17	IO53RSB1
A18	V_{CC}
A19	IO50RSB1
A20	IO48RSB1
A21	IO45RSB1
A22	IO44RSB1
A23	IO43RSB1
A24	TDI
A25	TRST
A26	IO40RSB0
A27	NC
A28	IO39RSB0
A29	IO38RSB0
A30	IO36RSB0
A31	IO35RSB0
A32	GDC0/IO32RSB0
A33	NC
A34	V_{CC}
A35	IO30RSB0
A36	IO27RSB0

132-Pin QFN	
Pin Number	**AGL030 Function**
A37	IO22RSB0
A38	IO19RSB0
A39	NC
A40	IO18RSB0
A41	IO16RSB0
A42	IO14RSB0
A43	V_{CC}
A44	IO11RSB0
A45	IO08RSB0
A46	IO06RSB0
A47	IO05RSB0
A48	IO02RSB0
B1	IO81RSB1
B2	IO78RSB1
B3	GND
B4	IO75RSB1
B5	NC
B6	GND
B7	IO70RSB1
B8	NC
B9	GND
B10	IO66RSB1
B11	IO63RSB1
B12	FF/IO60RSB1
B13	IO57RSB1
B14	GND
B15	IO54RSB1
B16	IO52RSB1
B17	GND
B18	IO49RSB1
B19	IO46RSB1
B20	GND
B21	IO42RSB1
B22	TMS
B23	TDO
B24	IO41RSB0

132-Pin QFN	
Pin Number	**AGL030 Function**
B25	GND
B26	NC
B27	IO37RSB0
B28	GND
B29	GDA0/IO33RSB0
B30	NC
B31	GND
B32	IO29RSB0
B33	IO26RSB0
B34	IO23RSB0
B35	IO20RSB0
B36	GND
B37	IO17RSB0
B38	IO15RSB0
B39	GND
B40	IO12RSB0
B41	IO09RSB0
B42	GND
B43	IO04RSB0
B44	IO01RSB0
C1	IO82RSB1
C2	IO79RSB1
C3	NC
C4	IO74RSB1
C5	GEA0/IO72RSB1
C6	NC
C7	NC
C8	V_{CCI}B1
C9	IO65RSB1
C10	IO62RSB1
C11	IO61RSB1
C12	IO58RSB1
C13	NC
C14	NC
C15	IO51RSB1
C16	V_{CCI}B1

132-Pin QFN	
Pin Number	**AGL030 Function**
C17	IO47RSB1
C18	NC
C19	TCK
C20	NC
C21	V_{PUMP}
C22	V_{JTAG}
C23	NC
C24	NC
C25	NC
C26	GDB0/IO34RSB0
C27	NC
C28	$V_{CCI}B0$
C29	IO28RSB0
C30	IO25RSB0
C31	IO24RSB0
C32	IO21RSB0
C33	NC
C34	NC
C35	$V_{CCI}B0$
C36	IO13RSB0
C37	IO10RSB0
C38	IO07RSB0
C39	IO03RSB0
C40	IO00RSB0
D1	GND
D2	GND
D3	GND
D4	GND

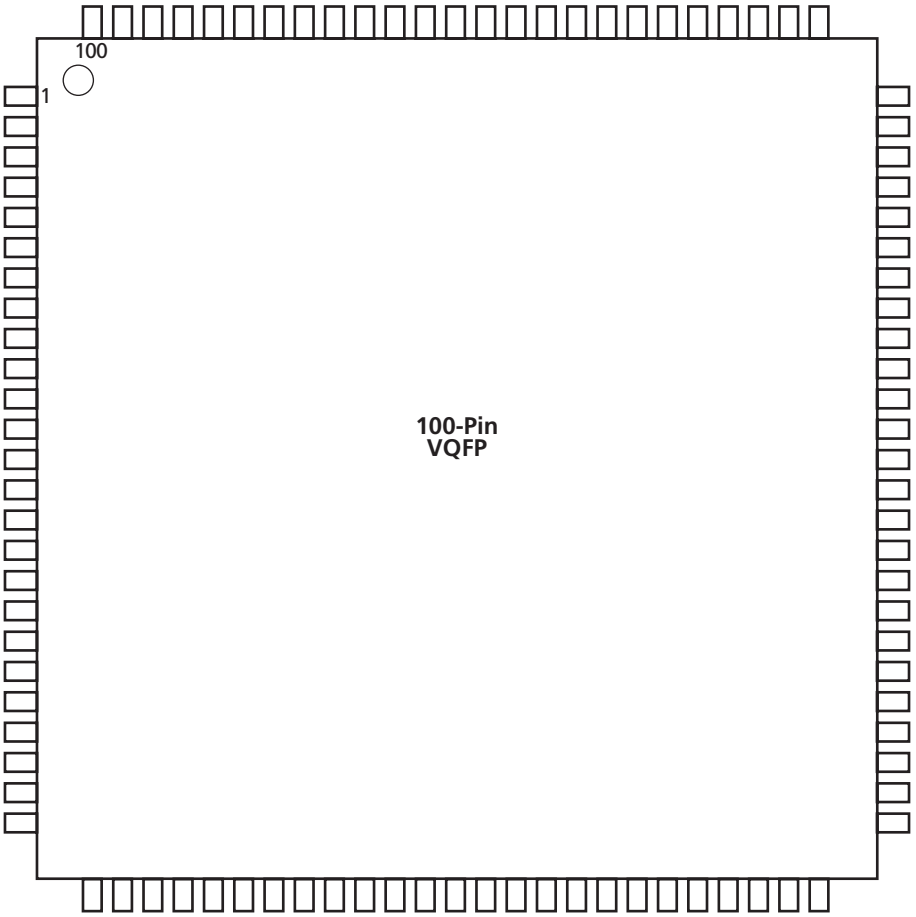
132-Pin QFN	
Pin Number	**AGL125 Function**
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	V_{CCI}B1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	V_{CCPLF}
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	V_{CC}
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	V_{CC}
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	V_{CC}
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	V_{CC}
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	V_{CC}
A35	IO44RSB0
A36	GBA2/IO41RSB0

132-Pin QFN	
Pin Number	**AGL125 Function**
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	V_{CCI}B0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	V_{CC}
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	V_{COMPLF}
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

132-Pin QFN	
Pin Number	**AGL125 Function**
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	V_{CC}
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	V_{CCI}B1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	V_{CCI}B1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

132-Pin QFN	
Pin Number	**AGL125 Function**
C17	IO83RSB1
C18	V_{CCI}B1
C19	TCK
C20	VMV1
C21	V_{PUMP}
C22	V_{JTAG}
C23	V_{CCI}B0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	V_{CCI}B0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	V_{CC}
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	V_{CCI}B0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

100-Pin VQFP



Note: *This is the top view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

100-Pin VQFP	
Pin Number	**AGL030 Function**
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	V_{CC}
18	V_{CCI}B1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	FF/IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1

100-Pin VQFP	
Pin Number	**AGL030 Function**
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0

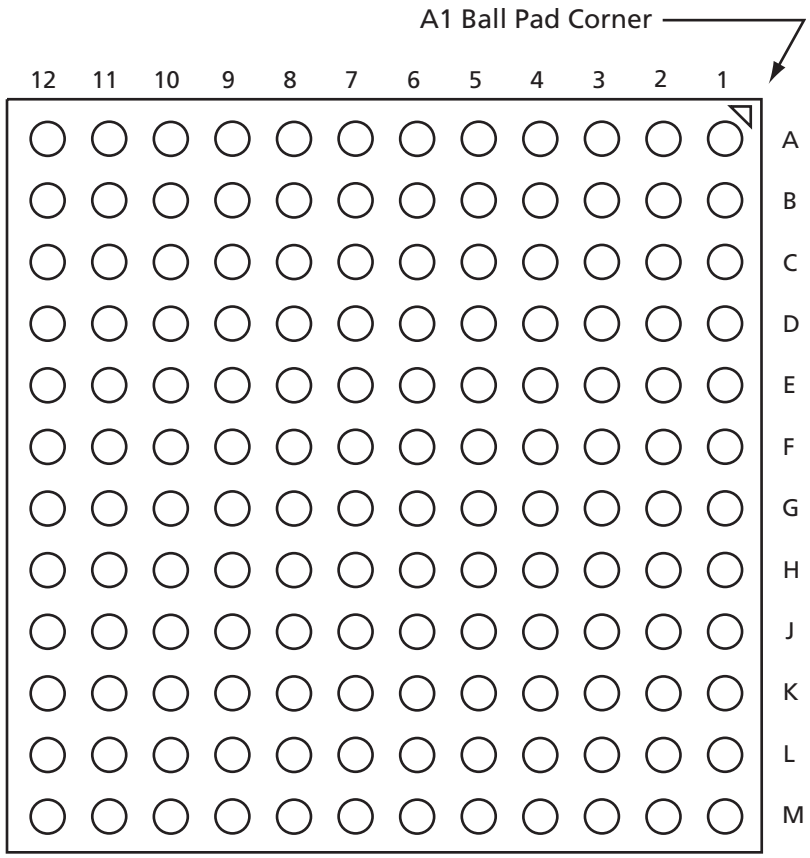
100-Pin VQFP	
Pin Number	**AGL030 Function**
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

100-Pin VQFP	
Pin Number	**AGL125 Function**
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	V_{COMPLF}
13	GFA0/IO122RSB1
14	V_{CCPLF}
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	V_{CC}
18	V_{CCI}B1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

100-Pin VQFP	
Pin Number	**AGL125 Function**
37	V_{CC}
38	GND
39	V_{CCI}B1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	V_{PUMP}
53	NC
54	TDO
55	TRST
56	V_{JTAG}
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	V_{CCI}B0
67	GND
68	V_{CC}
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

100-Pin VQFP	
Pin Number	**AGL125 Function**
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	V_{CCI}B0
88	GND
89	V_{CC}
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

144-Pin FBGA



Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

144-Pin FBGA	
Pin Number	**AGL125 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	V_{CC}
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	V_{CC}
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

144-Pin FBGA	
Pin Number	**AGL125 Function**
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	V_{CC}
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	V_{CCI}B1
E5	IO68RSB1
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO51RSB0
E9	V_{CCI}B0
E10	V_{CC}
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	V_{COMPLF}
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

144-Pin FBGA	
Pin Number	**AGL125 Function**
G1	GFA1/IO121RSB1
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	V_{CC}
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	V_{CC}
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	V_{CCI}B0
H11	IO49RSB0
H12	V_{CC}
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	V_{CCI}B1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	V_{CC}
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

144-Pin FBGA	
Pin Number	**AGL125 Function**
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	FF/GEB2/IO105RSB1
L4	IO102RSB1
L5	V_{CCI}B1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	V_{JTAG}
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	V_{CCI}B1
M11	V_{PUMP}
M12	GNDQ

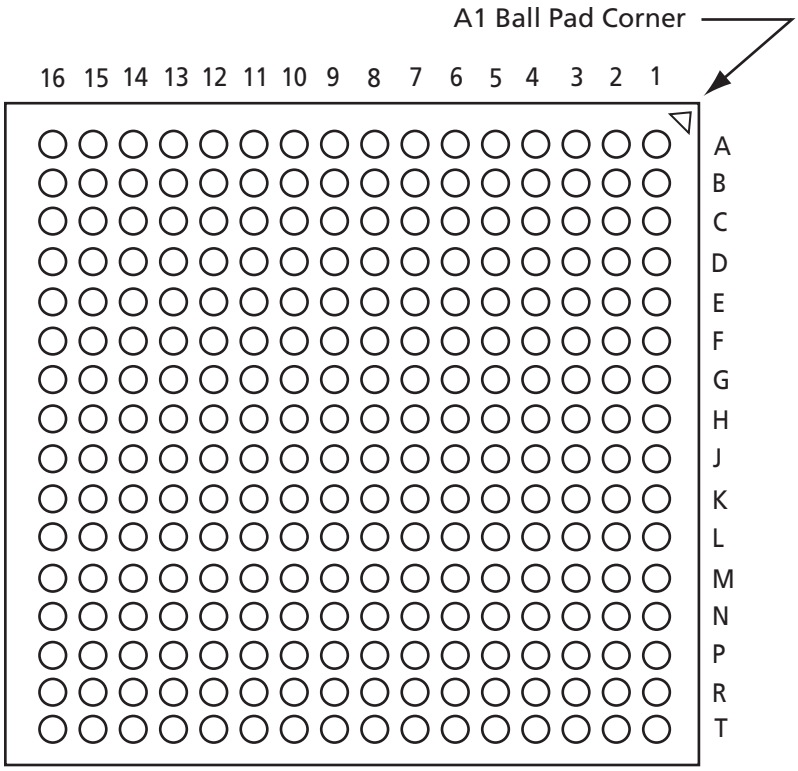
144-Pin FBGA	
Pin Number	**AGL600 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	V_{CC}
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	V_{CC}
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

144-Pin FBGA	
Pin Number	**AGL600 Function**
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	V_{CC}
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	V_{CCI}B3
E5	IO174NPB3
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	GCC1/IO69PDB1
E9	V_{CCI}B1
E10	V_{CC}
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	V_{COMPLF}
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1

144-Pin FBGA	
Pin Number	**AGL600 Function**
G1	GFA1/IO162PPB3
G2	GND
G3	V_{CCPLF}
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	V_{CC}
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	V_{CC}
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	V_{CCI}B1
H11	IO84PSB1
H12	V_{CC}
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	V_{CCI}B3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	V_{CC}
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1

144-Pin FBGA	
Pin Number	**AGL600 Function**
K1	GEB0/IO145NDB3
K2	GEA1/IO144PDB3
K3	GEA0/IO144NDB3
K4	GEA2/IO143RSB2
K5	IO119RSB2
K6	IO111RSB2
K7	GND
K8	IO94RSB2
K9	GDC2/IO91RSB2
K10	GND
K11	GDA0/IO88NDB1
K12	GDB0/IO87NDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO142RSB2
L4	IO136RSB2
L5	V_{CCI}B2
L6	IO115RSB2
L7	IO103RSB2
L8	IO97RSB2
L9	TMS
L10	V_{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO141RSB2
M3	IO138RSB2
M4	IO123RSB2
M5	IO126RSB2
M6	IO134RSB2
M7	IO108RSB2
M8	IO99RSB2
M9	TDI
M10	V_{CCI}B2
M11	V_{PUMP}
M12	GNDQ

256-Pin FBGA



Note: *This is the bottom view of the package.*

Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.actel.com/products/solutions/package/docs.aspx.

256-Pin FBGA	
Pin Number	**AGL600 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0

256-Pin FBGA	
Pin Number	**AGL600 Function**
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	V_{CCI}B0
E7	V_{CCI}B0
E8	IO25RSB0

256-Pin FBGA	
Pin Number	**AGL600 Function**
E9	IO31RSB0
E10	V_{CCI}B0
E11	V_{CCI}B0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3
F5	V_{CCI}B3
F6	GND
F7	V_{CC}
F8	V_{CC}
F9	V_{CC}
F10	V_{CC}
F11	GND
F12	V_{CCI}B1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	V_{CCI}B3
G6	V_{CC}
G7	GND
G8	GND
G9	GND
G10	GND
G11	V_{CC}
G12	V_{CCI}B1

256-Pin FBGA	
Pin Number	**AGL600 Function**
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3
H3	GFB1/IO163PPB3
H4	V_{COMPLF}
H5	GFC0/IO164NPB3
H6	V_{CC}
H7	GND
H8	GND
H9	GND
H10	GND
H11	V_{CC}
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	V_{CCPLF}
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	V_{CC}
J7	GND
J8	GND
J9	GND
J10	GND
J11	V_{CC}
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1

256-Pin FBGA	
Pin Number	**AGL600 Function**
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	$V_{CCI}B3$
K6	V_{CC}
K7	GND
K8	GND
K9	GND
K10	GND
K11	V_{CC}
K12	$V_{CCI}B1$
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	$V_{CCI}B3$
L6	GND
L7	V_{CC}
L8	V_{CC}
L9	V_{CC}
L10	V_{CC}
L11	GND
L12	$V_{CCI}B1$
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3

256-Pin FBGA	
Pin Number	**AGL600 Function**
M5	VMV3
M6	$V_{CCI}B2$
M7	$V_{CCI}B2$
M8	IO117RSB2
M9	IO110RSB2
M10	$V_{CCI}B2$
M11	$V_{CCI}B2$
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	V_{JTAG}
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2

256-Pin FBGA	
Pin Number	**AGL600 Function**
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	V_{PUMP}
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2

256-Pin FBGA	
Pin Number	**AGL600 Function**
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

Datasheet Information

Datasheet Categories

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Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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The datasheet supplement gives specific device information for a derivative family that differs from the general family datasheet. The supplement is to be used in conjunction with the datasheet to obtain more detailed information and for specifications that do not differ between the two families.

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www.actel.com

Actel Corporation
2061 Stierlin Court
Mountain View, CA
94043-4655 USA
Phone 650.318.4200
Fax 650.318.4600

Actel Europe Ltd.
River Court, Meadows Business Park
Station Approach, Blackwater
Camberley Surrey GU17 9AB
United Kingdom
Phone +44 (0) 1276 609 300
Fax +44 (0) 1276 607 540

Actel Japan
EXOS Ebisu Bldg. 4F
1-24-14 Ebisu Shibuya-ku
Tokyo 150 Japan
Phone +81.03.3445.7671
Fax +81.03.3445.7668
www.jp.actel.com

Actel Hong Kong
Suite 2114, Two Pacific Place
88 Queensway, Admiralty
Hong Kong
Phone +852 2185 6460
Fax +852 2185 6488
www.actel.com.cn

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