Integrated Dual Codec and DSP Microcomputer

Preliminary Technical Data — AD73422-40K

FEATURES

Single (+2.7V to +5.5V) Supply Operation

Codec

- Dual 16-Bit A/D Converter
- Dual 16-Bit D/A Converter
- Programmable Input/Output Sample Rates
- 75 dB ADC SNR
- 70 dB DAC SNR
- 64 kS/s Maximum Sample Rate
- -90 dB Crosstalk
- Low Group Delay (25μS typ per channel)
- Programmable Input/Output Gain
- Flexible Serial Port which allows extra AD733xx devices to be cascaded
- On-chip Reference

DSP Microcomputer

- 30 ns Instruction Cycle Time from 16.67 MHz Crystal @ 5.0 Volts
- 33 MIPS Sustained Performance
- Single-Cycle Instruction Execution
- Single-Cycle Context Switch
- 3-Bus Architecture Allows Dual Operand Fetches in Every Instruction Cycle
- Multifunction Instructions
- Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 100 Cycle Recovery from Power-Down Condition
- Low Power Dissipation in Idle Mode

APPLICATIONS

- General Purpose Analog I/O
- Speech Processing
- Cordless and Personal Communications
- Telephony
- Wireless Local Loop
- Active Control of Sound & Vibration
- Data Communications

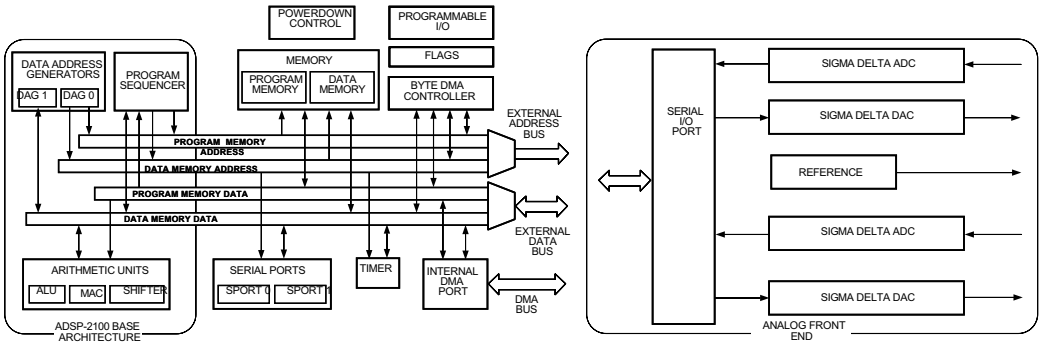
GENERAL DESCRIPTION

The AD73422-40K combines an AD73322 Dual Analog Front End (AFE) with an ADSP-218x DSP core in a single device. It is suitable for a variety of applications in the speech and telephony area including low bit rate, high quality compression, speech enhancement, recognition and synthesis. The low group delay characteristic of the part makes it suitable for single or multi-channel active control applications.. The AD73422-40K features a dual 16-bit linear codec with programmable Analog I/O gain, sample rates and serial transfer rates.

The ADSP-218x features the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory. It is optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The AD73422-40K features 40K bytes of on-chip DSP memory configured as 8K words (24-bit) of program RAM, and 8K words (16-bit) of data RAM. Power down circuitry is also provided to meet the low power needs of battery operated portable equipment. The AD73422-40K is available in a 119-ball Plastic Ball Grid Array (PBGA) package.

AD73422 BLOCK DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

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AD73422 BLOCK DIAGRAM

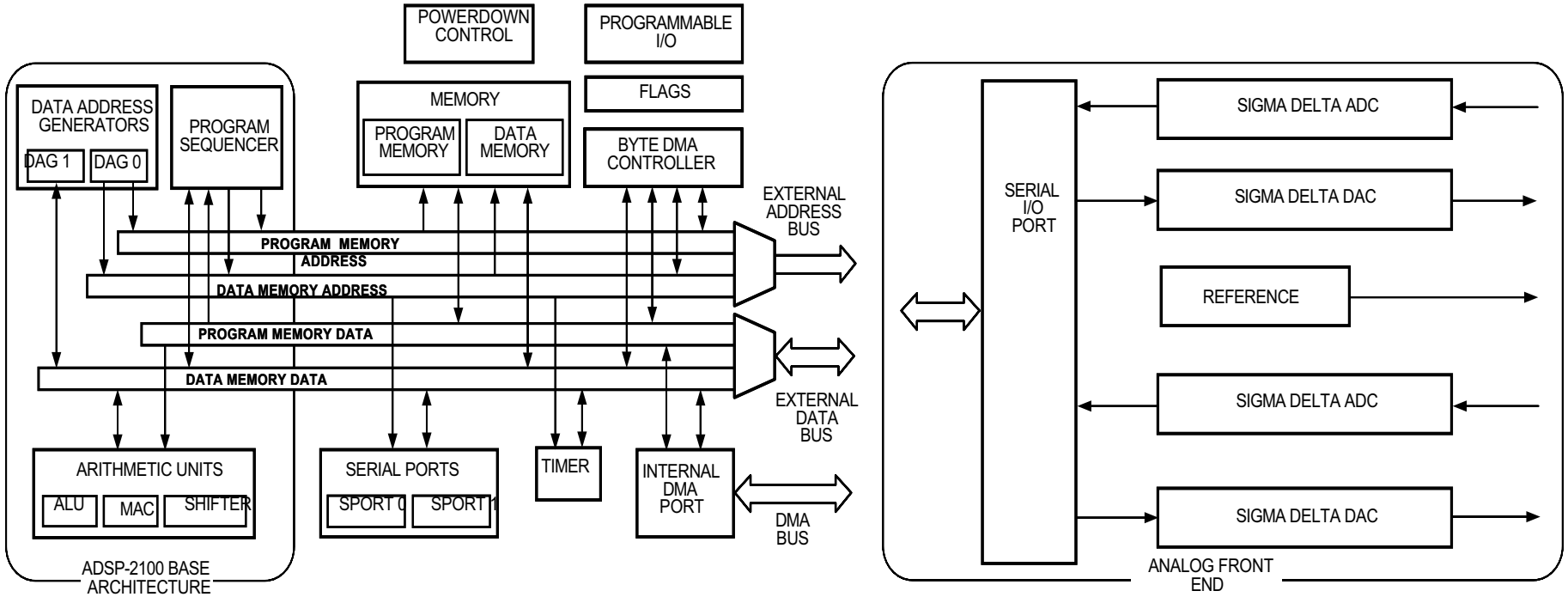


Figure 1. AD73422-40K Block Diagram

CONNECTIONS ON PLASTIC BGA

The AD73422-40K is packaged in a 119-ball PBGA. In order to facilitate good layout practice by isolating the digital and mixed-signal sections of the device, the ball-out has been configured according to Figure 1. The main section is taken up with DSP connections while the next two sections provide connectivity to the CODEC digital and analog sections.

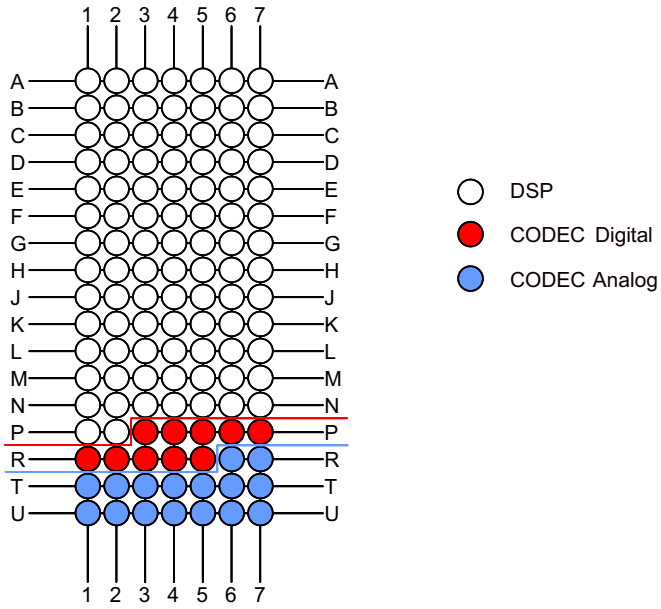
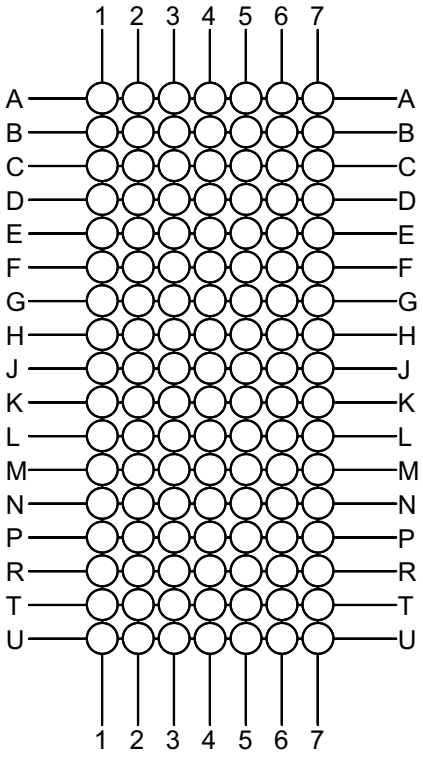


Figure 1. PBGA Connectivity



PBGA Ball Configurations

PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name	PBGA Number	Ball Name
A1	IRQE/PF4	E3	RFS0	J5	D22	N7	D13
A2	DMS	E4	A3/IAD2	J6	D21	P1	EBR
A3	VDD	E5	A2/IAD1	J7	D20	P2	D0/IAD13
A4	CLKIN	E6	A1/IAD0	K1	ELOUT	P3	DVDD
A5	A11/IAD10	E7	A0	K2	ELIN	P4	DGND
A6	A7/IAD6	F1	DR0	K3	EINT	P5	RESETC
A7	A4/IAD3	F2	SCLK0	K4	D19	P6	SCLK
B1	IRQL0/PF5	F3	DT1	K5	D18	P7	MCLK
B2	PMS	F4	PWDACK	K6	D17	R1	SDO
B3	WR	F5	BGH	K7	D16	R2	SDOFS
B4	XTAL	F6	PF0[MODE A]	L1	BG	R3	SDIFS
B5	A12/IAD11	F7	PF1[MODE B]	L2	D3/IACK	R4	SDI
B6	A8/IAD7	G1	TFS1	L3	D5/IAL	R5	SE
B7	A5/IAD4	G2	RFS1	L4	D8	R6	REFCAP
C1	IRQL1/PF6	G3	DR1	L5	D9	R7	REFOUT
C2	IOMS	G4	GND	L6	D12	T1	VFBP1
C3	RD	G5	PWD	L7	D15	T2	VINP1
C4	VDD	G6	VDD	M1	EBG	T3	VFBN1
C5	A13/IAD12	G7	PF2[MODE C]	M2	D2/IAD15	T4	VINN1
C6	A9/IAD8	H1	SCLK1	M3	D4/IS	T5	VFBN2
C7	GND	H2	ERESET	M4	D7/IWR	T6	VINN2
D1	IRQ2/PF7	H3	RESET	M5	VDD	T7	VFBP2
D2	CMS	H4	PF3	M6	D11	U1	AGND
D3	BMS	H5	FL0	M7	D14	U2	AVDD
D4	CLKOUT	H6	FL1	N1	BR	U3	VOUTP2
D5	GND	H7	FL2	N2	D1/IAD14	U4	VOUTN2
D6	D10/IAD9	J1	EMS	N3	VDD	U5	VOUTP1
D7	A6/IAD5	J2	EE	N4	D6/IRD	U6	VOUTN1
E1	DT0	J3	ECLK	N5	GND	U7	VINP2
E2	TFS0	J4	D23	N6	D10		

Outline Dimensions

(Dimensions shown in mm)

119-Pin Plastic Ball Grid Array
(B-119)