3

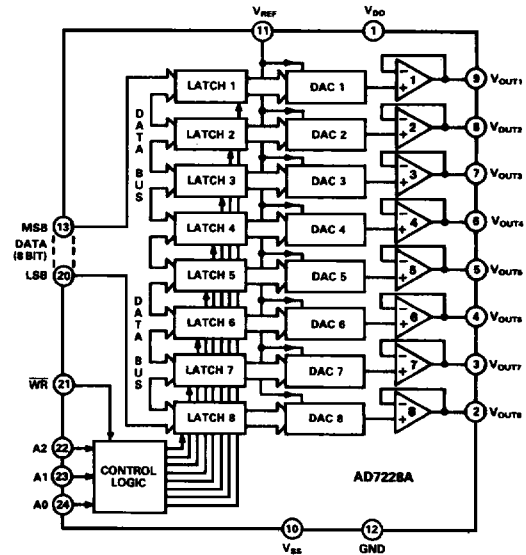## FEATURES
Eight 8-Bit DACs with Output Amplifiers
Operates with Single or Dual Supplies
µP Compatible (95ns $\overline{WR}$ Pulse)
No User Trims Required
Skinny 24-Pin DIPs, SOIC, and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION

The AD7228A contains eight 8-bit voltage-mode digital-to-analog converters, with output buffer amplifiers and interface logic on a single monolithic chip. No external trims are required to achieve full specified performance for the part.

Separate on-chip latches are provided for each of the eight D/A converters. Data is transferred into the data latches through a common 8-bit TTL/CMOS (5V) compatible input port. Address inputs A0, A1 and A2 determine which latch is loaded when $\overline{WR}$ goes low. The control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 to +10V when using dual supplies. The part is also specified for single supply +15V operation using a reference of +10V and single supply +5V operation using a reference of +1.23V. Each output buffer amplifier is capable of developing +10V across a 2kΩ load.

The AD7228A is fabricated on an all ion-implanted, high-speed, Linear Compatible CMOS (LC²MOS) process which has been specifically developed to integrate high-speed digital logic circuits and precision analog circuits on the same chip.

PRODUCT HIGHLIGHTS

1. **Eight DACs and Amplifiers in Small Package**
   The single-chip design of eight 8-bit DACs and amplifiers allows a dramatic reduction in board space requirements and offers increased reliability in systems using multiple converters. Its pinout is aimed at optimizing board layout with all analog inputs and outputs at one side of the package and all digital inputs at the other.

2. **Single or Dual Supply Operation**
   The voltage-mode configuration of the DACs allows single supply operation of the AD7228A. The part can also be operated with dual supplies giving enhanced performance for some parameters.

3. **Microprocessor Compatibility**
   The AD7228A has a common 8-bit data bus with individual DAC latches, providing a versatile control architecture for simple interface to microprocessors. All latch enable signals are level triggered and speed compatible with most high-performance 8-bit microprocessors.

AD7228A—SPECIFICATIONS

DUAL SUPPLY ($V_{DD} = 10.8V$ to $16.5V$; $V_{SS} = -5V \pm 10\%$; $GND = 0V$; $V_{REF} = +2V$ to $+10V^1$; $R_L = 2k\Omega$, $C_L = 100pF$ unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AB Version[2]	AC Version	AT Version	AU Version	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	$V_{DD} = +15V \pm 10\%$, $V_{REF} = +10V$
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error[4]	±1	±1/2	±1	±1/2	LSB max	Typical tempco is 5ppm/°C with $V_{REF} = +10V$
Zero Code Error						
@25°C	±25	±15	±25	±15	mV max	Typical tempco is 30µV/°C
T_{min} to T_{max}	±30	±20	±30	±20	mV max	
Minimum Load Resistance	2	2	2	2	kΩ min	$V_{OUT} = +10V$
REFERENCE INPUT						
Voltage Range[1]	2 to 10	2 to 10	2 to 10	2 to 10	V_{min} to V_{max}	
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
AC Feedthrough	−70	−70	−70	−70	dB typ	$V_{REF} = 8V$ p-p Sine Wave @ 10kHz/
DIGITAL INPUTS						
Input High Voltage, V_{INH}	2.4	2.4	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	0.8	0.8	V max	
Input Leakage Current	±1	±1	±1	±1	µA max	$V_{IN} = 0V$ or V_{DD}
Input Capacitance[5]	8	8	8	8	pF max	
Input Coding	Binary	Binary	Binary	Binary		
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/µs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	µs max	$V_{REF} = +10V$; Settling Time to ±1/2LSB
Negative Full-Scale Change	5	5	5	5	µs max	$V_{REF} = +10V$; Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. $V_{REF} = 0V$; $\overline{WR} = V_{DD}$
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. $V_{REF} = +10V$; $\overline{WR} = 0V$
POWER SUPPLIES						
V_{DD} Range	10.8/16.5	10.8/16.5	10.8/16.5	10.8/16.5	V_{min}/V_{max}	For Specified Performance
V_{SS} Range	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	−4.5/−5.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	
I_{SS}						Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
@25°C	14	14	14	14	mA max	
T_{min} to T_{max}	18	18	20	20	mA max	

SINGLE SUPPLY[7] ($V_{DD} = +15V \pm 10\%$, $V_{SS} = GND = 0V$; $V_{REF} = +10V$; $R_L = 2k\Omega$, $C_L = 100pF$ unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AB	AC	AT	AU	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error[3]	±2	±1	±2	±1	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Minimum Load Resistance	2	2	2	2	kΩ min	$V_{OUT} = +10V$
REFERENCE INPUT						
Input Resistance	2	2	2	2	kΩ min	
Input Capacitance[5]	500	500	500	500	pF max	Occurs when each DAC is loaded with all 1s.
DIGITAL INPUTS	As per Dual Supply Specifications					
DYNAMIC PERFORMANCE[5]						
Voltage Output Slew Rate	2	2	2	2	V/µs min	
Voltage Output Settling Time						
Positive Full-Scale Change	5	5	5	5	µs max	Settling Time to ±1/2LSB
Negative Full-Scale Change	7	7	7	7	µs max	Settling Time to ±1/2LSB
Digital Feedthrough	50	50	50	50	nV secs typ	Code transition all 0s to all 1s. $V_{REF} = 0V$; $\overline{WR} = V_{DD}$
Digital Crosstalk[6]	50	50	50	50	nVsecs typ	Code transition all 0s to all 1s. $V_{REF} = +10V$; $\overline{WR} = 0V$.
POWER SUPPLIES						
V_{DD} Range	13.5/16.5	13.5/16.5	13.5/16.5	13.5/16.5	V_{min}/V_{max}	For Specified Performance
I_{DD}						Outputs Unloaded; $V_{IN} = V_{INL}$ or V_{INH}
@25°C	16	16	16	16	mA max	
T_{min} to T_{max}	20	20	22	22	mA max	

NOTES

[1]V_{OUT} must be less than V_{DD} by 3.5V to ensure correct operation.
[2]Temperature ranges are as follows:
  AB, C Versions; −40°C to +85°C
  AT, U Versions; −55°C to +125°C
[3]Total Unadjusted Error includes zero code error, relative accuracy and full-scale error.
[4]Calculated after zero code error has been adjusted out.
[5]Sample tested at 25°C to ensure compliance.
[6]The glitch impulse transferred to the output of one converter (not addressed) due to a change in the digital input code to another addressed converter.
[7]Single +5V operation is also possible with degraded performance (see Figure 14).
Specifications subject to change without notice.

REV. 0

+5V SUPPLY OPERATION (V_{DD} = +5V ± 5%, V_{SS} = 0 to −5V ± 10%, GND = 0V, V_{REF} = +1.25V, R_L = 2kΩ, C_L =100pF unless otherwise stated.) All specifications T_{min} to T_{max} unless otherwise noted.

Parameter	AD7228AB	AD7228AC	AD7228AT	AD7228AU	Units	Conditions/Comments
STATIC PERFORMANCE						
Resolution	8	8	8	8	Bits	
Relative Accuracy	±2	±2	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±4	±2	±4	±2	LSB max	
Zero Code Error						
@ 25°C	±30	±20	±30	±20	mV max	
T_{min} to T_{max}	±40	±30	±40	±30	mV max	
REFERENCE INPUT						
Reference Input Range	1.2	1.2	1.2	1.2	V min	
	1.3	1.3	1.3	1.3	V max	
Reference Input Resistance	2	2	2	2	kΩ min	
Reference Input Capacitance	500	500	500	500	pF max	
POWER REQUIREMENTS						
Positive Supply Range	4.75/5.25	4.75/5.25	4.75/5.25	4.75/5.25	V min/V max	For Specified Performance
Positive Supply Current						
@ 25°C	16	16	16	16	μA max	
T_{min} to T_{max}	20	20	22	22	μA max	
Negative Supply Current						
@ 25°C	14	14	14	14	μA max	
T_{min} to T_{max}	18	18	20	20	μA max	

NOTES
All other specifications as per Dual Supply Specifications except for negative full-scale settling-time when V_{SS} = 0V.
Specifications subject to change without notice.

SWITCHING CHARACTERISTICS[1, 2] (See Figures 1, 2; V_{DD} = +5V ± 5% or +10.8V to +16.5V; V_{SS} = 0V or −5V ±10%)

Parameters	Limit at 25°C All Grades	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	Address to $\overline{WR}$ Setup Time
t_2	0	0	0	ns min	Address to $\overline{WR}$ Hold Time
t_3	70	90	100	ns min	Data Valid to $\overline{WR}$ Setup Time
t_4	10	10	10	ns min	Data Valid to $\overline{WR}$ Hold Time
t_5	95	120	150	ns min	Write Pulse Width

NOTES
[1]Sample tested at 25°C to ensure compliance. All input rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 5$ns.
[2]Timing measurement reference level is $\dfrac{V_{INH} + V_{INL}}{2}$

INTERFACE LOGIC INFORMATION

Address lines A0, A1 and A2 select which DAC accepts data
from the input port. Table I shows the selection table for the
eight DACs with Figure 1 showing the input control logic.
When the $\overline{WR}$ signal is low, the input latch of the selected
DAC is transparent, and its output responds to activity on the
data bus. The data is latched into the addressed DAC latch on
the rising edge of $\overline{WR}$. While $\overline{WR}$ is high, the analog outputs
remain at the value corresponding to the data held in their
respective latches.

AD7228A Control Inputs				AD7228A
$\overline{WR}$	A2	A1	A0	Operation
H	X	X	X	No Operation Device Not Selected
L	L	L	L	DAC 1 Transparent
⌃	L	L	L	DAC 1 Latched
L	L	L	H	DAC 2 Transparent
L	L	H	L	DAC 3 Transparent
L	L	H	H	DAC 4 Transparent
L	H	L	L	DAC 5 Transparent
L	H	L	H	DAC 6 Transparent
L	H	H	L	DAC 7 Transparent
L	H	H	H	DAC 8 Transparent

H = High State   L = Low State   X = Don't Care
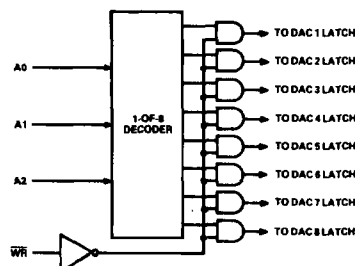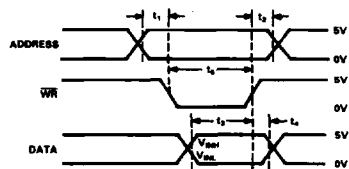
Table I. AD7228A Truth Table

Figure 1. Input Control Logic

NOTE:
THE SELECTED INPUT LATCH IS TRANSPARENT WHILE $\overline{WR}$ IS LOW.
THUS INVALID DATA DURING THIS TIME CAN CAUSE SPURIOUS OUTPUTS

Figure 2. Write Cycle Timing Diagram

AD7228A

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . $-0.3V, +17V$

V_{DD} to V_{SS} . . . . $-0.3V, +24V$

Digital Input Voltage to GND . . . . $-0.3V, V_{DD}$

V_{REF} to GND . . . . $-0.3V, V_{DD}$

V_{OUT} to GND[1] . . . . V_{SS}, V_{DD}

Power Dissipation (Any Package) to $+75°C$ 1000mW

Derates above 75°C by . . . . 2.0mW/°C

Operating Temperature

Commercial . . . . $-40°C$ to $+85°C$

Industrial . . . . $-40°C$ to $+85°C$

Extended . . . . $-55°C$ to $+125°C$

Storage Temperature . . . . $-65°C$ to $+150°C$

Lead Temperature (Soldering, 10secs) . . . . $+300°C$

NOTE

[1]Outputs may be shorted to any voltage in the range V_{SS} to V_{DD} provided that the power dissipation of the package is not exceeded. Typical short circuit current for a short to GND or V_{SS} is 50mA.
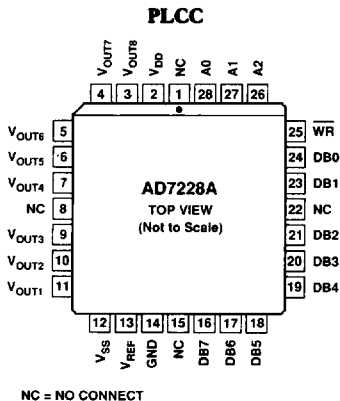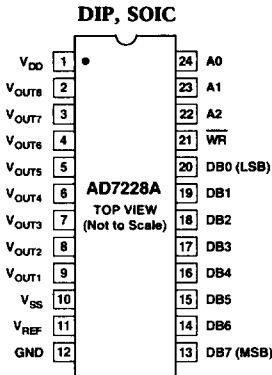
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

WARNING!

PIN CONFIGURATIONS

DIP, SOIC

V_{DD}	1	24	A0
V_{OUT8}	2	23	A1
V_{OUT7}	3	22	A2
V_{OUT6}	4	21	$\overline{WR}$
V_{OUT5}	5	20	DB0 (LSB)
V_{OUT4}	6	19	DB1
V_{OUT3}	7	18	DB2
V_{OUT2}	8	17	DB3
V_{OUT1}	9	16	DB4
V_{SS}	10	15	DB5
V_{REF}	11	14	DB6
GND	12	13	DB7 (MSB)

AD7228A TOP VIEW (Not to Scale)

PLCC

Top pins: V_{OUT7} 4, V_{OUT8} 3, V_{DD} 2, NC 1, A0 28, A1 27, A2 26

V_{OUT6}	5	25	$\overline{WR}$
V_{OUT5}	6	24	DB0
V_{OUT4}	7	23	DB1
NC	8	22	NC
V_{OUT3}	9	21	DB2
V_{OUT2}	10	20	DB3
V_{OUT1}	11	19	DB4

AD7228A TOP VIEW (Not to Scale)

Bottom pins: V_{SS} 12, V_{REF} 13, GND 14, NC 15, DB7 16, DB6 17, DB5 18

NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7228ABN	$-40°C$ to $+85°C$	± 2 max	N-24
AD7228ACN	$-40°C$ to $+85°C$	± 1 max	N-24
AD7228ABP	$-40°C$ to $+85°C$	± 2 max	P-28A
AD7228ACP	$-40°C$ to $+85°C$	± 1 max	P-28A
AD7228ABR	$-40°C$ to $+85°C$	± 2 max	R-24
AD7228ACR	$-40°C$ to $+85°C$	± 1 max	R-24
AD7228ABQ	$-40°C$ to $+85°C$	± 2 max	Q-24
AD7228ACQ	$-40°C$ to $+85°C$	± 1 max	Q-24
AD7228ATQ[3]	$-55°C$ to $+125°C$	± 2 max	Q-24
AD7228AUQ[3]	$-55°C$ to $+125°C$	± 1 max	Q-24

NOTES

[1]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet and availability.

[2]N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip; R = Small Outline IC (SOIC). For outline information see Package Information section.

[3]These grades will be available to /883B processing only.