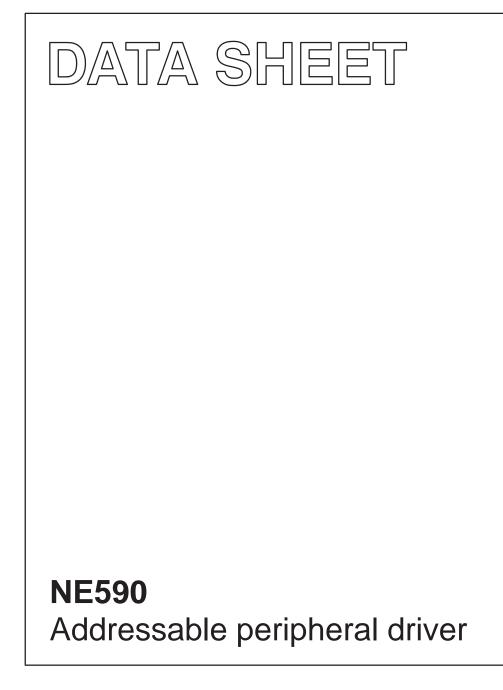
INTEGRATED CIRCUITS



Product data Supersedes data of 1994 Aug 31 File under Integrated Circuits, IC11 Handbook 2001 Aug 03





NE590

DESCRIPTION

The NE590 addressable peripheral driver is a high current latched driver, similar in function to the 9334 address decoder. The device has eight Darlington power outputs, each capable of 250 mA load current. The outputs are turned on or off by respectively loading a logic HIGH or logic LOW into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a \overline{CE} input line. A common clear input, \overline{CLR} , turns all outputs off when a logic LOW is applied.

The NE590 has eight open-collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin plastic DIP package.

FEATURES

- 8 high current outputs
- Low-loading bus compatible inputs
- Power-on clear ensures safe operation
- NE590 will operate in addressable or demultiplex mode
- Allows random (addressed) data entry
- Easily expandable
- NE590 is pin compatible with 54/74LS259

APPLICATIONS

- Relay driver
- Indicator lamp driver
- Triac trigger
- LED display digit driver
- Stepper motor driver

PIN CONFIGURATIONS

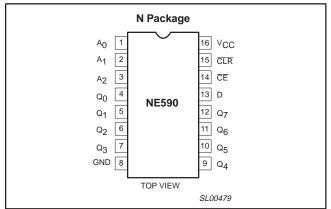


Figure 1. Pin Configuration

PIN DESCRIPTION

PIN	SYMBOL	NAME & FUNCTION
1-3	A ₀ -A ₂	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	Q ₀ -Q ₇	The 8 device outputs. The NE590 has open-collector Darlington outputs.
13	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that:
		"1" turns output switch "ON" "0" turns output switch "OFF"
		Thus in logic terms, the NE590 inverts data to the relevant output.
14	CE	The chip enable. When this input is LOW, the output latches will accept data. When \overline{CE} goes HIGH, all outputs will retain their existing state regardless of address or data input conditions.
15	CLR	The clear input. When CLR goes LOW all output switches are turned "OFF". A HIGH data input will override the clear function on the addressed latch.

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Dual In-Line Package (DIP)	0 °C to +70 °C	NE590N	SOT38-4

NE590

BLOCK DIAGRAM

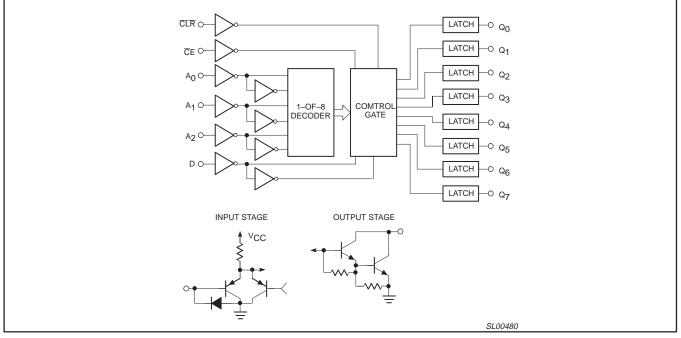


Figure 2. Block Diagram

TRUTH TABLE

		INPU	TS						OUTI	PUTS				MODE
CLR	CE	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q_3	Q_4	Q_5	Q_6	Q ₇	
L	Н	Х	Х	Х	Х	н	Н	Н	Н	Н	Н	Н	Н	Clear
L	L	L	L	L	L	н	Н	Н	Н	Н	Н	Н	Н	
L	L	н	L	L	L	L	Н	Н	Н	Н	Н	Н	Н	
L	L	L	Н	L	L	н	Н	Н	Н	Н	Н	Н	Н	Demultiplex
L	L	Н	Н	L	L	н	L	Н	Н	Н	Н	Н	Н	
L	L	L	Н	Н	Н	н	Н	Н	Н	н	н	Н	н	
L	L	Н	Н	Н	Н	н	Н	Н	Н	н	н	Н	L	
н	Н	Х	Х	Х	Х	Q _{N-1}								Memory
н	L	L	L	L	L	н	Q _{N-1}							
н	L	Н	L	L	L	L	Q _{N-1}							
н	L	L	Н	L	L	Q _{N-1}	Н	Q _{N-1}						Addrossoble Letab
н	L	Н	Н	L	L	Q _{N-1}	L	Q _{N-1}						Addressable Latch
н	L	L	Н	Н	Н	Q _{N-1}							Н	
н	L	Н	Н	Н	Н	Q _{N-1}							L	

NOTES:

X = Don't care condition

 Q_{N-1} = Previous output state

L = Low voltage level/"OFF" output state

H = High voltage level/"ON" output state

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Product data

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT		
V _{CC}	Supply voltage	-0.5 to +7	V		
V _{IN}	Input voltage	-0.5 to +15	V		
V _{OUT}	Output voltage	0 to +7	V		
I _{OUT}	Output current Each output All outputs	300 1000	mA		
P _D	Maximum power dissipation ¹ T _{amb} = 25 °C (still air)	1450	mW		
T _{amb}	Ambient temperature range	0 to +70	°C		
Тj	Junction temperature	165	°C		
T _{stg}	Storage temperature range	-65 to +150			
T _{sld}	Lead soldering temperature (10 sec max)	230	°C		

NOTE:

1. Derate above 25 $^\circ\text{C}$ at the following rates:

N package at 11.6 mW/°C.

DC ELECTRICAL CHARACTERISTICS

 V_{CC} = 4.75 V to 5.25 V; 0 $^{\circ}C \geq T_{amb} \leq$ +70 $^{\circ}C;$ unless otherwise specified. 1

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			
SYMBOL	PARAMETER	TEST CONDITIONS	Min	Min Typ		UNIT	
V _{IH}	HIGH-level input voltage		2.0			V	
V _{IL}	LOW-level input voltage				0.8		
V _{OL}	LOW-level output voltage	I_{OL} = 250 mA; T_{amb} = 25 °C		1.0	1.3		
		Over temperature			1.5	V	
I _{IH}	HIGH-level input current	V _{IN} =V _{CC}		0.1	10	μΑ	
I _{IL}	LOW-level input current CE input All other inputs	V _{IN} = 0 V		-25 -15	60 50	μA μA	
I _{OH}	Leakage current	V _{OUT} = 5.25 V		10	250	μA	
I _{CCL} I _{CCH}	Supply current All outputs LOW All outputs HIGH	$V_{S} = V_{CC} = 5 V$		33 15	50 50	mA mA	
PD	Power dissipation	No output load			350	mW	

NOTES:

1. All typical values are at V_{CC} = 5 V and T_{amb} = 25 °C.

NE590

SWITCHING CHARACTERISTICS

 $V_{CC} = 5 \text{ V}; \text{ T}_{amb} = 25 \text{ °C}.$

CVMDOL	DADAMETED	то	FROM		Limits			
SYMBOL	PARAMETER	то	FROM	Min	Min Typ Max			
t _{PLH} t _{PHL}	Propagation delay time Low-to-High ¹ High-to-Low ¹	Output	CE		65 115	150 230	ns	
t _{PLH} t _{PHL}	Low-to-High ² High-to-Low ²	Output	Data		65 120	130 240	ns	
t _{PLH} t _{PHL}	Low-to-High ³ High-to-Low ³	Output	Address		100 130	200 260	ns	
t _{PLH} t _{PHL}	Low-to-High ⁴ High-to-Low ⁴	Output	CLR		65	130	ns	
Switching	setup requirements							
t _{S(H)}		Chip enable	High data	210			ns	
t _{S(L)}		Chip enable	Low data	210			ns	
t _{S(A)}		Chip enable	Address	30			ns	
t _{H(H)}		Chip enable	High data	40			ns	
t _{H(L)}		Chip enable	Low data	30			ns	
t _{PW(E)}	Chip enable pulse width ¹			120			ns	

NOTES:

1. See Turn-On and Turn-Off Delays, Enable to Output and Enable Pulse Width timing diagram.

2. See Turn-On and Turn-Off Delays, Data to Output timing diagram.

3. See Turn-On and Turn-Off Delays, Address to Output timing diagram.

4. See Turn-Off Delay, Clear to Output timing diagram.

5. See Setup and Hold Time, Data to Enable timing diagram.

6. See Setup Time, Address to Enable timing diagram.

FUNCTIONAL DESCRIPTION

These peripheral drivers have latched outputs which hold the input data until cleared. The NE590 has active-Low, open-collector outputs. All outputs are cleared when power is first applied.

Addressable Latch Function

Any given output can be turned on or off by presenting the address of the output to be set or cleared to the three address pins, by holding the "D" input High to turn on the selected input, or by holding it Low to turn off, holding the \overline{CLR} input High, and bringing the \overline{CE} input Low. Once an output is turned on or off, it will remain so until addressed again, or until all outputs are cleared by bringing the \overline{CLR} , \overline{CE} , and "D" inputs Low.

Demultiplexer Operation

By bringing the CLR and CE inputs Low and the "D" input High, the addressed output will remain on and all other outputs will be off. This condition will remain only as long as the output is addressed.

High Current Outputs

The obvious advantage of these devices over the 9334 and N74LS259 (which provide a similar function) is the fact that the NE590 is capable of output currents of 250 mA at each of its eight outputs. It should be noted, however, that the load power dissipation would be over 2.5 W if all 8 outputs were to carry their full rated load current at one time. Since the total power dissipation is limited by the package to 1 W, and since the power dissipation due to supply current is 0.25 W, the total load power dissipation by the device is limited to 0.75 W, and decreases as ambient temperature rises.

The maximum die junction temperature must be limited to 165 $^{\circ}$ C, and the temperature rise above ambient and the junction temperature are defined as:

$$T_{R} = \theta_{JA} \times P$$
$$T_{j} = T_{amb} + T_{R}$$

where

 θ_{IA} is die junction to ambient thermal resistance.

P_D is total power dissipation

T_R is junction temperature rise above ambient

T_i is die junction temperature

T_{amb} is ambient (surrounding medium) temperature

For example, if we are using the NE590 in a plastic package in an application where the ambient temperature is never expected to rise above 50 °C, and the output current at the 8 outputs, when on, are 100, 40, 50, 200, 15, 30, 80, and 10 mA, we find from the graph of output voltage versus load current that the output voltages are expected to be about 0.92, 0.75, 0.78, 1.04, 0.5, 0.7, 0.9, and 0.4 V, respectively. Total device power due to these loads is found to be 473.5 mW. Adding the 250 mW due to the power supply brings total device power dissipation to 723.5 mW. The thermal resistance is 83 °C per W for plastic packages. Using the equations above we find:

 $T_R = 83 \times 0.7235 = 60 \ ^\circ C$ $T_i = 50 + 60 = 100 \ ^\circ C$

Thus we find that T_j is below the 165 °C maximum and this package could be used in this application. The graphs of total load power versus ambient temperature would also give us this same information, although interpreting the graphs would not yield the same accuracy.

Philips Semiconductors

Addressable peripheral driver

NE590



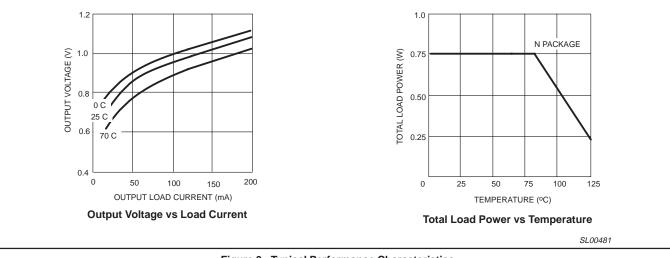


Figure 3. Typical Performance Characteristics

NE590

TIMING DIAGRAMS

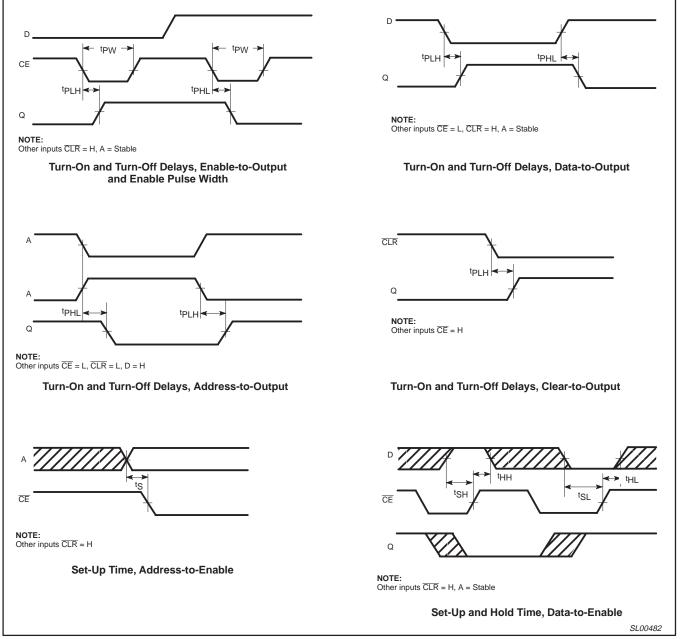


Figure 4. Timing Diagrams

NE590

TYPICAL APPLICATIONS

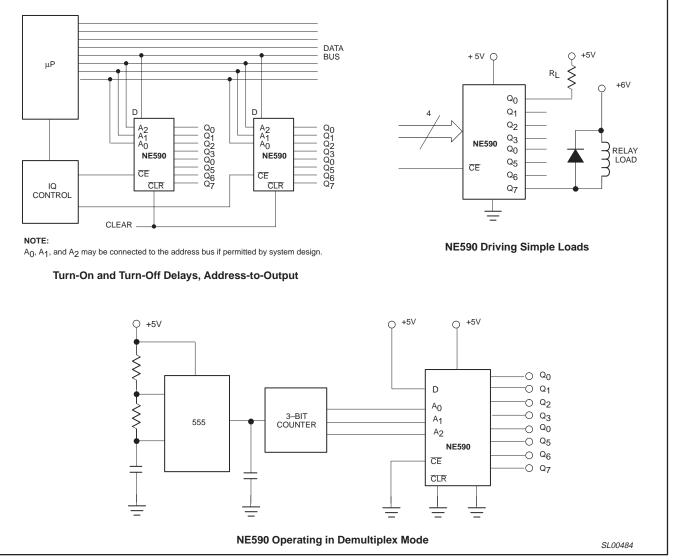
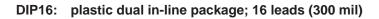
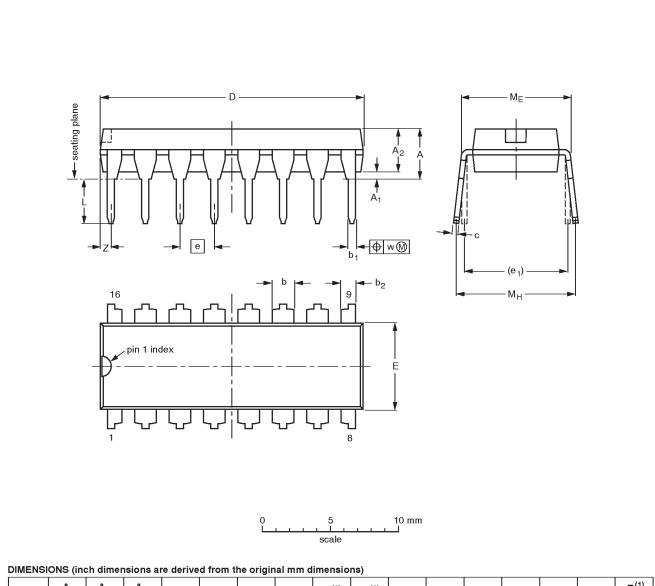


Figure 5. Typical Applications

2001 Aug 03

Addressable peripheral driver





UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	с	D ⁽¹⁾	Е ⁽¹⁾	е	e ₁	L	ME	м _н	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		EUROPEAN					
VERSION	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE	
SOT38-4						-92-11-17 95-01-14	

NE590

NE590

Data sheet status

Data sheet status ^[1]	Product status ^[2]	Definitions
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