25AA010A/25LC010A
25AA020A/25LC020A
25AA040A/25LC040A
25AA080A/25LC080A
25AA080B/25LC080B
25AA160A/25LC160A
25AA160B/25LC160B
25AA320A/25LC320A
25AA640A/25LC640A
25AA128/25LC128
25AA256/25LC256
25AA512/25LC512
25AA1024/25LC1024

SPI Serial EEPROM Family Data Sheet

Features:

- Max Clock Speed
  - 10 MHz (1K-256K)
  - 20 MHz (512K-1M)
- Byte and Page-level Write Operations
- Low-power CMOS Technology
  - Typical Write current: 5 mA
  - Typical Read current: 5 mA @ 10 MHz
    7 mA @ 20 MHz
  - Typical Standby current: 1 μA
- Write Cycle Time: 5 ms max.
  6 ms max. (25XX1024)
- Self-timed Erase and Write Cycles
- Erase Functions (25XX512 and 25XX1024)
  - Page Erase: 6 ms max.
  - Sector Erase: 15 ms max.
  - Chip Erase: 15 ms max.
- Built-in Write Protection
  - Power on/off data protection circuitry
  - Write enable latch
  - Write-protect pin
- Block/Sector Write Protection
  - Protect none, 1/4, 1/2 or all of array
- Sequential Read
- High Reliability
  - Data retention: > 200 years
  - ESD protection: > 4000V
  - Endurance > 1M Erase/Write Cycles
- Available in Standard 8-pin and 6-pin Packages
- Temperature Ranges Supported:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Pin Function Table

Name	Function
$\overline{CS}$	Chip Select
SO	Serial Data Output
$\overline{WP}$	Write-Protect
VSS	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Hold Input
VCC	Supply Voltage

Description:

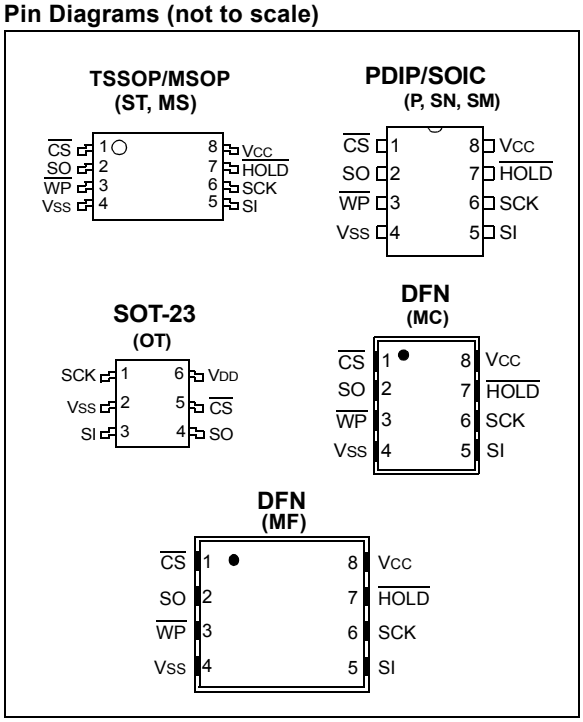
Microchip Technology Inc. supports the Serial Peripheral Interface (SPI) compatible serial bus architecture with low-voltage serial Electrically Erasable PROMs (EEPROM) that range in density from 1 Kbits up to 1 Mbits. Byte-level and page-level functions are supported, but the higher density 512 Kbit and 1 Mbit devices also feature Sector and Chip erase functions typically associated with Flash-based products.

The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select ($\overline{CS}$) input.

Communication to the device can be paused via the hold pin ($\overline{HOLD}$). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The entire series of SPI compatible devices are available in the standard 8-lead PDIP and SOIC packages, as well as the more advanced packages such as the 8-lead TSSOP, MSOP, 2x3 DFN, 5x6 DFN and 6-lead SOT-23. All packages are RoHS compliant with a Pb-free (Matte Tin) finish.

Pin Diagrams (not to scale)



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DEVICE SELECTION TABLE

Part Number	Density (bits)	Organization	VCC Range	Max Speed (MHz)	Page Size (Bytes)	Temp. Range	Packages
25LC010A	1K	128 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA010A	1K	128 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC020A	2K	256 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA020A	2K	256 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC040A	4K	512 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST, MC, OT
25AA040A	4K	512 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST, MC, OT
25LC080A	8K	1024 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST
25AA080A	8K	1024 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST
25LC080B	8K	1024 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA080B	8K	1024 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC160A	16K	2048 x 8	2.5-5.5V	10	16	I, E	P, MS, SN, ST
25AA160A	16K	2048 x 8	1.8-5.5V	10	16	I	P, MS, SN, ST
25LC160B	16K	2048 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA160B	16K	2048 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC320A	32K	4096 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA320A	32K	4096 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC640A	64K	8192 x 8	2.5-5.5V	10	32	I, E	P, MS, SN, ST
25AA640A	64K	8192 x 8	1.8-5.5V	10	32	I	P, MS, SN, ST
25LC128	128K	16,384 x 8	2.5-5.5V	10	64	I, E	P, SN, SM, ST, MF
25AA128	128K	16,384 x 8	1.8-5.5V	10	64	I	P, SN, SM, ST, MF
25LC256	256K	32,768 x 8	2.5-5.5V	10	64	I, E	P, SN, SM, ST, MF
25AA256	256K	32,768 x 8	1.8-5.5V	10	64	I	P, SN, SM, ST, MF
25LC512	512K	65,536 x 8	2.5-5.5V	20	128	I, E	P, SM, MF
25AA512	512K	65,536 x 8	1.8-5.5V	20	128	I	P, SM, MF
25LC1024	1024K	131,072 x 8	2.5-5.5V	20	256	I, E	P, SM, MF
25AA1024	1024K	131,072 x 8	1.8-5.5V	20	256	I	P, SM, MF

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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature under bias.....-40°C to +125°C

ESD protection on all pins.....4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: This is an overview of AC and DC Characteristics. Please refer to the device data sheet for production specs.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**	**Densities**
D001	VIH	High-level input voltage	.7 VCC	VCC + 1	V		All
D002	VIL	Low-level input voltage	-0.3	0.3 VCC	V	VCC ≥ 2.7V **(Note 1)**	All
D003	VIL		-0.3	0.2 VCC	V	VCC ≥ 2.7V **(Note 1)**	All
D004	VOL	Low-level output voltage	—	0.4	V	IOL = 2.1 mA, VCC = 4.5V	All
D005	VOL		—	0.2	V	IOL = 1.0 mA, VCC = 2.5V	All
D006	VOH	High-level output voltage	VCC -0.5	—	V	IOH = -400 µA	All
D007	ILI	Input leakage current	—	±1	µA	$\overline{CS}$ = VCC, VIN = VSS or VCC	All
D008	ILO	Output leakage current	—	±1	µA	$\overline{CS}$ = VCC, VOUT = VSS or VCC	All
D009	CINT	Internal capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, VCC = 5.0V **(NOTE 1)**	All
D010	ICC Read	Operating current	— 10 5		mA	VCC = 5.5V; FCLK = 20.0 MHz; Vcc = 2.5V; FCLK = 10.0 MHz	512K and 1M
			2.5 0.5	6 2.5	mA	VCC = 5.5V; FCLK = 10.0 MHz; Vcc = 2.5V; FCLK = 5.0 MHz	1K-256K
D011	ICC WRITE		— 7 5		mA	VCC = 5.5V Vcc = 2.5V	512K and 1M
			0.16 0.15	5 3	mA	VCC = 5.5V VCC = 2.5V	1K-256K
D012	ICCS	Standby current	—	20 12	µA	$\overline{CS}$ = VCC = 5.5V, 125°C $\overline{CS}$ = VCC = 5.5V, 85°C (Inputs tied to VCC or VSS)	512K and 1M
			—	5 1	µA	$\overline{CS}$ = VCC = 5.5V, 125°C $\overline{CS}$ = VCC = 5.5V, 85°C (Inputs tied to VCC or VSS)	1K-256K
D13	ICCSPD	Deep power-down current	—	1	µA	$\overline{CS}$ = VCC = 5.5V (Inputs tied to VCC or VSS)	512K and 1M

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): V_{CC} = +1.8V to 5.5V T_A = -40°C to +85°C Automotive (E): V_{CC} = +2.5V to 5.5V T_A = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
1	F_{CLK}	Clock frequency	— — —	20 10 2	MHz	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	512K and 1M
			— — —	10 5 3	MHz	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	1K-256K
2	T_{CSS}	$\overline{CS}$ setup time	25 50 250	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	512K and 1M
			50 100 150	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	1K-256K
3	T_{CSH}	$\overline{CS}$ hold time **(Note 3)**	50 100 150	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	512K and 1M
			100 200 250	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	1K-256K
4	T_{CSD}	$\overline{CS}$ disable time	50	—	ns		1K-256K
5	T_{SU}	Data setup time	5 10 50	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	512K and 1M
			10 20 30	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	1K-256K
6	T_{HD}	Data hold time	10 20 100	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	512K and 1M
			20 40 50	—	ns ns ns	$4.5 \le V_{CC} \le 5.5$ $2.5 \le V_{CC} < 4.5$ $1.8 \le V_{CC} < 2.5$	1K-256K
7	T_R	CLK rise time **(Note 1)**	—	20	ns		512K and 1M
			—	100	ns		128K and 256K
			—	500	ns		8K and 16K
			—	2000	ns		1K-4K, 32K-64K
8	T_F	CLK fall time **(Note 1)**	—	20	ns		512K and 1M
			—	100	ns		128K and 256K
			—	500	ns		8K and 16K
			—	2000	ns		1K-4K, 32K-64K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes T_{HI} time.

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TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
9	THI	Clock high time	25 50 250	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			50 100 150	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
10	TLO	Clock low time	25 50 250	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			50 100 150	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
11	TCLD	Clock delay time	50	—	ns		All
12	TCLE	Clock enable time	50	—	ns		All
13	TV	Output valid from clock low	—	25 50 250	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			—	50 100 160	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
14	THO	Output hold time **(Note 1)**	0	—	ns		
15	TDIS	Output disable time **(Note 1)**	—	25 50 250	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			—	40 80 160	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
16	THS	$\overline{\text{HOLD}}$ setup time	10 20 100	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			20 40 80	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
17	THH	$\overline{\text{HOLD}}$ Hold time	10 20 100	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			20 40 80	— —	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes THI time.

TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Electrical Characteristics: Industrial (I): VCC = +1.8V to 5.5V TA = -40°C to +85°C Automotive (E): VCC = +2.5V to 5.5V TA = -40°C to 125°C				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**	**Densities**
18	THZ	$\overline{\text{HOLD}}$ low to output High-Z **(Note 1)**	15 30 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			30 60 160	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
19	THV	$\overline{\text{HOLD}}$ high to output valid	15 30 150	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	512K and 1M
			30 60 160	—	ns ns ns	4.5 ≤ VCC ≤ 5.5 2.5 ≤ VCC < 4.5 1.8 ≤ VCC < 2.5	1K-256K
20	TREL	$\overline{\text{CS}}$ high to Standby mode	—	100	µs	1.8V ≤ VCC ≥ 5.5V	512K and 1M
21	TPD	$\overline{\text{CS}}$ high to Deep power-down	—	100	µs	1.8V ≤ VCC ≥ 5.5V	512K and 1M
22	TCE	Chip erase cycle time	—	15	ms	1.8V ≤ VCC ≥ 5.5V	512K and 1M
23	TSE	Sector erase cycle time	—	15	ms	1.8V ≤ VCC ≥ 5.5V	512K and 1M
24	TWC	Internal write cycle time	—	6	ms	Byte or Page mode and Page Erase	512K and 1M
			—	5	ms	Byte or Page mode	1K-256K
25	—	Endurance **(Note 2)**	> 1M	—	E/W Cycles	Per Page	512K and 1M
						Per Byte	1K-256K

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but established by characterization and qualification. For endurance estimates in a specific application, please consult the Total Endurance™ Model, which can be obtained from Microchip's web site: www.microchip.com.

3: Includes THI time.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
VLO = 0.2V	—
VHI = VCC - 0.2V	**(Note 1)**
VHI = 4.0V	**(Note 2)**
CL = 30 pF	—
Timing Measurement Reference Level	
Input Output	0.5 VCC 0.5 VCC

Note 1: For VCC ≤ 4.0V.

2: For VCC > 4.0V.

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FIGURE 1-1: HOLD TIMING

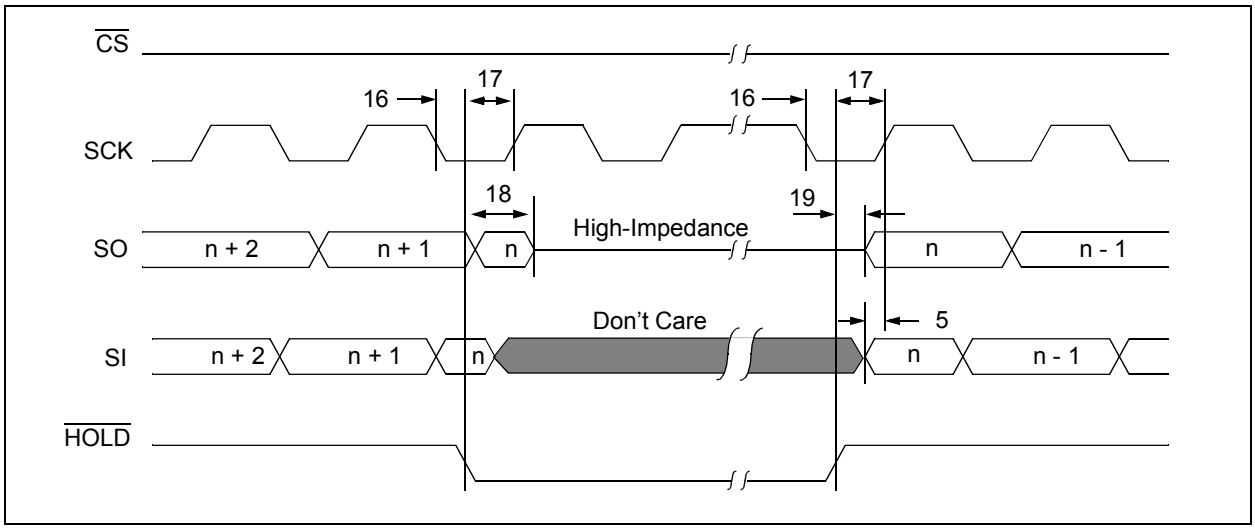


FIGURE 1-2: SERIAL INPUT TIMING

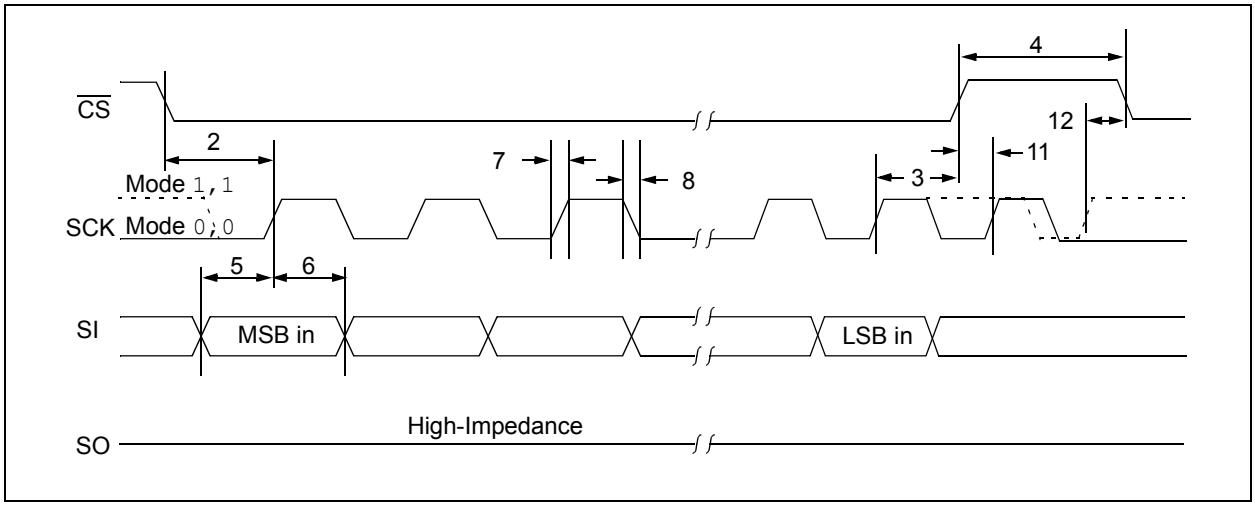
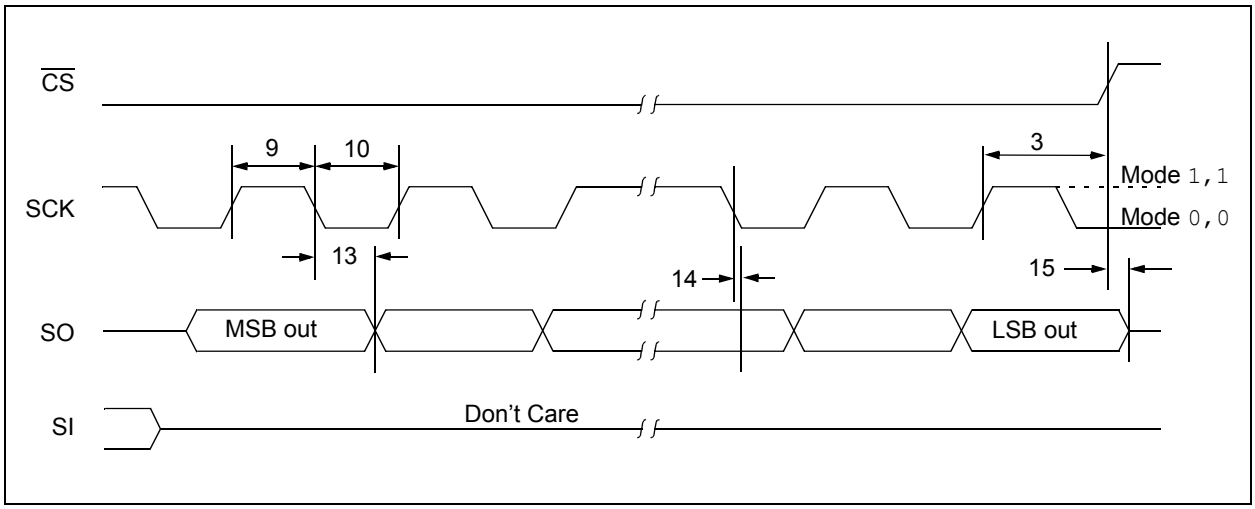


FIGURE 1-3: SERIAL OUTPUT TIMING



2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25-Series of Serial EEPROMs is designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC® microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in firmware to match the SPI protocol.

This family of EEPROMs contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{CS}$ pin must be low and the $\overline{HOLD}$ pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses and data are transferred MSB first, LSB last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{CS}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the $\overline{HOLD}$ input and place the EEPROM in 'HOLD' mode. After releasing the $\overline{HOLD}$ pin, operation will resume from the point when the $\overline{HOLD}$ was asserted.

Block Diagram

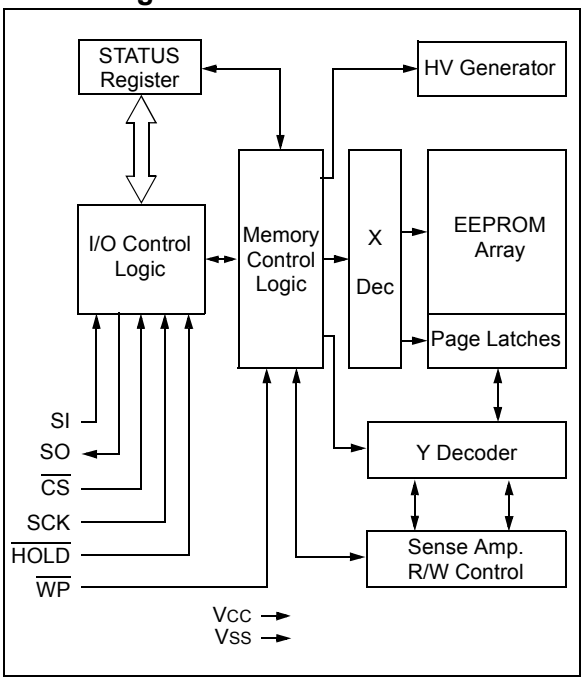


TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
Instructions for all devices.		
READ	0000 0011	Read data from memory array beginning at selected address
WRITE	0000 0010	Write data to memory array beginning at selected address
WREN	0000 0110	Set the write enable latch (enable write operations)
WRDI	0000 0100	Reset the write enable latch (disable write operations)
RDSR	0000 0101	Read STATUS register
WRSR	0000 0001	Write STATUS register
Additional Instructions for 25XX512 and 25XX1024		
PE	0100 0010	Page Erase – erase one page in memory array
SE	1101 1000	Sector Erase – erase one sector in memory array
CE	1100 0111	Chip Erase – erase all sectors in memory array
RDID	1010 1011	Release from Deep power-down and read electronic signature
DPD	1011 1001	Deep Power-Down mode

2.2 Read Sequence

The device is selected by pulling $\overline{CS}$ low. The 8-bit READ instruction is transmitted to the EEPROM followed by the address. After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. The data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses.

The internal Address Pointer is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached, the address counter rolls over to address 00000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{CS}$ pin. See Figure 2-1A/B/C for byte read.

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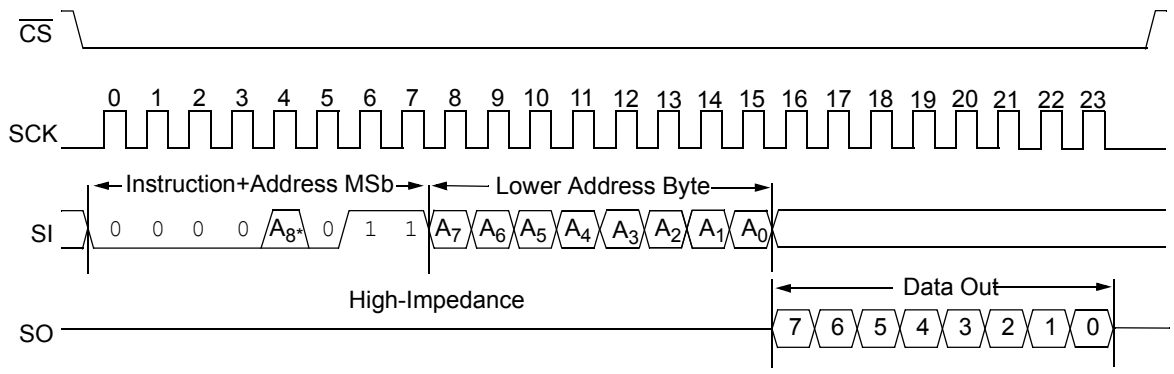
TABLE 2-2: READ/WRITE SEQUENCE ADDRESSING

Density	Address Bits	Highest Address	Page Size
1K	7	007F	16 Bytes
2K	8	00FF	16 Bytes
4K	9	01FF	16 Bytes
8K	10	03FF	16 or 32 Bytes*
16K	11	07FF	16 or 32 Bytes*
32K	12	0FFF	32 Bytes
64K	12	1FFF	32 Bytes
128K	14	3FFF	64 Bytes
256K	15	7FFF	64 Bytes
512K	16	FFFF	256 Bytes
1024K	17	1FFFF	256 Bytes

Note: Version A – 16 Bytes
Version B – 32 Bytes

FIGURE 2-1A: READ SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING



* A_8 is a don't care for 1K and 2K upper address bit.

FIGURE 2-1B: READ SEQUENCE WITH 16-BIT ADDRESSING

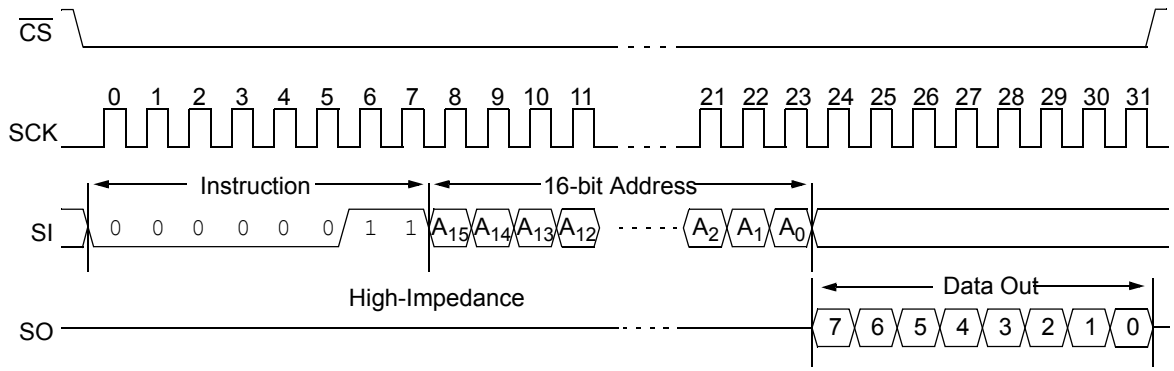
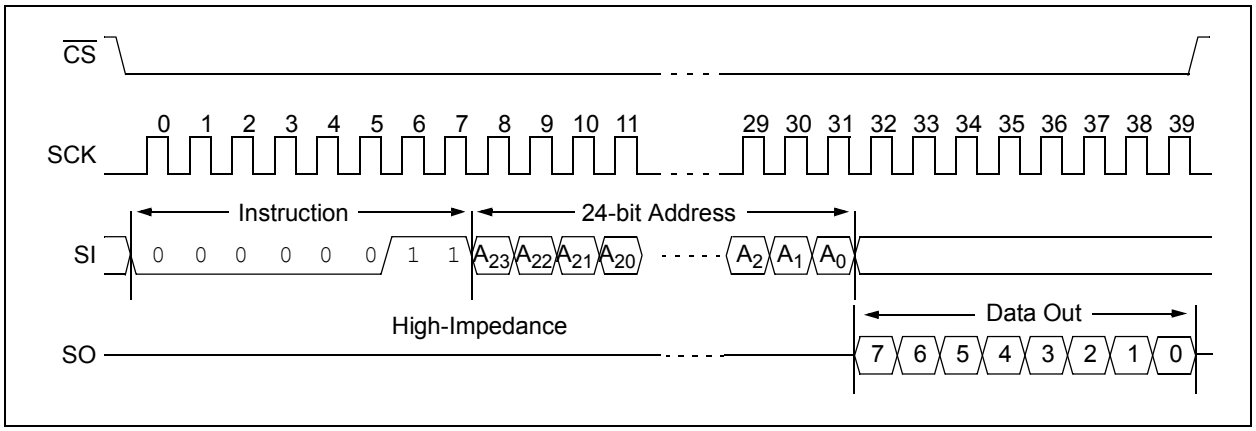


FIGURE 2-1C: READ SEQUENCE WITH 24-BIT ADDRESSING



2.3 Write Sequence

Prior to any attempt to write data to the EEPROM, the write enable latch must be set by issuing the `WREN` instruction (Figure 2-4). This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, $\overline{CS}$ must be brought high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set.

A write sequence includes an automatic, self timed erase cycle. It is not required to erase any portion of the memory prior to issuing a Write command.

Once the Write Enable Latch is set, the user may proceed by setting $\overline{CS}$ low, issuing a `WRITE` instruction, followed by the address and then the data to be written. Depending upon the density, a page of data that ranges from 16 bytes to 256 bytes can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. See Table 2-2 for information on page sizes.

In the 24XX512 and 24XX1024 devices, the entire page is always refreshed regardless of whether the entire page is written. For this reason, endurance for these devices is specified per page.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size'), and end at addresses that are integer multiples of page size – 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

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For the data to be actually written to the array, $\overline{CS}$ must be brought high after the Least Significant bit (D0) of the nth data byte has been clocked in. If $\overline{CS}$ is brought high at any other time, the write operation will not be completed. Refer to Figure 2-2A/B/C and Figure 2-3A/B/C/D for more detailed illustrations on the byte write sequence and the page write sequence, respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP and WEL bits (Figure 2-6). A read attempt of a memory array location will not be possible during a write cycle. When the write cycle is completed, the write enable latch is reset.

FIGURE 2-2A: BYTE WRITE SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING

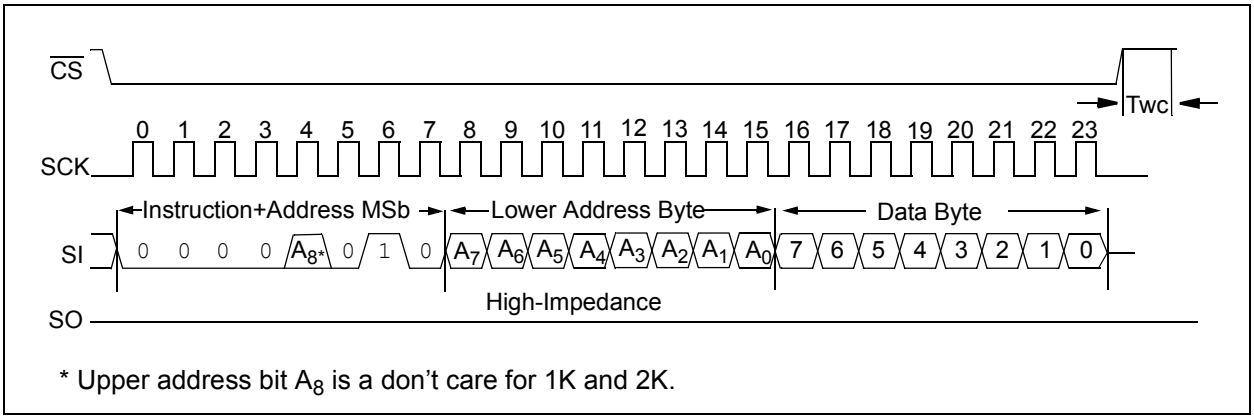


FIGURE 2-2B: BYTE WRITE SEQUENCE WITH 16-BIT ADDRESSING

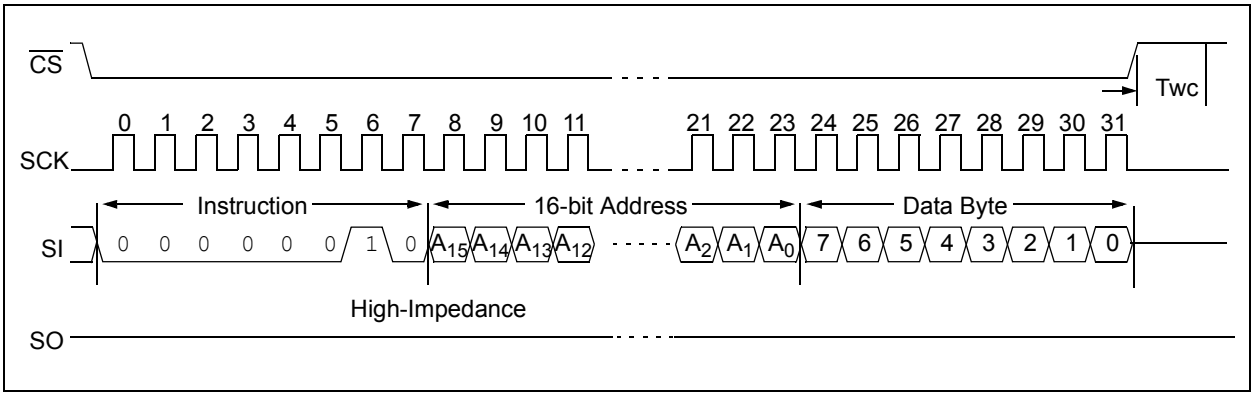


FIGURE 2-2C: BYTE WRITE SEQUENCE WITH 24-BIT ADDRESSING

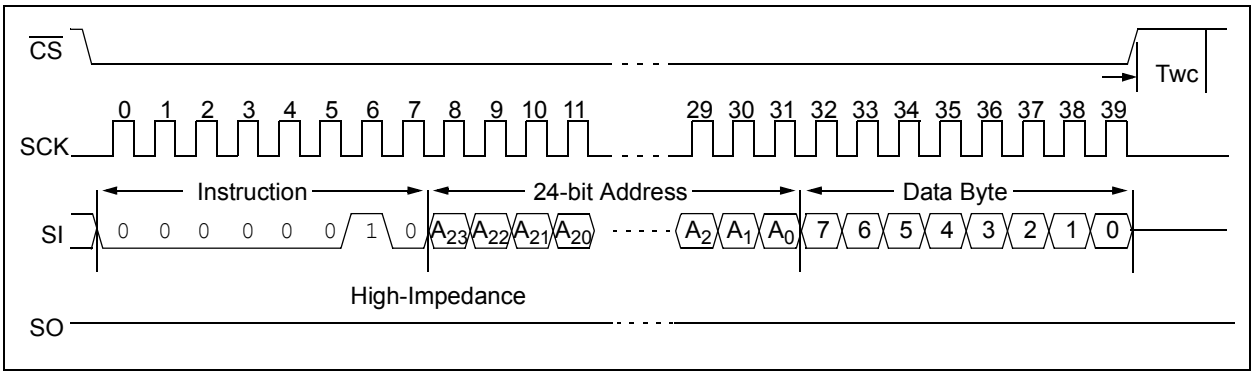
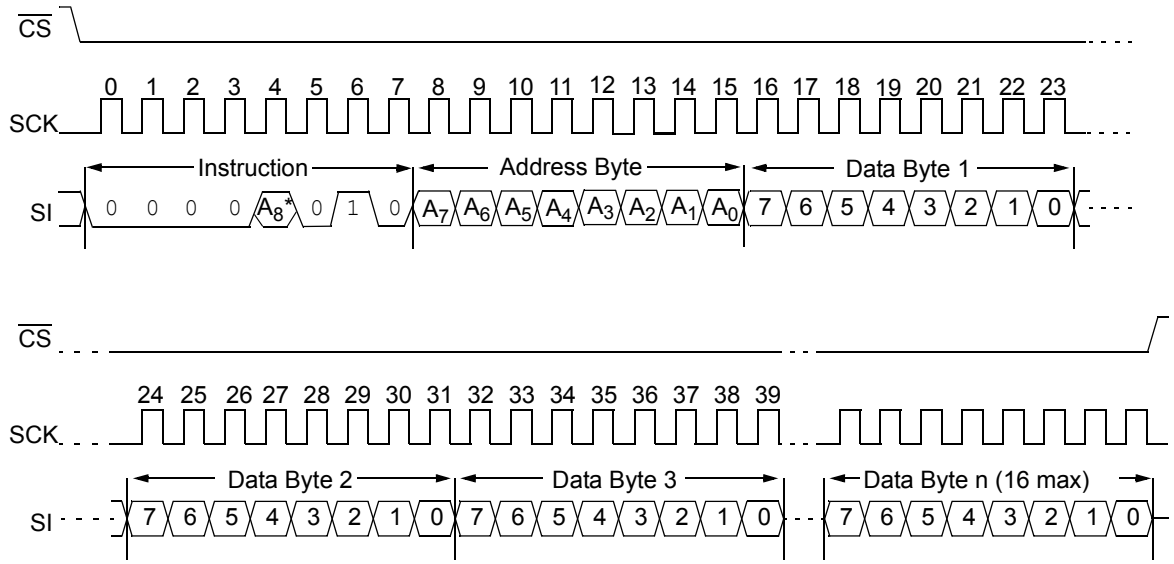


FIGURE 2-3A: PAGE WRITE SEQUENCE WITH EITHER 8-BIT OR 9-BIT ADDRESSING



* Upper address bit A_8 is a don't care for 1K and 2K.

FIGURE 2-3B: PAGE WRITE SEQUENCE WITH 16-BIT ADDRESSING

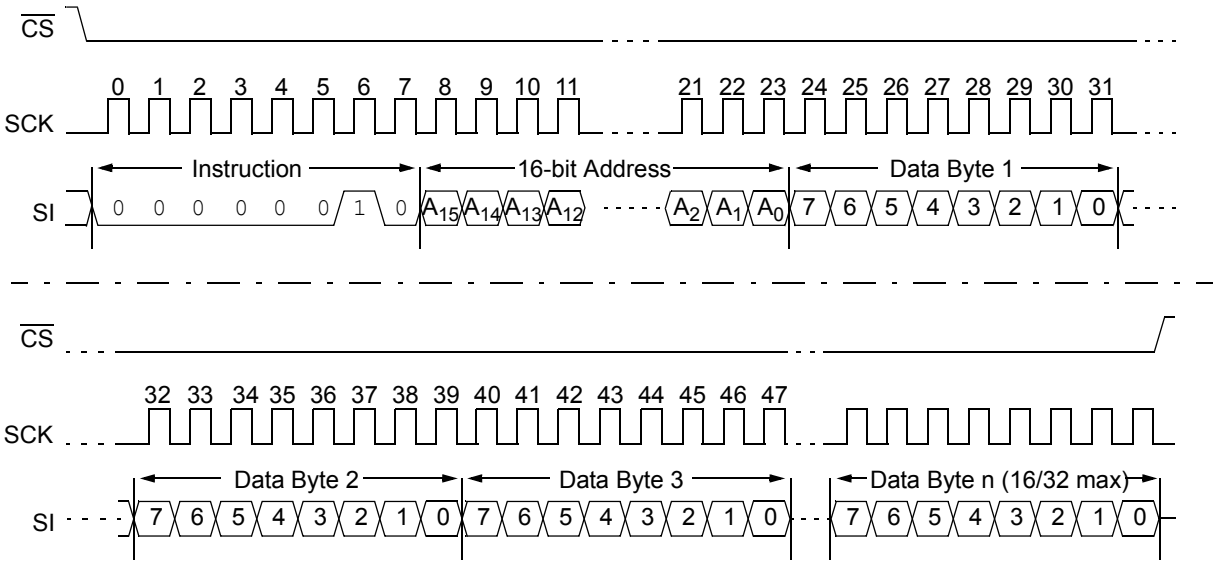


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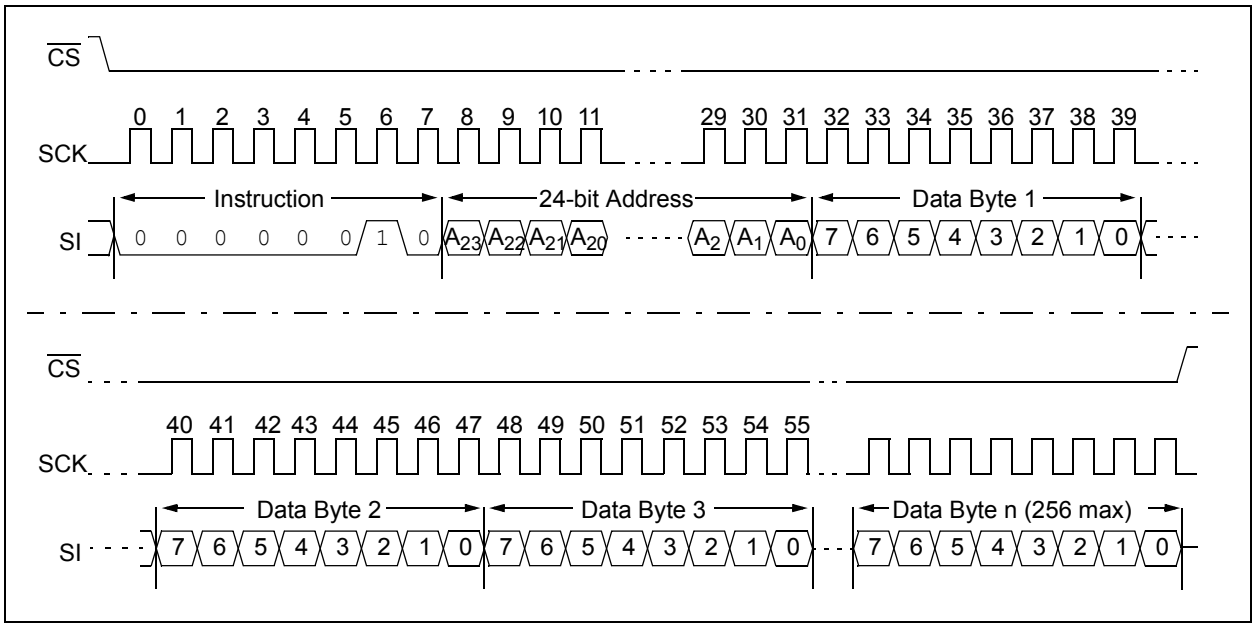
FIGURE 2-3C: PAGE WRITE SEQUENCE WITH 24-BIT ADDRESSING



2.4 Write Enable (WREN) and Write Disable (WRDI)

The EEPROM contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- $\overline{WP}$ pin is brought low (1K, 2K, 4K only)

Additional instructions available on 25XX512 and 25XX1024:

- PE instruction successfully executed
- SE instruction successfully executed
- CE instruction successfully executed

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)

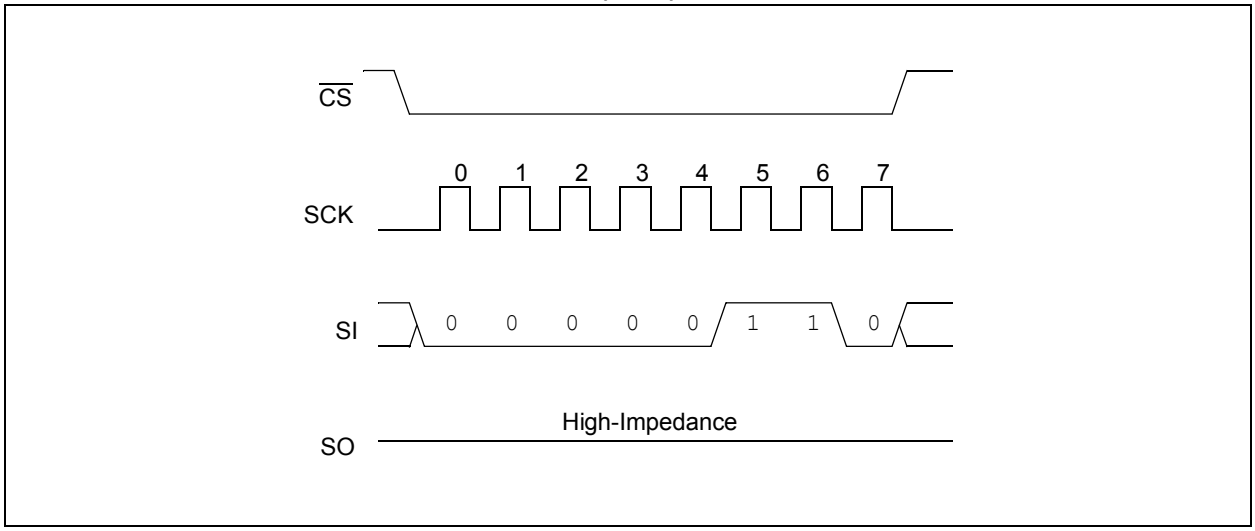
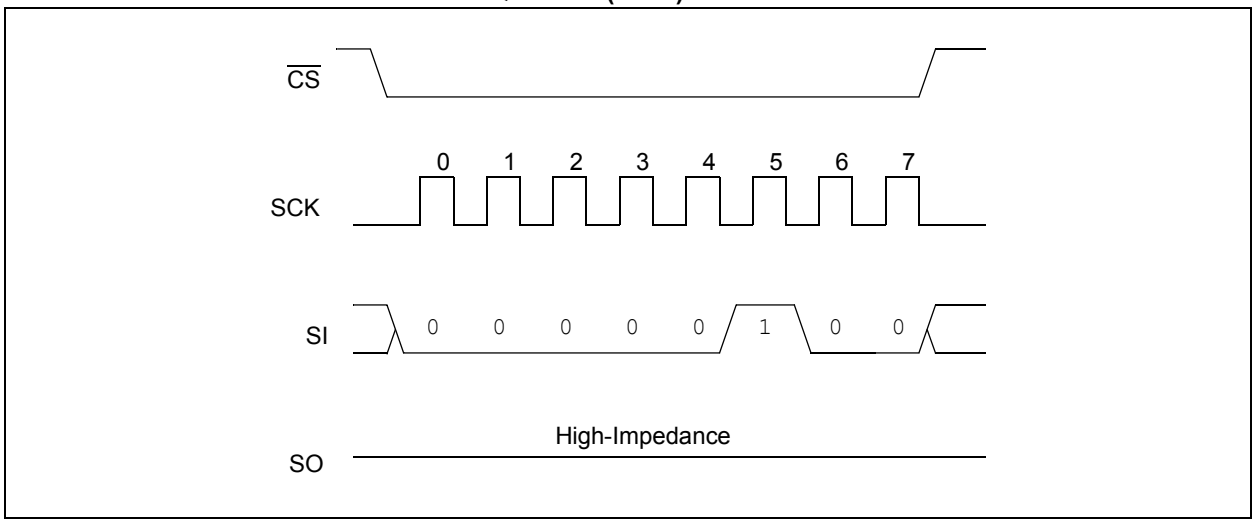


FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-3: STATUS REGISTER

7	6	5	4	3	2	1	0
W/R	—	—	—	W/R	W/R	R	R
WPEN	X	X	X	BP1	BP0	WEL	WIP
W/R = writable/readable. R = read-only.							

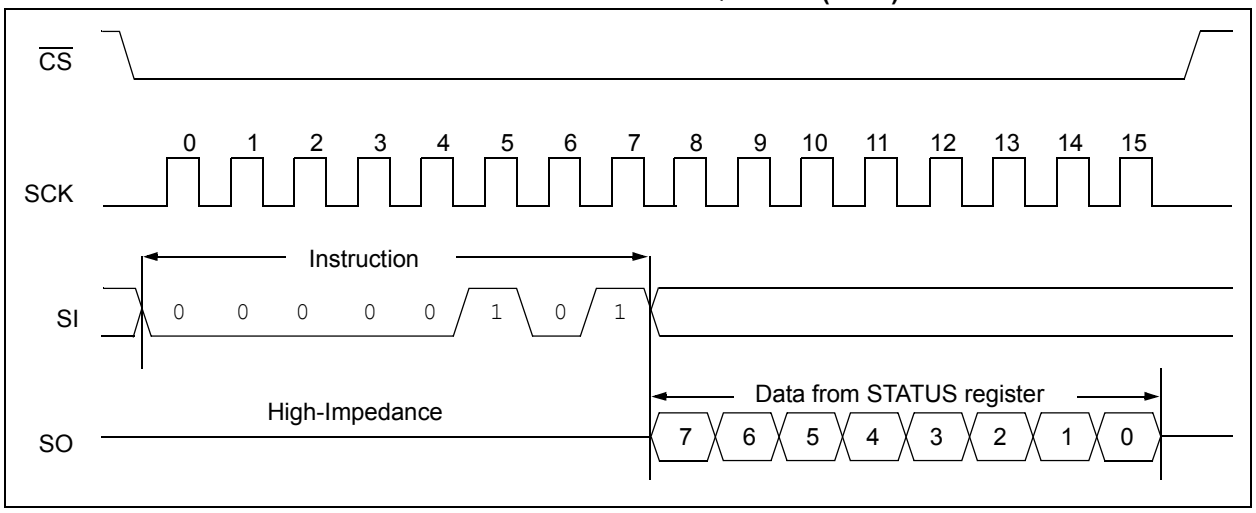
Note: WPEN bit not available in 24XX010A, 24XX020A and 24XX040A devices.

The Write-In-Process (WIP) bit indicates whether the EEPROM is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The Write Enable Latch (WEL) bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The Block Protection (BP0 and BP1) bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction. These bits are nonvolatile and are shown in Table 2-4. See Figure 2-6 for the RDSR timing sequence.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



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2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-3. The user is able to select one of four levels of protection for the array by writing to the appropriate bits in the STATUS register. The array is divided up into four segments. The user has the ability to write-protect none, one, two, or all four of the segments of the array. The partitioning is controlled as is shown in Table 2-4.

In EEPROM densities starting at 8 Kbits and higher, the Write-Protect Enable (WPEN) bit is a nonvolatile bit that is available as an enable bit for the $\overline{WP}$ pin. The Write-Protect ($\overline{WP}$) pin and the Write-Protect Enable (WPEN) bit in the STATUS register control the programmable hardware write-protect feature. Hardware write protection is enabled when $\overline{WP}$ pin is low and the WPEN bit is high. Hardware write protection is disabled when either the $\overline{WP}$ pin is high or the WPEN bit is low. When the chip is hardware write-protected, only writes to nonvolatile bits in the STATUS register are disabled. See Table 2-6 for a matrix of functionality on the WPEN bit. See Figure 2-7 for the WRSR timing sequence.

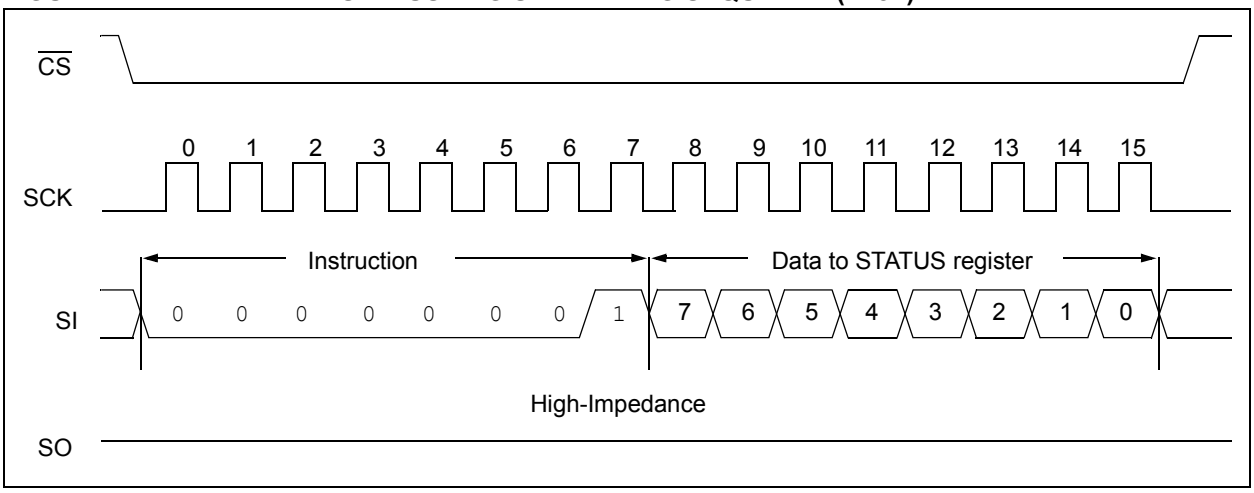
TABLE 2-4: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected	Array Addresses Unprotected
0	0	none	All (Sectors 0, 1, 2 and 3)
0	1	Upper 1/4 (Sector 3)	Lower 3/4 (Sectors 0, 1 and 2)
1	0	Upper 1/2 (Sectors 2 and 3)	Lower 1/2 (Sectors 0 and 1)
1	1	All (Sectors 0, 1, 2 and 3)	none

TABLE 2-5: ARRAY PROTECTED ADDRESS LOCATIONS

Density	Upper 1/4 (Sector 3)	Upper 1/2 (Sectors 2 and 3)	All Sectors
1K	60h-7Fh	40h-7Fh	00h-7Fh
2K	C0h-FFh	80h-FFh	00h-FFh
4K	180h-1FFh	100h-1FFh	000h-1FFh
8K	300h-3FFh	200h-3FFh	000h-3FFh
16K	600h-7FFh	400h-7FFh	000h-7FFh
32K	C00h-FFFh	800h-FFFh	000h-FFFh
64K	1800h-1FFFh	1000h-1FFFh	0000h-1FFFh
128K	3000h-3FFFh	2000h-3FFFh	0000h-3FFFh
256K	6000h-7FFFh	4000h-7FFFh	0000h-7FFFh
512K	C000h-FFFFh	8000h-FFFFh	0000h-FFFFh
1024K	18000h-1FFFFh	10000h-1FFFFh	00000h-1FFFFh

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- $\overline{CS}$ must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The Serial EEPROM powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS}$ = 1)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on $\overline{CS}$ is required to enter active State

TABLE 2-6: WRITE-PROTECT FUNCTIONALITY MATRIX

WEL (SR bit 1)	WPEN (SR bit 7) *	$\overline{WP}$ (pin 3)	Protected Blocks	Unprotected Blocks	STATUS Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Writable	Writable
1	1	0 (low)	Protected	Writable	Protected
1	1	1 (high)	Protected	Writable	Writable

X = Don't Care
* = WPEN bit is not available on 24XX010A/020A/040A.

2.9 Page Erase

The Page Erase is a typical Flash function that has been implemented only on the 512 Kbit and 1024 Kbit Serial EEPROMs. This function is used to erase all bits (FFh) inside a given page. A Write Enable (WREN) instruction must be given prior to attempting a Page Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Page Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-8A/B) and two or three address bytes. Any address inside the page to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Page Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Page Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Page Erase cycle is complete.

If a Page Erase function is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

FIGURE 2-8A: PAGE ERASE SEQUENCE WITH 24-BIT ADDRESSING

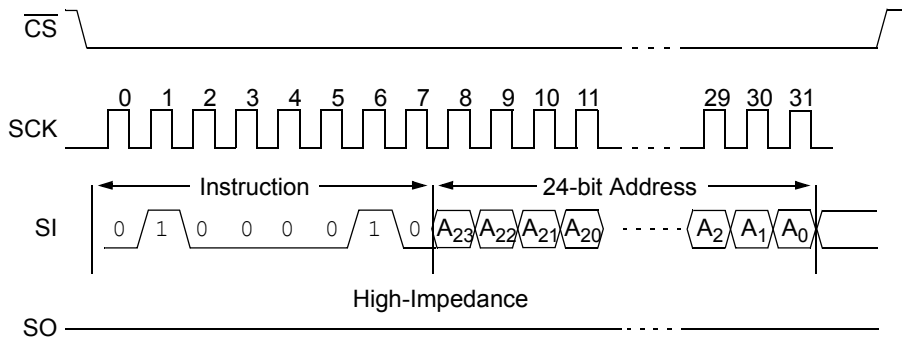


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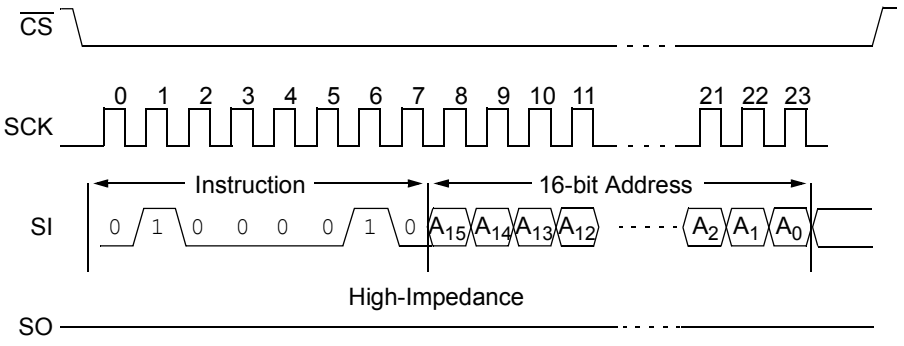
FIGURE 2-8B: PAGE ERASE SEQUENCE WITH 16-BIT ADDRESSING



2.10 Sector Erase

The Sector Erase is a typical Flash function that has been implemented only on the 512 Kbit and 1024 Kbit Serial EEPROMs. This function is used to erase all bits (FFh) inside a given sector. A Write Enable (WREN) instruction must be given prior to attempting a Sector Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch.

The Sector Erase function is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-9A/B), and two or three address bytes. Any address inside the sector to be erased is a valid address.

$\overline{CS}$ must then be driven high after the last bit if the address or the Sector Erase will not execute. Once the $\overline{CS}$ is driven high, the self-timed Sector Erase cycle is started. The WIP bit in the STATUS register can be read to determine when the Sector Erase cycle is complete.

If a `SECTOR ERASE` instruction is given to an address that has been protected by the Block Protect bits (BP0, BP1) then the sequence will be aborted and no erase will occur.

See Table 2-2 and Table 2-3 for Sector Addressing.

FIGURE 2-9A: SECTOR ERASE SEQUENCE WITH 24-BIT ADDRESSING

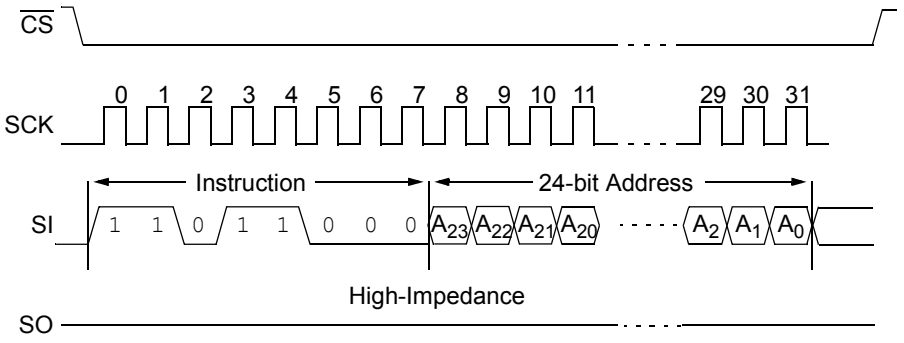
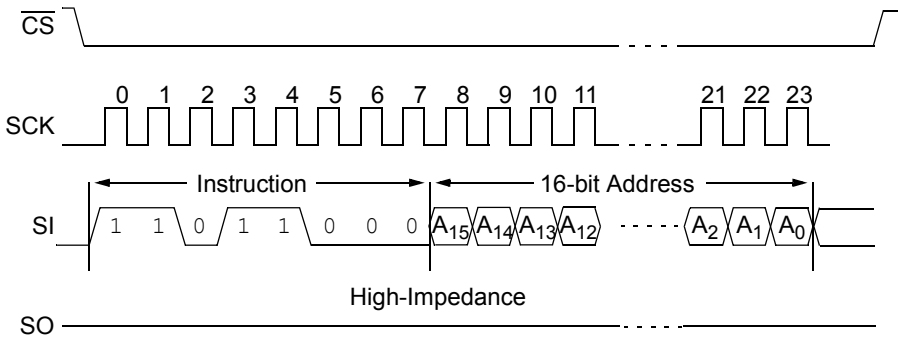


FIGURE 2-9B: SECTOR ERASE SEQUENCE WITH 16-BIT ADDRESSING

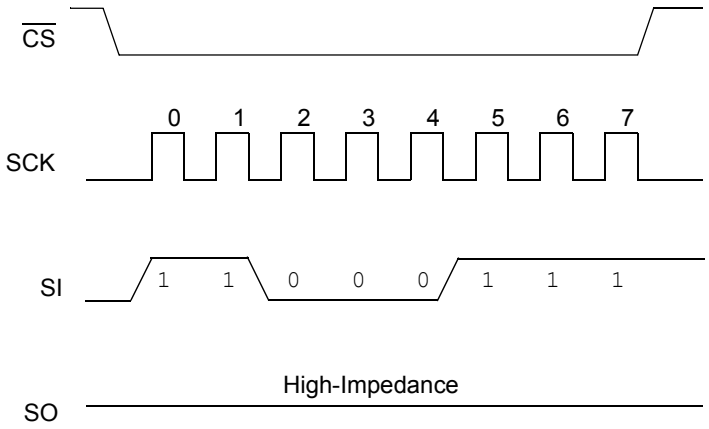


2.11 Chip Erase

The Chip Erase function will erase all bits (FFh) in the array. A Write Enable (WREN) instruction must be given prior to executing a Chip Erase. This is done by setting $\overline{CS}$ low and then clocking out the proper instruction into the EEPROM. After all eight bits of the instruction are transmitted, the $\overline{CS}$ must be brought high to set the write enable latch. The Chip Erase function is entered by driving the $\overline{CS}$ low, followed by the instruction code (Figure 2-10) onto the SI line.

The $\overline{CS}$ pin must be driven high after the eighth bit of the instruction code has been given or the Chip Erase function will not be executed. Once the $\overline{CS}$ pin is driven high, the self-timed Chip Erase function begins. While the device is executing the Chip Erase function the WIP bit in the STATUS register can be read to determine when the Chip Erase function is complete. The Chip Erase function is ignored if either of the Block Protect bits (BP0, BP1) are not '0', meaning ¼, ½, or all of the array is protected.

FIGURE 2-10: CHIP ERASE SEQUENCE



2.12 Deep Power-Down Mode

Deep Power-Down mode is available on the high-density 25XX512 and 25XX1024 Serial EEPROMs and is the lowest power consumption state for these devices. While in the Deep Power-Down mode, these devices will not respond to any of the Read or Write commands, and therefore it can be used as an additional software write protection feature.

The Deep Power-Down mode is entered by driving $\overline{CS}$ low, followed by the instruction code (Figure 2-11) onto the SI line, followed by driving $\overline{CS}$ high.

If the $\overline{CS}$ pin is not driven high after the eighth bit of the instruction code has been given, the device will not execute Deep power-down. Once the $\overline{CS}$ line is driven high, there is a delay (T_{DP}) before the current settles to its lowest consumption.

All instructions given during Deep Power-Down mode are ignored except the Read Electronic Signature Command (RDID). The RDID command will release the device from Deep power-down and outputs the electronic signature on the SO pin, and then returns the device to Standby mode after delay (T_{REL}).

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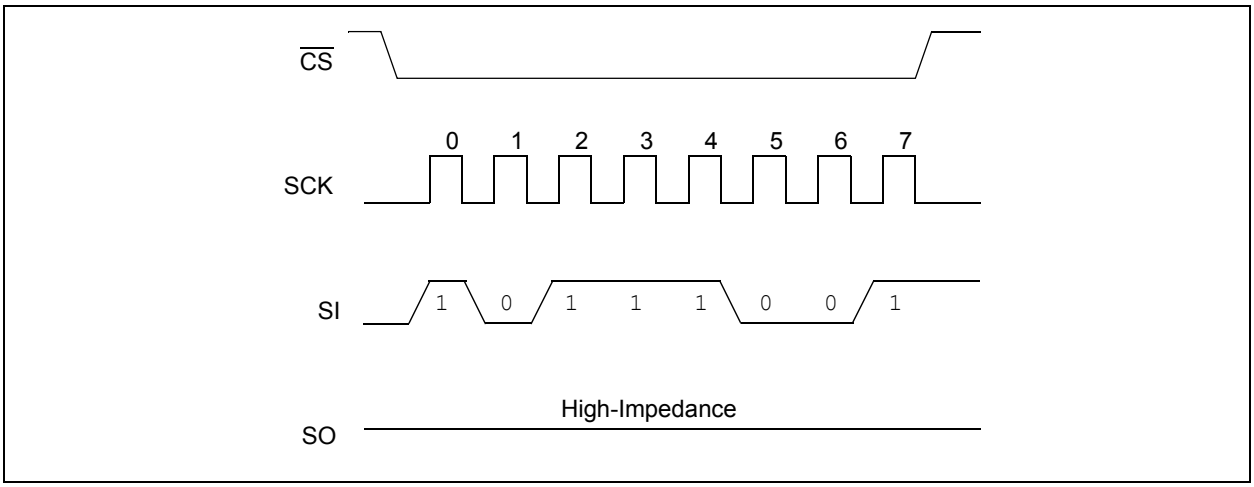
Deep Power-Down mode automatically releases at device power-down. Once power is restored to the device, it will power-up in the Standby mode.

FIGURE 2-11: DEEP POWER-DOWN SEQUENCE



2.13 Release from Deep Power-Down and Read Electronic Signature

Once a device has entered Deep Power-Down mode all instructions are ignored except the Release from Deep Power-down and Read Electronic Signature command. This command can also be used when the device is not in Deep Power-down, to read the electronic signature out on the SO pin unless another command is being executed such as Erase, Program or Write STATUS register.

Release from Deep Power-Down mode and Read Electronic Signature is entered by driving $\overline{CS}$ low, followed by the RDID instruction code (Figure 2-12A/B).Then a dummy address of 24 bits (A23-A0) for the 25XX1024 and 16 bits (A15-A0) for the 25XX512 can be sent. After the last bit of the dummy address is clocked in, the 8-bit Electronic signature is clocked out on the SO pin. After the signature has been read out at least once, the sequence can be terminated by driving $\overline{CS}$ high. The device will then return to Standby mode and will wait to be selected so it can be given new instructions. If additional clock cycles are sent after the electronic signature has been read once, it will continue to output the signature on the SO line until the sequence is terminated.

FIGURE 2-12A: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE (24-BITS)

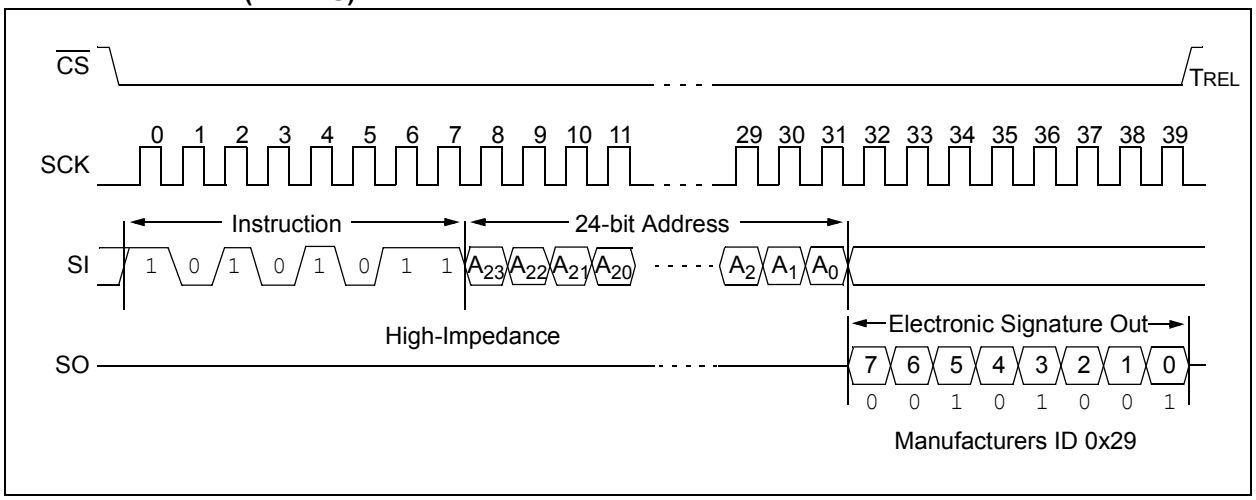
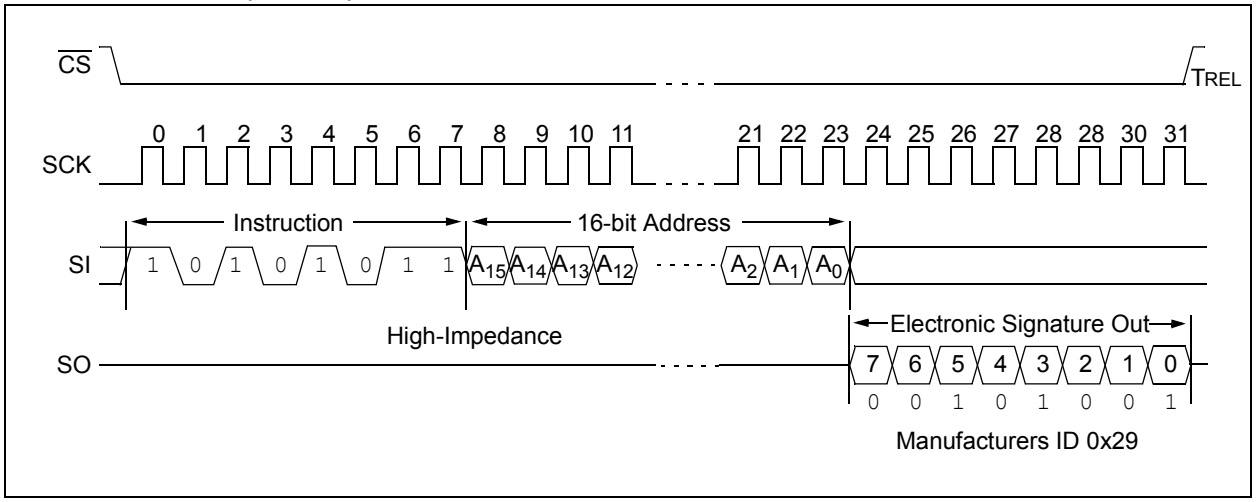


FIGURE 2-12B: RELEASE FROM DEEP POWER-DOWN AND READ ELECTRONIC SIGNATURE (16-BITS)



Driving $\overline{CS}$ high after the 8-bit RDID command, but before the Electronic Signature has been transmitted, will still ensure the device will be taken out of Deep Power-Down mode. However, there is a delay T_{REL} that occurs before the device returns to Standby mode (ICCS), as shown in Figure 2-13.

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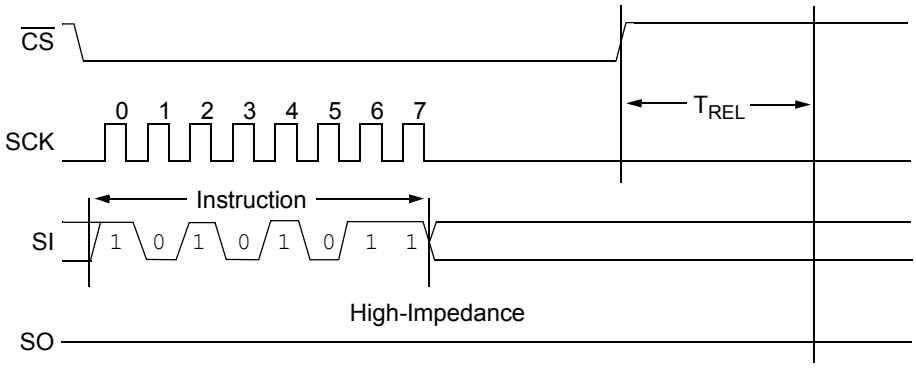
FIGURE 2-13: RELEASE FROM DEEP POWER-DOWN



3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Name	Pin Number	Function
$\overline{CS}$	1	Chip Select Input
SO	2	Serial Data Output
$\overline{WP}$	3	Write-Protect Pin
VSS	4	Ground
SI	5	Serial Data Input
SCK	6	Serial Clock Input
$\overline{HOLD}$	7	Hold Input
VCC	8	Supply voltage

3.1 Chip Select ($\overline{CS}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{CS}$ input signal. If $\overline{CS}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{CS}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{CS}$ is required prior to any sequence being initiated.

3.2 Serial Output (SO)

The SO pin is used to transfer data out of the EEPROM. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

3.3 Write-Protect ($\overline{WP}$)

The $\overline{WP}$ pin is a hardware write-protect input pin. In the lower densities of 4 Kbits and below, a logic low on this pin will reset the write enable latch and programming will be inhibited. However, if a write cycle is already in progress, $\overline{WP}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

In densities of 8 Kbits and higher the $\overline{WP}$ pin is used in conjunction with the WPEN bit in the STATUS register to prohibit writes to the nonvolatile bits in the STATUS register. When $\overline{WP}$ is low and WPEN is high, writing to the nonvolatile bits in the STATUS register are disabled. All other operations will function normally. When $\overline{WP}$ is set to a logic high, all functions, including writes to the nonvolatile bits in the STATUS register will operate normally. If the WPEN bit is set, a logic low on the $\overline{WP}$ pin during a STATUS register write sequence will disable writing to the STATUS register. If an internal write cycle has already begun, $\overline{WP}$ going low will have no effect on the write in progress.

The $\overline{WP}$ pin function is blocked when the WPEN bit in the STATUS register is low. This allows the user to install the EEPROM in a system with $\overline{WP}$ pin grounded and still be able to write to the STATUS register. The $\overline{WP}$ pin functions will be enabled when the WPEN bit is set to a logic high.

3.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock

3.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the EEPROM. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

3.6 Hold ($\overline{HOLD}$)

The $\overline{HOLD}$ pin is used to suspend transmission to the EEPROM while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{HOLD}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{HOLD}$ pin must be brought low while SCK is low, otherwise the $\overline{HOLD}$ function will not be invoked until the next SCK high-to-low transition. The EEPROM must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{HOLD}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Pulling the $\overline{HOLD}$ line low at any time will tri-state the SO line.

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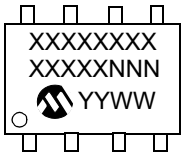
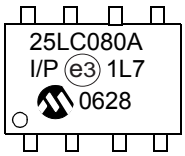
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

8-Lead PDIP



Example: Pb-Free



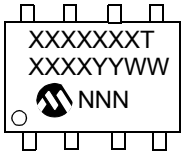
8-Lead PDIP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	25AA010A	25LC010A	25LC010A
25AA020A	25AA020A	25LC020A	25LC020A
25AA040A	25AA040A	25LC040A	25LC040A
25AA080A	25AA080A	25LC080A	25LC080A
25AA080B	25AA080B	25LC080B	25LC080B
25AA160A	25AA160A	25LC160A	25LC160A
25AA160B	25AA160B	25LC160B	25LC160B
25AA320A	25AA320A	25LC320A	25LC320A
25AA640A	25AA640A	25LC640A	25LC640A
25AA128	25AA128	25LC128	25LC128
25AA256	25AA256	25LC256	25LC256
25AA512	25AA512	25LC512	25LC512
25AA1024	25AA1024	25LC1024	25LC1024
Note: T = Temperature Grade (I, E).			

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

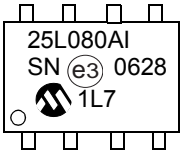
Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead SOIC



Example: Pb-Free



8-Lead SOIC Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	25AA01AT	25LC010A	25LC01AT
25AA020A	25AA02AT	25LC020A	25LC02AT
25AA040A	25AA04AT	25LC040A	25LC04AT
25AA080A	25A080AT	25LC080A	25L080AT
25AA080B	25A080BT	25LC080B	25L080BT
25AA160A	25A160AT	25LC160A	25L160AT
25AA160B	25A160BT	25LC160B	25L160BT
25AA320A	25AA32AT	25LC320A	25LC32AT
25AA640A	25AA64AT	25LC640A	25LC64AT
25AA128(2)	25AA128T	25LC128	25LC128T
25AA256(2)	25AA256T	25LC256	25LC256T
25AA512(2)	25AA512T	25LC512	25LC512T
25AA1024(3)	25AA1024	25LC1024	25LC1024

Note 1: T = Temperature Grade (I, E).
2: Density available in SN and SM versions.
3: Density only available in SM.

Legend:		
	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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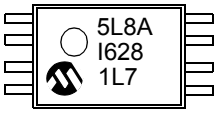
8-Lead TSSOP

Example: Pb-Free



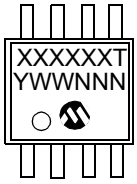
8-Lead TSSOP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	5A1A	25LC010A	5L1A
25AA020A	5A2A	25LC020A	5L2A
25AA040A	5A4A	25LC040A	5L4A
25AA080A	5A8A	25LC080A	5L8A
25AA080B	5A8B	25LC080B	5L8B
25AA160A	5AAA	25LC160A	5LAA
25AA160B	5AAB	25LC160B	5LAB
25AA320A	5ABA	25LC320A	5LBA
25AA640A	5ACA	25LC640A	5LCA
25AA128	5AD	25LC128	5LD
25AA256	5AE	25LC256	5LE
Note: T = Temperature Grade (I, E).			

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

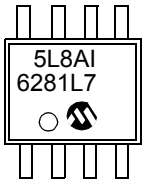
Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead MSOP



Example: Pb-Free



8-Lead MSOP Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA010A	5A1AT	25LC010A	5L1AT
25AA020A	5A2AT	25LC020A	5L2AT
25AA040A	5A4AT	25LC040A	5L4AT
25AA080A	5A8AT	25LC080A	5L8AT
25AA080B	5A8BT	25LC080B	5L8BT
25AA160A	5AAAT	25LC160A	5LAAT
25AA160B	5AABT	25LC160B	5LABT
25AA320A	5ABAT	25LC320A	5LBAT
25AA640A	5ACAT	25LC640A	5LCAT
Note: T = Temperature Grade (I, E).			

Legend:

XX...X	Part number or part number code
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code (2 characters for small packages)
e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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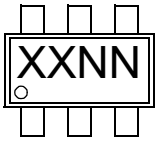
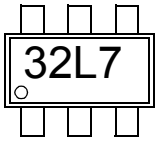
6-Lead SOT-23



Example: Pb-Free



6-Lead SOT-23 Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
25AA010A	12NN	25LC010A	15NN	16NN
25AA020A	22NN	25LC020A	25NN	26NN
25AA040A	32NN	25LC040A	35NN	36NN

Legend:

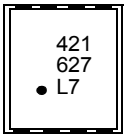
XX...X	Part number or part number code
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week ‘01’)
NNN	Alphanumeric traceability code (2 characters for small packages)
(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead 2x3 DFN

Example: Pb-Free



8-Lead 2x3 DFN Package Marking (Pb-Free)				
Device	**I-Temp Marking**	**Device**	**I-Temp Marking**	**E-Temp Marking**
25AA010A	401	25LC010A	404	405
25AA020A	411	25LC020A	414	415
25AA040A	421	25LC040A	424	425
Note: NN = Alphanumeric Traceability Code.				

Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator (e3), the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

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8-Lead 6x5 DFN-S

Example: Pb-Free

8-Lead 6x5 DFN-S Package Marking (Pb-Free)			
Device	**Line 1 Marking**	**Device**	**Line 1 Marking**
25AA128	25AA128	25LC128	25LC128
25AA256	25AA256	25LC256	25LC256
25AA512	25AA512	25LC512	25LC512
25AA1024	25AA1024	25LC1024	25LC1024
Note: T = Temperature Grade (I, E)			

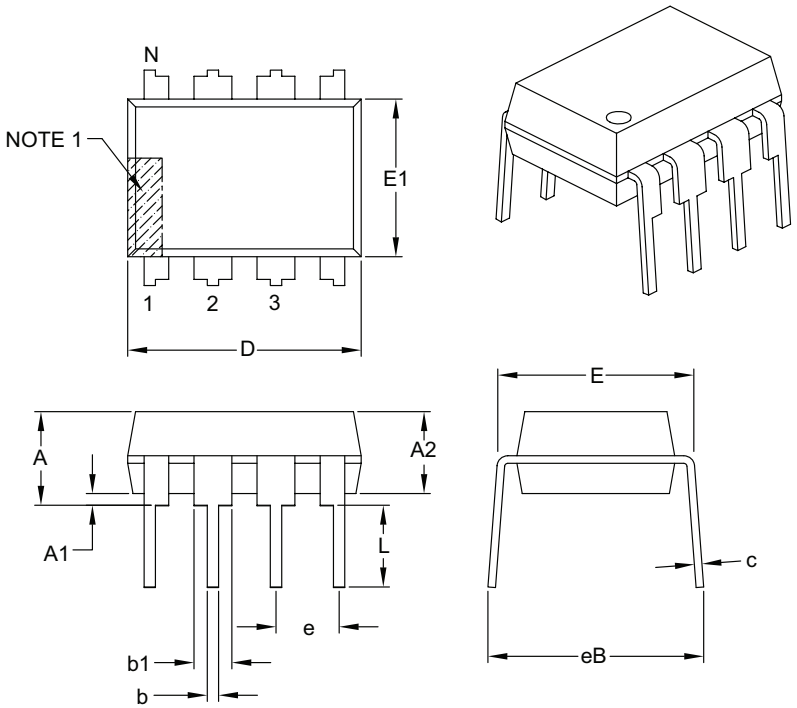
Legend:	XX...X	Part number or part number code
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code (2 characters for small packages)
	e3	Pb-free JEDEC designator for Matte Tin (Sn) plated devices

Note: For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located with the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-018B

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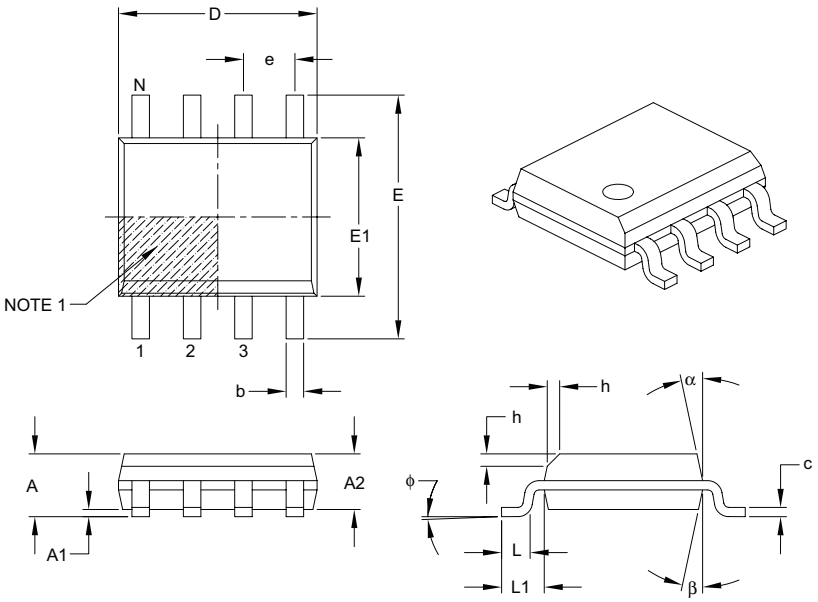
8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	φ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

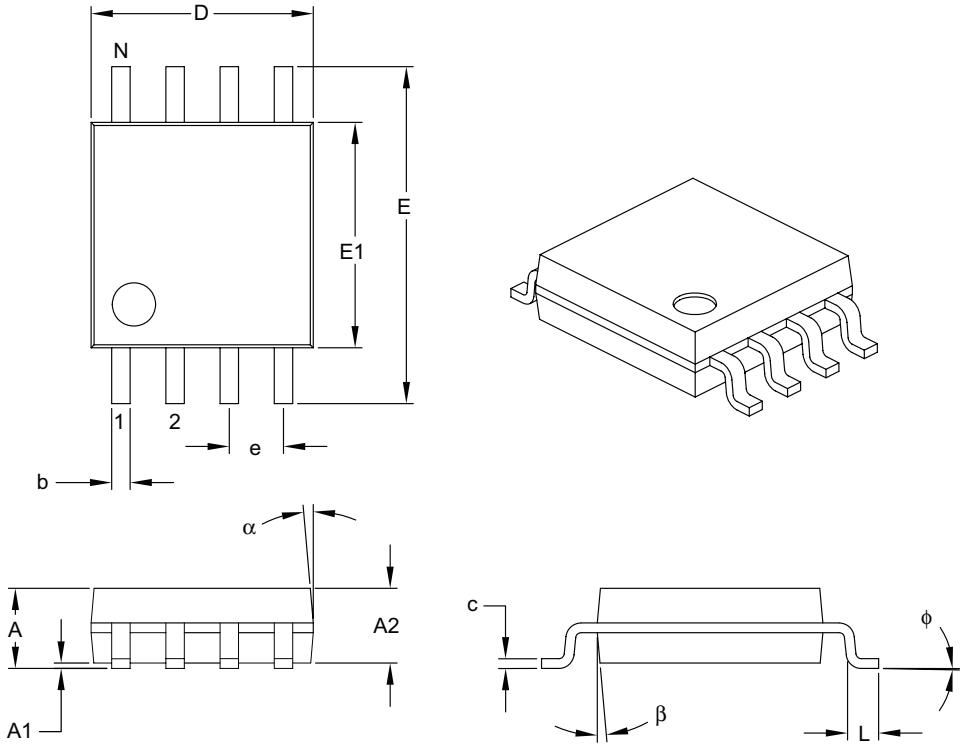
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SM) – Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	1.77	–	2.03
Molded Package Thickness	A2	1.75	–	1.98
Standoff §	A1	0.05	–	0.25
Overall Width	E	7.62	–	8.26
Molded Package Width	E1	5.11	–	5.38
Overall Length	D	5.13	–	5.33
Foot Length	L	0.51	–	0.76
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.15	–	0.25
Lead Width	b	0.36	–	0.51
Mold Draft Angle Top	α	–	–	15°
Mold Draft Angle Bottom	β	–	–	15°

Notes:

1. SOIJ, JEITA/EIAJ Standard, formerly called SOIC.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

Microchip Technology Drawing C04-056B

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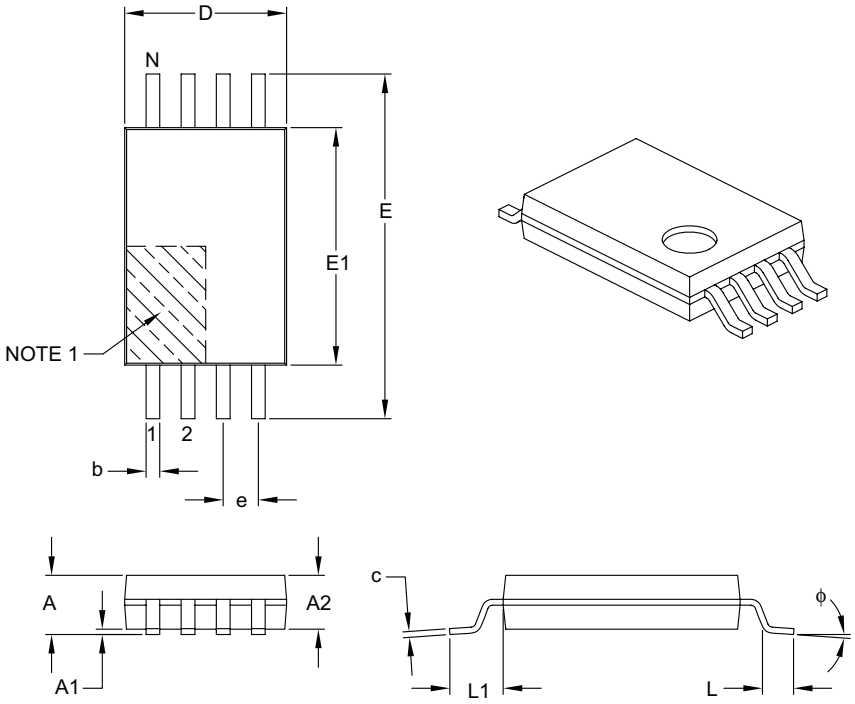
8-Lead Plastic Thin Shrink Small Outline (ST) – 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	–	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	2.90	3.00	3.10
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.19	–	0.30

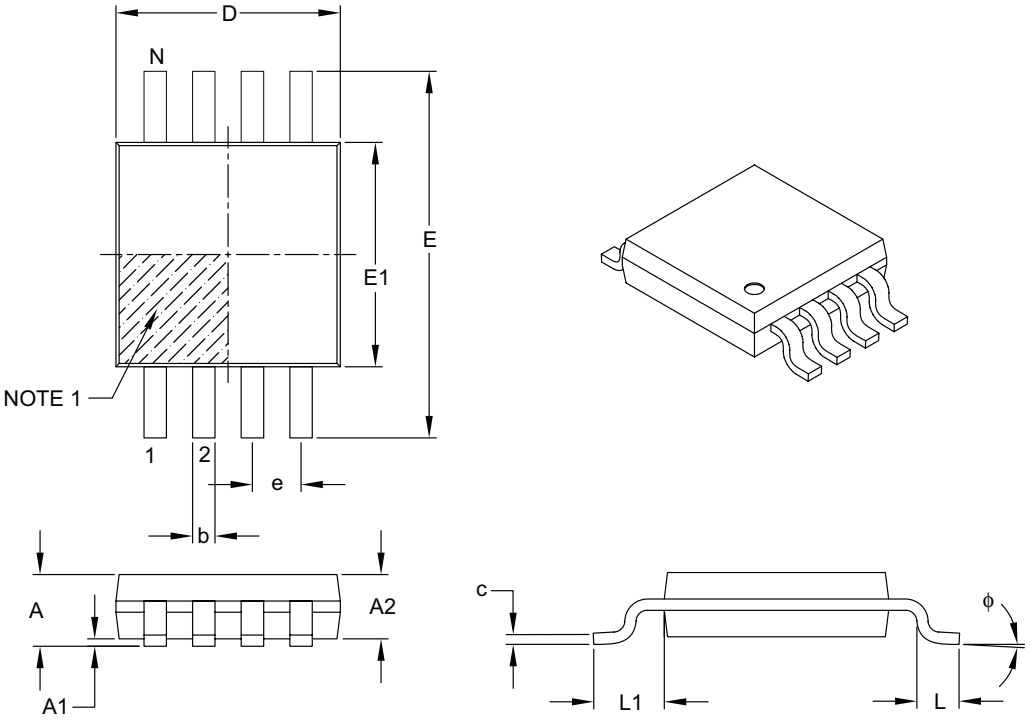
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-086B

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	–	0.15
Overall Width	E	4.90 BSC		
Molded Package Width	E1	3.00 BSC		
Overall Length	D	3.00 BSC		
Foot Length	L	0.40	0.60	0.80
Footprint	L1	0.95 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.08	–	0.23
Lead Width	b	0.22	–	0.40

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111B

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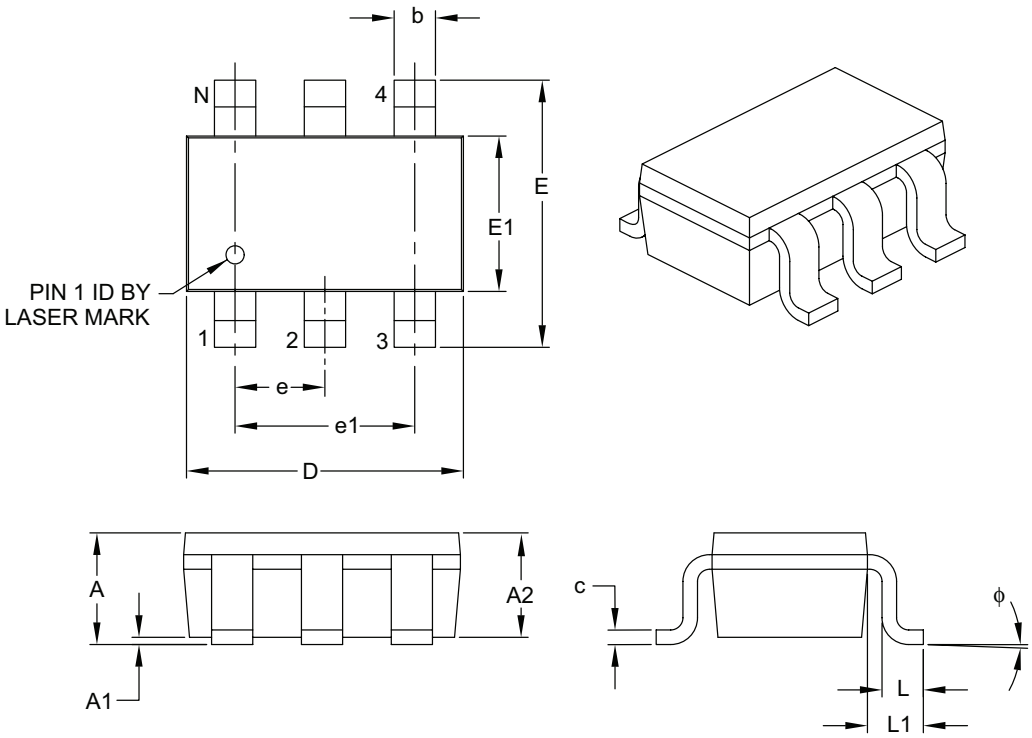
6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

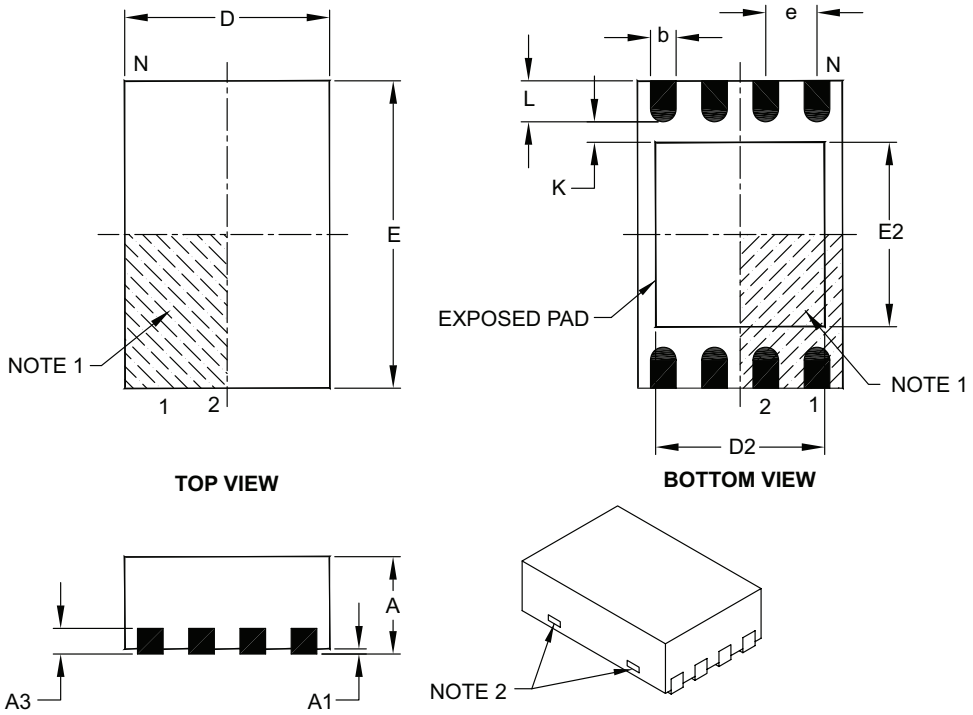
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

8-Lead Plastic Dual Flat, No Lead Package (MC) – 2x3x0.9 mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	2.00 BSC		
Overall Width	E	3.00 BSC		
Exposed Pad Length	D2	1.30	–	1.75
Exposed Pad Width	E2	1.50	–	1.90
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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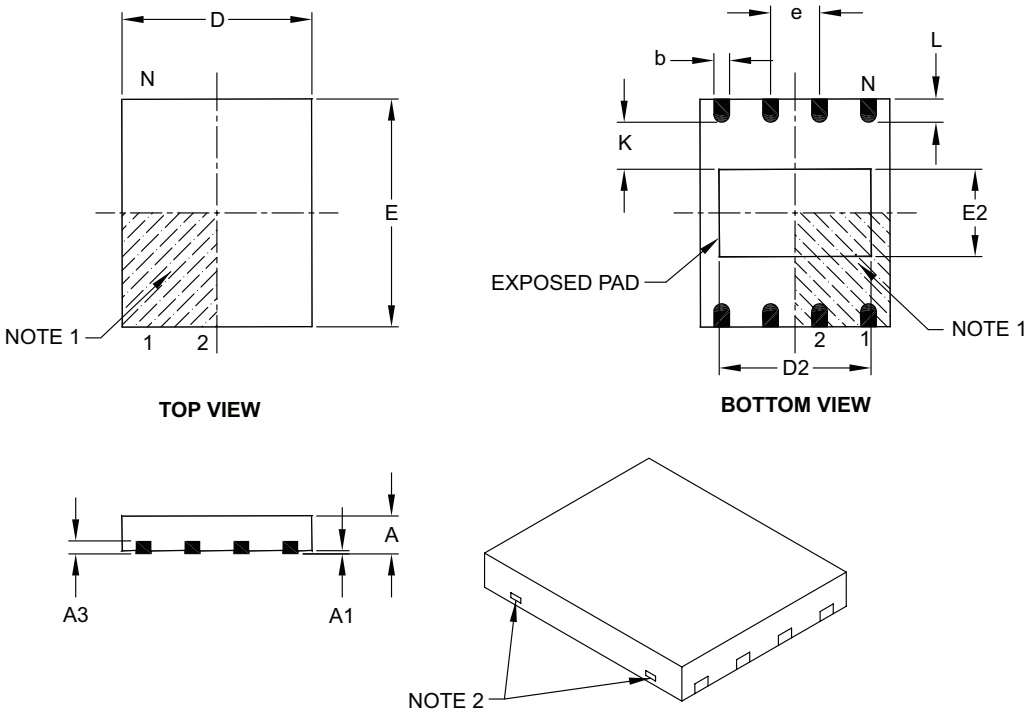
8-Lead Plastic Dual Flat, No Lead Package (MF) – 6x5 mm Body [DFN-S]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	0.80	0.85	1.00
Standoff	A1	0.00	0.01	0.05
Contact Thickness	A3	0.20 REF		
Overall Length	D	5.00 BSC		
Overall Width	E	6.00 BSC		
Exposed Pad Length	D2	3.90	4.00	4.10
Exposed Pad Width	E2	2.20	2.30	2.40
Contact Width	b	0.35	0.40	0.48
Contact Length	L	0.50	0.60	0.75
Contact-to-Exposed Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package may have one or more exposed tie bars at ends.
3. Package is saw singulated.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-122B

APPENDIX A: REVISION HISTORY

Revision A (05/2007)

Original release of document.
(Package Drawings Rev. AP)

Revision B (06/2007)

- Updated the 6-Lead SOT-23 packaging information
- Updated the Product Identification System information
- Minor corrections throughout document

Revision C (08/2007)

Removed “Preliminary” status for 512, 640A and 1024 devices.

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Device: 25AAXXXX/25LCXXXX Literature Number: DS22040C

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_____

_____

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_____

_____

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5. What deletions from the document could be made without affecting the overall usefulness?

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6. Is there any incorrect or misleading information (what and where)?

_____

_____

7. How would you improve this document?

_____

_____

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	X	/XX
Device Part Number	Packaging Medium	Temperature Range	Package

Device: EEPROM Series – 25
Voltage – AA = 1.8V-5.5V
LC = 2.5V-5.5V

Density:
010A = 1 Kbit
020A = 2 Kbit
040A = 4 Kbit
080A = 8 Kbit
080B = 8 Kbit
160A = 16 Kbit
160B = 16 Kbit
320A = 32 Kbit
640A = 64 Kbit
128 = 128 Kbit
256 = 256 Kbit
512 = 512 Kbit
1024 = 1024 Kbit (1Mbit)

Temperature Range:
I = -40°C to +85°C
E = -40°C to +125°C

Packaging Medium:
T = Tape and Reel (T/R)
Blank = Std. Pkg.

Package:
P = 8-lead Plastic DIP (300 mil body)
SN = 8-lead Plastic SOIC (3.90 mm body)
SM = 8-lead Plastic SOIC (5.28 mm body)
ST = 8-lead Plastic TSSOP (4.4 mm)
MS = 8-lead Plastic MSOP (3.0 mm)
MC = 8-lead 2x3 mm DFN (T/R only)
MF = 8-lead 6x5 mm DFN
OT = 6-lead SOT-23 (T/R only)

Examples:

a) 25AA010A-I/SN: 1K
b) 25AA040A-I/MS: 4K
c) 25LC040AT-I/OT: 4K
d) 25LC1024-I/SM: 1M
e) 25LC040AT-I/MC

NOTES:

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