



SINGLE AND DUAL LOW CAPACITANCE ESD / TRANSIENT PROTECTOR FOR 1.5 V SYSTEMS

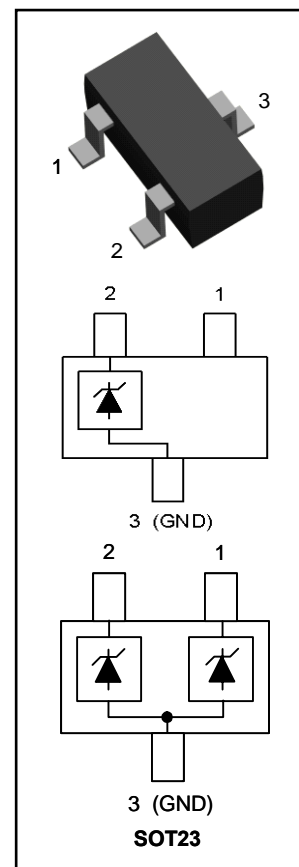
This patented Single and Dual Zener like ESD/Transient Protector has been designed to protect Sensitive Equipment against ESD and prevent Latch-Up events, offering a minimum insertion loss in High speed Data Lines in Communications ports used in Portable Consumer, Computing and Networking Applications operating at 1.5V and below.

SPECIFICATION FEATURES

- Maximum Capacitance of 10pF @ 0Vdc, 1 MHz
- Maximum Leakage Current of 2μA @ 1.5V
- Breakdown Voltage of 1.9V @ 1mA
- IEC61000-4-2 Compliance 15kV Air, 8kV Contact Discharge
- Industry Standard SOT23 Package

APPLICATIONS

- High Speed Data Transmission Lines
- Microcontroller and Microprocessor I/O Interfaces
- Portable Consumer Electronics
- Instrumentation Equipment
- LAN/WAN Equipment



MAXIMUM RATINGS

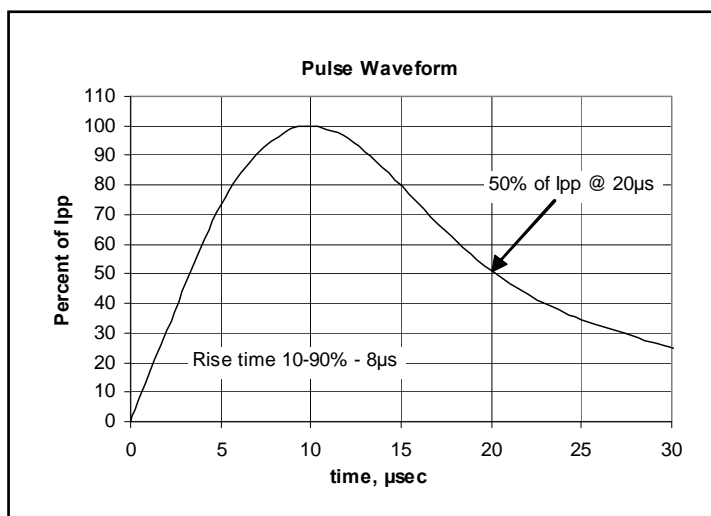
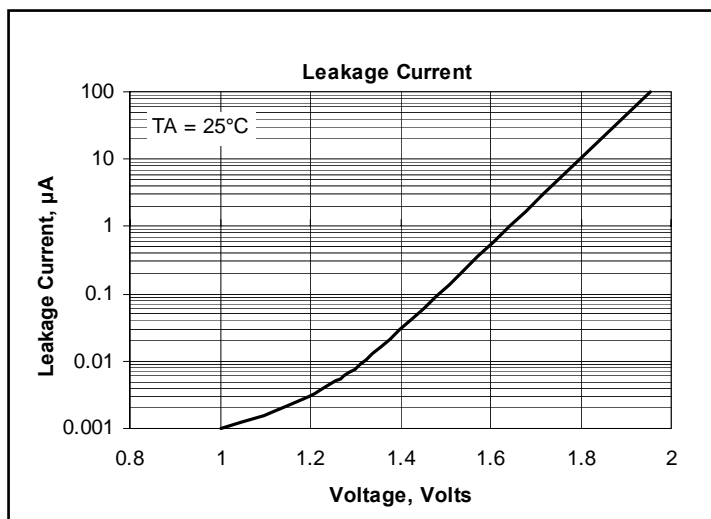
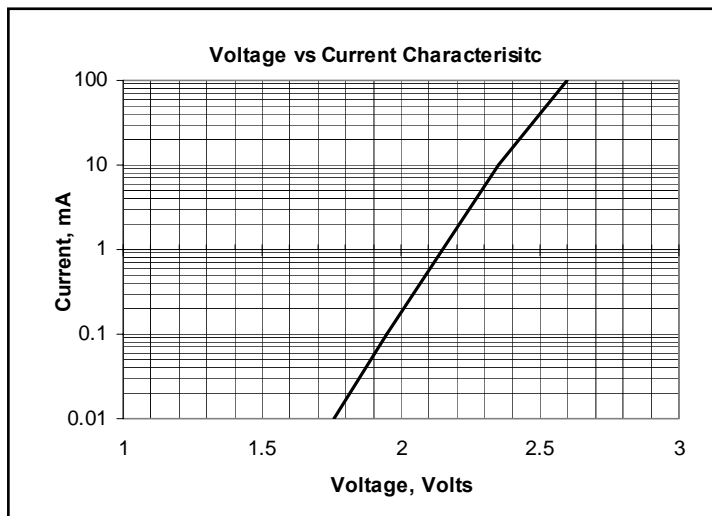
Rating	Symbol	Value	Units
Peak Pulse Power (8/20μs Waveform)	P_{pp}	50	W
ESD Voltage (HBM)	V_{ESD}	>25	kV
Operating Temperature Range	T_J	-55 to +125	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Lead Soldering Temperature (max 10 s)	T_L	260	°C

ELECTRICAL CHARACTERISTICS $T_j = 25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typical	Max	Units
Reverse Stand-Off Voltage	V_{WRM}				1.5	V
Reverse Breakdown Voltage	V_{BR}	$I_{BR} = 100\mu\text{A}$	1.75	1.8		V
		$I_{BR} = 1\text{mA}$	1.9	2.2		V
Reverse Leakage Current	I_R	$V_R = 1.5\text{V}$			2.0	μA
Clamping Voltage (8/20μs)	V_c	$I_{pp} = 1\text{A}$			4	V
Clamping Voltage (8/20μs)	V_c	$I_{pp} = 3\text{A}$			7	V
Maximum Peak Pulse Current	I_{pp}	8/20 μs Waveform			5	A
Off State Junction Capacitance	C_j	0 Vdc Bias f = 1MHz Between I/O pins and pin 3		6	10	pF

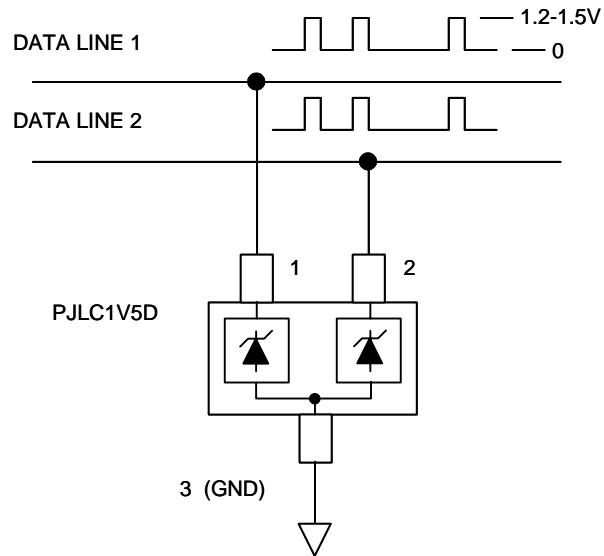


TYPICAL CHARACTERISTICS $T_j = 25^\circ\text{C}$

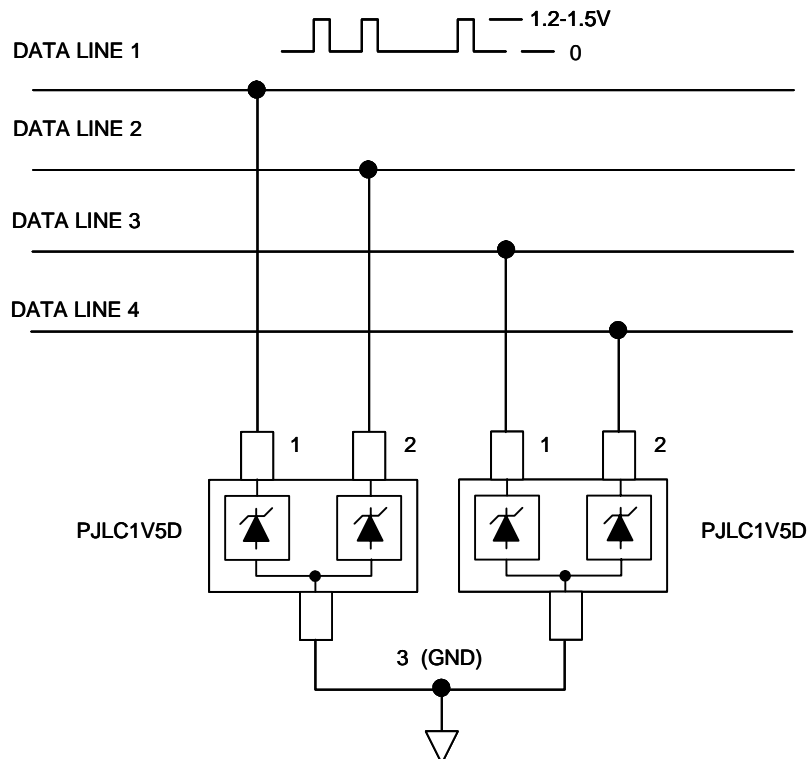


TYPICAL APPLICATION INFORMATION

ESD Protection for two Data Lines

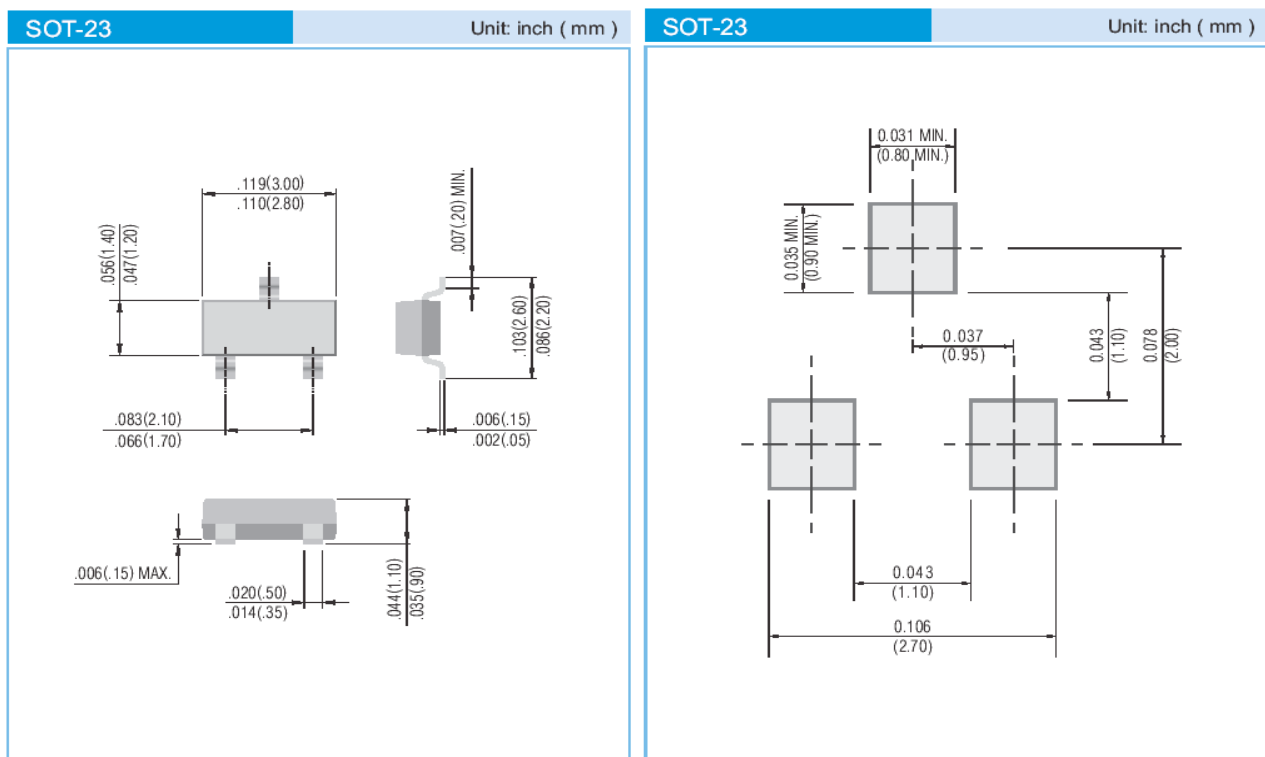


ESD Protection for Four Data Lines





PACKAGE AND PAD LAYOUT DIMENSIONS



Device	Marking Code
PJLC1V5	T1L
PJLC1V5D	T2L

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