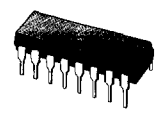
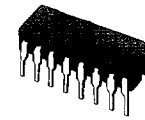
M54/74HCT160/161
M54/74HCT162/163

SYNCHRONOUS PRESETTABLE 4-BIT COUNTER

- HIGH SPEED
  f_{MAX} = 50 MHz (TYP.) AT V_{CC} = 5 V
- LOW POWER DISSIPATION
  I_{CC} = 4 µA (MAX.) AT 25 °C
- OUTPUT DRIVE CAPABILITY
  10 LSTTL LOADS
- BALANCED PROPAGATION DELAYS
  $t_{PLH} \approx t_{PHL}$
- SYMMETRICAL OUTPUT IMPEDANCE
  $I_{OH} = I_{OL}$ = 4 mA (MIN.)
- COMPATIBLE WITH TTL OUTPUTS
  V_{IH} = 2V (MIN.); V_{IL} = 0.8V (MAX.)
- PIN AND FUNCTION COMPATIBLE
  WITH 54/74LS160 ~ 163



B1R
(Plastic Package)



F1R
(Ceramic Package)

M1R
(Micro Package)

C1R
(Chip Carrier)

ORDER CODES :

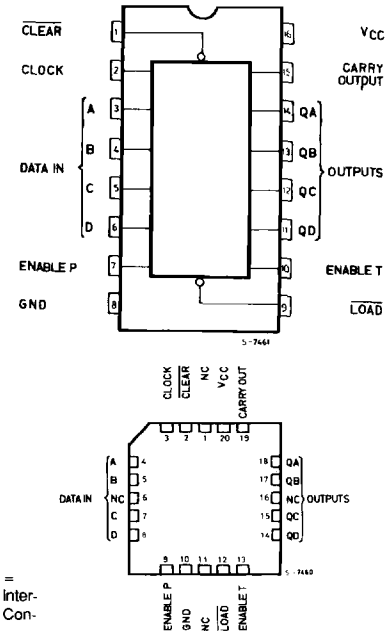
M54HCTXXXF1R M74HCTXXXM1R
M74HCTXXXB1R M74HCTXXXC1R

DESCRIPTION

M54/74HCT160 Decade, Asynchronous Clear
M54/74HCT161 Binary, Asynchronous Clear
M54/74HCT162 Decade, Synchronous Clear
M54/74HCT163 Binary, Synchronous Clear

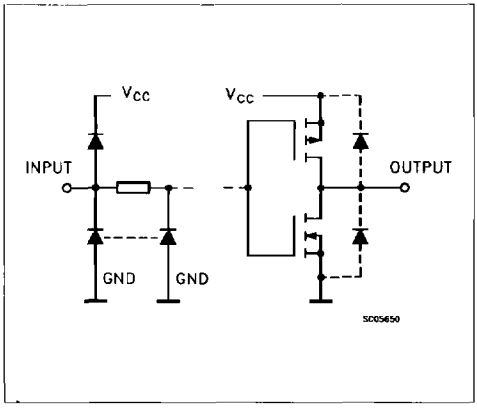
The M54/74HCT160, 161, 162 and 163 are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERS fabricated with silicon gate C^2MOS technology. They have the same high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
The M54/74HCT160/162 are BCD Decade counters and the M54/74HCT161/163 are 4 bit binary counters. The CLOCK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLEAR}$ inputs are active Low.
Presetting of all four IC's is synchronous on the rising edge of the CLOCK. The function on the M54/74HCT162/163 is synchronous to CLOCK, while the M54/74HCT160/161 counters are cleared asynchronously. Two enable inputs (TE and PE) and CARRY output are provided to enable easy cascading of counters, which facilities easy implementation of N-bit counters without using external gates. This integrated circuit has input and output characteristics that are fully compatible with 54/74 LSTTL logic families. M54/74HCT devices are designed to directly interface HSC^2MOS systems with TTL and NMOS components. They are also plug in replacements for LSTTL devices giving a reduction of power consumption. All inputs are equipped with

PIN CONNECTIONS (top view)



NC = No Internal Con-

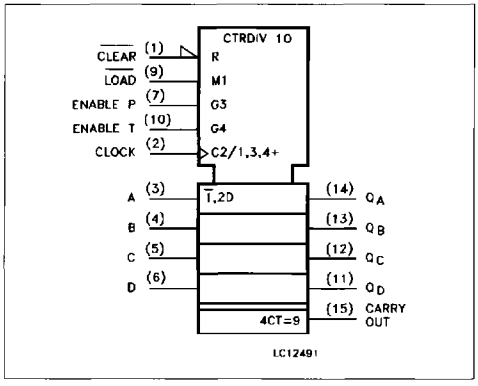
INPUT AND OUTPUT EQUIVALENT CIRCUIT



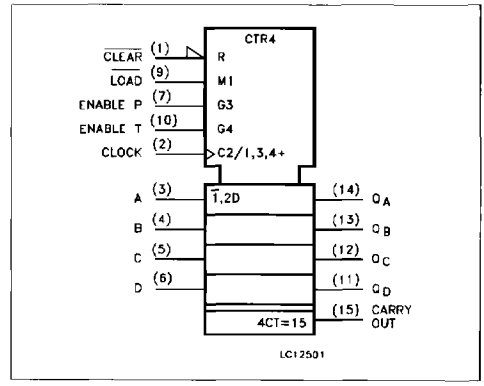
PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Master Reset
2	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
3, 4, 5, 6	A, B, C, D	Data Inputs
7	ENABLE P	Count Enable Input
10	ENABLET	Count Enable Carry Input
9	$\overline{\text{LOAD}}$	Parallel Enable Input
14, 13, 12, 11	QA to QD	Flip Flop Outputs
15	CARRY OUTPUT	Terminal Count Output
8	GND	Ground (0V)
16	Vcc	Positive Supply Voltage

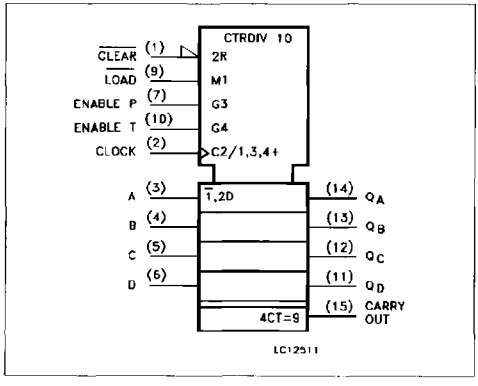
IEC LOGIC SYMBOL (HCT160)



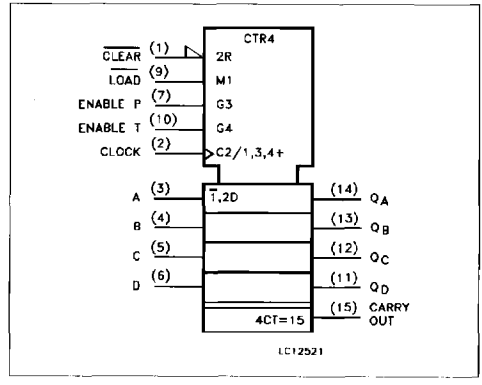
IEC LOGIC SYMBOL (HCT161)



IEC LOGIC SYMBOL (HCT162)



IEC LOGIC SYMBOL (HCT163)

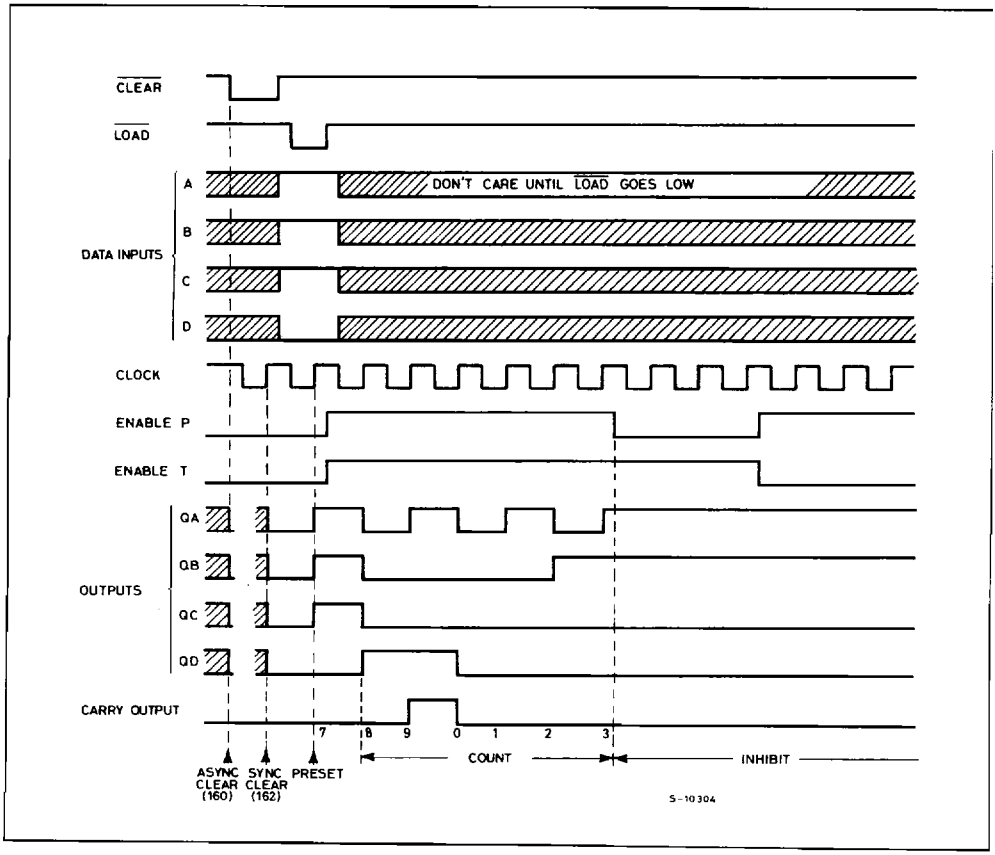


TRUTH TABLE

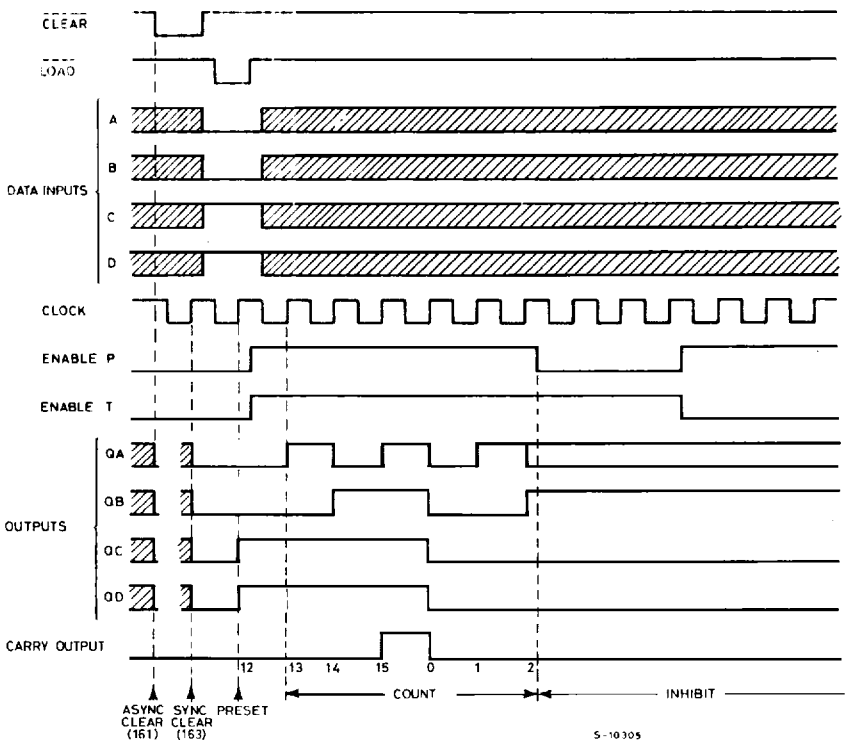
M54/74HCT160/161 INPUTS					M54/74HCT162/163 INPUTS					OUTPUTS				FUNCTION
$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	$\overline{CLR}$	$\overline{LD}$	PE	TE	CK	QA	QB	QC	QD	
L	X	X	X	X	L	X	X	X	⌐	L	L	L	L	RESET TO "0"
H	L	X	X	⌐	H	L	X	X	⌐	A	B	C	D	PRESET DATA
H	H	X	L	⌐	H	H	X	L	⌐	NO CHANGE				NO COUNT
H	H	L	X	⌐	H	H	L	X	⌐	NO CHANGE				NO COUNT
H	H	H	H	⌐	H	H	H	H	⌐	COUNT UP				COUNT
H	X	X	X	⌙	X	X	X	X	⌙	NO CHANGE				NO COUNT

Note: X : Don't Care
A, B, C, D : Logi level of data inputs
Carry : CARRY = TE • Q_A • Q_B • $\overline{Q_C}$ • Q_D ..... (M54/74HCT160/162)
: CARRY = TE • Q_A • Q_B • Q_C • Q_D ..... (M54/74HCT161/163)

TIMING CHART (HCT160/162 : decade counter)

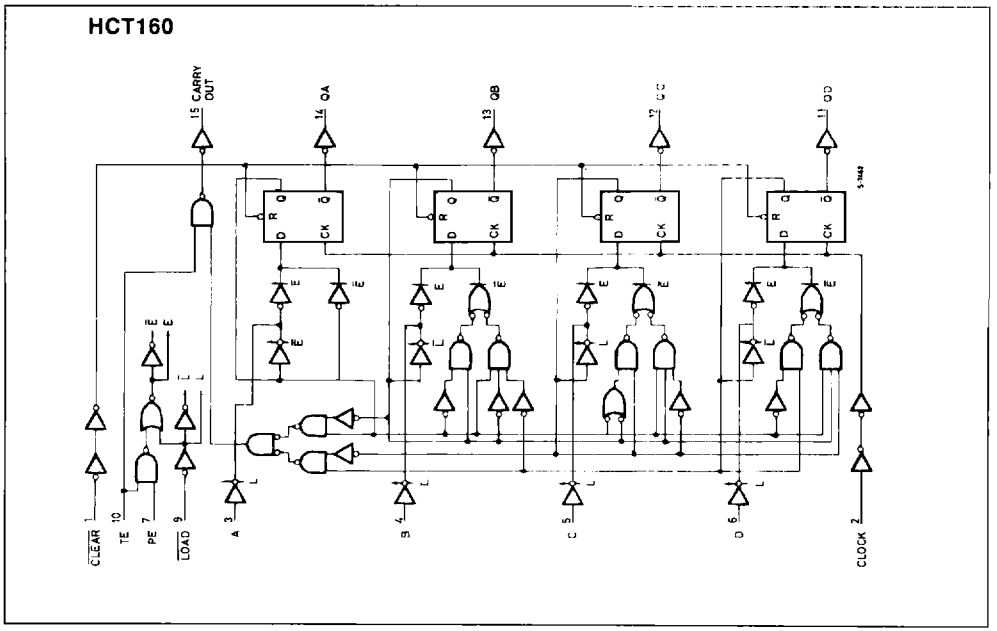


TIMING CHART (HCT161/163 : binary counter)



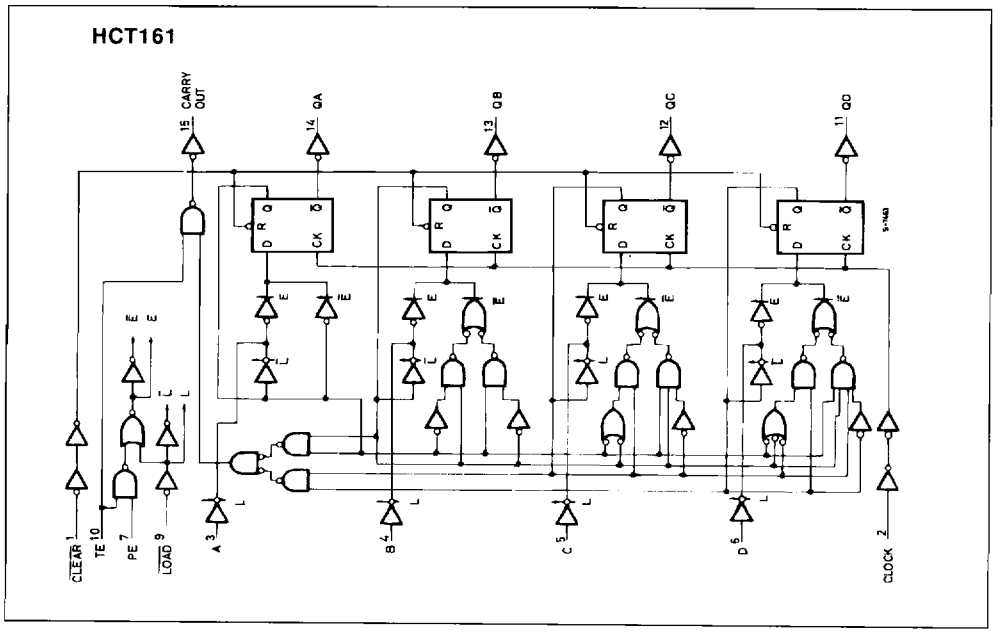
LOGIC DIAGRAM

HCT160

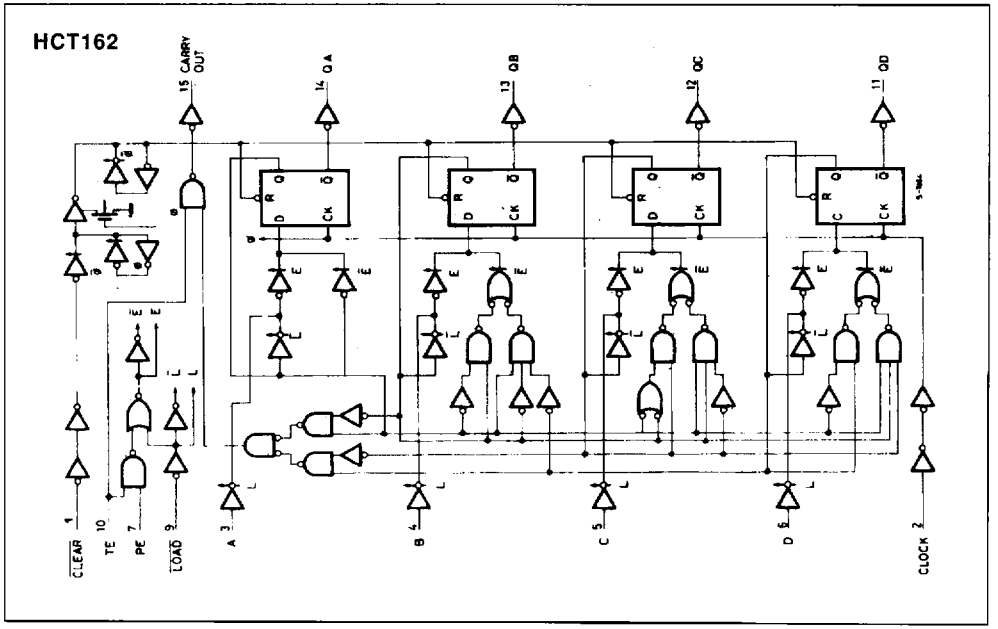


LOGIC DIAGRAM

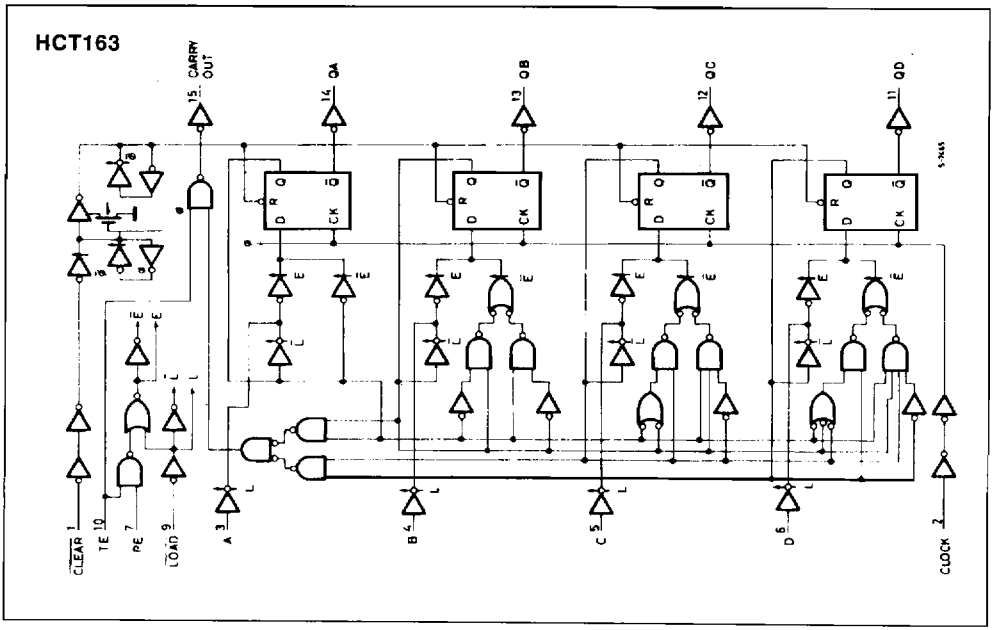
HCT161



LOGIC DIAGRAM



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.
(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature: **M54HC** Series **M74HC** Series	-55 to +125 -40 to +85	°C °C
t_r, t_f	Input Rise and Fall Time (V_{CC} = 4.5 to 5.5V)	0 to 500	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions			Value							Unit
		V_{CC} (V)			T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4.5 to 5.5			2.0			2.0		2.0		V
V_{IL}	Low Level Input Voltage	4.5 to 5.5					0.8		0.8		0.8	V
V_{OH}	High Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O=-20 µA	4.4	4.5		4.4		4.4		V
				I_O=-4.0 mA	4.18	4.31		4.13		4.10		
V_{OL}	Low Level Output Voltage	4.5	V_I = V_{IH} or V_{IL}	I_O= 20 µA		0.0	0.1		0.1		0.1	V
				I_O= 4.0 mA		0.17	0.26		0.33		0.4	
I_I	Input Leakage Current	5.5	V_I = V_{CC} or GND				±0.1		±1		±1	µA
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND				4		40		80	µA
ΔI_{CC}	Additional worst case supply current	5.5	Per Input pin V_I = 0.5V or V_I = 2.4V Other Inputs at V_{CC} or GND				2.0		2.9		3.0	mA

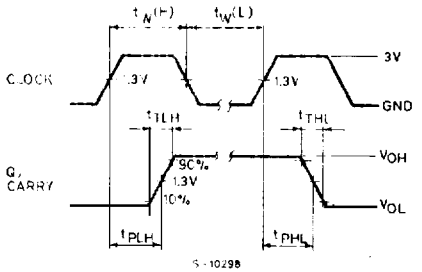
AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6 ns)

Symbol	Parameter	Test Conditions		Value							Unit
		V_{CC} (V)		T_A = 25 °C 54HC and 74HC			-40 to 85 °C 74HC		-55 to 125 °C 54HC		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	4.5			8	15		19		22	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK - Q)	4.5			23	36		45		54	ns
t_{PLH} t_{PHL}	Propagation Delay Time (CK-CO)	4.5			27	42		53		63	ns
t_{PLH}	Propagation Delay Time (TE-CO)	4.5			21	33		41		50	ns
t_{PLH}	Propagation Delay Time (CLEAR - Q)	4.5	for HCT160/161 only		26	40		50		60	ns
t_{PHL}	Propagation Delay Time (CLEAR-CO)	4.5	for HCT160/161 only		28	43		54		65	ns
f_{MAX}	Maximum Clock Frequency	4.5		31	49		25		21		MHz
$t_{W(H)}$ $t_{W(L)}$	Minimum Pulse Width (CK)	4.5			8	15		19		22	ns
$t_{W(L)}$	Minimum Pulse Width $\overline{\text{(CLEAR)}}$	4.5	for HCT160/161 only		8	15		19		22	ns
t_s	Minimum Set-up Time (LOAD, PE, TE)	4.5			11	20		25		30	ns
t_s	Minimum Set-up Time (A, B, C, D)	4.5			5	15		19		22	ns
t_s	Minimum Set-up Time $\overline{\text{(CLEAR)}}$	4.5	for HCT162/163 only		5	15		19		22	ns
t_h	Minimum Hold Time	4.5				5		5		8	ns
t_{REM}	Minimum Removal Time $\overline{\text{(CLEAR)}}$	4.5	for HCT160/161 only		5	15		19		22	ns
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD} (*)	Power Dissipation Capacitance				33						pF

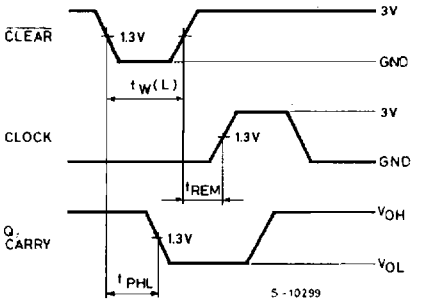
(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operting current can be obtained by the following equation. $I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

SWITCHING CHARACTERISTICS TEST WAVEFORM

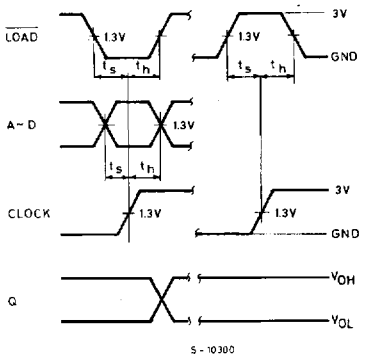
COUNT MODE



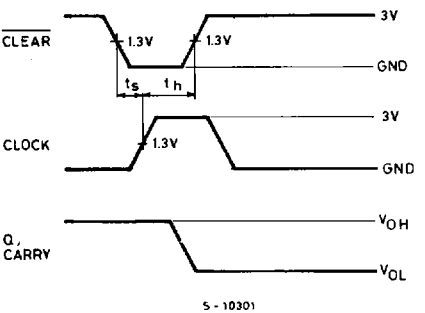
CLEAR MODE (HCT160/161)



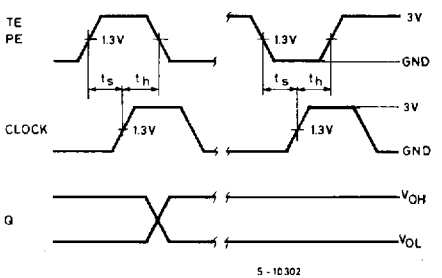
PRESET MODE



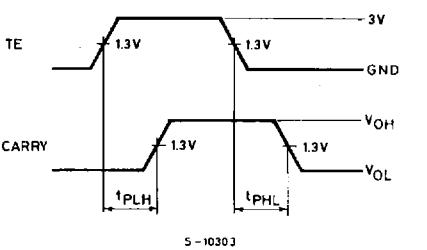
CLEAR MODE (HCT162/163)



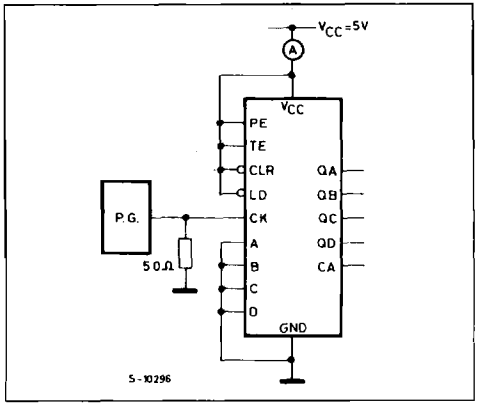
COUNTENABLE MODE



CASCADE MODE
(fix maximum count)



TEST CIRCUIT I_{CC} (Opr.)



TOTAL OPERATING CURRENT WHEN USING A CAPACITIVE LOAD

When the outputs drive a capacitive load, the total current can be calculated as follows :

For M74HCT160/162 :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{5} + \frac{C_c}{10} + \frac{C_d}{10} + \frac{C_{ca}}{10} \right)$$

For M74HCT161/163 :

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \cdot \left(\frac{C_a}{2} + \frac{C_b}{4} + \frac{C_c}{8} + \frac{C_d}{16} + \frac{C_{ca}}{16} \right)$$

C_a to C_{ca} are the capacitors loading the outputs.

TYPICAL APPLICATION