IS24C04B

2-WIRE

4Kb SERIAL EEPROM

TABLE OF CONTENTS

4K-bit
2-WIRE SERIAL CMOS EEPROM

ADVANCED INFORMATION
JANUARY 2010

1 FEATURES

- Two-Wire Serial Interface, I²C™ Compatible
  - Bi-directional data transfer protocol
- Wide-voltage Operation
  - Vcc = 1.8V to 5.5V
- Speed: 400 KHz (1.8V) and 1 MHz (2.5V~5.5V)
- Standby current: 1 μA (max.), 1.8V
- Operating current: 3 mA (max.), 5.5V
- Hardware Data Protection
  - Write Protect Pin
- Sequential & Random Read Features
- Memory organization: 4Kb (512 x 8)
- Page Size: 16 bytes
- Page write mode
  - Partial page writes allowed
- Self timed write cycle: 5 ms (max.)
- Noise immunity on inputs, besides Schmitt trigger
- High-reliability
  - Endurance: 1 million cycles
  - Data retention: 100 years
- Industrial temperature grade
- Packages: SOIC/SOP, TSSOP and uDFN
- Lead-free, RoHS, Halogen free, Green

2 DESCRIPTION

The IS24C04B is an industrial standard electrically erasable programmable read only memory (EEPROM) device that utilizes the industrial standard 2-wire interface for communications. The IS24C04B contains a memory array of 4K bits (512x8), which is organized in 16-byte per page.

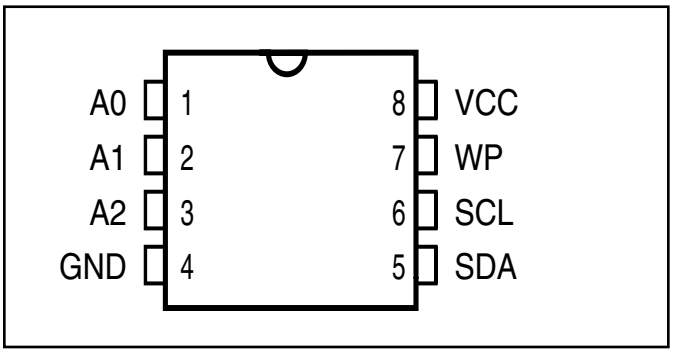
The EEPROM operates in a wide voltage range from 1.8V to 5.5V, which fits most application. The product provides low-power operations and low standby current. The device is offered in Lead-free, RoHS, halogen free or Green package. The available package types are 8-pin SOIC/SOP, TSSOP and UDFN.

The IS24C04B is compatible to the standard 2-wire bus protocol. The simple bus consists of Serial Clock (SCL) and Serial Data (SDA) signals. Utilizing such bus protocol, a Master device, such as a microcontroller, can usually control one or more Slave devices, alike this IS24C04B. The bit stream over the SDA line includes a series of bytes, which identifies a particular Slave device, an instruction, an address within that Slave device, and a series of data, if appropriate. The IS24C04B also has a Write Protect function via WP pin to cease from overwriting the data stored inside the memory array.

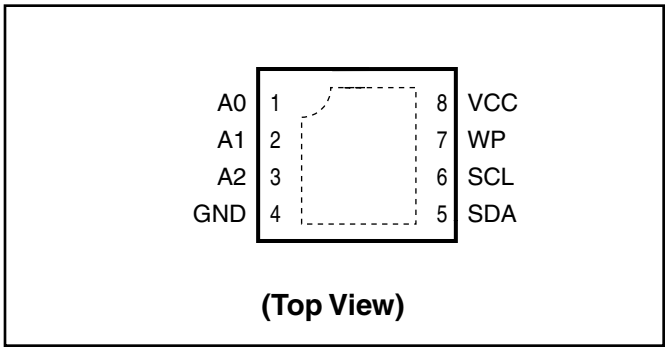
In order to refrain the state machine entering into a wrong state during power-up sequence or a power toggle off-on condition, a power on reset circuit is embedded. During power-up, the device does not respond to any instructions until the supply voltage (Vcc) has reached an acceptable stable level above the reset threshold voltage. Once Vcc passes the power on reset threshold, the device is reset and enters into the Standby mode. This would also avoid any inadvertent Write operations during power-up stage. During power-down process, the device will enter into standby mode, once Vcc drops below the power on reset threshold voltage. In addition, the device will be in standby mode after receiving the Stop command, provided that no internal write operation is in progress. Nevertheless, it is illegal to send an command unless the Vcc is within its operating level.

3 PIN CONFIGURATION

8-Pin SOIC, TSSOP



8-pad UDFN



4 PIN DESCRIPTIONS

A0-A2	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL
This input clock pin is used to synchronize the data transfer to and from the device.

SDA
The SDA is a bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wired with other open drain or open collector outputs. However, the SDA pin requires a pull-up resistor connected to the power supply.

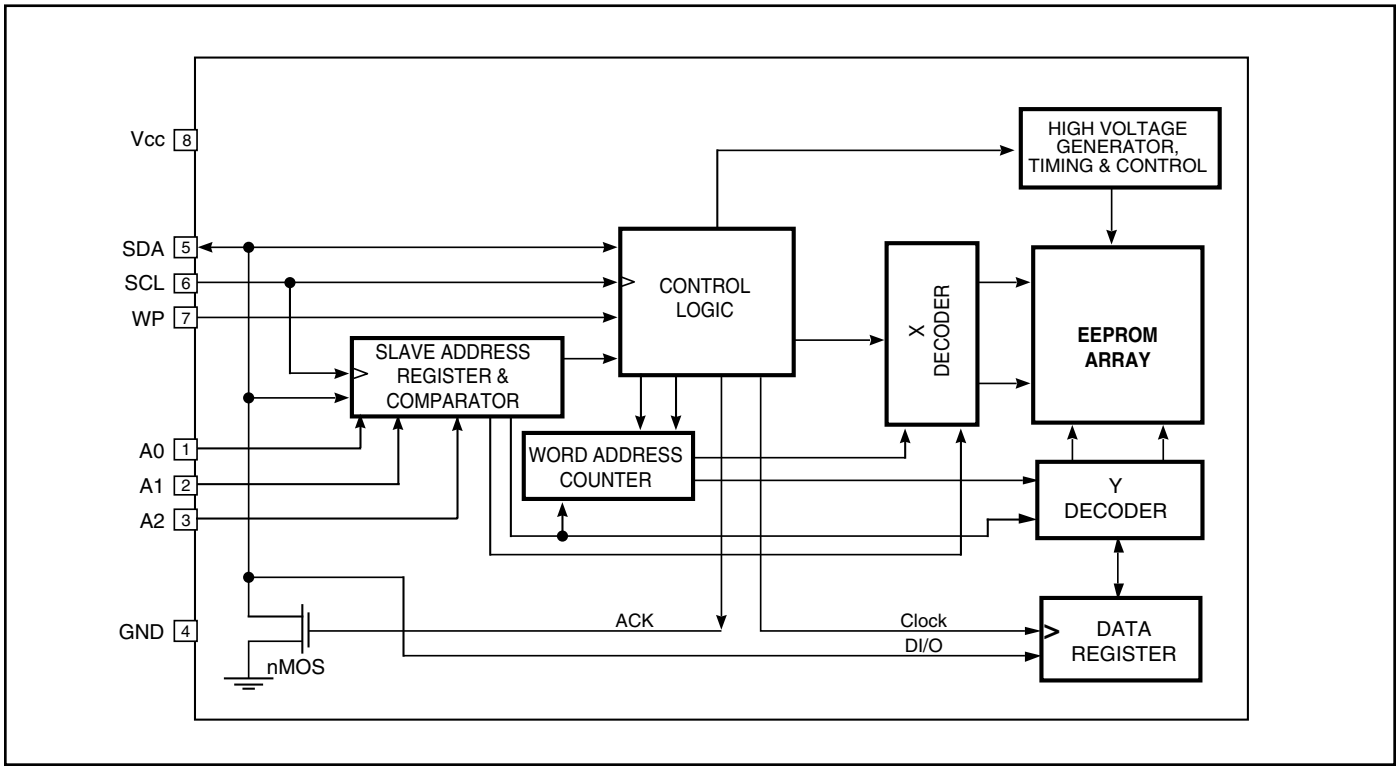
A0, A1, A2
The A0, A1 and A2 are the device address inputs.
For IS24C04B, the A1 and A2 pins are address inputs, but A0 is no-connect. Internally, the A0 is floated, while A1 and A2 are defaulted to "zero". Thus, a total of 4 devices can be connected on a single bus system.

WP
WP is the Write Protect pin. While the WP pin is connected to the power supply of IS24C04B, the entire array becomes Write Protected (i.e. the device becomes Read only). When WP is tied to Ground or left floating, the normal write operations are allowed.

Vcc
Supply voltage

GND
Ground of supply voltage

5 FUNCTIONAL BLOCK DIAGRAM



6 DEVICE OPERATION

The IS24C04B serial interface supports communications using industrial standard 2-wire bus protocol, such as I^2C^{TM}.

2-WIRE BUS

The two-wire bus is defined as Serial Data (SDA), and Serial Clock (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The IS24C04B is the Slave device.

The Bus Protocol:

Data transfer may be initiated only when the bus is not busy.

During a data transfer, the SDA line must remain stable whenever the SCL line is high. Any changes in the SDA line while the SCL line is high will be interpreted as a Start or Stop condition.

The state of the SDA line represents valid data after a Start condition. The SDA line must be stable for the duration of the High period of the clock signal. The data on the SDA line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a Start condition and terminated by a Stop condition.

Start Condition

The Start condition precedes all commands to the device and is defined as a High to Low transition of SDA when SCL is High. The EEPROM monitors the SDA and SCL lines and will not respond until the Start condition is met.

Stop Condition

The Stop condition is defined as a Low to High transition of SDA when SCL is High. All operations must end with a Stop condition.

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an ACK. The Acknowledging device pulls down the SDA line.

Reset

The IS24C04B contains a reset function in case the 2-wire bus transmission is accidentally interrupted (e.g. a power loss), or needs to be terminated mid-stream. The reset is initiated when the Master device creates a Start condition. To do this, it may be necessary for the Master device to monitor the SDA line while cycling the SCL up to nine times. (For each clock signal transition to High, the Master checks for a High level on SDA.)

Standby Mode

While in standby mode, the power consumption is minimal. The IS24C04B enters into standby mode during one of the following conditions: a) After Power-up, while no Opcode is sent; b) After the completion of an operation and followed by the Stop signal, provided that the previous operation is not Write related; or c) After the completion of any internal write operations.

DEVICE ADDRESSING

The Master begins a transmission by sending a Start condition, then sends the address of the particular Slave devices to be communicated. The Slave device address is 8 bits format as shown in Fig. 5.

The four most significant bits of the Slave address are fixed (1010) for IS24C04B.

The next three bits, A1, A2 and B0 of the Slave address are specifically related to EEPROM. Up to four IS24C04B units may be connected to the 2-wire bus. The bits A1 and A2 are used to compare with the hardwired input values on both A1 and A2 pins. While bit B0 is being employed to address either the upper or the lower 256 bytes of the device.

The last bit of the Slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, Read operation is selected. While it is set to 0, Write operation is selected.

After the Master transmits the Start condition and Slave address byte appropriately, the associated 2-wire Slave device, IS24C04B, will respond with ACK on the SDA line. Then IS24C04B will pull down the SDA on the ninth clock cycle, signaling that it received the eight bits of data.

The IS24C04B then prepares for a Read or Write operation by monitoring the bus.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the Start condition and the Slave address information (with the R/W set to Zero) to the Slave device. After the Slave generates an ACK, the Master sends the byte address that is to be written into the address pointer of the IS24C04B. After receiving another ACK from the Slave, the Master device transmits the data byte to be written into the address memory location. The IS24C04B acknowledges once more and the Master generates the Stop condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The IS24C04B is capable of 16-byte Page-Write operation. A Page-Write is initiated in the same manner as a Byte Write, but instead of terminating the internal Write cycle after the first data word is transferred, the Master device can transmit up to 15 more bytes. After the receipt of each data word, the EEPROM responds immediately with an ACK on SDA line, and the four lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If a byte address is incremented from the last byte of a page, it returns to the first byte of that page. If the Master device should transmit more than 16 bytes prior to issuing the Stop condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 16 bytes are received and the Stop condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the IS24C04B in a single Write cycle. All inputs are disabled until completion of the internal Write cycle.

Acknowledge (ACK) Polling

The disabling of the inputs can be used to take advantage of the typical Write cycle time. Once the Stop condition is issued to indicate the end of the host's Write operation, the IS24C04B initiates the internal Write cycle. ACK polling can be initiated immediately. This involves issuing the Start condition followed by the Slave address for a Write operation. If the EEPROM is still busy with the Write operation, no ACK will be returned. If the IS24C04B has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

READ OPERATION

Read operations are initiated in the same manner as Write operations, except that the (R/W) bit of the Slave address is set to “1”. There are three Read operation options: current address read, random address read and sequential read.

Current Address Read

The IS24C04B contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a Read or Write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the EEPROM receives the Slave Addressing Byte with a Read operation (R/W bit set to “1”), it will respond an ACK and transmit the 8-bit data byte stored at address location n+1. The Master should not acknowledge the transfer but should generate a Stop condition so the IS24C04B discontinues transmission. If 'n' is the last byte of the memory, the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Address Read

Selective Read operations allow the Master device to select at random any memory location for a Read operation. The Master device first performs a 'dummy' Write operation by sending the Start condition, Slave address and byte address of the location it wishes to read. After the

IS24C04B acknowledges the byte address, the Master device resends the Start condition and the Slave address, this time with the R/W bit set to one. The EEPROM then responds with its ACK and sends the data requested. The Master device does not send an ACK but will generate a Stop condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the IS24C04B sends the initial byte sequence, the Master device now responds with an ACK indicating it requires additional data from the IS24C04B. The EEPROM continues to output data for each ACK received. The Master device terminates the sequential Read operation by pulling SDA High (no ACK) indicating the last data word to be read, followed by a Stop condition. The data output is sequential, with the data from address n followed by the data from address n+1,n+2 ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential Read operation. When the memory address boundary of the array is reached, the address counter “rolls over” to address 0, and the device continues to output data. (Refer to Figure 10. Sequential Read Diagram).

7 TIMING DIAGRAMS

FIGURE 1. TYPICAL SYSTEM BUS CONFIGURATION

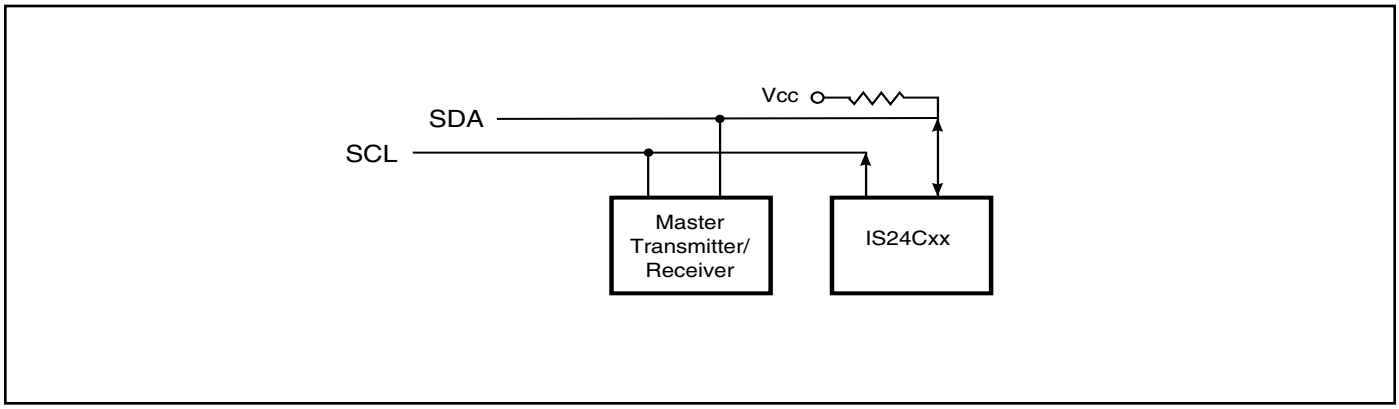


FIGURE 2. OUTPUT ACKNOWLEDGE

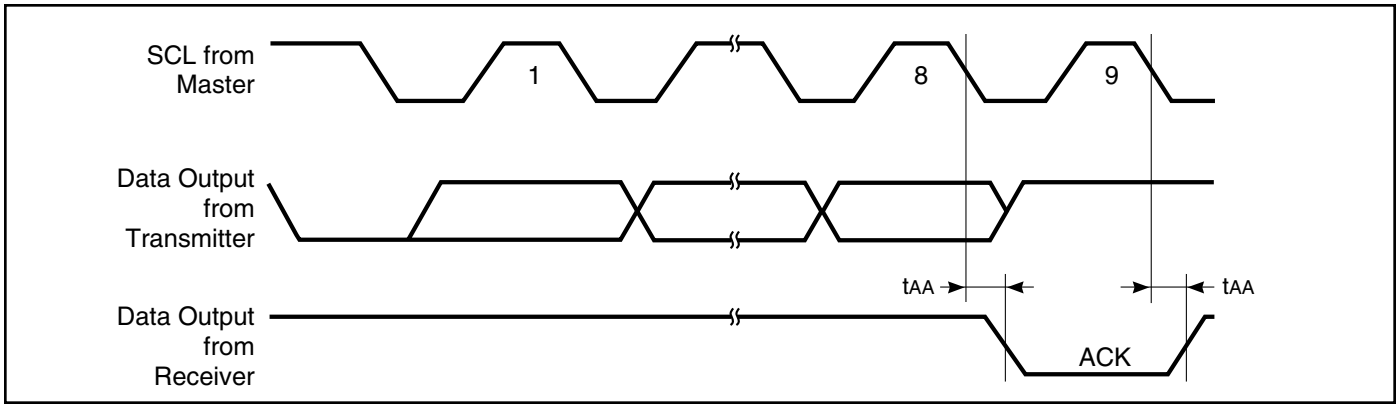


FIGURE 3. START AND STOP CONDITIONS

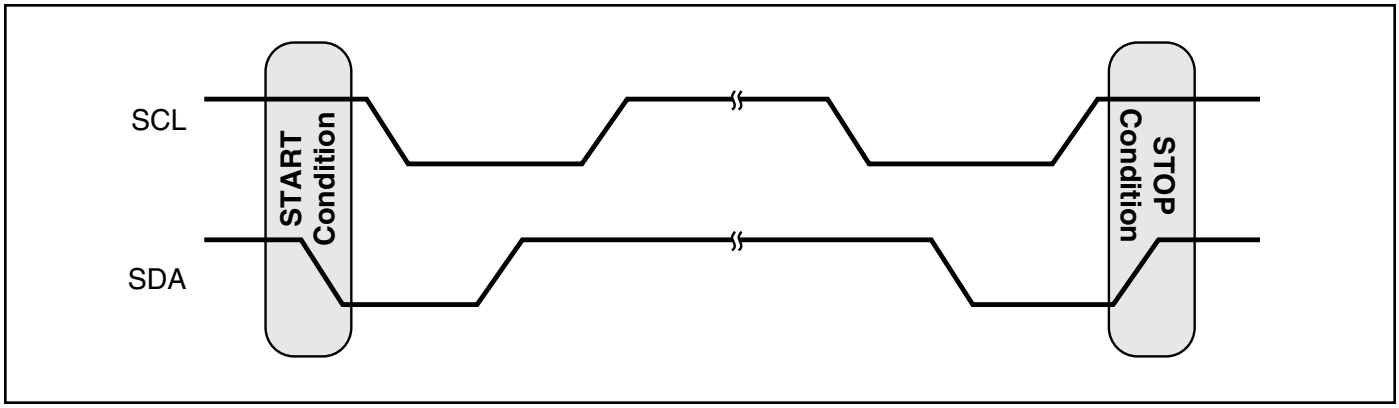


FIGURE 4. DATA VALIDITY PROTOCOL

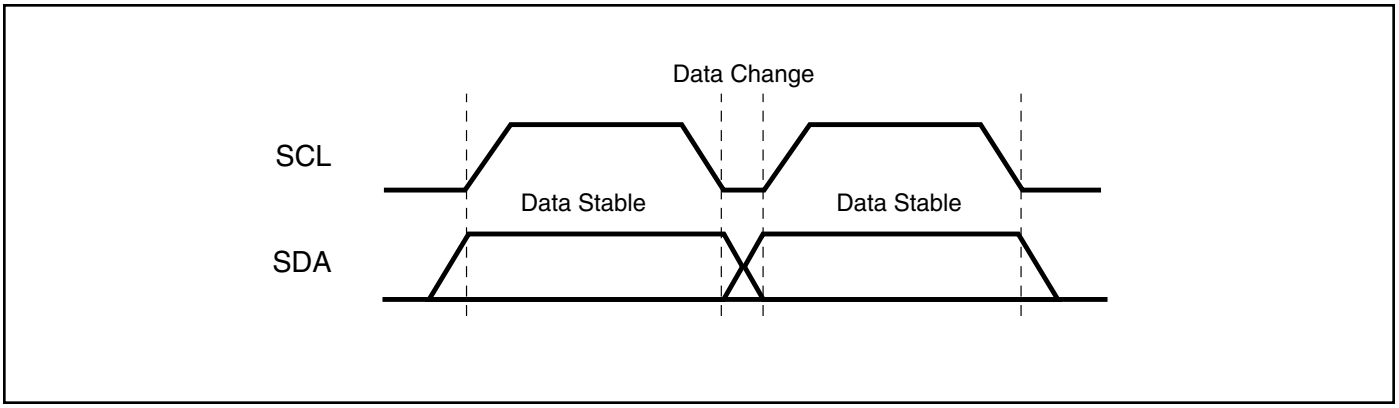


FIGURE 5. SLAVE ADDRESS

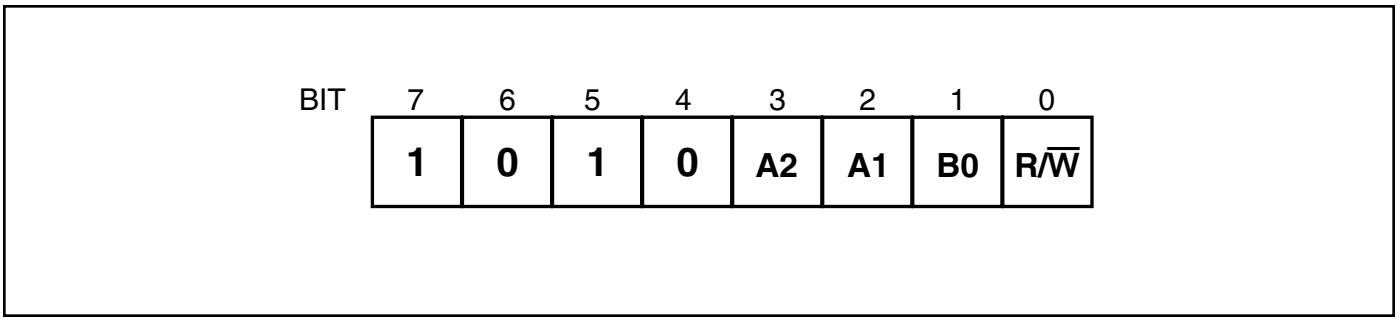
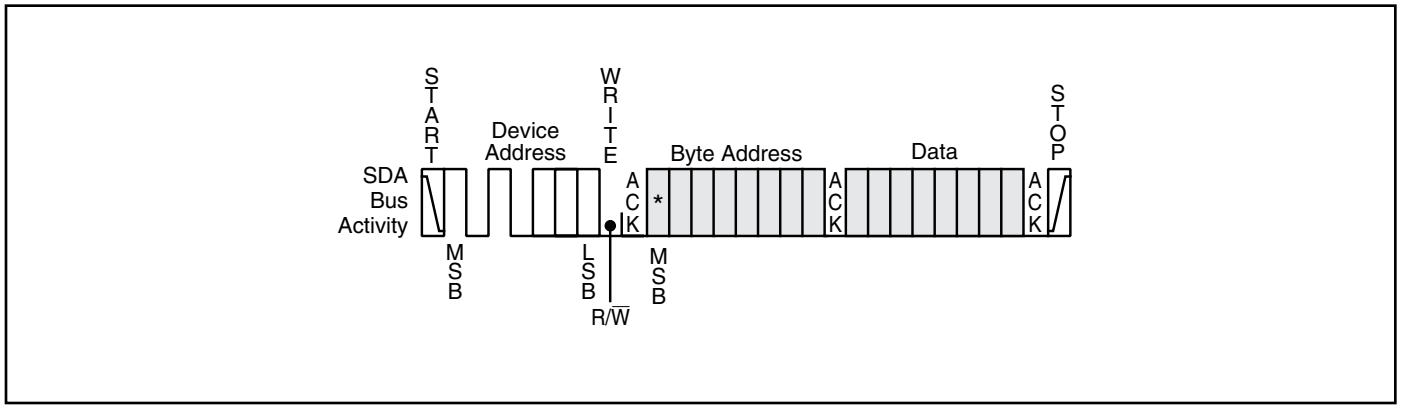
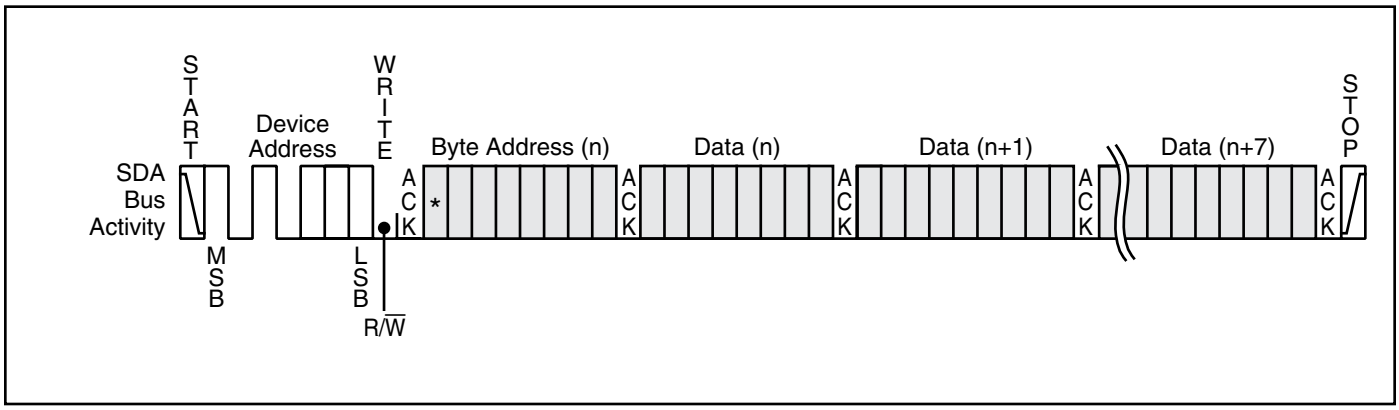


FIGURE 6. BYTE WRITE



* = Don't care bit for IS24C01B

FIGURE 7. PAGE WRITE



* = Don't care bit for IS24C01B

FIGURE 8. CURRENT ADDRESS READ

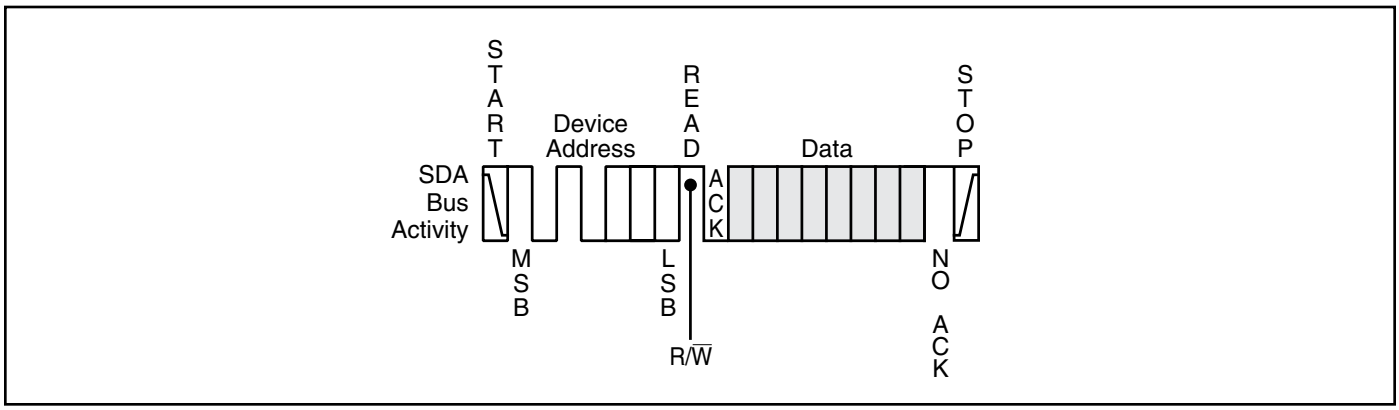
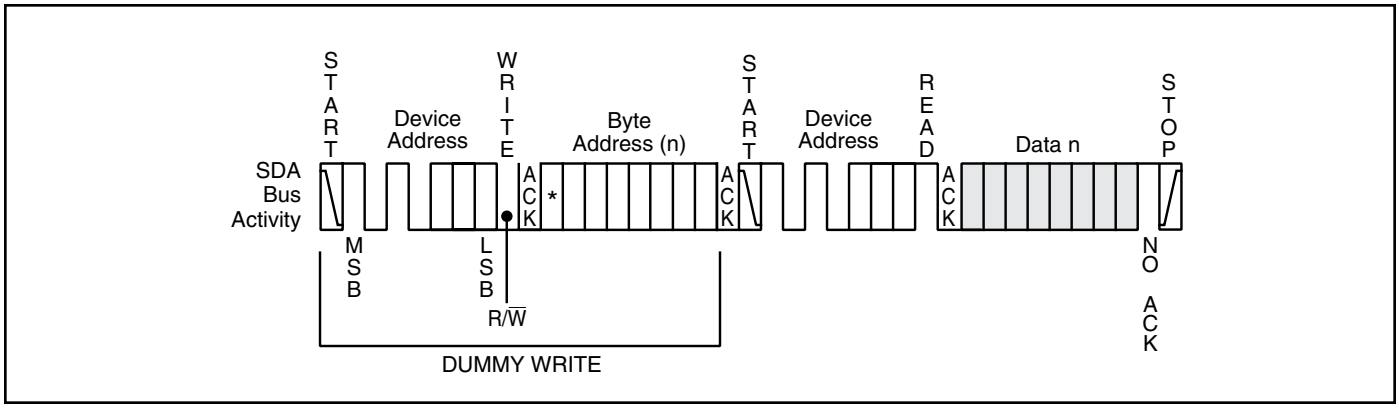
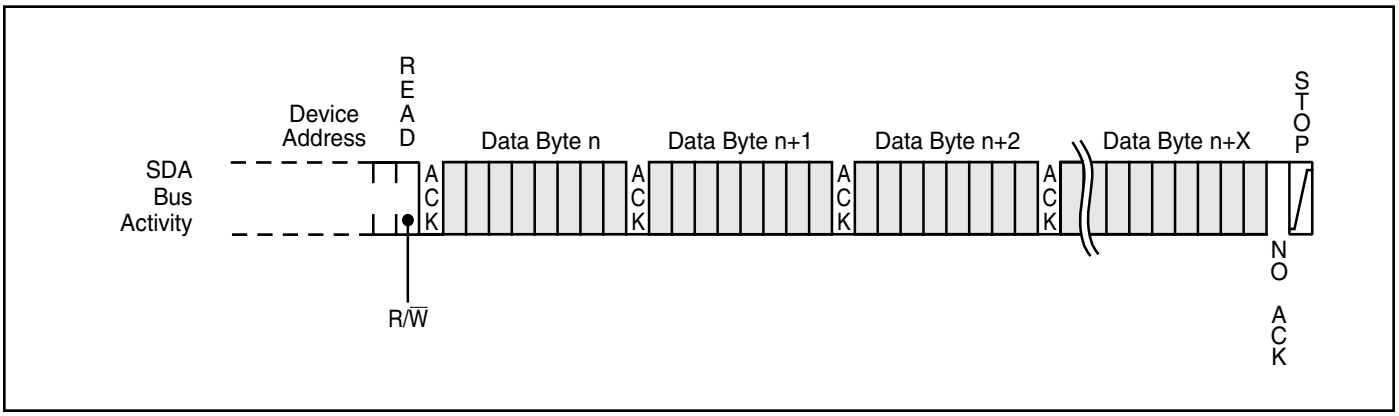


FIGURE 9. RANDOM ADDRESS READ



* = Don't care bit for IS24C01B

FIGURE 10. SEQUENTIAL READ



AC WAVEFORMS

Figure 11. Bus Timing

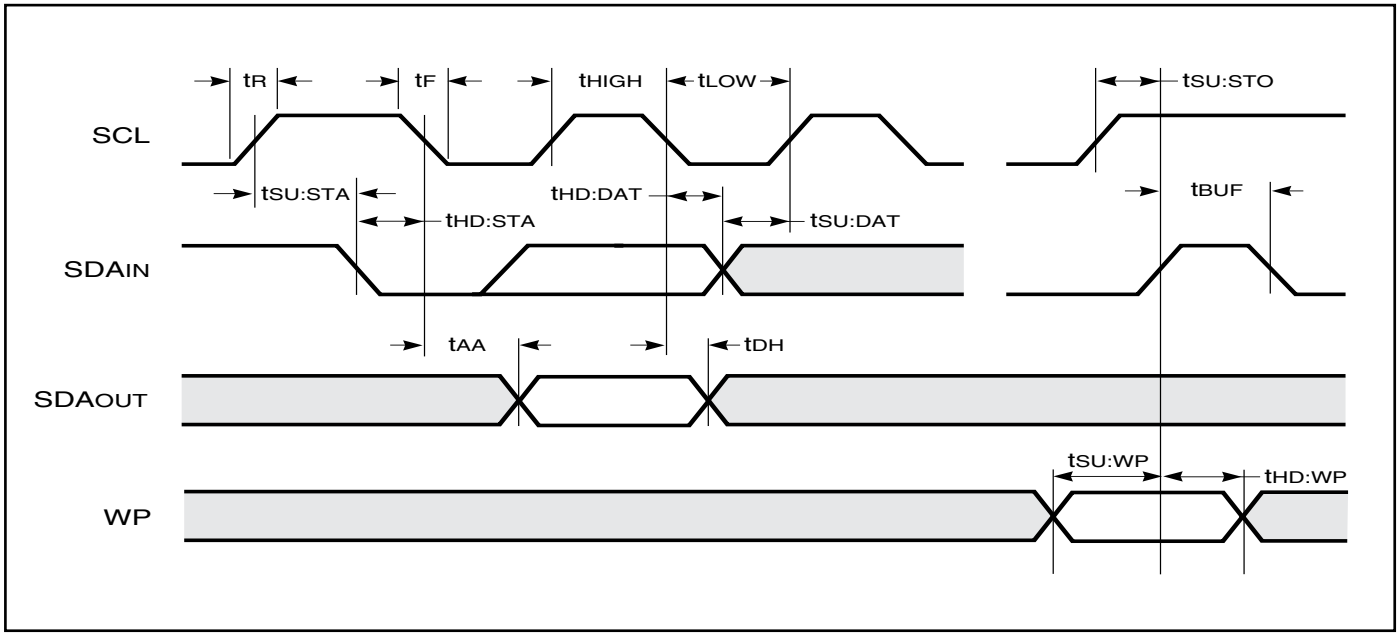
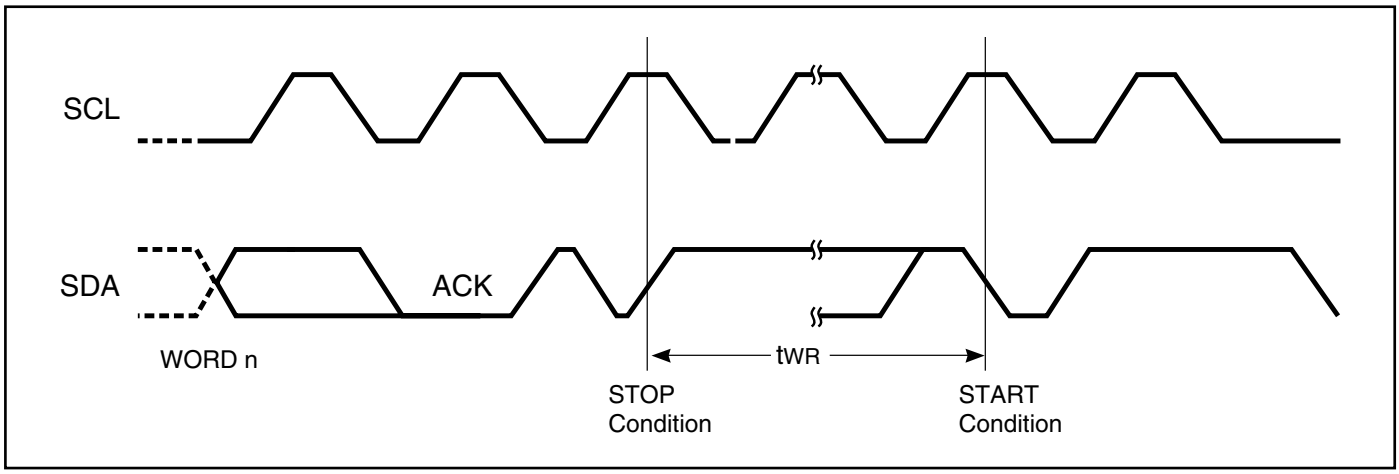


Figure 12. Write Cycle Timing



8 ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
Vs	Supply Voltage	-0.5 to + 6.5	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

OPERATING RANGE

Range	Ambient Temperature (T_A)	Vcc
Industrial	–40°C to +85°C	1.8V to 5.5V

Note: ISSI offers Industrial grade for Commercial applications (0°C to +70°C).

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max	Unit
C_{IN}	Input Capacitance	VIN = 0V	6	pF
$C_{I/O}$	Input /Output Capacitance	VI/O = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters and not 100% tested.
2. Test conditions: TA = 25°C, f = 1 MHz, Vcc = 5.0V.

9 DC ELECTRICAL CHARACTERISTICS

Industrial (T_A = -40°C to +85°C), Vcc = 1.8V ~ 5.5V

Symbol	Parameter [1]	Vcc	Test Conditions	Min.	Max.	Unit
Vcc	Supply Voltage			1.8	5.5	V
V_{IH}	Input High Voltage (SDA, SCL, WP)			0.7 * VCC	VCC + 1	V
V_{IL}	Input Low Voltage (SDA, SCL, WP)			-1	0.3 * VCC	V
I_{LI}	Input Leakage Current (SDA, SCL, WP, A0, A1 & A2)	5V	V_{IN} = 0V ~ VCC, standby mode	—	2	µA
I_{LO}	Output Leakage Current	5V	V_{OUT} = 0V~VCC, SDA in Hi-Z	—	2	µA
V_{OL1}	Output Low Voltage	1.8V	I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output Low Voltage	3V	I_{OL} = 2.1 mA	—	0.4	V
I_{sb1}	Standby Current	1.8V	V_{IN} = Vcc or GND	—	1	µA
		2.5V	V_{IN} = Vcc or GND	—	1	µA
		5.5V	V_{IN} = Vcc or GND	—	3	µA
I_{CC1}	Read Current	1.8V	Read at 400 KHz	—	0.8	mA
		4.5V	Read at 1 MHz	—	2	mA
		5.5V	Read at 1 MHz	—	2	mA
I_{CC2}	Write Current	1.8V	Write at 400 KHz	—	1	mA
		4.5V	Write at 1 MHz	—	3	mA
		5.5V	Write at 1 MHz	—	3	mA

Notes: [1] The parameters are characterized but not 100% tested.

10 AC ELECTRICAL CHARACTERISTICS

Industrial (T_A = -40°C to +85°C), Supply Voltage = 1.8V to 5.5V

Symbol	Parameter [1] [2]	1.8V ≤ Vcc < 2.5V		2.5V ≤ Vcc < 4.5V		4.5V ≤ Vcc ≤ 5.5V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCK Clock Frequency		400		1000		1000	KHz
t_{LOW}	Clock Low Period	1200	—	400	—	400	—	ns
t_{HIGH}	Clock High Period	600	—	400	—	400	—	ns
T_R	SCL and SDA Rise Time	—	300	—	300	—	300	ns
T_F	SCL and SDA Fall Time	—	300	—	100	—	100	ns
$t_{SU:STA}$	Start Condition Setup Time	500	—	200	—	200	—	ns
tsu:sto	Stop Condition Setup Time	500	—	200	—	200	—	ns
$t_{HD:STA}$	Start Condition Hold Time	500	—	200	—	200	—	ns
$t_{SU:DAT}$	Data In Setup Time	100	—	40	—	40	—	ns
$t_{HD:DAT}$	Data In Hold Time	0	—	0	—	0	—	ns
T_{AA}	Clock to Output Access time (SCL Low to SDA Data Out Valid)	100	900	50	400	50	400	ns
T_{DH}	Data Out Hold Time (SCL Low to SDA Data Out Change)	100	—	50	—	50	—	ns
t_{WR}	Write Cycle Time	—	5	—	5	—	5	ms
t_{BUF}	Bus Free Time Before New Transmission	1000	—	400	—	400	—	ns
$t_{SU:WP}$	WP pin Setup Time	1000	—	400	—	400		ns
$t_{HD:WP}$	WP pin Hold Time	1000	—	400	—	400	—	ns
T	Noise Suppression Time	—	100	—	50	—	50	ns

Notes:
[1] The parameters are characterized but not 100% tested.
[2] AC measurement conditions:
R_L (connects to Vcc): 1.3 kΩ (2.5V, 5.0V), 10 kΩ (1.8V)
C_L = 100 pF
Input pulse voltages: 0.3 Vcc to 0.7 Vcc
Input rise and fall times: ≤ 50 ns
Timing reference voltages: half Vcc level

11 ORDERING INFORMATION

Industrial Range*: –40°C to +85°C, Lead-free

Voltage Range	Part Number*	Package Type* (8-pin)
1.8V to 5.5V	IS24C04B-2GLI-TR	150-mil SOIC (JEDEC)
	IS24C04B-2ZLI-TR	3 x 4.4 mm TSSOP
	IS24C04B-2UDLI-TR	2 x 3 x 0.55mm UDFN

*

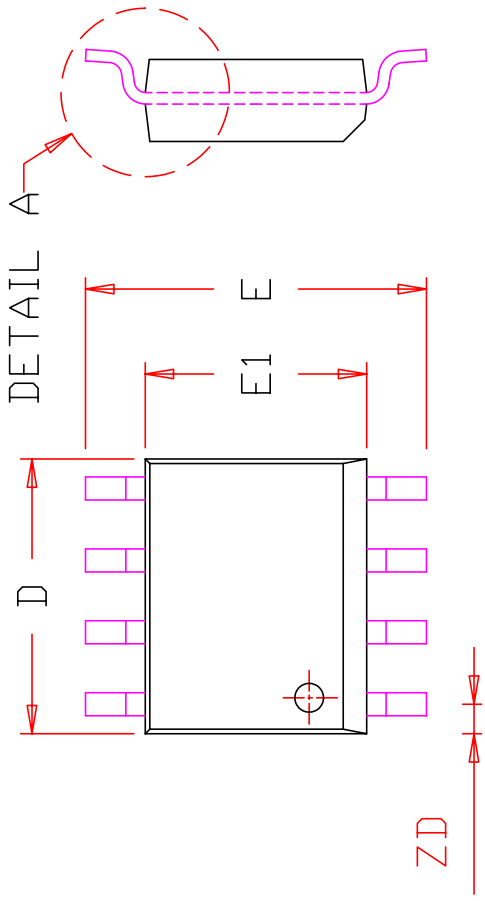
1. Contact ISSI Sales Representatives for availability and other package information.
2. The listed part numbers are packed in tape and reel “-TR” (4K per reel). UDFN is 5K per reel.
3. Refer to ISSI website for related declaration document on lead free, RoHS, halogen free or Green, whichever is applicable.
4. ISSI offers Industrial grade for Commercial applications (0°C to +70°C).

12 PACKAGE INFORMATION

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
b	0.33	—	0.51	0.013	—	0.020
D	4.80	—	5.00	0.189	—	0.197
E	5.80	—	6.20	0.228	—	0.244
E1	3.80	—	4.00	0.150	—	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	—	1.27	0.015	—	0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
θ	0	—	8°	0	—	8°

NOTE :

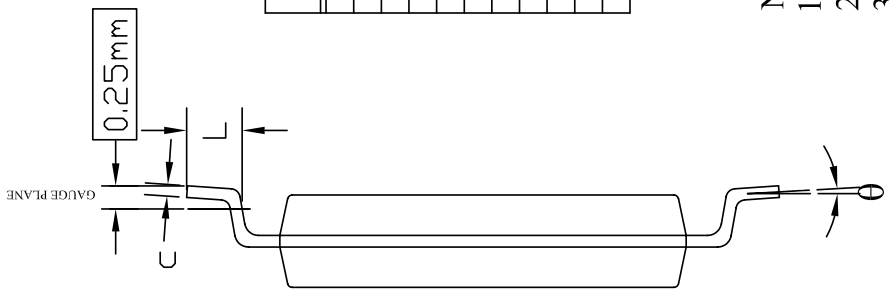
1. CONTROLLING DIMENSION : MM
2. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION.

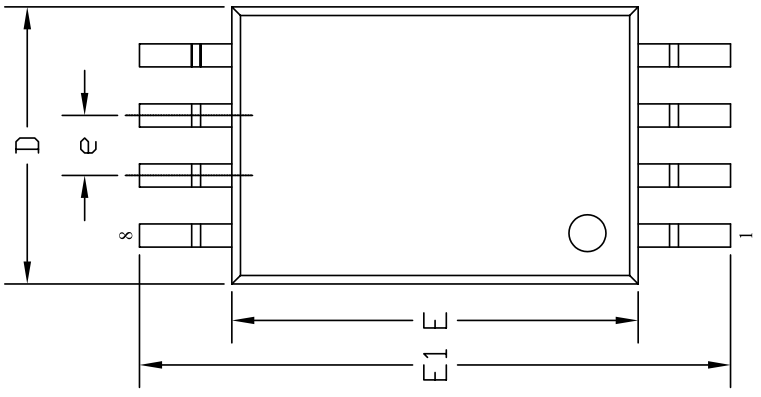


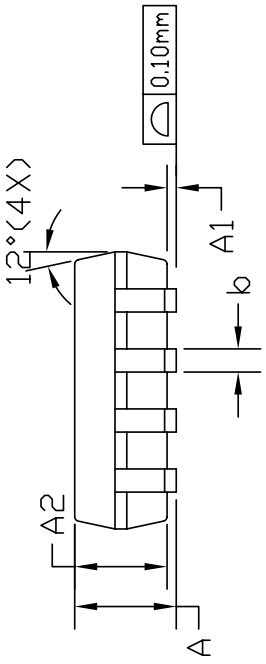
ISSI	TITLE	8L 150mil SOP Package Outline	REV.	C	DATE	07/30/2009

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	---	0.30	0.007	---	0.012
c	0.09	---	0.20	0.004	---	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	6.40 BSC			0.252 BSC		
E	4.30	4.40	4.50	0.169	0.173	0.177
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	---	8°	0°	---	8°

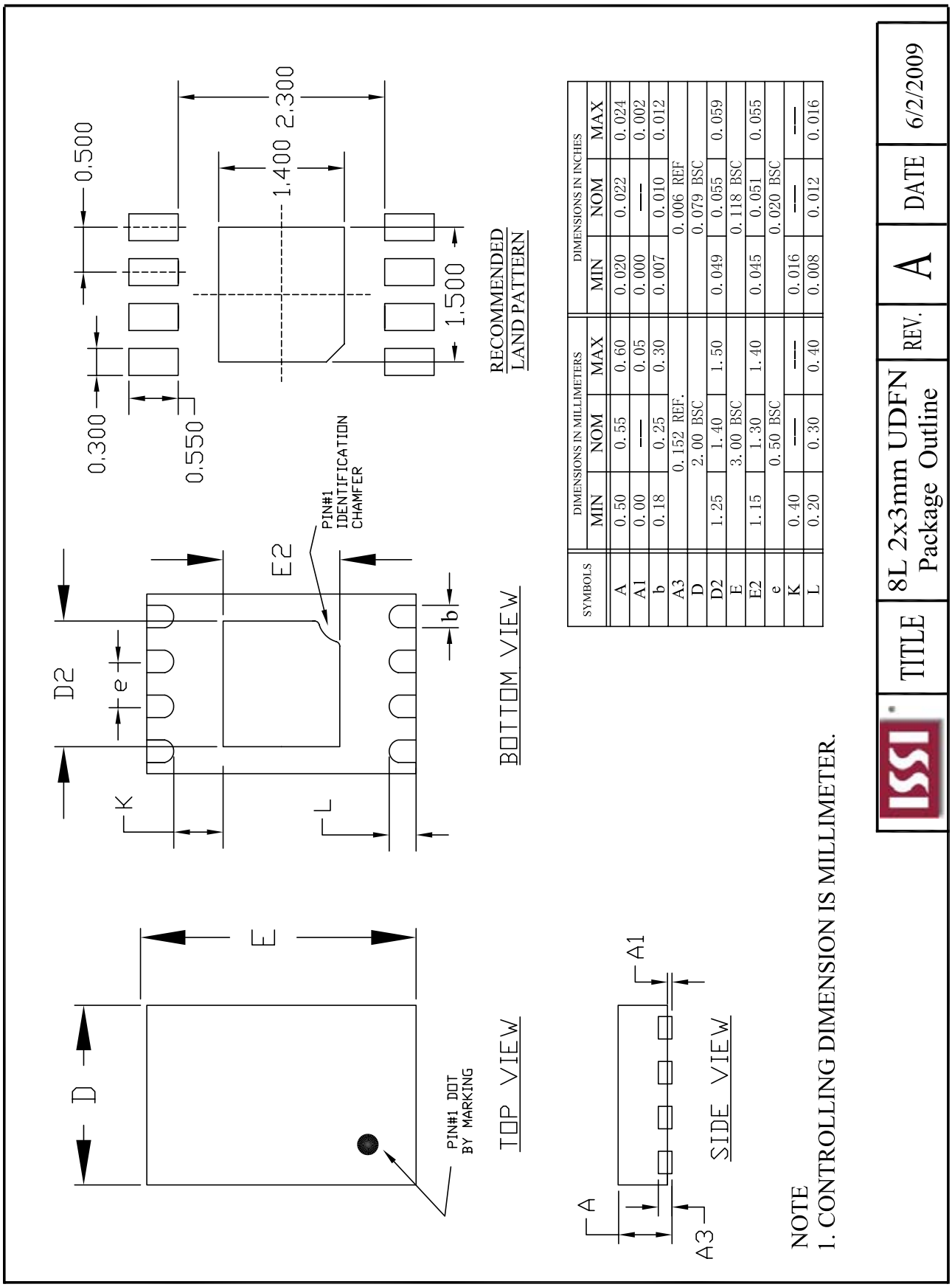
NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
2. REFER TO JEDEC STANDARD MO-153 AA.
3. PACKAGE MAY HAVE EXPOSED TIE BAR.
4. DIMENSION "D" AND "E1" DOES NOT INCLUDE MOLD PROTRUSION.
5. DIMENSION "b" DOES NOT INCLUDE DAM BAR PROTRUSION.







	TITLE	REV.	DATE
ISSI	8L 3x4.4mm TSSOP Package Outline	A	5/11/2009



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	—	0.05	0.000	—	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A3		0.152 REF.			0.006 REF	
D		2.00 BSC			0.079 BSC	
D2	1.25	1.40	1.50	0.049	0.055	0.059
E		3.00 BSC			0.118 BSC	
E2	1.15	1.30	1.40	0.045	0.051	0.055
e		0.50 BSC			0.020 BSC	
K	0.40	—	—	0.016	—	—
L	0.20	0.30	0.40	0.008	0.012	0.016