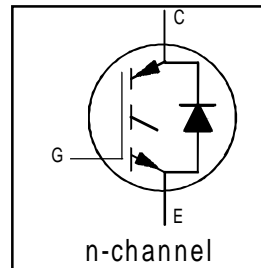


INSULATED GATE BIPOLAR TRANSISTOR WITH
ULTRAFAST SOFT RECOVERY DIODE

IRG4BC15UD-S
IRG4BC15UD-L
UltraFast CoPack IGBT

Features

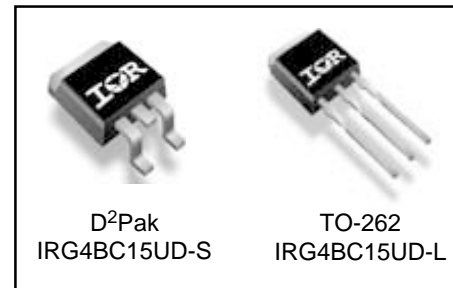
- UltraFast: Optimized for high frequencies from 10 to 30 kHz in hard switching
- IGBT Co-packaged with ultra-soft-recovery antiparallel diode
- Industry standard D²Pak & TO-262 packages



$V_{CES} = 600V$
$V_{CE(on)} \text{ typ.} = 2.02V$
@ $V_{GE} = 15V, I_C = 7.8A$

Benefits

- Best Value for Appliance and Industrial Applications
- High noise immune "Positive Only" gate drive- Negative bias gate drive not necessary
- For Low EMI designs- requires little or no snubbing
- Single Package switch for bridge circuit applications
- Compatible with high voltage Gate Driver IC's
- Allows simpler gate drive



Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	14	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	7.8	
I_{CM}	Pulsed Collector Current ①	42	
I_{LM}	Clamped Inductive Load Current ②	42	
$I_F @ T_C = 100^\circ C$	Diode Continuous Forward Current	4.0	
I_{FM}	Diode Maximum Forward Current	16	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	49	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	19	
T_J	Operating Junction and	-55 to +150	$^\circ C$
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case - IGBT	—	—	2.7	$^\circ C/W$
$R_{\theta JC}$	Junction-to-Case - Diode	—	—	7.0	
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount ⑤	—	—	80	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state) ⑥	—	—	40	
Wt	Weight	—	2 (0.07)	—	g (oz)

IRG4BC15UD-S/L

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage ^③	600	—	—	V	$V_{GE} = 0V, I_C = 250\mu A$	
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.63	—	V/°C	$V_{GE} = 0V, I_C = 1.0mA$	
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	2.02	2.4	V	$V_{GE} = 15V$ $I_C = 7.8A$	
		—	2.56	—			$I_C = 14A$
		—	2.21	—			$I_C = 7.8A, T_J = 150^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		$V_{CE} = V_{GE}, I_C = 250\mu A$	
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-10	—	mV/°C	$V_{CE} = V_{GE}, I_C = 250\mu A$	
g_{fe}	Forward Transconductance ^④	4.1	6.2	—	S	$V_{CE} = 100V, I_C = 7.8A$	
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	μA	$V_{GE} = 0V, V_{CE} = 600V$	
		—	—	1400		$V_{GE} = 0V, V_{CE} = 600V, T_J = 150^\circ\text{C}$	
V_{FM}	Diode Forward Voltage Drop	—	1.5	1.8	V	$I_C = 4.0A$	
		—	1.4	1.7		$I_C = 4.0A, T_J = 150^\circ\text{C}$	
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$	

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	
Q_g	Total Gate Charge (turn-on)	—	23	35	nC	$I_C = 7.8A$ $V_{CC} = 400V$ $V_{GE} = 15V$	
Q_{ge}	Gate - Emitter Charge (turn-on)	—	4.0	6.0			
Q_{gc}	Gate - Collector Charge (turn-on)	—	9.6	14			
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$T_J = 25^\circ\text{C}$ $I_C = 7.8A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 75\Omega$ Energy losses include "tail" and diode reverse recovery.	
t_r	Rise Time	—	20	—			
$t_{d(off)}$	Turn-Off Delay Time	—	160	240			
t_f	Fall Time	—	83	120			
E_{on}	Turn-On Switching Loss	—	0.24	—	mJ	$T_J = 150^\circ\text{C}$, $I_C = 7.8A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 75\Omega$ Energy losses include "tail" and diode reverse recovery.	
E_{off}	Turn-Off Switching Loss	—	0.26	—			
E_{ts}	Total Switching Loss	—	0.50	0.63			
$t_{d(on)}$	Turn-On Delay Time	—	16	—	ns	$T_J = 150^\circ\text{C}$, $I_C = 7.8A, V_{CC} = 480V$ $V_{GE} = 15V, R_G = 75\Omega$ Energy losses include "tail" and diode reverse recovery.	
t_r	Rise Time	—	21	—			
$t_{d(off)}$	Turn-Off Delay Time	—	180	—			
t_f	Fall Time	—	220	—			
E_{ts}	Total Switching Loss	—	0.76	—	mJ		
L_E	Internal Emitter Inductance	—	7.5	—	nH	Measured 5mm from package	
C_{ies}	Input Capacitance	—	410	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0MHz$	
C_{oes}	Output Capacitance	—	37	—			
C_{res}	Reverse Transfer Capacitance	—	5.3	—			
t_{rr}	Diode Reverse Recovery Time	—	28	42	ns	$T_J = 25^\circ\text{C}$	$I_F = 4.0A$ $V_R = 200V$ $di/dt 200A/\mu s$
		—	38	57		$T_J = 125^\circ\text{C}$	
I_{rr}	Diode Peak Reverse Recovery Current	—	2.9	5.2	A	$T_J = 25^\circ\text{C}$	
		—	3.7	6.7		$T_J = 125^\circ\text{C}$	
Q_{rr}	Diode Reverse Recovery Charge	—	40	60	nC	$T_J = 25^\circ\text{C}$	
		—	70	110		$T_J = 125^\circ\text{C}$	
$di_{(rec)M}/dt$	Diode Peak Rate of Fall of Recovery During t_b	—	280	—	A/ μs	$T_J = 25^\circ\text{C}$	
		—	240	—		$T_J = 125^\circ\text{C}$	

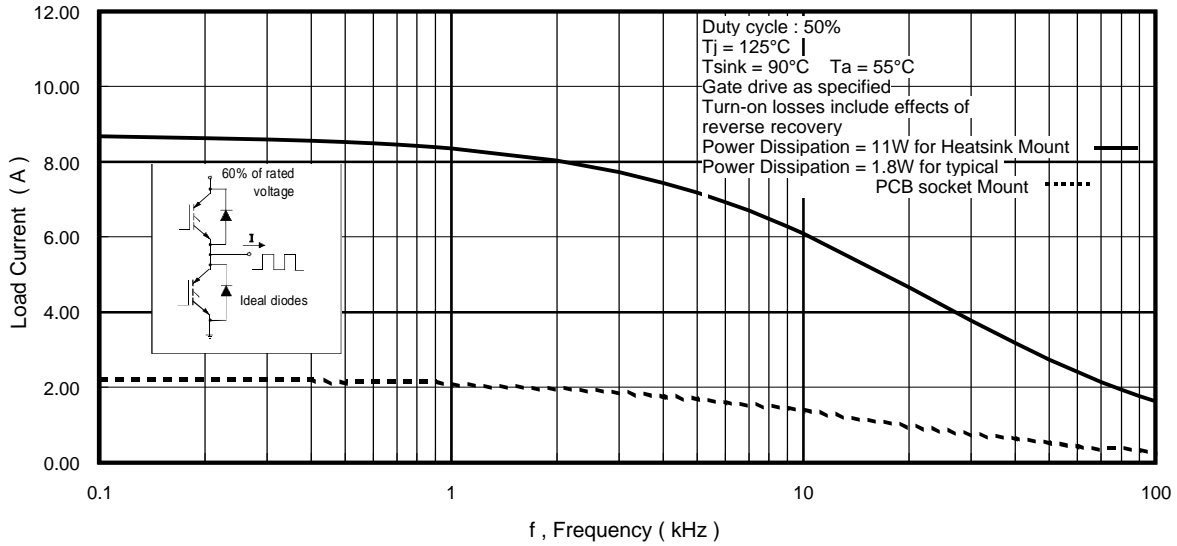


Fig. 1 - Typical Load Current vs. Frequency
 (Load Current = I_{RMS} of fundamental)

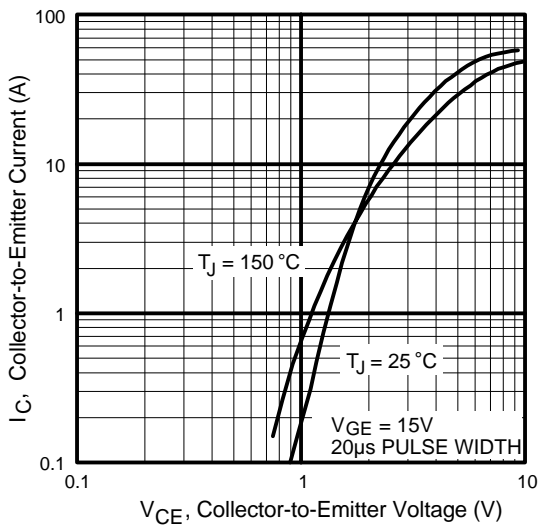


Fig. 2 - Typical Output Characteristics

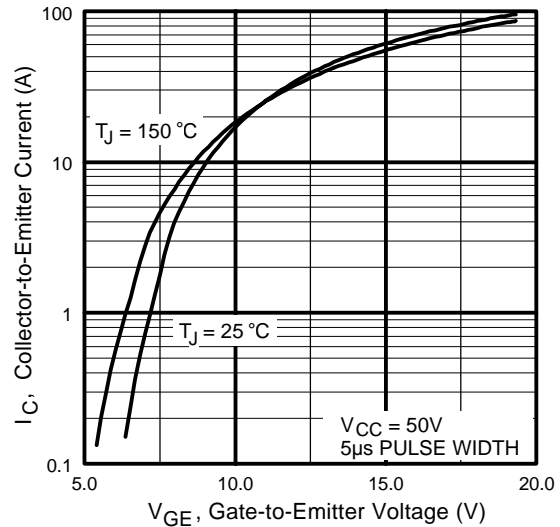


Fig. 3 - Typical Transfer Characteristics

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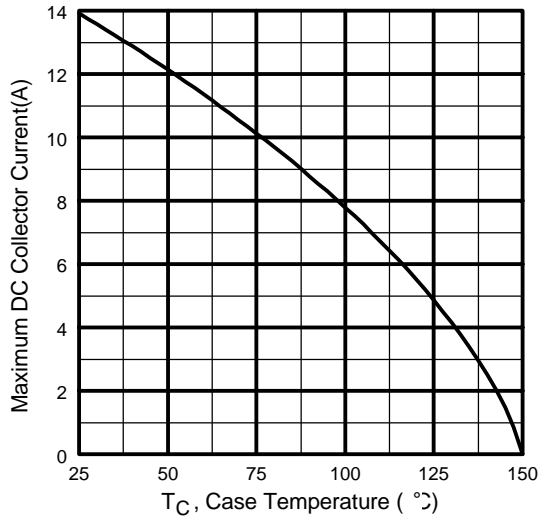


Fig. 4 - Maximum Collector Current vs. Case Temperature

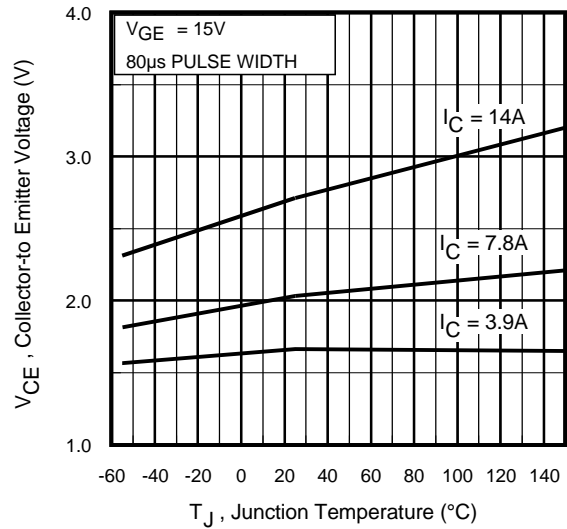


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

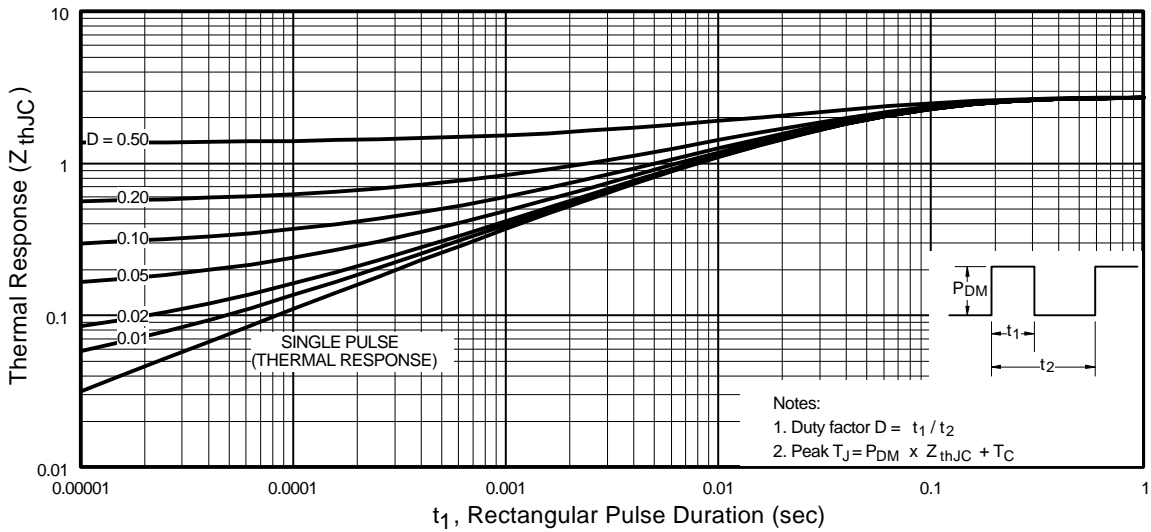


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

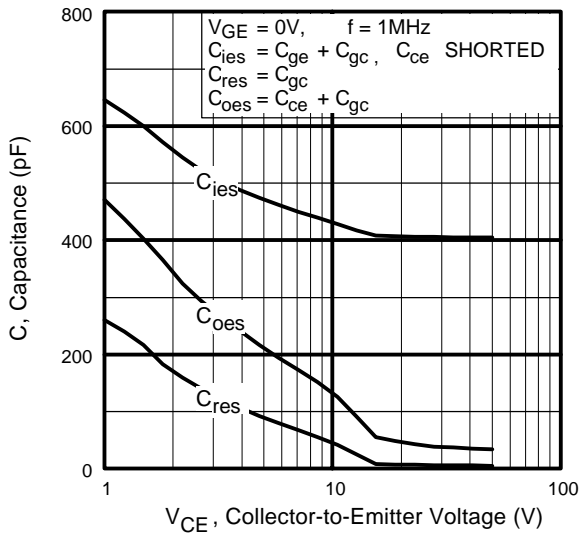


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

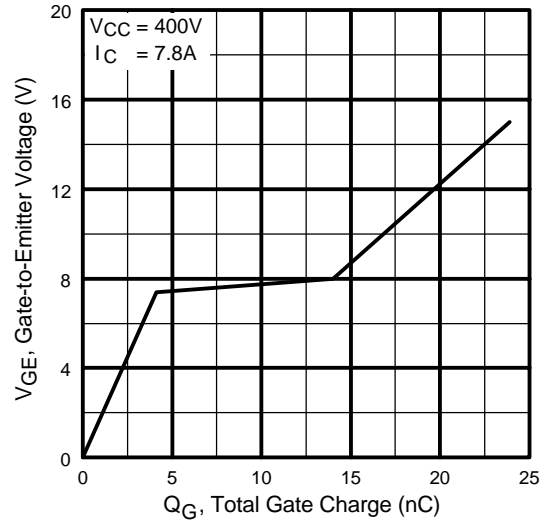


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

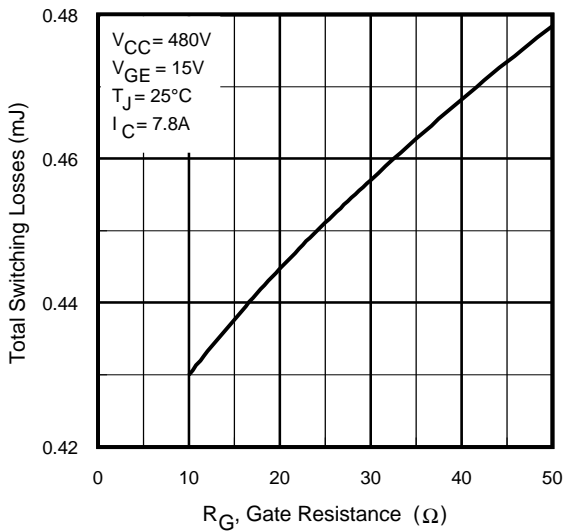


Fig. 9 - Typical Switching Losses vs. Gate Resistance

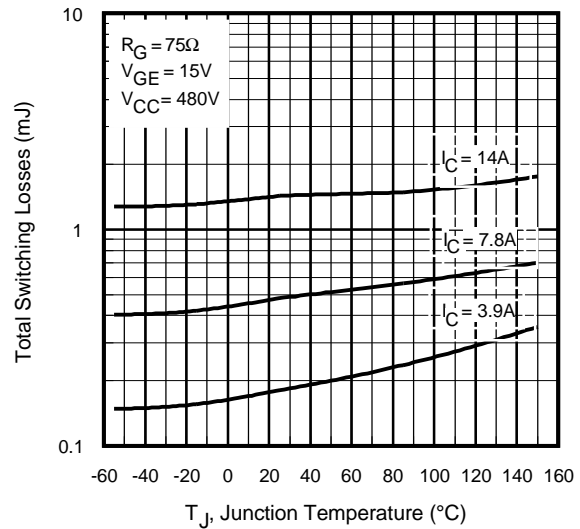


Fig. 10 - Typical Switching Losses vs. Junction Temperature

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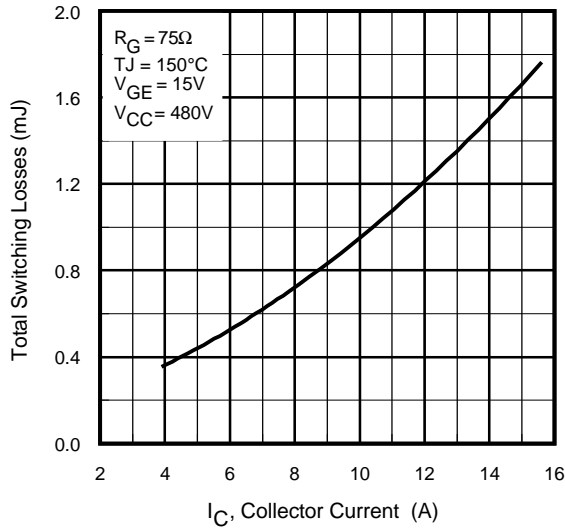


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

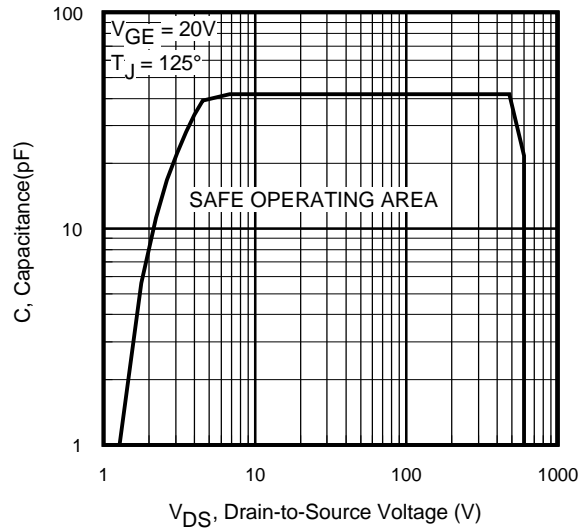


Fig. 12 - Turn-Off SOA

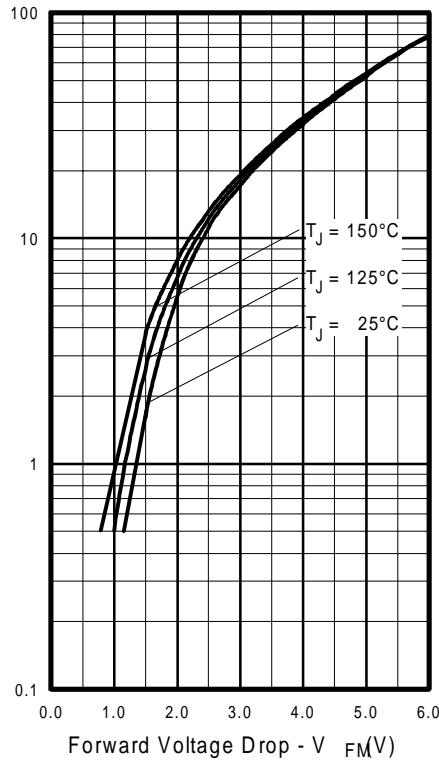


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

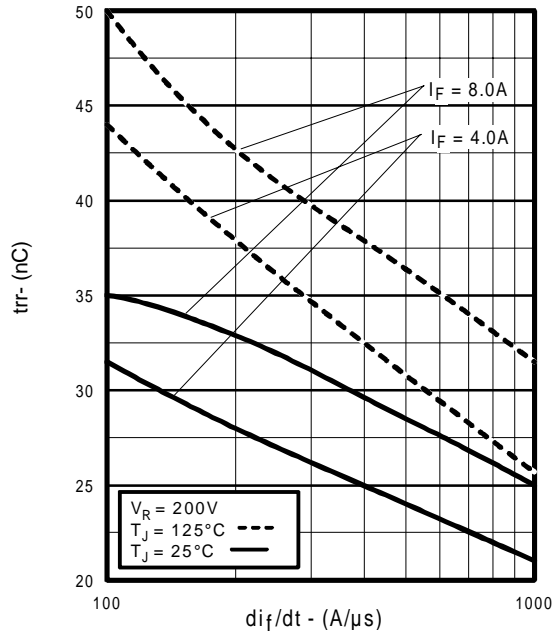


Fig. 14 - Typical Reverse Recovery vs. di_f/dt

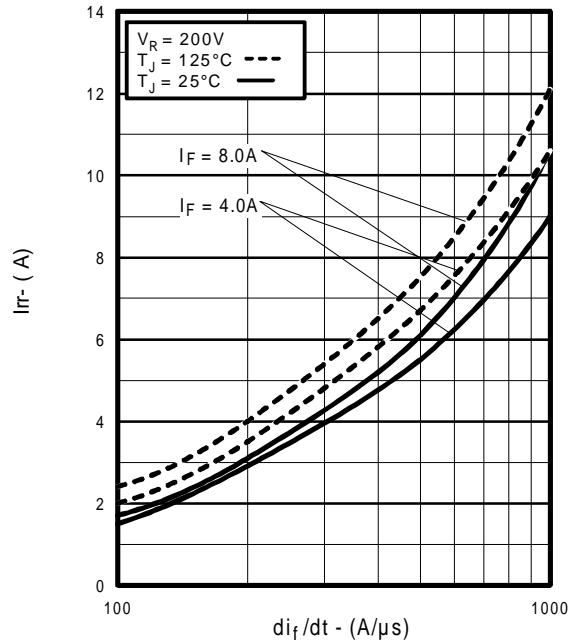


Fig. 15 - Typical Recovery Current vs. di_f/dt

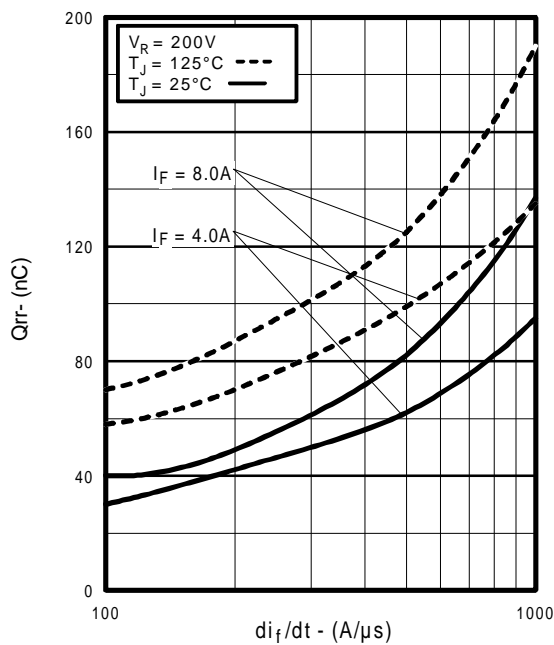


Fig. 16 - Typical Stored Charge vs. di_f/dt

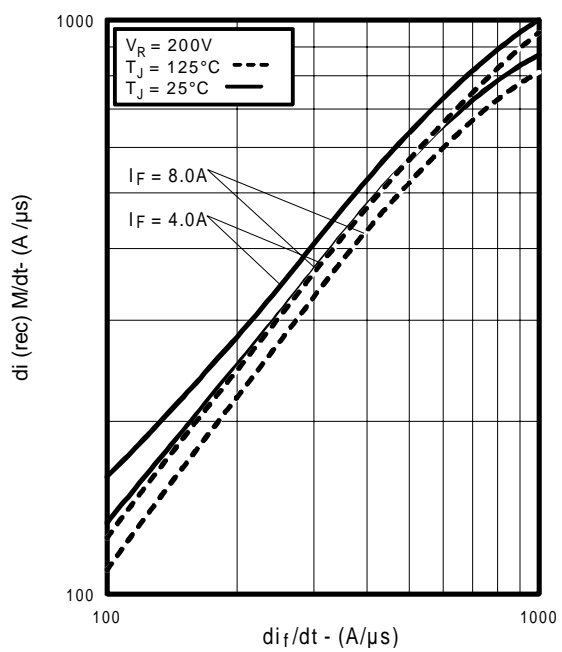


Fig. 17 - Typical $di_{(rec)M}/dt$ vs. di_f/dt ,

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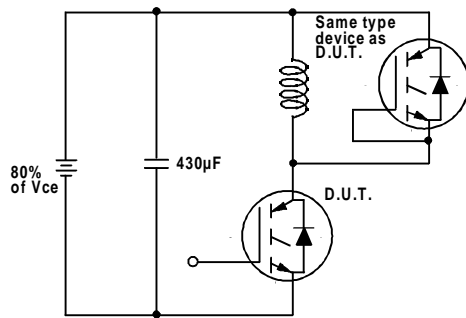


Fig. 18a - Test Circuit for Measurement of I_{LM} , E_{on} , $E_{off}(\text{diode})$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

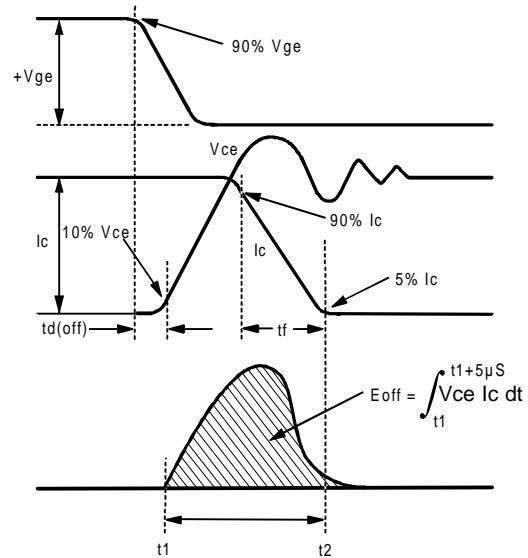


Fig. 18b - Test Waveforms for Circuit of Fig. 18a, Defining E_{off} , $t_{d(off)}$, t_f

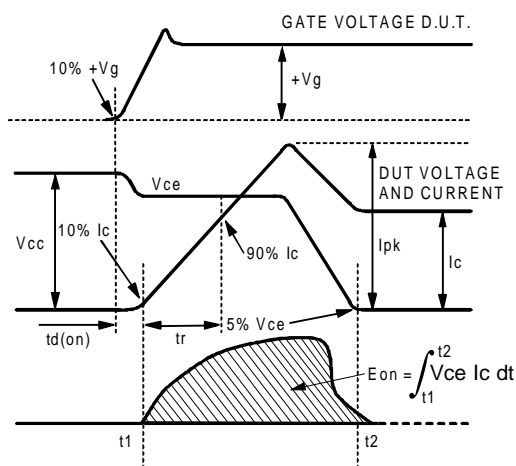


Fig. 18c - Test Waveforms for Circuit of Fig. 18a, Defining E_{on} , $t_{d(on)}$, t_r

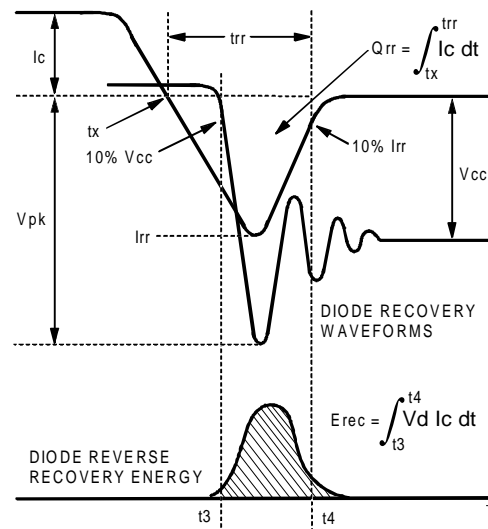


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

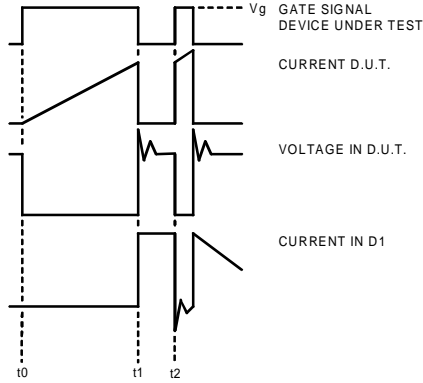


Figure 18e. Macro Waveforms for Figure 18a's Test Circuit

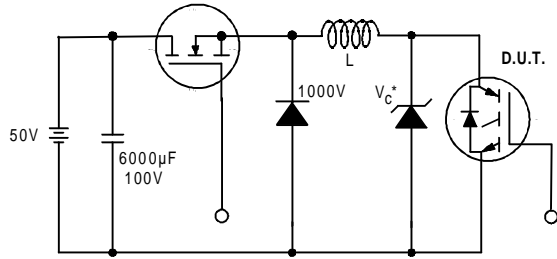


Figure 19. Clamped Inductive Load Test Circuit

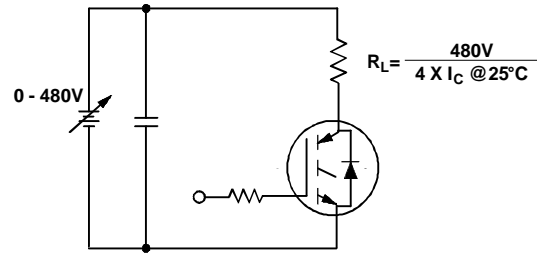
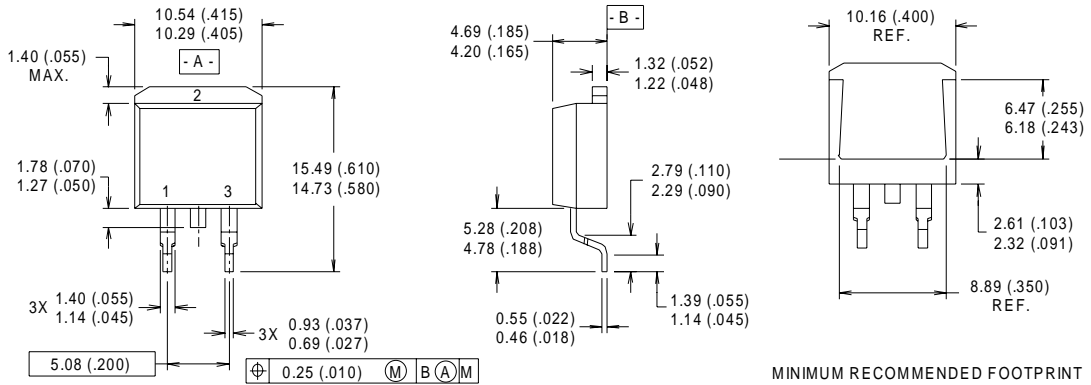


Figure 20. Pulsed Collector Current Test Circuit

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D²Pak Package Outline



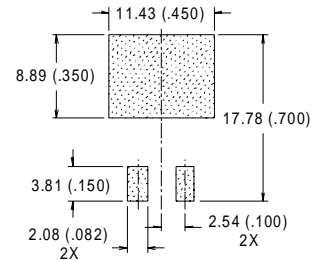
NOTES:

- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

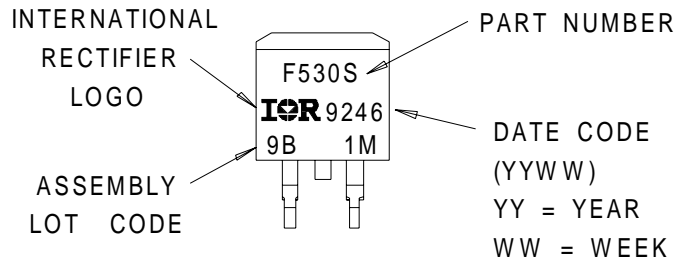
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

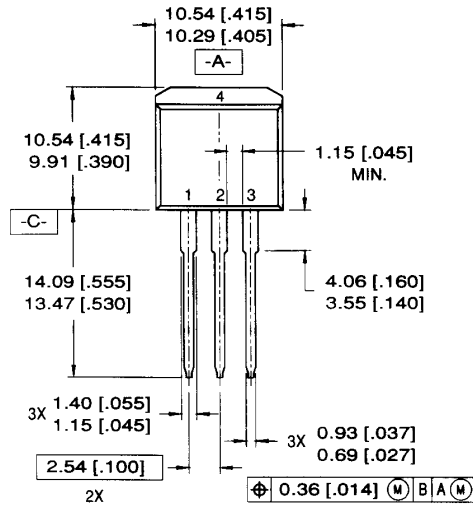
MINIMUM RECOMMENDED FOOTPRINT



D²Pak Part Marking Information



TO-262 Package Outline



LEAD ASSIGNMENTS

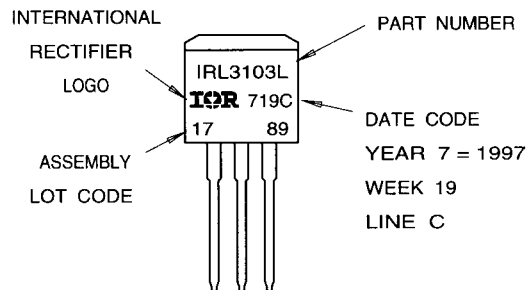
- | | |
|-----------|------------|
| 1 = GATE | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN |

NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

TO-262 Part Marking Information

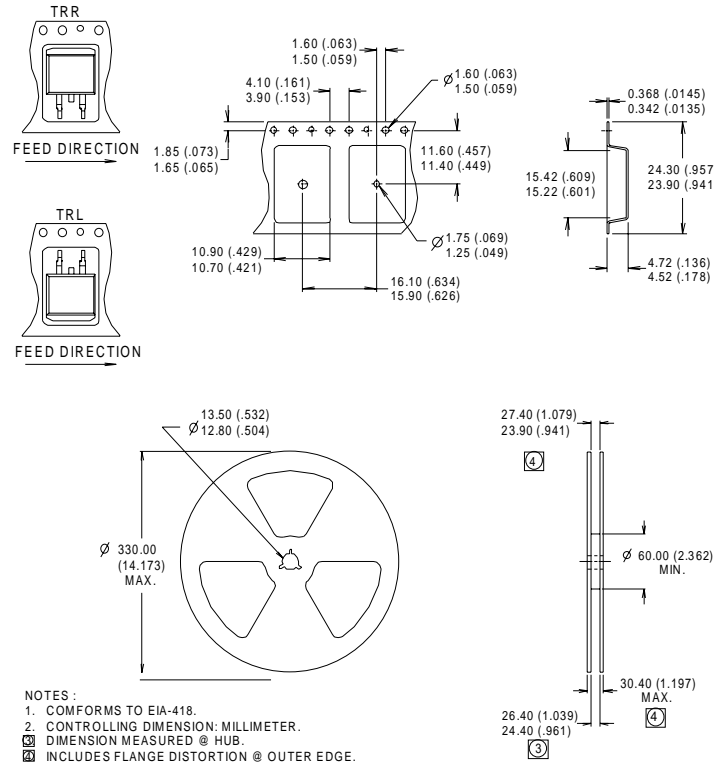
EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"



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D²Pak Tape & Reel Information



Notes:

- ① Repetitive rating: $V_{GE}=20V$; pulse width limited by maximum junction temperature.
- ② $V_{CC}=80\%(V_{CES})$, $V_{GE}=20V$, $L=10\mu H$, $R_G = 75\Omega$
- ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
- ④ Pulse width $5.0\mu s$, single shot.
- ⑤ This only applies to TO-262 package.

⑥ This applies to D²Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.06/01