Integrated Device Technology, Inc.

FAST CMOS 16-BIT BIDIRECTIONAL 3.3V TO 5V TRANSLATOR

IDT54/74FCT164245T

FEATURES:

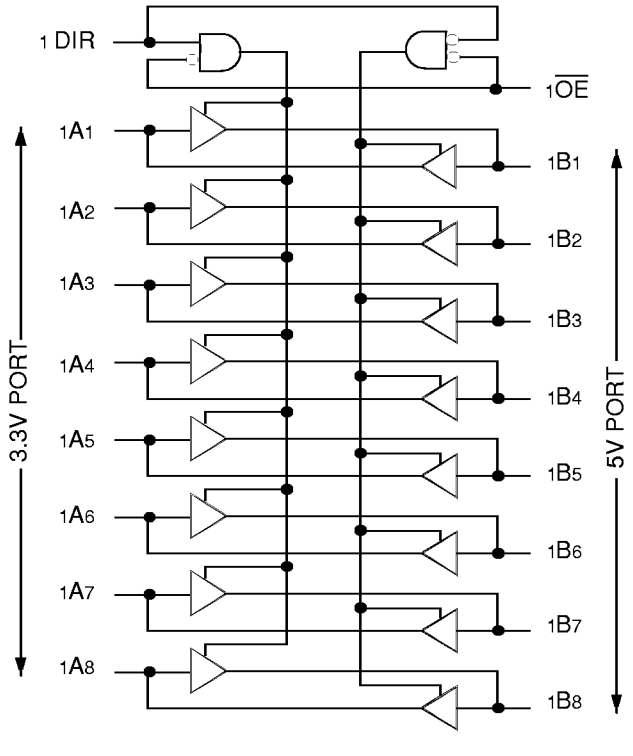
- 0.5 MICRON CMOS Technology
- Bidirectional interface between 3.3V and 5V busses
- Control inputs can be driven from either 3.3V or 5V circuits
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- 25 MIL Center SSOP and Cerpack Packages
- Extended commercial range of -40°C to +85°C
- V_{CC1} = 5V ±10%, V_{CC2} = 2.7V to 3.6V
- High drive outputs (-32mA I_{OH}, 64mA I_{OL}) on 5V port
- Power-off disable on both ports permits "live insertion"
- Typical V_{OLP} (Output Ground Bounce) < 0.9V at V_{CC1} = 5V, V_{CC2} = 3.3V, T_A = 25°C

DESCRIPTION:

The FCT164245T 16-bit 3.3V-to-5V translator is built using advanced dual metal CMOS technology. This high-speed, low-power transceiver is designed to interface between a 3.3V bus and a 5V bus in a mixed 3.3V/5V supply environment. This enables system designers to interface TTL compatible 3.3V components with 5V components. The direction and output enable controls operate these devices as either two independent 8-bit transceivers or one 16-bit transceiver. The A port interfaces with the 3.3V bus; the B port interfaces with the 5V bus. The direction control (xDIR) pin controls the direction of data flow. The output enable ($x\overline{OE}$) overrides the direction control and disables both ports. These control signals can be driven from either 3.3V or 5V devices.

The FCT164245T is ideally suited for driving high capacitance loads and low impedance backplanes. The output buffers are designed with Power-Off Disable capability to allow "hot insertion" of boards when used as backplane drivers. They also allow interface between a mixed supply system and external 5V peripherals.

FUNCTIONAL BLOCK DIAGRAM



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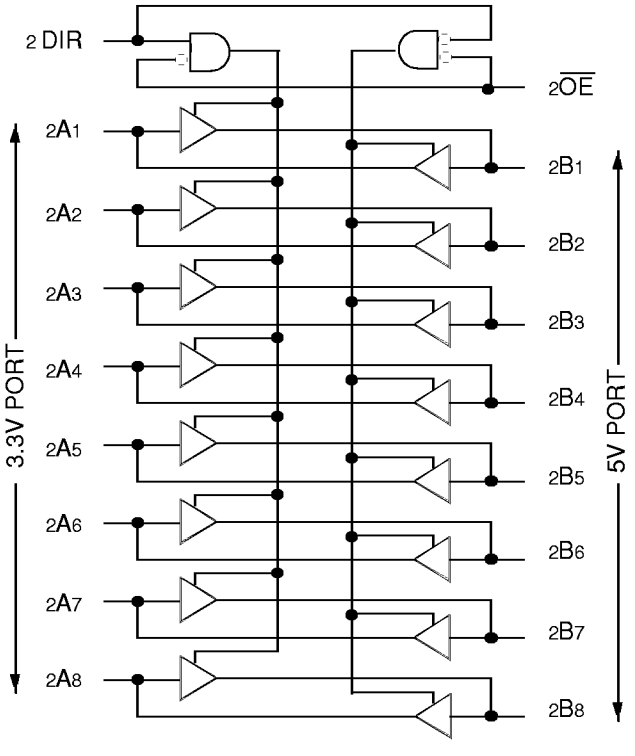

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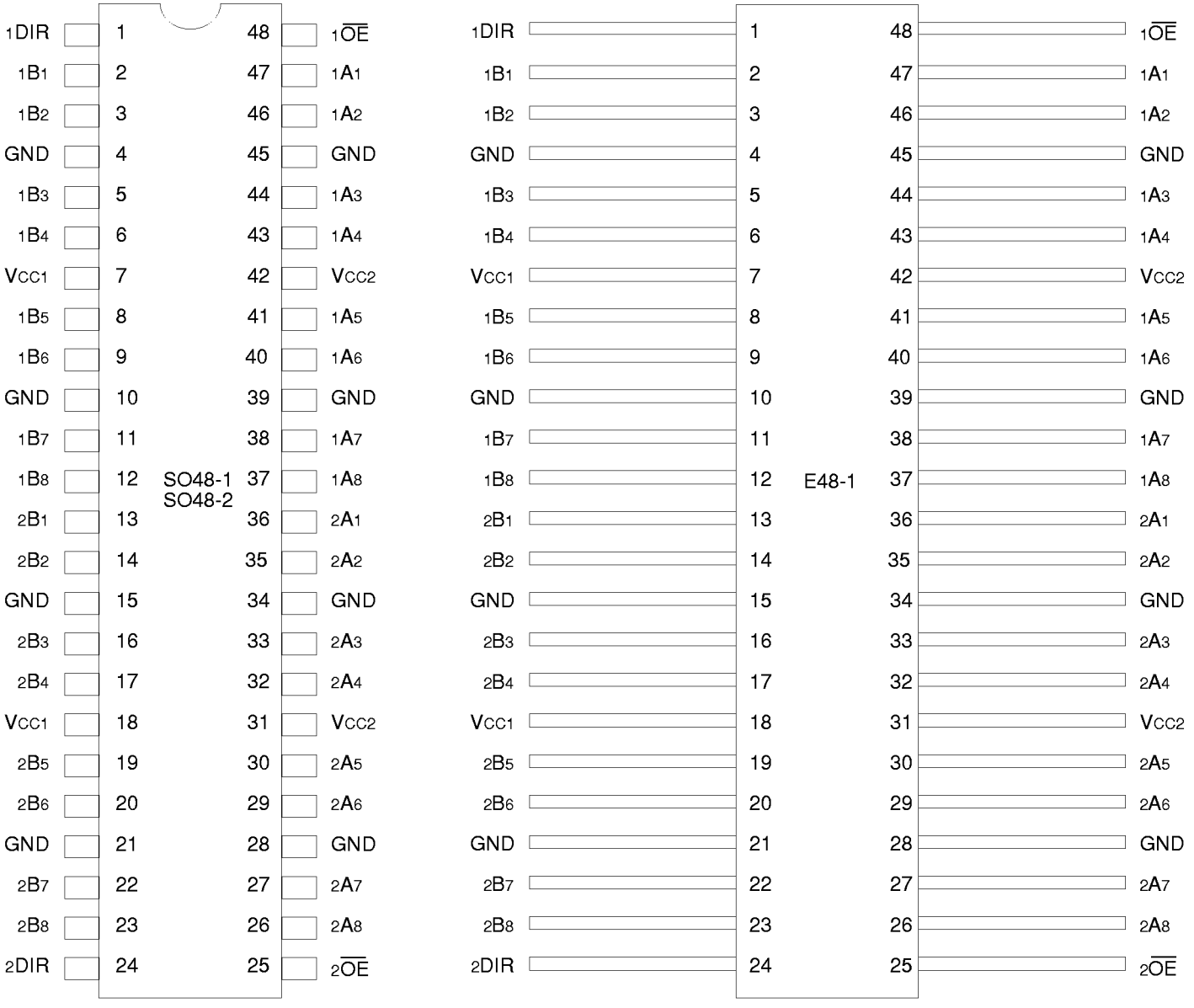
PIN CONFIGURATIONS



POWER SUPPLY SEQUENCING

In the IDT54/74FCT164245T the condition of $V_{CC1} \geq (V_{CC2} - 0.5V)$ must be maintained at all times. For the range of $V_{CC1} = (V_{CC2} - 0.5V)$ to $V_{CC1} = (V_{CC2} + 0.9V)$, both the A and B ports will remain in a high impedance state.

PIN DESCRIPTION

Pin Names	Description
$x\overline{OE}$	Output Enable Input (Active LOW)
xDIR	Direction Control Input
xAx	Side A Inputs or 3-State Outputs (3.3V Port)
xBx	Side B Inputs or 3-State Outputs (5V Port)

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FUNCTION TABLE(1)

Inputs		Outputs
$x\overline{OE}$	xDIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

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NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC1} +0.5	–0.5 to V_{CC1} +0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +120	–60 to +120	mA

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NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All device terminals except V_{CC2}.
3. Power supply terminals V_{CC2}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	3.5	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (A PORT - 3.3V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 2.7V to 3.6V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = 5.5V	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.	V_I = V_{CC2}	—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)		V_I = GND	—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC2} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = V_{CC2} = Min.	I_{OH} = –0.1mA	V_{CC2}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA MIL.	2.4	3.0	—	
		V_{CC2} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC1} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{CC2} = Min.	I_{OL} = 16mA	—	0.2	0.4	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.50	
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		–70	–105	–150	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 1.5V[3]		–40	–60	–90	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC2L} I_{CC2H} I_{CC2Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.35	2.0	mA

NOTES:
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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (B PORT - 5V)

Following Conditions Apply Unless Otherwise Specified:
V_{CC1} = 5V ± 10%, V_{CC2} = 2.7V to 3.6V; Commercial: T_A = –40°C to +85°C, Military: T_A = –55°C to +125°C,

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input and I/O pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)	V_{CC1} = Max.	V_I = V_{CC1}	—	—	±5	µA
	Input HIGH Current (I/O pins)	V_{CC2} = Max.		—	—	±15	
I_{IL}	Input LOW Current (Input pins)		V_I = GND	—	—	±5	
	Input LOW Current (I/O pins)			—	—	±15	
V_{IK}	Clamp Diode Voltage	V_{CC1} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
V_{OH}	Output HIGH Voltage	V_{CC1} = Min.	I_{OH} = –3mA	2.5	3.5	—	V
		V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL. I_{OH} = –15mA COM'L.	2.4	3.5	—	
			I_{OH} = –24mA MIL. I_{OH} = –32mA COM'L.[5]	2.0	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC1} = Min., V_{CC2} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL. I_{OL} = 64mA COM'L.	—	0.2	0.55	V
I_{OFF}	Input/Output Power Off Leakage	V_{CC1} = 0V, V_{CC2} = 0V, V_{IN} or $V_O \le$ 4.5V		—	—	±100	µA
I_{OS}	Short Circuit Current[4]	V_{CC1} = Max., V_{CC2} = Max., V_O = GND[3]		–80	–140	–225	mA
I_O	Output Drive Current	V_{CC1} = Max., V_{CC2} = Max., V_O = 2.5V[3]		–50	–75	–180	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CC1L} I_{CC1H} I_{CC1Z}	Quiescent Power Supply Current	V_{CC1} = Max., V_{IN} = GND or V_{CC2} V_{CC2} = Max.		—	0.08	1.5	mA

2555 tbl 06

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1} = 5.0V, V_{CC2} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5 Duration of the condition can not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC1} = Max., V_{CC2} = Max., V_{IN} = V_{CC2} -0.6V[3]		—	12	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open x$\overline{OE}$ = xDIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC2} V_{IN} = GND	—	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC1} = Max., V_{CC2} = Max. Outputs Open fi = 10MHz 50% Duty Cycle x$\overline{OE}$ = xDIR = GND One Bit Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	1.2	4.7	mA
		V_{CC1} = Max., V_{CC2} = Max Outputs Open fi = 2.5MHz 50% Duty Cycle x$\overline{OE}$ = xDIR = GND Sixteen Bits Toggling	V_{IN} = V_{CC2} - 0.6V V_{IN} = GND	—	3.5	8.5[5]	

2555 tbl 07

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC1}= 5.0V, V_{CC2}= 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC1} + I_{CC2} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC1}= Quiescent Current (I_{CC1L}, I_{CC1H} and I_{CC1Z})
   I_{CC2}= Quiescent Current (I_{CC2L}, I_{CC2H} and I_{CC2Z})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

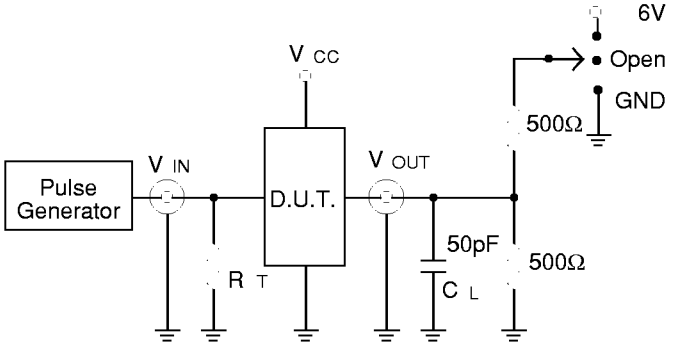
Symbol	Parameter	Condition[1]	Com'l.		Mil.		Unit
			Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay A to B	C_L = 50pF R_L = 500Ω	1.5	5.0	—	—	ns
t_{PLH} t_{PHL}	Propagation Delay B to A		1.5	5.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to B		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to B		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to A		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time x$\overline{OE}$ to A		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to B[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to B[3]		1.5	6.0	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time xDIR to A[3]		1.5	6.5	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time xDIR to A[3]		1.5	6.0	—	—	ns

2555 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

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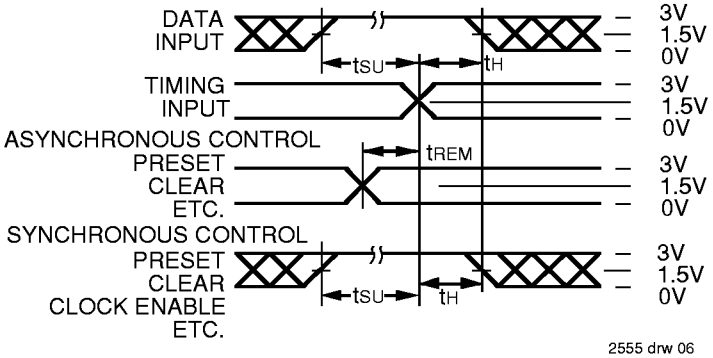
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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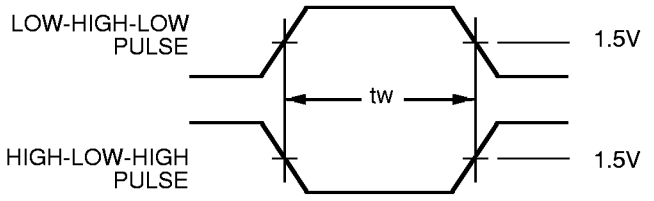
PULSE WIDTH



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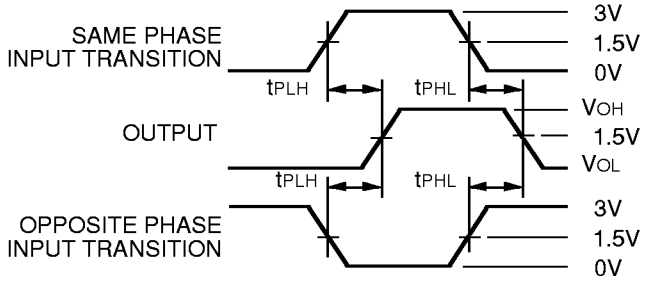
PROPAGATION DELAY



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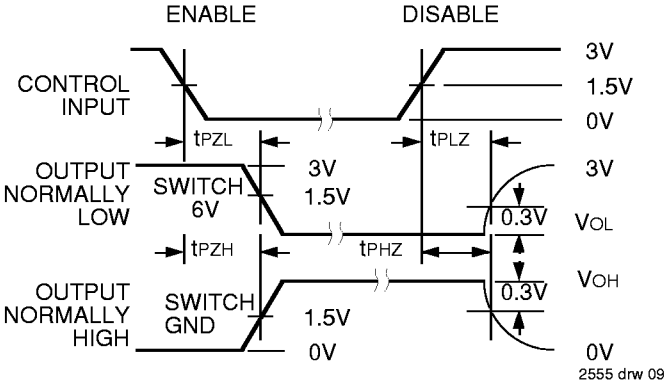
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

ORDERING INFORMATION